2EI4 Design Project #1: AC to DC Conversion

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I hereby declare that the work presented in this report is original, and any external sources or materials used have been duly cited in accordance with the accepted standards of academic integrity and ethical research practices.

Summary

This project aims to create a DC power supply delivering a consistent output of 10 mA at 3V ± 0.1V, simulating input from a 120V (rms) 1 kHz source. Utilizing the Analog Discovery 2 (AD2) function generator, the design encompasses essential power supply stages: transformer simulation, rectification, filtering, and an optional regulator. Key design parameters, including transformer turns ratio, rectifier type, and filter components, will be meticulously calculated, considering safety and component limitations.

Emphasis is placed on robust safety measures, meticulous calculations, and comprehensive simulations before practical implementation. The report will succinctly outline the design choices, including transformer specifications, rectifier topology, and filter components, ensuring clarity and adherence to safety standards. Simulations will be validated against actual measurements, fostering a deep understanding of the power supply's performance characteristics. The discussion section will focus on result comparisons, potential discrepancies, and safety considerations, offering a holistic view of the project's achievements and limitations.

Design

Transformer

To address the potential hazards associated with a 120V (rms) AC current, a transformer is introduced into the circuit design. In the LTSpice schematic, an input voltage of 4.6V is employed. Considering that the AC current of 120V is rms, the corresponding peak voltage can be calculated as 120V/0.707, resulting in approximately 169.7V. Since a non-rms AC current is utilized as the input to the rectifier, the transformer ratio is determined using the peak voltage. The calculated ratio is 169.7/4.6, yielding a transformer ratio of 36.90, which is then approximated to 36:1. However, for the AD2 simulation, where the input voltage varies to 5.7V, the corresponding transformer ratio becomes 169.7/5.7, resulting in a ratio of approximately 29.77:1. These considerations highlight the importance of adjusting the transformer ratio based on the specific input voltage in each simulation scenario.

Rectifier

Given that the circuit will be powered by an AC source, the incorporation of a rectifier becomes imperative to address both the positive and negative phases of the power input. Consequently, a full-wave rectifier, employing four 1N4148 diodes, has been chosen for this purpose. The 1N4148 diode, as indicated in the datasheet, exhibits a maximum voltage drop of 1V when in the ON state. However, it is noteworthy that upon further investigation, variations in the forward voltage drop ranging from 0.7V to 1V have been identified, contingent upon the input voltage, as documented by ultralibrarian.com. On how the rectifier operates is defined in the calculation aspect of the report.

Filter

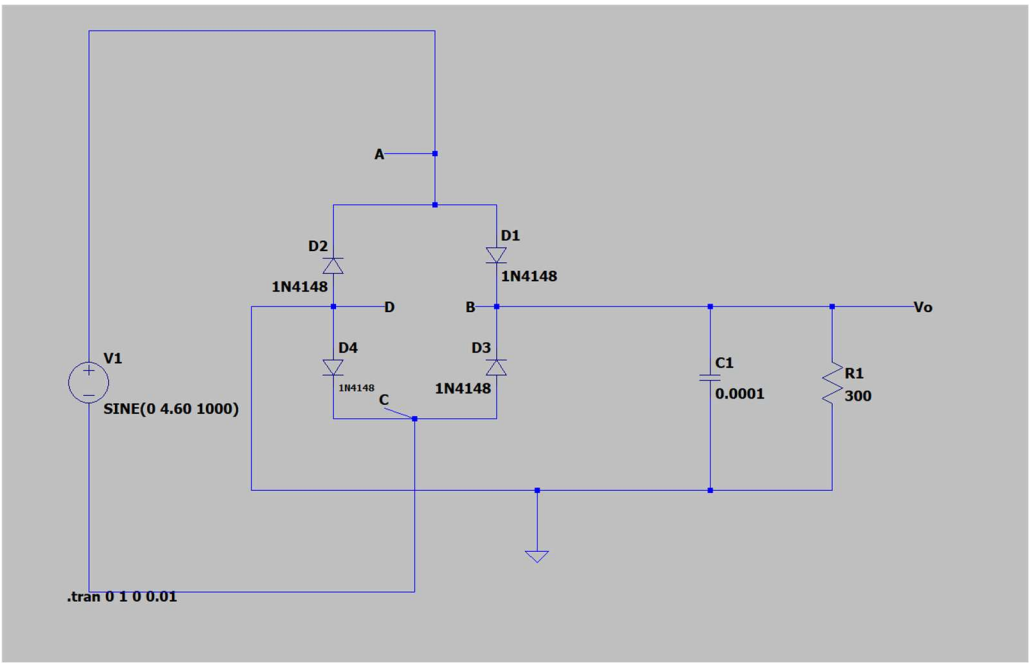
The components used to make this filter was purely the capacitor which is connected in parallel to the load resistor. This type of filter is called the capacitor filter. The capacitor which was chosen is a 100 micro-farad capacitor from the 2EI4 kit.

Regulator

For the design and circuit schematic which I have implemented, there is no regulator which was integrated.

Circuit Schematic

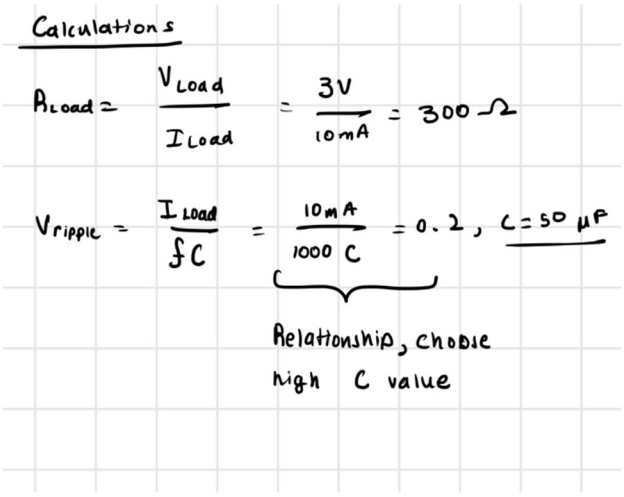
The following picture is the completed circuit analysis which uses a full wave bridge rectifier with a capacitor filter.



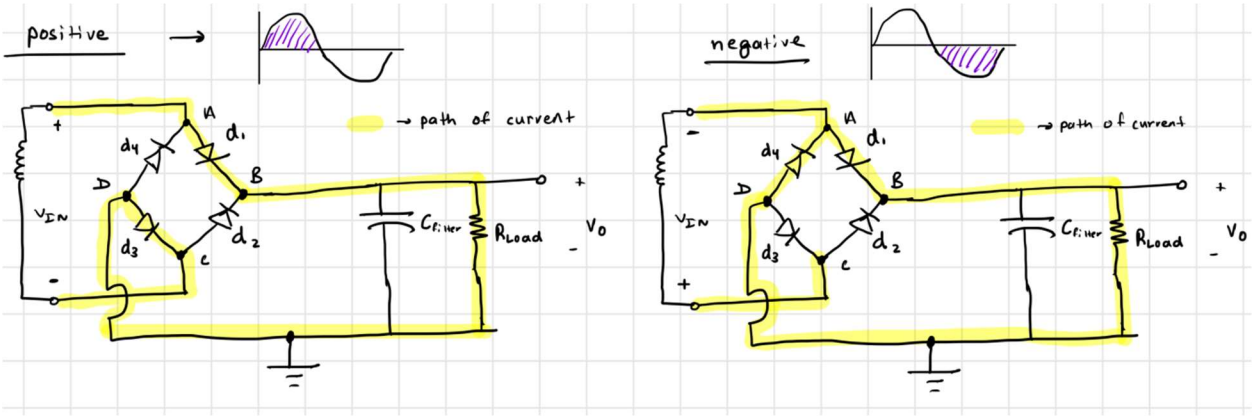
Circuit Diagram LTSpice

Calculations for Components

The following picture are the calculations which were done to obtain the value of the load resistor and the capacitor as well. The design specifies that the output should be at a 3V DC 10mA current, which provides me enough details to solve for R_{load}. As for the capacitance, the value isn't bound to anything however, there is a relationship between the ripple Voltage and the Capacitance which is used. As seen in my calculations, V_{ripple} and Capacitance are inversely proportional to each other, which means that if I want to minimize the Ripple voltage, making the output voltage as flat as possible, the capacitance needs as large as it can be. That is the reasoning behind why I chose the highest capacitance which was available to me which was 100uF from the 2CI4 kit instead of the calculated value. I could join capacitors in parallel, but I chose not to just for simplicity.

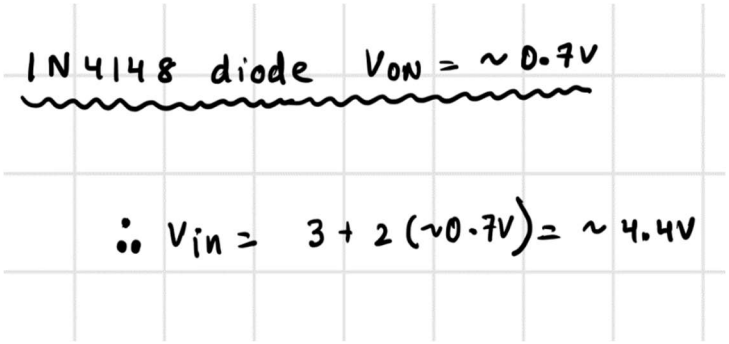


Resistor and Capacitor Calculations



Positive and Negative Sinusoidal Current Path

As for the calculation of V_{input}, I decided to dive a bit more deeply into how the full wave bridge rectifier will work. During the positive and negative aspects of the input voltage, I can see that the current goes through 2 diodes each time, therefore it would mean that the drop that V_{input} receives from its initial state is $2*(V_{ON})$, where V_{ON} is the forward voltage drop of the diode. Since V_{ON} is ~0.7V and



our desired voltage is 3V, the input voltage would be 3+2*(~0.7V) = ~4.4V. This indicates that the input voltage would need to be around 4.4V.

Expected Performance

As outlined in the preceding design calculations, the anticipated performance of the circuit aligns with a 10 mA current at 3V ± 0.1V. The load resistor has been appropriately chosen to accommodate the specified current, and the inclusion of a capacitor serves the purpose of mitigating excessive ripple voltage. The input voltage, crucially determined by the forward drop of the diodes, is subject to variations due to the dependency of the diode's drop on the received voltage. This variability introduces a consideration for potential fluctuations in the input voltage.

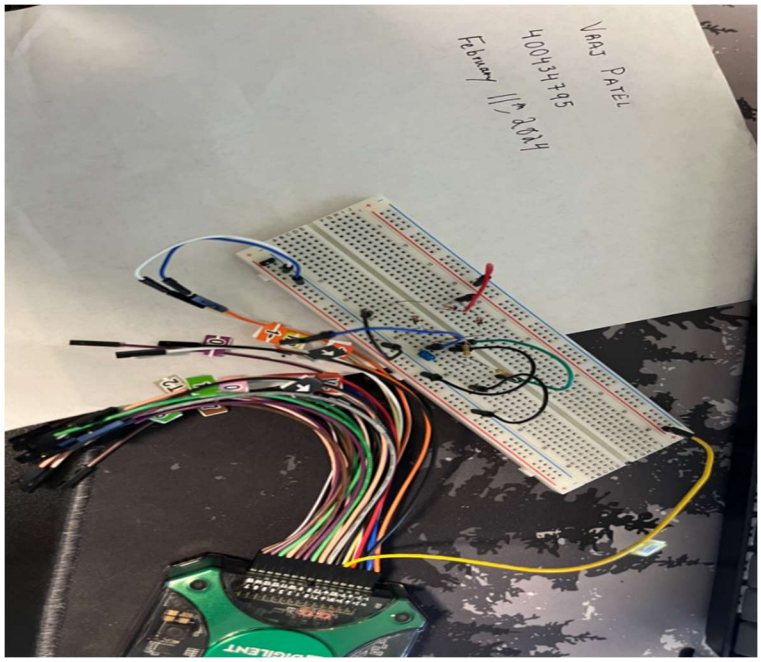
Discussion

In formulating the design for the full-wave bridge rectifier with a capacitance filter, meticulous attention was given to navigate design trade-offs, ensuring a delicate equilibrium between efficiency and cost. Optimal capacitance values for the filter were contemplated, recognizing that higher capacitance could enhance ripple reduction but at the expense of increased costs and physical space. This reflects the inherent trade-off between efficiency versus cost and size versus performance. The decision to employ a single high-capacitance capacitor rather than multiple parallel-connected capacitors was made for simplicity, acknowledging the trade-off in complexity versus performance. Robust design margins were incorporated, emphasizing the selection of components with voltage and current ratings well beyond anticipated maximum values to establish safety buffers against potential voltage or current surges. Additionally, thorough research on the 1N4148 diodes was conducted in advance to ensure awareness of their breakdown voltage and current characteristics, adding an extra layer of safety. The careful consideration of load resistor values was pivotal, as it dictates the current flowing through the diode, underscoring the importance of selecting an appropriate load resistor value.

Measurement and Analysis

Circuit Photograph

The following photograph is the real-life circuit which was made for appropriate AC → DC conversion.



In real life Circuit Schematic

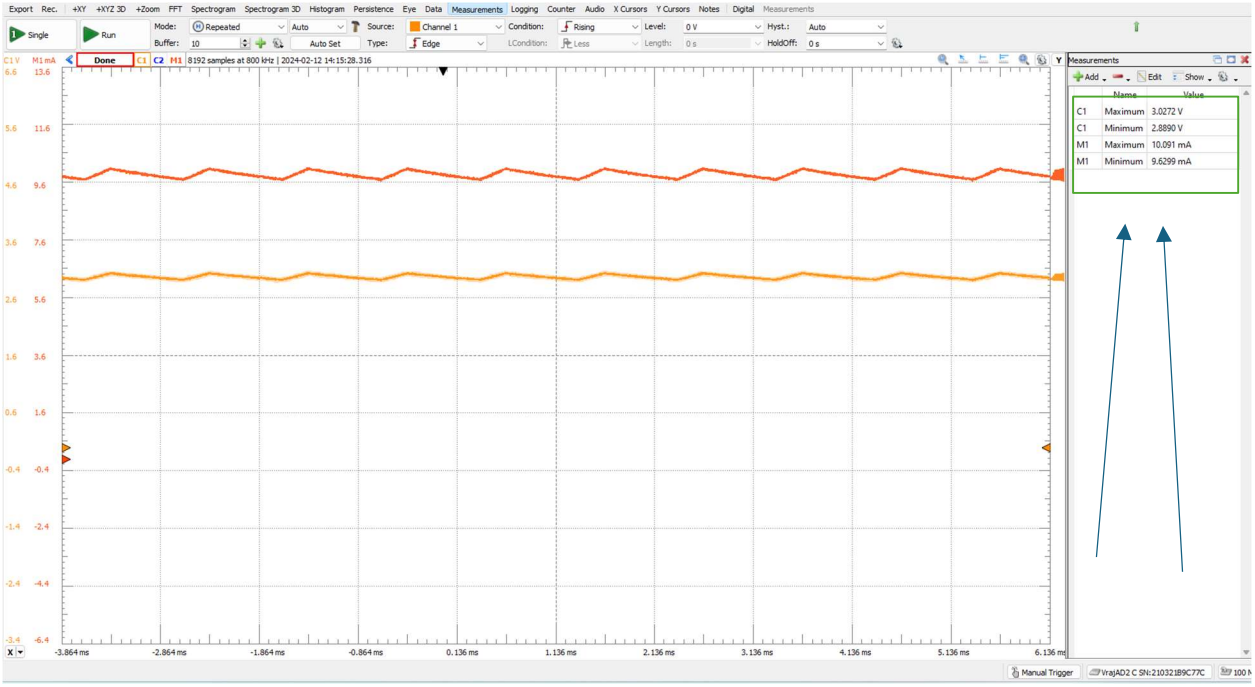
Measurement Procedure

In the process of evaluating the circuit's performance, meticulous attention was given to the proper connection of AD2 pins, ensuring precise alignment with the designated channels 1+ and 1- on the breadboard (depicted as blue pins in the accompanying image). Initial attempts to simulate the circuit with the input voltage mirrored from the simulation yielded suboptimal results, hovering around 2.7V. Recognizing the need for an augmented input voltage, I experimented with a 5V input—AD2's maximum capacity—only to fall short of the desired 3V DC output. Consequently, a novel approach involving the introduction of another waveform as ground, featuring a sinusoidal wave with a 180-degree phase shift, was adopted. This strategic maneuver effectively increased the input voltage, culminating in the successful acquisition of the targeted measurements.

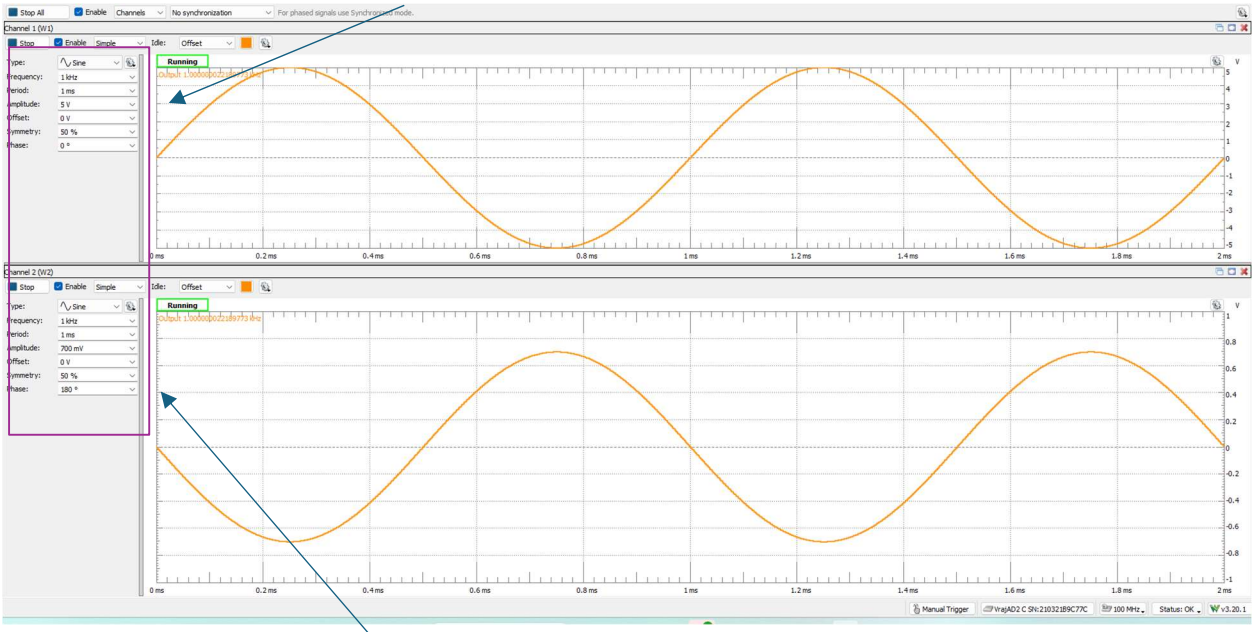
Measurement Results

After tweaking some values around with the waveforms, I finally got the output which I was looking for. As seen in the oscilloscope output, the maximum voltage outputted was ~3V and the current through the resistor is ~10mA.

Oscilloscope Output



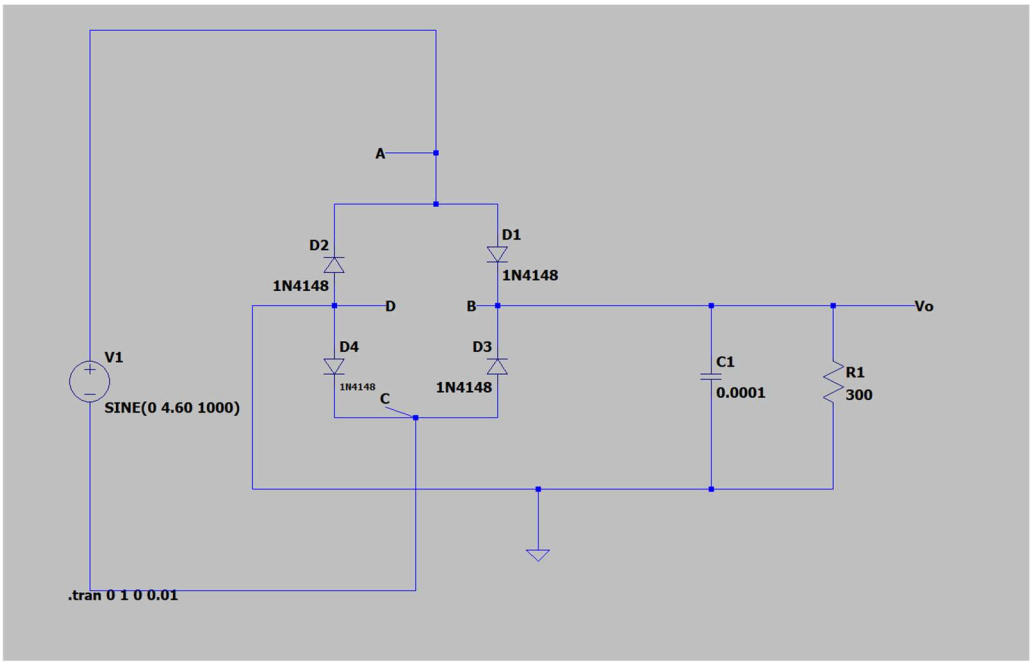
AD2 - Current and Output Voltage



AD2 - Input Waveforms

Simulation

Circuit Schematic – Simulator



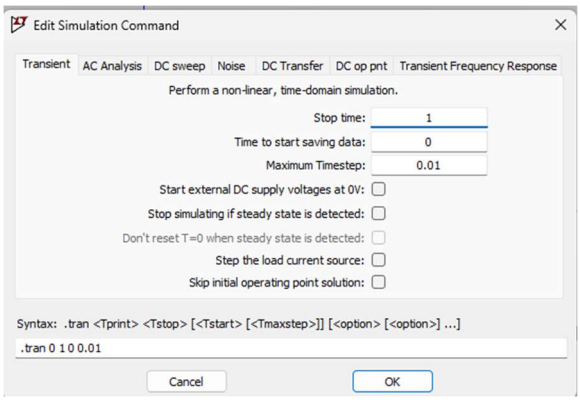
LTSpice - Simulation Schematic

Netlist

*** C:\Users\vrajp\OneDrive\Desktop\2nd year\2nd Sem\2EI\2EI Project #1.asc**
V1 A C SINE(0 4.60 1000)
D1 A Vo 1N4148
D2 0 A 1N4148
D3 C Vo 1N4148
D4 0 C 1N4148
R1 Vo 0 300
C1 Vo 0 0.0001
.model D D
.lib C:\Users\vrajp\AppData\Local\LTspice\lib\cmp\standard.dio
.tran 0 1 0 0.01
.backanno
.end

Simulation Conditions

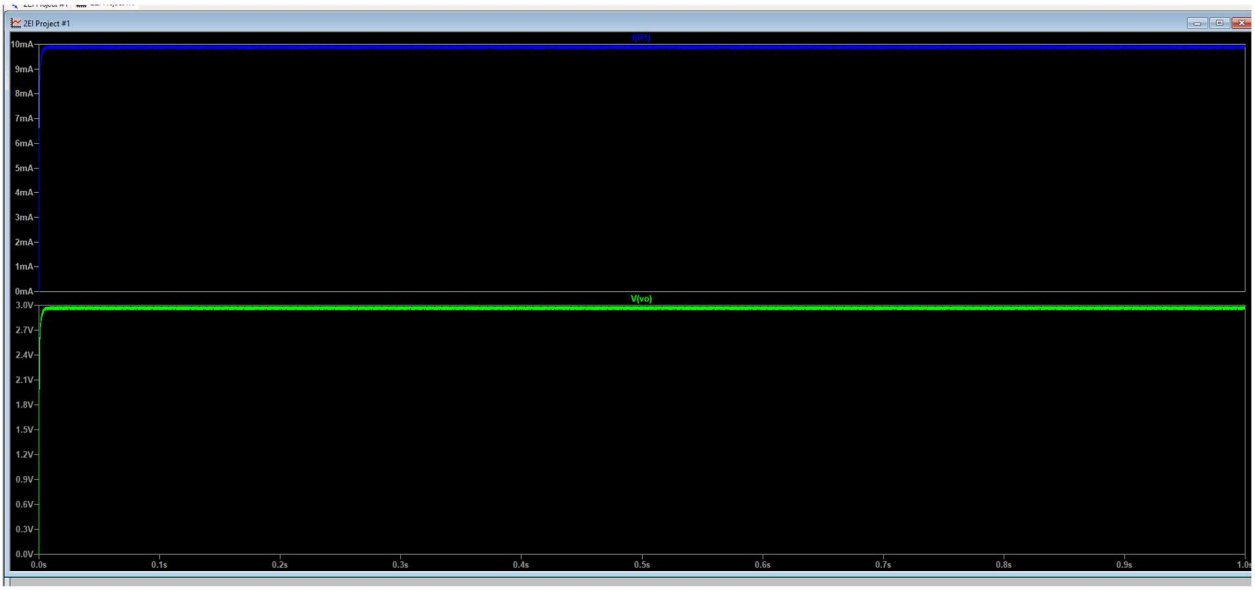
The selected simulation methodology for this study is transient simulation, chosen for its efficacy in facilitating a comprehensive observation of the circuit's performance dynamics. A stop time of 1 second has been judiciously determined to afford a sufficiently detailed analysis of the voltage stability within the circuit. Opting for a higher stop time is deemed imperative to ensure a nuanced examination of the circuit's behavior, as an inadequate temporal scope would hinder the accurate measurement of its performance characteristics.



Simulation Conditions LTSpice

Simulation Output

The simulation output shows that the circuit is successful in obtaining a 3V DC power at 10mA of current from the specified input Voltage.



Simulation Output LTSpice

Discussion

Comparing Results

Upon meticulous comparison between the simulation and AD2 results, a striking resemblance emerges in terms of output characteristics, aligning precisely with the anticipated 10 mA at 3V ± 0.1V specifications. Despite the visual disparity between the breadboard circuit and its LTSpice counterpart, the essential performance metrics converge harmoniously. Aligning the physical circuit with the LTSpice model posed a noteworthy challenge during measurement acquisition. Notably, the AD2 simulation exhibits a more triangular waveform compared to its LTSpice counterpart. This discrepancy can be attributed to the excessive 1s period in the LTSpice simulation, which might be deemed excessive, especially given the 1000Hz frequency of the input voltage. Upon closer inspection, the triangular nuances in the AD2 simulation correlate coherently with the LTSpice simulation when zoomed in.

Discrepancies

The discrepancies between the AD2 circuit and the LTSpice circuit primarily stem from the inherent differences between simulation environments and real-world conditions. The input voltage variation, where the AD2 circuit required an increase from 4.6V to 5.7V compared to LTSpice, can be attributed to the simulation's idealized conditions. Simulation tools assume a perfect domain with zero internal resistance in voltage sources and negligible wire resistance, leading to a need for an increased input voltage in the real-world scenario. Additionally, the forward drop of diodes plays a crucial role. While simulations consider ideal conditions, real-world diodes exhibit voltage drop variations based on the applied voltage. These factors highlight the challenges of translating simulations into practical implementations, emphasizing the need for iterative adjustments and real-world measurements to refine the design.

Limitations

A prominent limitation observed in the circuit design pertained to the presence of ripple voltage despite the implementation of a capacitor filter. While increasing capacitance or incorporating a regulator could potentially enhance ripple reduction, the current design faces constraints in achieving optimal stability in the output. Real-world variations in components, including diodes and capacitors, further contributed to limitations in accuracy and performance. The factors discussed in the discrepancies section underscored the challenges in maintaining precise conformity between the theoretical design and its real-world manifestation. There is also a limitation of the load since the maximum load to achieve 10mA would be 300 ohms. The no load voltage would also stay the same

Problems Encountered

A significant challenge encountered during the project centered around determining the input voltage for both the LTSpice and AD2 simulations. Addressing this in LTSpice involved a closer examination of the full-wave bridge rectifier. It was observed that the input voltage would surpass twice the diode drop at the output. Investigating the diode's characteristics, the datasheet indicated a maximum drop of 1V, suggesting the potential for achieving a lower drop. Further research suggested an average drop of 0.7V. Assuming a diode drop range of 0.7V to 1.0V, the LTSpice design's input voltage was appropriately set at 4.6V.

For the AD2 simulation, the realization that the required input voltage was greater posed a challenge, especially given the AD2's maximum output of 5V. To overcome this limitation, a solution involved connecting another waveform with a 180-degree phase shift to augment the input voltage above 5V. The determination of the final input voltage for the AD2 was achieved through an iterative guess-and-check method.