LAB 1 Introduction to DE2 ECE533S

Due at the end of your 1st lab section

I. General Information

1. Please ensure that your workspace is clean after the lab session.
2. Please DO NOT save any file in the lab PCs. If you wish to save your work, please bring your own USB.
3. You must attend each lab. If you must be absent, please email TAs in advance. You may attend another section with special permission. Please be aware that the lab equipment is limited, so priorities will be given to students registered for the section. You are free to implement your controller code prior to the lab and demonstrate it to the TA.
4. The PC password is '**energy**'.

II. Introduction

The Altera DE2 board is used as the digital control platform throughout the term. The DE2 board manual is posted on Portal, as well as some links for Verilog references. During the first lab you will implement a flexible counter-based Digital Pulse-width Modular (DPWM), to be used as part of your SMPS digital controller. The DPWM is responsible for producing two gating pulses to the synchronous boost converter. The two gating pulses, C1 and C2, have a frequency of f_s, corresponding to the switching frequency of the boost converter. The gating pulses are complimentary and must be non-overlapping to avoid shoot-through in the power-stage. The duration of the two non-overlapping periods, which correspond to the dead-times DT1 and DT2, should be independently controlled for efficiency optimization. Note that your DPWM block will be modified later in the course to accommodate additional features, therefore you should write your code in a modular fashion.

III. Objectives

1. Get familiarized with the operation of the Altera DE2 FPGA board, including the various peripherals, the switches, LEDs and LCD display. You may find online verilog examples useful. http://www.asic-world.com/examples/verilog/.
2. Implement and test the DPWM block as defined in Fig. 1 and Table 1.

Fig 1. DPWM Block specifications.

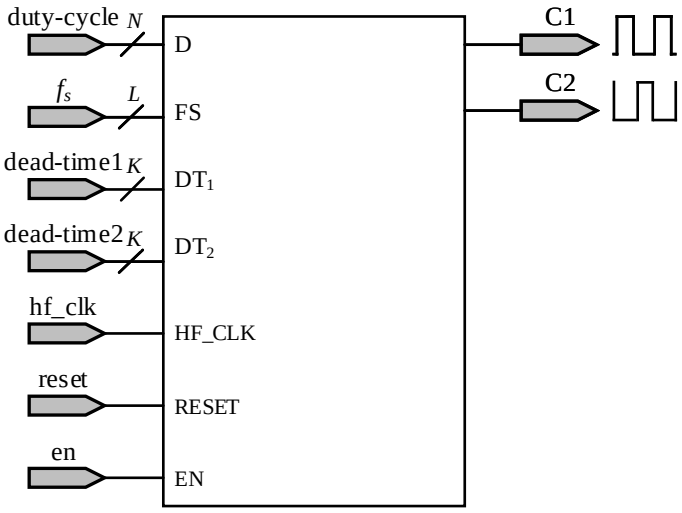

Table 1: DPWM Signals

Signal	Bits	Specification
D	N (design dependent)	Duty-cycle command coming from the digital controller. The resolution of the signal should be maximized at each switching frequency, based on the capabilities of the FPGA. The DPWM duty-cycle is updated only once per switching cycle and D is sampled on the rising edge of HF_CLK at the start of each switching cycle.
DT1, DT2	K (design dependent)	Control signals for the two independently adjustable dead-times. Each dead-time should be controllable within a range of ~ 10ns-100ns, with as much resolution as possible, given the clock frequency.
HF_CLK	1	High-frequency DPWM clock. The clock frequency should be generated internally and maximized to achieve the highest possible DPWM resolution at each target switching frequency. The clock frequency is limited by the FPGA hardware and must be constrained to avoid timing violations within the logic.
RESET	1	Asynchronous reset (active high) for the DPWM counter. Both C1 and C2 should be zero when in the reset mode.
EN	1	Enable signal used to disable both C1 and C2 during faults (without resetting the DPWM counter)
FS	L (design dependent)	Switching frequency control signal. The switching frequency can be adjusted by changing the counter settings. FS should be controllable within a range of 50-200 kHz with at least 10 values.

IV. Evaluation

1. Demonstrate the operation of your DPWM block to the TA, including the programmable frequency, programmable duty-cycle and programmable dead-time functionality. You should use the switches on the DE2 board to adjust these parameters. Use the scope to measure all relevant quantities.
2. Determine the maximum DPWM resolution over the range of f_s.
3. Using the scope determine the minimum and maximum duty-cycle, which is useful for dynamic operation (note the limitations of the oscilloscope when taking your measurements).