Version: 1.0

Technical Specification

MODEL NO: VD1400-MOA (ES120MC1)

The content of this information is subject to be changed without notice.

Please contact E Ink or its agent for further information.

☐Customer's Confirmation

Customer _____

Date _____

By _____

☐E Ink's Confirmation

Approved By Hero Chen

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Prepared By 丁建福

Revision History

Rev.	Issued Date	Revised Contents
1.0	20210728	Create

TECHNICAL SPECIFICATION

CONTENTS

1. Application

The VD1400-MOA is a reflective electrophoretic E Ink® display module based on the plastic active matrix TFT substrate and E Ink® FPL technology. It has a 12.0” active area with 2560(H) x 1600(V) pixels, the display is capable to display images with 16 grays driven by the external display controller and the associated waveform file.

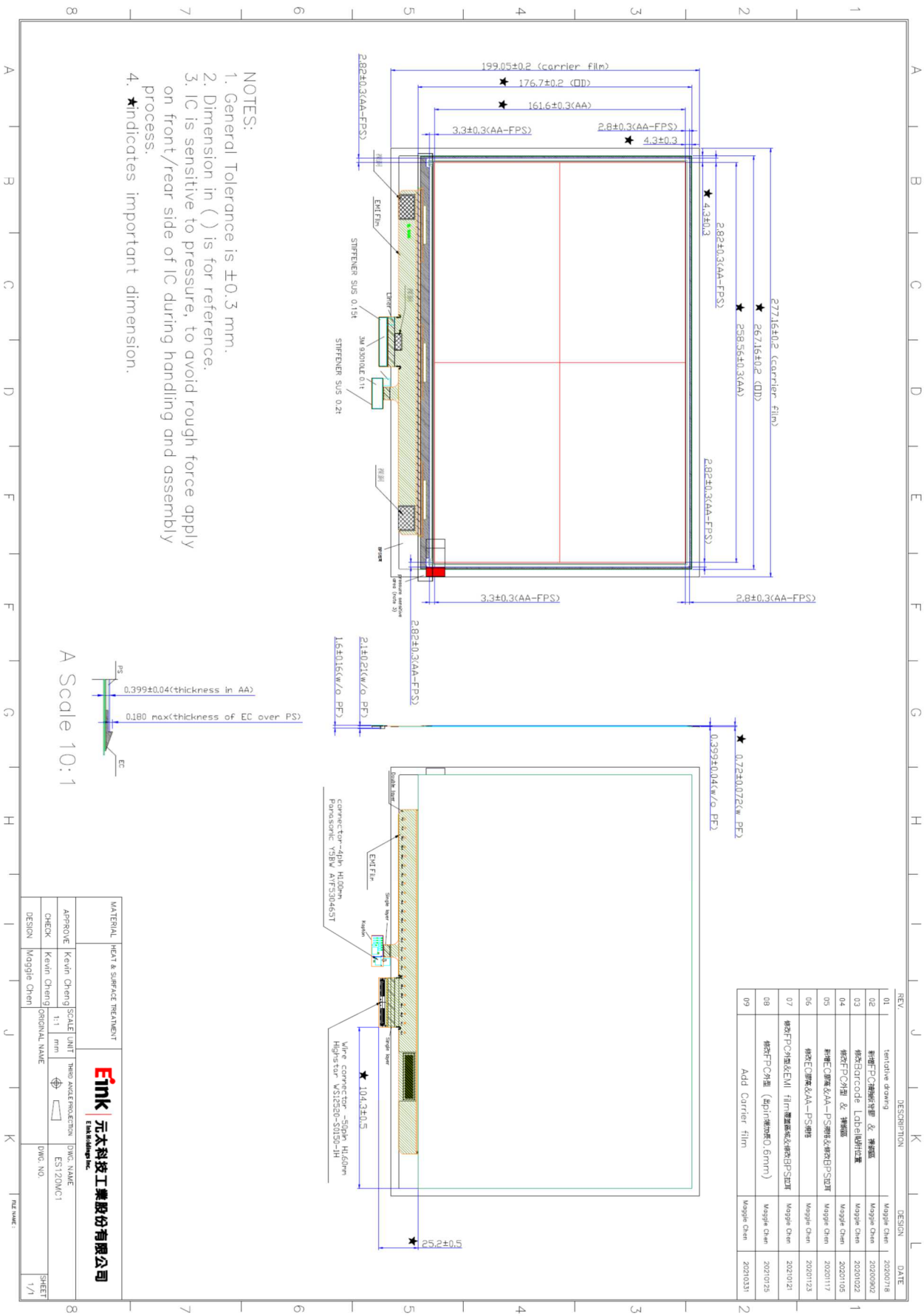
2. Features

- High contrast reflective/electrophoretic technology
- 2560(H) x 1600(V) display
- 16 grayscale
- Ultra-wide viewing angle
- Ultra-low power consumption
- Pure reflective mode
- Commercial temperature range
- Landscape type
- Plastic substrate

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	12.0	Inch	
Display Resolution	2560(H) x 1600(V)	Pixel	
Active Area	258.56(H) x 161.60(V)	mm	
Pixel Pitch	0.101(H) x 0.101(V)	mm	254dpi
Pixel Configuration	Square		
Outline Dimension	267.16(H) x 176.70(V) × 0.40 (D)	mm	
Module Weight	26.5	g	w/o FP
Number of Gray	16 Gray Level (monochrome)		Include white
Display operating mode	Reflective mode		
Surface treatment	Non		

4. Mechanical Drawing of EPD Module



5. Output Interface

5-1) Connector Type of Panel

Panel FPC side: Highstar WS12505-S0150-1H
Wire side: IPEX 20438-050T-*01

5-2) Pin Assignment of Panel

Pin #	Signal	I/O	Description	Remark
1	VGL	P	Negative power supply gate driver	
2	VGH	P	Positive power supply gate driver	
3	VDD	P	Digital power supply drivers(3.3V)	
4	OEV	I	Output mode selection gate driver	
5	CKV	I	Clock Gate Driver	
6	FPL_VCOM1	P	Common voltage	Note 5-3
7	TFT_VCOM	P	Common voltage	Note 5-3
8	VDD	P	Digital power supply drivers(3.3V)	
9	VSS	P	Ground	
10	CKH	I	Clock source driver	
11	D0	I	Data signal source driver	
12	D1	I	Data signal source driver	
13	D2	I	Data signal source driver	
14	D3	I	Data signal source driver	
15	D4	I	Data signal source driver	
16	D5	I	Data signal source driver	
17	D6	I	Data signal source driver	
18	D7	I	Data signal source driver	
19	D8	I	Data signal source driver	Cannot share pin with
20	D9	I	Data signal source driver	
21	D10	I	Data signal source driver	
22	D11	I	Data signal source driver	
23	D12	I	Data signal source driver	
24	D13	I	Data signal source driver	
25	D14	I	Data signal source driver	
26	D15	I	Data signal source driver	
27	VSS	P	Ground	
28	SPH	I	Start pulse source driver	
29	LEH	I	Latch enable source driver	
30	OEH	I	Output enable source driver	
31	XON	I	E Ink internal test pin	Note 5-2
32	VSH	P	Positive power supply source driver	

33	VSL	P	Negative power supply source driver	
34	Border	P	Border connection	
35	FPL_VCOM2	P	No Connection	
36	SHR_IN	I	Source Shift direction	Note 5-4
37	STL1_IN	I	Source Start pulse input	
38	STL2_IN	I	Source Start pulse input	
39	DISP_THRM_POS	I	Thermistors +	
40	DISP_THRM_GND	P	Thermistors GND	
41	UD_IN	I	Gate Shift direction	Note 5-5
42	STV1_IN	I	Gate Start pulse input	
43	STV2_IN	I	Gate Start pulse input	
44	NC		No Connection	
45	VSS	P	Ground	
46	VDD2	P	SPI flash power supply (1.8V)	
47	SPI_SCL	I	Serial Data Clock for Flash memory	Note 5-1
48	SPI_NCS	I	Chip Select for Flash memory	Note 5-1
49	SPI_SDI	I	Serial Data Input for Flash memory	Note 5-1
50	SPI_SDO	O	Serial Data Output for Flash memory	Note 5-1

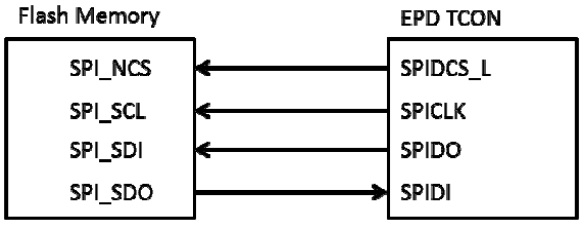
5-3) Connector Type of Panel (TR1)

Panasonic AYF530465T

5-4) Pin Assignment of Panel

Pin #	Signal	I/O	Description	Remark
1	DISP_THRM_POS	I	Temperature sensor input	Murata NCP18XH103
2	NC			
3	NC			
4	DISP_THRM_GND	P	Ground for temperature sensor	

Note 5-1



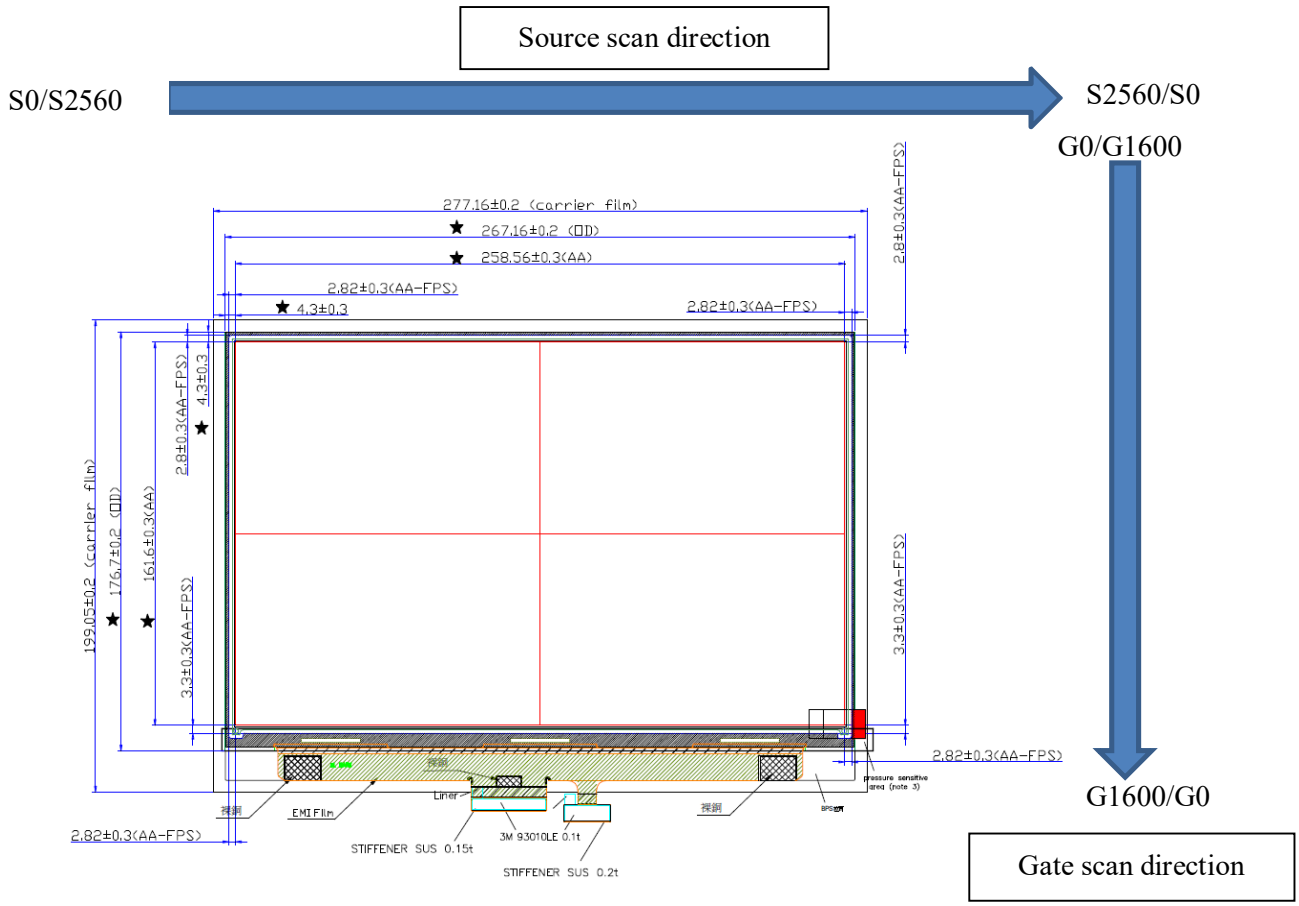
Note 5-2: Please connect to VDD voltage by 10K resistance.

Note 5-3: Connect to system board Vcom power.

Note 5-4: If SHR_IN = H, then the source starts pulse input to STL2_IN. If SHR_IN = L, then start pulse input to STL1_IN.

Note 5-5: If UD_IN = H, then gate start pulse input to STV1_IN. If UD_IN = L, then start pulse input to STV2_IN.

5-3) Panel Scan Directions



6. Electrical Characteristics

6-1) Absolute Maximum Ratings of the panel only

Parameter	Symbol	Rating	Unit	Remark
Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +5.0	V	--
Positive Supply Voltage	VSH	-0.3 to +18.0	V	--
Negative Supply Voltage	VSL	+0.3 to -18.0	V	--
Max Drive Voltage Range	VSH – VSL	36.0	V	--
Supply Voltage	VGH	-0.3 to VGL+50.0	V	--
Supply Voltage	VGL	-25.0 to +0.3	V	--
Supply Range	VGH-VGL	10.0 to +45.0	V	--
Operating Temp. Range	TOTR	0 to +50	℃	--
Storage Temperature	TSTG	-25 to +70	℃	--

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that VDD be constrained to the range GND < VDD. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either GND or VDD). Unused outputs must be left open. This device may be light-sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

6-2) Panel DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	V_{SS}		-	0	-	V
Logic Voltage supply	V_{DD}		3.0	3.3	3.6	V
	I_{VDD}	V_{DD}=3.3V		19.82	22.15	mA
SPI Voltage supply (Active)	V_{DD2}		1.65	1.8	1.95	V
	I_{VDD2}	V_{DD}=1.8V		19.82	22.15	mA
SPI Voltage supply (Standby)	V_{DD2}		1.65	1.8	1.95	V
	I_{VDD2}	V_{DD}=1.8V		0.2		mA
Gate Negative supply	V_{GL}		-20.5	-20	-20.5	V
	I_{GL}	V_{GL} =-20V		1.73	19.94	mA
Gate Positive supply	V_{GH}		27.5	28	28.5	V

	I_{GH}	V_{GH} = 28V		1.16	1.32	mA
Source Negative supply	V_{NEG}		-15.4	-15	-14.6	V
	I_{NEG}	V_{NEG} = -15V		1.34	156.74	mA
Source Positive supply	V_{POS}		14.6	15	15.4	V
	I_{POS}	V_{POS} = 15V		1.07	170.96	mA
Asymmetry source	V_{Asym}	V_{POS}+V_{NEG}	-800	0	800	mV
Common voltage	V_{COM}		-4	Adjusted	-0.1	V
	I_{COM}			0.91	1.3	mA
Power panel	P			170.45	5426.95	mW
Standby power panel	P_{STBY}			0.66		mW

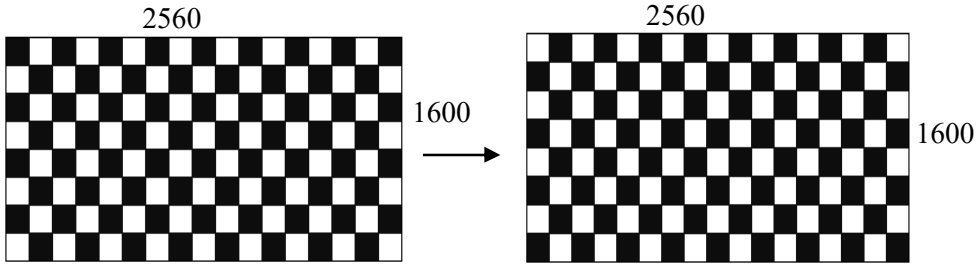
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Currents **(Note 5)**	ISH	VSH = 15V	-		472	mA
	ISL	VSL = -15V	-		432	mA
	IGH	VGH = 28V	-		192	mA
	IGL	VGL =-20V	-		164	mA
	ICOM	--	-		-	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Input “H” voltage	VIH	--	0.8VDD		VDD	V
Digital Input “L” voltage	VIL	--	GND		0.2VDD	V

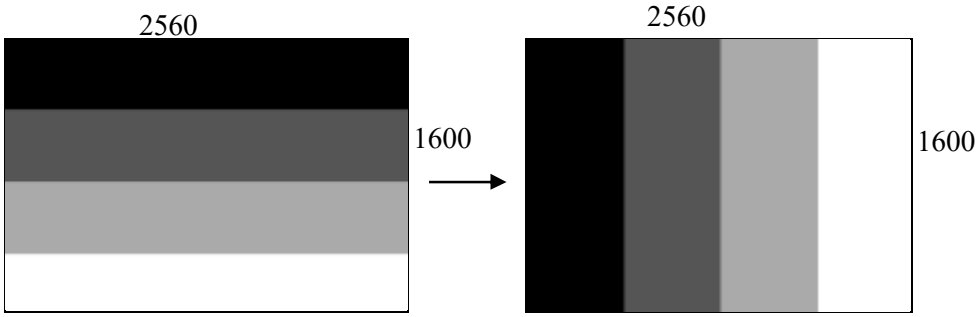
Note:

1. The power consumption in this field is provided for the purpose as follows:
   1-1. The selection of suitable PMIC in the market to drive EPD normally.
   1-2. Estimation of voltage-drop at the input side of PMIC for the setting of threshold-voltage of battery.
2. The maximum average Currents for power consumption are measured using a 75 Hz waveform with the following pattern transition in both B/W: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)
3. The Typical average current for power consumption is measured using a 75 Hz waveform with the following pattern transition:
   3-1. For displays with a grayscale image, it is from horizontal 4 grayscale patterns to vertical 4 grayscale patterns without dithering process. (Note 6-2)
4. The standby power is the consumed power when the panel controller is in standby mode.
5. The Maximum Currents are measured using a 75 Hz waveform with the following pattern transition in both B/W: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)
   - It is performed with decoupling capacitors on each power rail as below table (Note 6-3).
   - The minimum value in the table of Maximum current is produced by the charging mechanism between decoupling capacitors.
6. The listed electrical/optical characteristics are only guaranteed under the controller and waveform provided by E Ink.
7. Vcom is recommended to be set in the range of assigned value ± 0.1 V
8. Use of measuring instruments: Oscilloscope0 (Model: Tektronix MDO3024)

Note 6-1:
The maximum average current and Maximum Currents for B/W



Note 6-2:
The typical power consumption for B/W display



Note 6-3:
The decoupling capacitors on each power rail for Max. Currents

Power rail	Capacitors suggested (uF / Tolerance)
ISH	4.7uF x 2pcs / ±10%
ISL	4.7uF x 2pcs / ±10%
IGH	2.2 uF x 1 pcs / ±10%
IGL	4.7uF x 1 pcs / ±10%
IDD	4.7uF x 1 pcs / ±10%

6-3) Panel DC Characteristics for Device Battery-Life Estimation

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	V_{SS}		-	0	-	V
Logic Voltage supply	V_{DD}		3.0	3.3	3.6	V
	I_{VDD}	V_{DD}=3.3V		19.82	22.15	mA
SPI Voltage supply (Active)	V_{DD2}		1.65	1.8	1.95	V
	I_{VDD2}	V_{DD}=1.8V		19.82	22.15	mA
SPI Voltage supply (Standby)	V_{DD2}		1.65	1.8	1.95	V
	I_{VDD2}	V_{DD}=1.8V		0.2		mA
Gate Negative supply	V_{GL}		-20.5	-20	-20.5	V
	I_{GL}	V_{GL} =-20V		1.73	9.96	mA
Gate Positive supply	V_{GH}		27.5	28	28.5	V
	I_{GH}	V_{GH} = 28V		1.16	1.2	mA
Source Negative supply	V_{NEG}		-15.4	-15	-14.6	V
	I_{NEG}	V_{NEG} = -15V		1.34	67.99	mA
Source Positive supply	V_{POS}		14.6	15	15.4	V

	I_{POS}	V_{POS} = 15V		1.07	61.41	mA
Asymmetry source	V_{Asym}	$V_{POS}+V_{NEG}$	-800	0	800	mV
Common voltage	V_{COM}		-4	Adjusted	-0.1	V
	I_{COM}			0.91	1.09	mA
Power panel	P			170.456	2249.075	mW
Standby power panel	P_{STBY}			0.6		mW

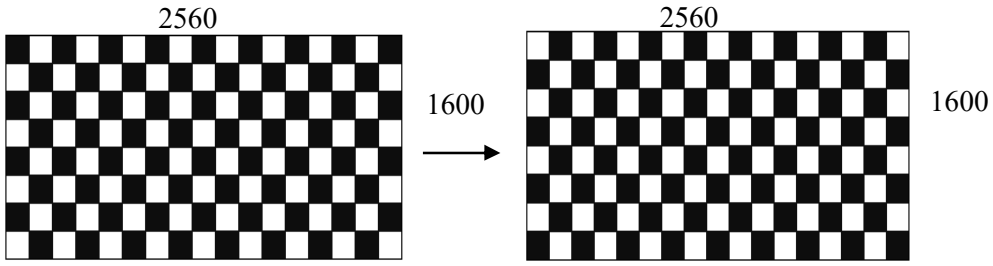
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Currents (Note 5)	ISH	V_{SH} = 15V	-		472	mA
	ISL	V_{SL} = -15V	-		432	mA
	IGH	V_{GH} = 28V	-		192	mA
	IGL	V_{GL} =-20V	-		164	mA
	ICOM	--	-		-	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Input “H” voltage	VIH	--	0.8VDD		VDD	V
Digital Input “L” voltage	VIL	--	GND		0.2VDD	V

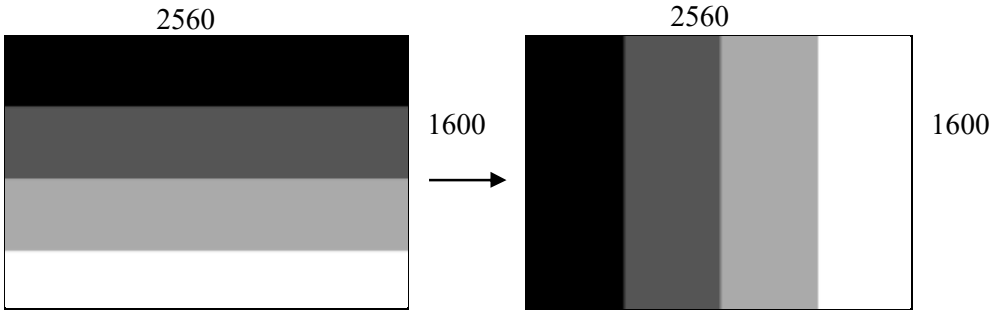
Note :

1. The power consumption in this field is measured in whole updated time by 400 ms (at 25 degrees C) for device battery life estimation.
2. The maximum average Currents for power consumption are measured using a 75 Hz waveform with the following pattern transition in both B/W: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-4)
3. The Typical average current for power consumption is measured using a 75 Hz waveform with the following pattern transition:
   3-1. For displays with a grayscale image, it is from horizontal 4 grayscale patterns to vertical 4 grayscale patterns without dithering process. (Note 6-5)
4. The standby power is the consumed power when the panel controller is in standby mode.
5. The Maximum Currents are measured using a 75 Hz waveform with the following pattern transition in both B/W: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-4)
   - It is performed with decoupling capacitors on each power rail as below table (Note 6-6).
   - The minimum value in the table of Maximum current is produced by the charging mechanism between decoupling capacitors.
6. The listed electrical/optical characteristics are only guaranteed under the controller and waveform provided by E Ink.
7. Vcom is recommended to be set in the range of assigned value ± 0.1 V
8. Use of measuring instruments: Oscilloscope (Model: Tektronix MDO3054)

Note 6-4
The maximum average current and Maximum Currents for B/W.



Note 6-5
The typical power consumption for B/W display.



Note 6-6
The decoupling capacitors on each power rail for Max. Currents

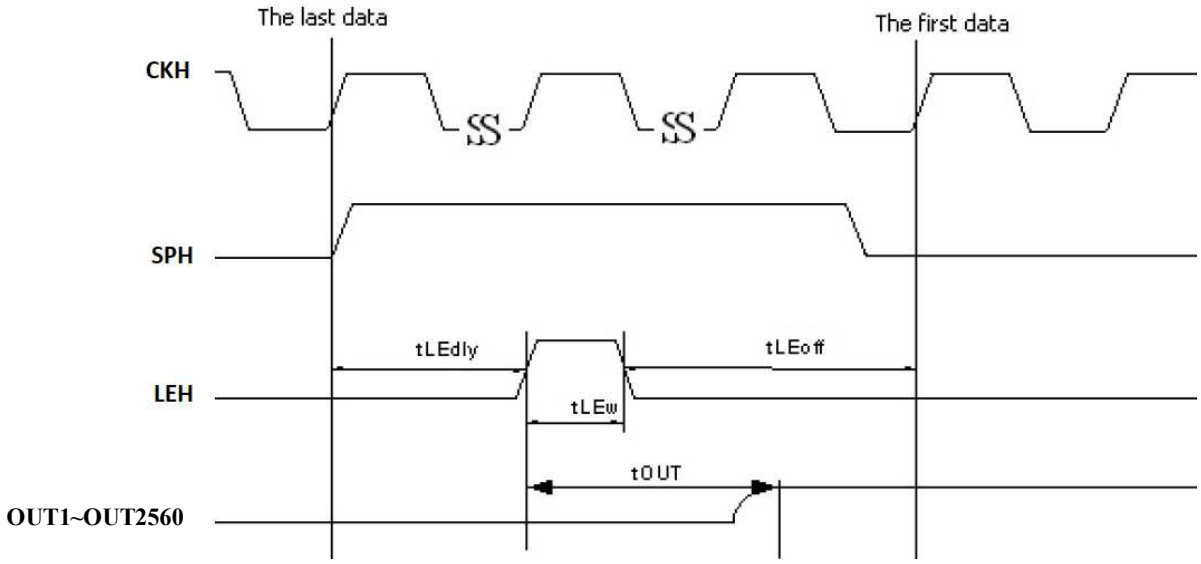
Power rail	Capacitors suggested (uF / Tolerance)
ISH	4.7uF x 2pcs / ±10%
ISL	4.7uF x 2pcs / ±10%
IGH	2.2 uF x 1 pcs / ±10%
IGL	4.7uF x 1 pcs / ±10%
IDD	4.7uF x 1 pcs / ±10%

6-4) Panel AC characteristics

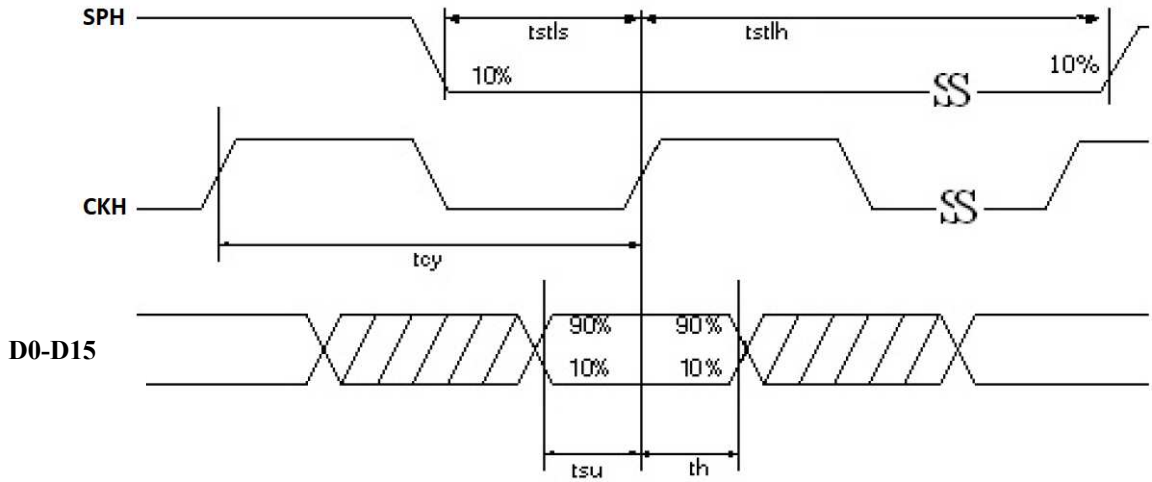
The following specifications apply for: VDD - VSS = 3.0V to 3.6V, TOPR = 25°C, CL=20pF

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
Clock frequency	fckv	-	-	200	kHz
Minimum “L” clock pulse width (for V_{DD}=3.3V)	twL	500			ns
Minimum “H” clock pulse width (for V_{DD}=3.3V)	twH	500			ns
Clock rise time	trckv	-	-	100	ns
Clock fall time	tfckv	-	-	100	ns
SPV setup time	tSU	100	-	twH-100	ns
SPV hold time	tH	100	-	twH-100	ns
Pulse rise time	trspv	-	-	100	ns
Pulse fall time	tfspv	-	-	100	ns
Clock CKH cycle time (for V_{DD}=3.3V)	tcy	16.67		-	ns

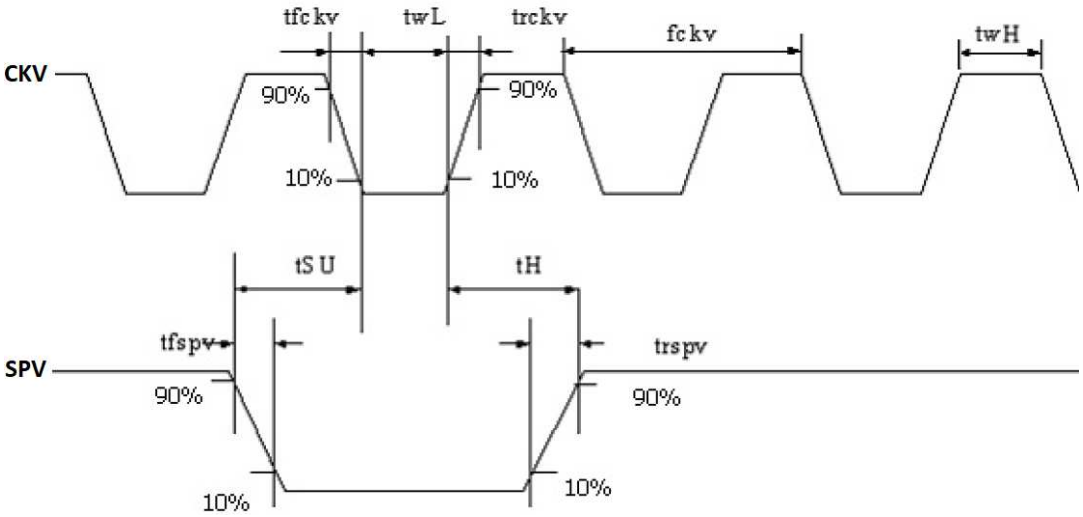
D0 ~ D15 setup time (for V_{DD}=3.3V)	tsu	8	-	-	ns
D0 ~ D15 hold time (for V_{DD}=3.3V)	th	8	-	-	ns
SPH setup time	tstls	0.5* tcy	-	0.8* tcy	ns
SPH hold time	tstlh	0.5* tcy	-		ns
LEH on delay time (for V_{DD}=3.3V)	tLEdly	10.5* tcy	-	-	ns
LEH high-level pulse width (When VDD=2.5V to 3.6V)	tLEw	300	-	-	ns
LEH off delay time (for V_{DD}=3.3V)	tLEoff	200	-	-	ns
Output setting time to +/- 30mV(C_{load}=200pF)	tout	-	-	20	us



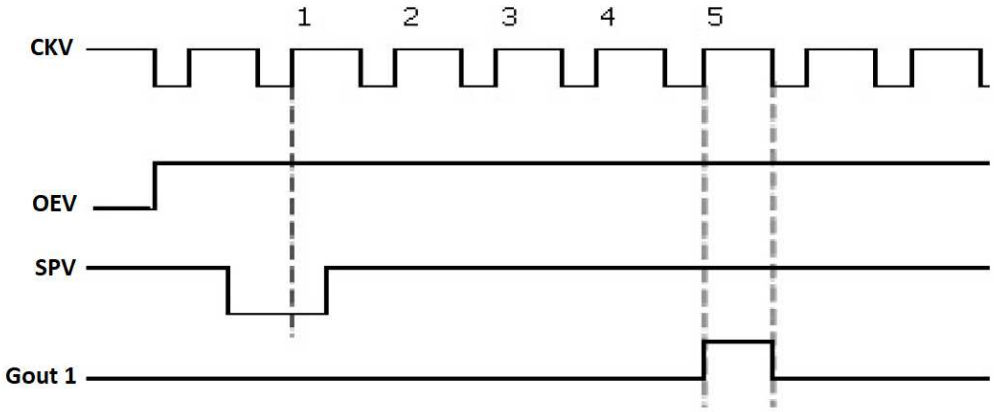
Output latch control signals



Clock & data timing



CKV & SPV timing



Gate output timing

Note：First gate line on timing.

6-5) Refresh Rate

The module was applied at a maximum refresh rate of 75 Hz.

Parameter	Min	Max
Refresh Rate	-	75 Hz

6-6) Data transmission waveform

This timing mode is depicted in Figure 6-1 and Figure 6-2 and it refers to the timing of Source Driver Output Enable (OEH) and Gate Driver Clock (CKV). Note, that in this mode LGON follows CKV timing.

Mode	3	Resolution 2560x1600				
SDCK[MHz]	44.00					
Pixels per SDCK	8					
Line Parameters [SDCK]	LSL	LBL	LDL	LEL	GDCK_STA	LGONL
	14	10	320	18	4	264
Line Parameters [us]	-	-	-	-	-	-
	0.32	0.23	7.27	0.40	0.09	6.00
Frame Parameters [Lines]	FSL	FBL	FDL	FEL	-	FR[Hz]
	1	4	1,600	18	-	74.99
Frame Parameters[us]	-	-	-	-	-	-
	8.22	32.86	13145.45	147.89	-	-

Timing parameters table

Note:

1. For parameters definition, see EPD panel timing.
2. For Isis controller GDCK_STA and LGONL are not settable parameters; GDCK_STA = LBL, LGONL = LDL + 0.5
3. For Freescale SOC GDOE low pulse represent FSL and GDSP pulses with the first period of FBL.

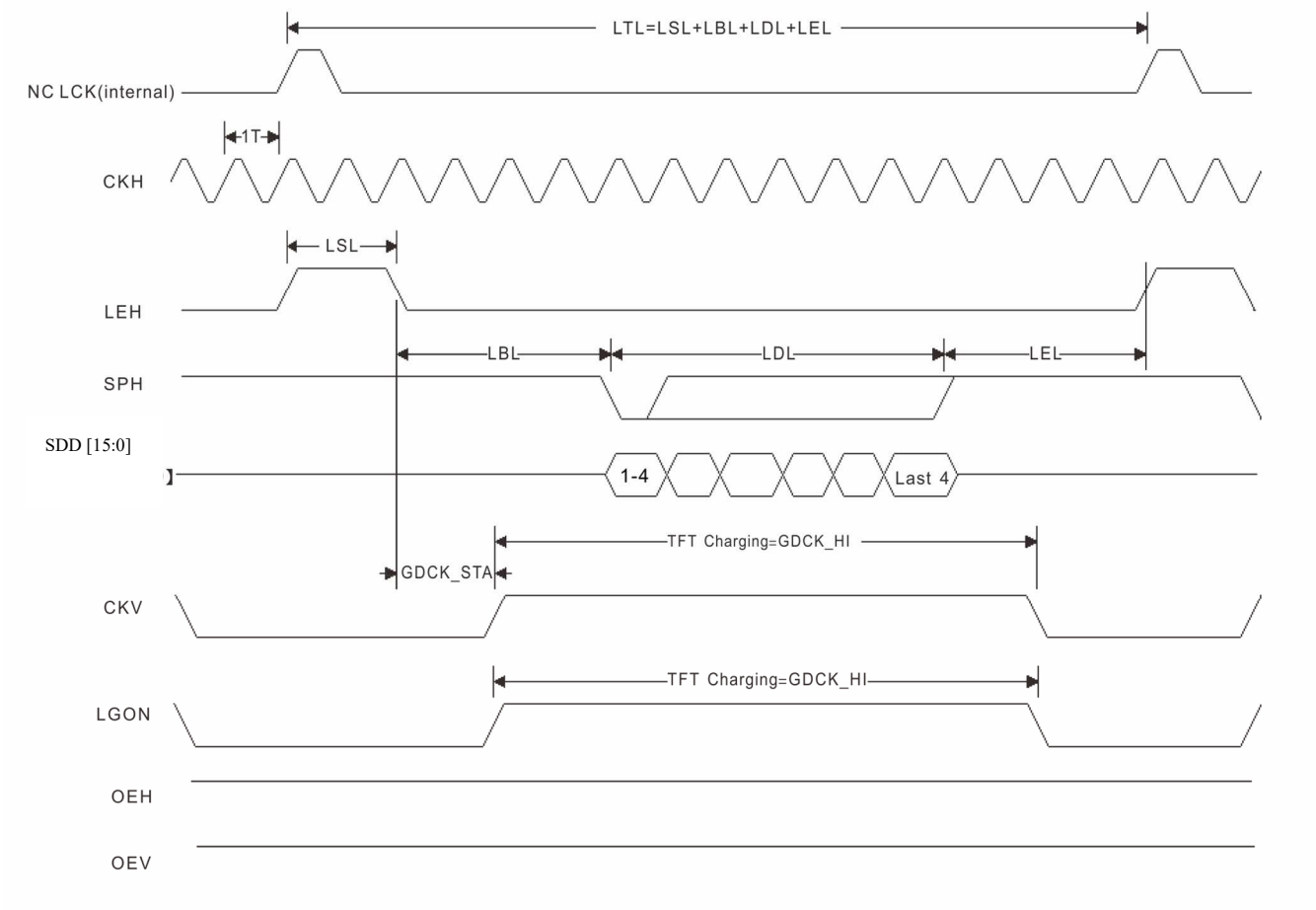


Figure 6-1 Line Timing in Mode 3

Note: LCK is an internal signal and it is shown for reference only.

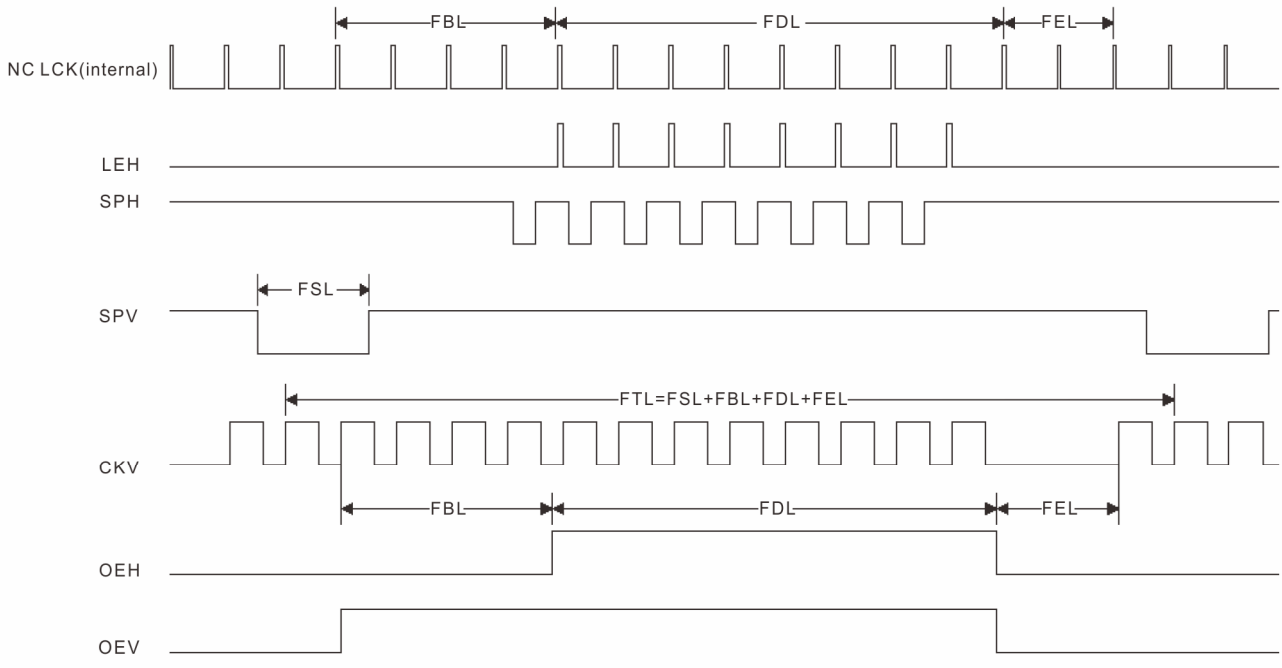


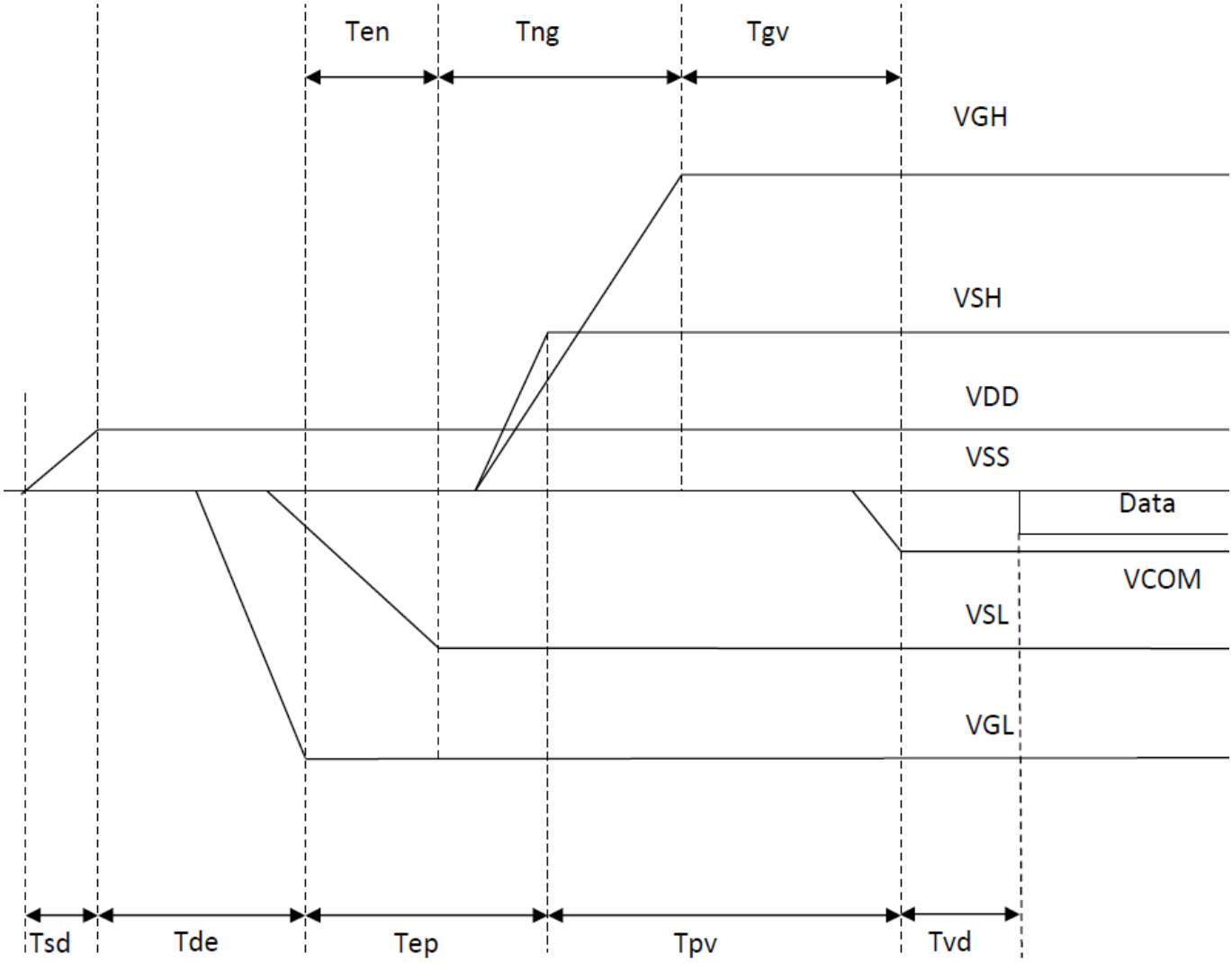
Figure 6-2 Frame Timing in Mode 3

7. Power Sequence

To prevent IC failure in power resetting, the power sequence must be followed as below.

7-1) Power on Sequence

Power Rails must be sequenced in the following order：
1. VSS → VDD → VNEG → VPOS (Source driver) → VCOM
2. VSS → VDD → VGL → VGH (Gate driver)

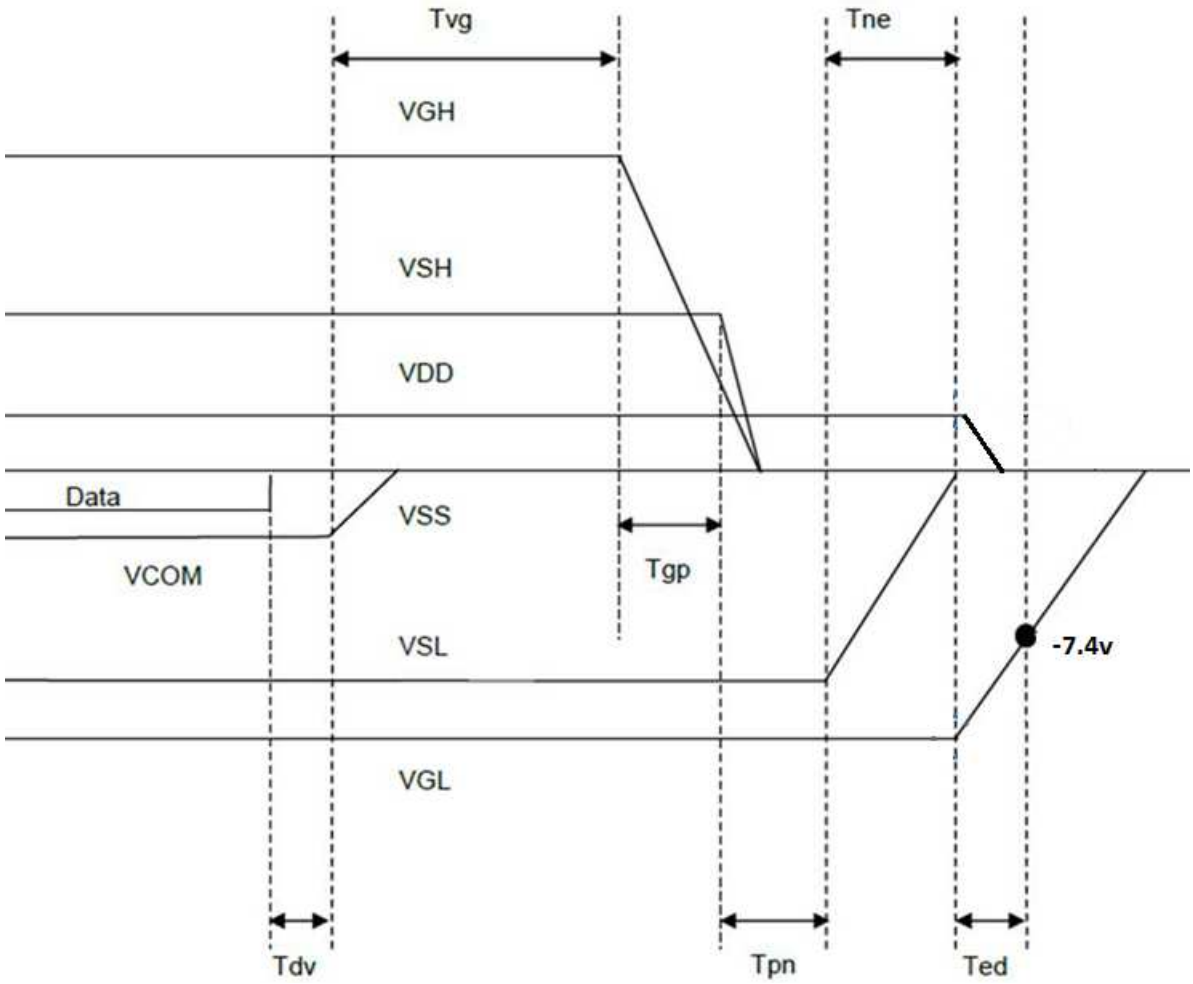


Power-on sequence

	Min	Max
Tsd	30us	-
Tde	100us	-
Tep	1000us	-
Tpv	100us	-
Tvd	100us	-
Ten	0us	-

Tng	1000us	-
Tgv	100us	-

7-2) Power off Sequence



Power-off sequence

	Min	Max	Remark
Tdv	100µs	-	-
Tvg	0µs	-	-
Tgp	0µs	-	-
Tpn	0µs	-	-
Tne	0µs	-	-
Ted	0.5s	-	Discharged point @ -7.4 Volt

Note 7-1：Supply voltages decay through pull-down resistors.

Note 7-2: Begin to turn off VGL power after VNEG and VPOS are completely or almost discharged to GND state.

Note 7-3：VGL must remain negative of Vcom during the decay period

8. Optical Characteristics

8-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

T = 25°C

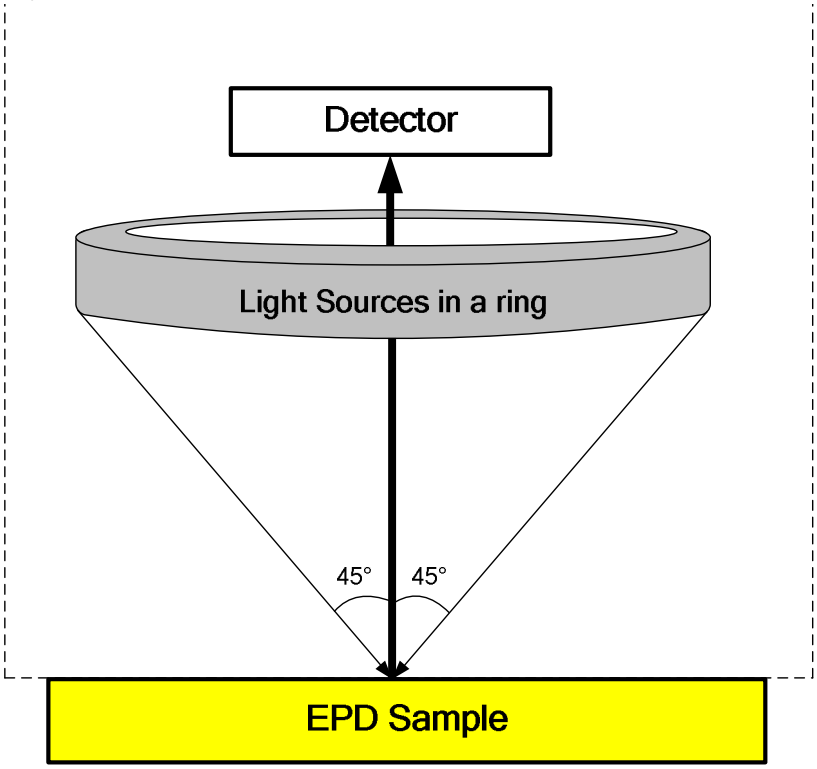
Symbol	Parameter	Conditions	Min	Typ.	Max	Unit	Note
R	Reflectance	White	32	42	-	%	Note 9-1
Gn	Nth Grey Level	-	-	DS+(WS-DS)×n/(m-1)	-	L*	-
CR	Contrast Ratio	-	12	18	-		-

WS: White state, DS: Dark state, Gray state from Dark to White: DS、G1、G2…、Gn…、Gm-2、WS
m: 4、8、16 when 2、3、4 bits mode
Note 8-1: Luminance meter: Eye-One Pro Spectrophotometer.

8-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):

CR = Rl/Rd



8-3) Reflection Ratio

The reflection ratio is expressed as：
R = Reflectance Factorwhite board × (Lcenter / Lwhite board)
Lcenter is the luminance measured at the center in a white area (a* ~ b* ~ 0). Lwhite board is the luminance of a standard whiteboard. Both are measured with an equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9. Handling, Safety, and Environmental Requirements and Remark

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied to the active area and the back of a glass. For the best part, it is not allowed.
The module storage environment must be under reliability test storage items criteria.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface to protect the EPD. A transparent protective plate should have sufficient strength to resist an external force.
(3) You should adopt a radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by the electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers, or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hands or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene, and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long-time contact with PS causes deformations and color fading.

Datasheet status	
Product specification	This datasheet contains formal product specifications.
Limiting values	
Limiting values given are by the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification are not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

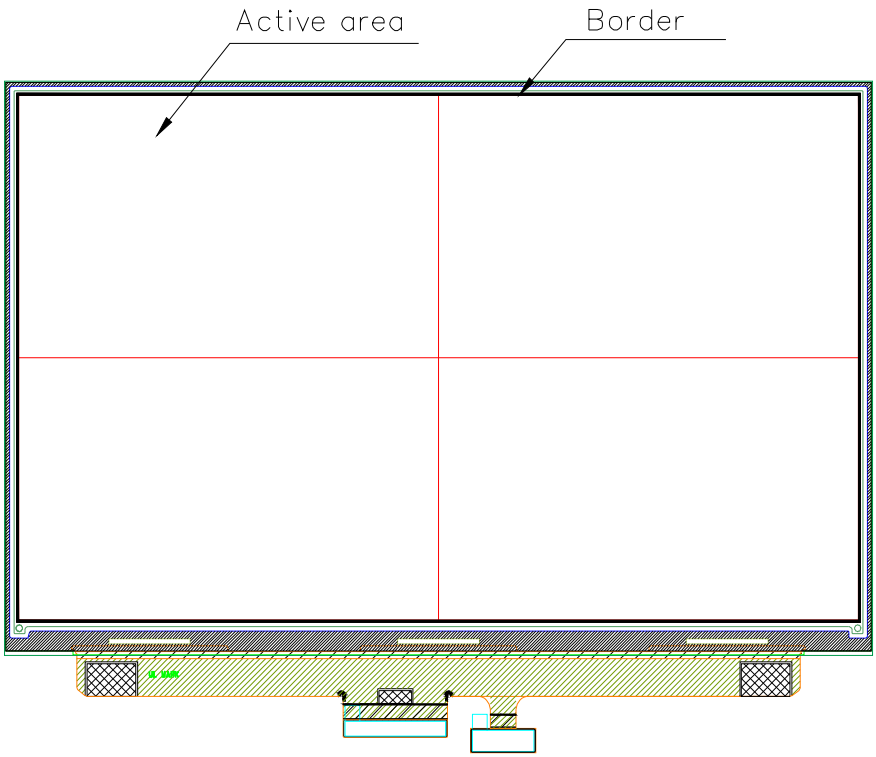
10. Reliability Test

ITEM	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = +50°C, RH = 30% for 240hrs	IEC 60 068-2-2Be	--
2	Low-Temperature Operation	T = 0°C for 240hrs	IEC 60 068-2-1Ae	--
3	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168hrs	IEC 60 068-2-78	
4	Low-Temperature Storage	T = -25°C for 240hrs (Test in white pattern)	IEC 60 068-2-1Ab	
5	High Temperature High Humidity Storage	T=+60C RH=80% for 240hrs (Test in White Pattern)	IEC 60 068-2-78	
6	High Temperature Storage	T=+70C RH=40% for 240hrs (Test in White Pattern)	IEC 60 068-2-2 Bb	--
7	Temperature Cycle	-25℃→ +70℃, 100 Cycles 30mins - 30mins (Test in white pattern)	IEC 60 068-2-14Nb	--
8	Solar radiation test	765 W/m^2 for 168hrs,40℃ (Test in white pattern)	IEC 60068-2-5Sa	--
9	Electrostatic Effect (non-operating)	(Machine model)+/- 250V 0Ω, 200pF	IEC 62179 IEC 62180	--

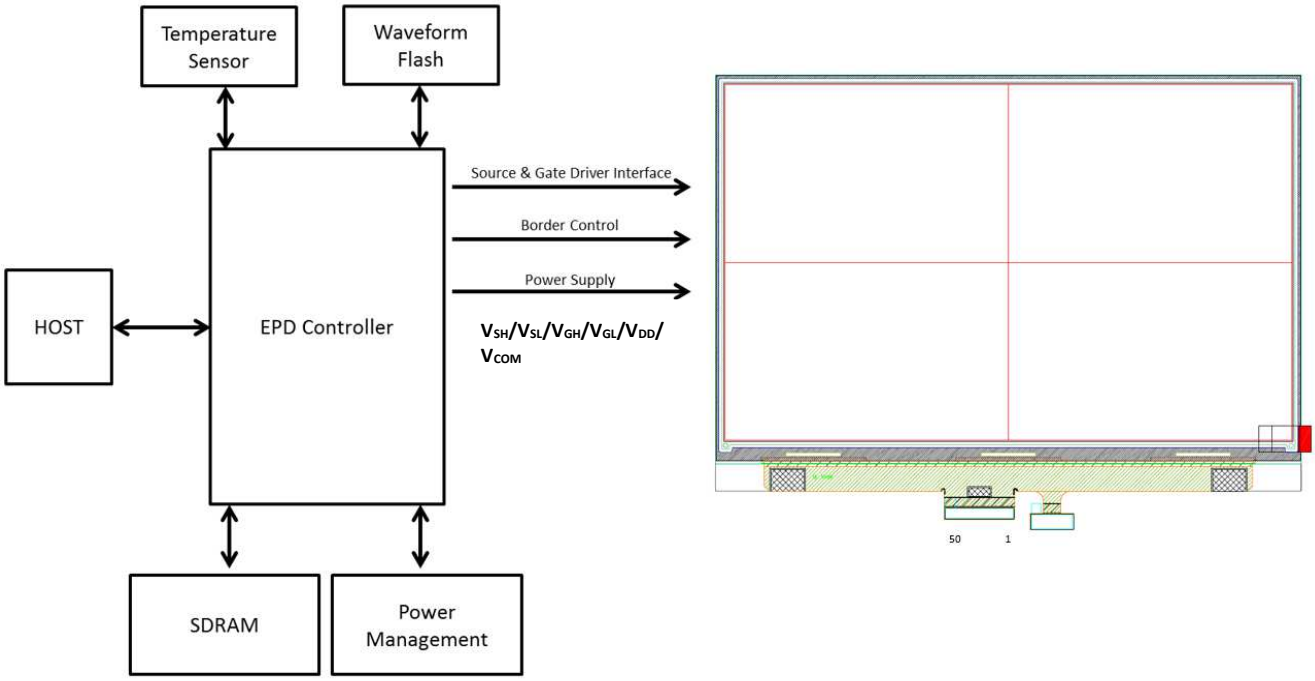
Note: The protective film must be removed before the temperature test.

[Criteria]
n the standard conditions, there is not display function NG issue occurred. (Including line defect, no image). All the cosmetic specification is judged before the reliability stress.

11. Border definition

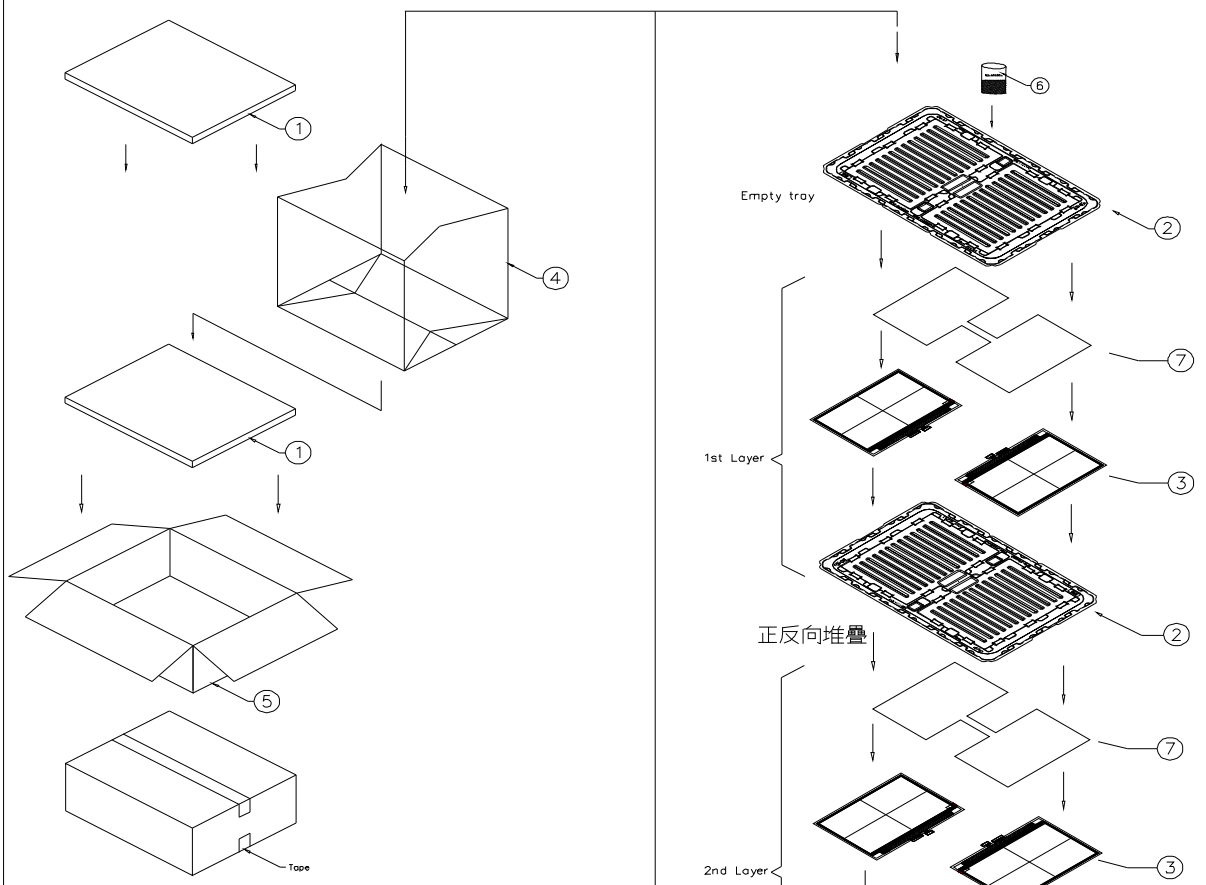


12. Block diagram



13. Packing

REV	DESCRIPTION	DESIGN	DATE
01	INITIAL RELEASE	Maggie Chen	20210409



NOTE:

1. One layer include: 2 pcs panel,
   1 pc epe cusion sheet & 1 pc tray
2. Q'TY: 24 pcs panel/carton.
3. Dimension: 558*370*170mm
4. Tray 需 180°堆疊, 堆疊後可從側邊檢視圓弧防呆方向是否正確

ITEM	DESCRIPTION	Q'TY	REMARK
7	EPE CUSHION SHEET	12	抗靜電
6	30g加厚複合紙活礦乾燥劑 73*95mm(禹科JK0030)	2	
5	CARTON INTERNAL	1	
4	FOLDED BAG,OTHER(562*393*593)	1	抗靜電
3	ES120MC1	24	
2	TRAY	13	抗靜電
1	EPE FOAM	2	

MTL.SPEC.	UNSPECIFIED TOL'S ±5.0mm ANGLE ROUGHNESS	REMARK	E Ink 元太科技工業股份有限公司 E Ink Holdings Inc.

APPROVE	Kevin Cheng	SCALE	UNIT	SHEET	DWG.TITLE
CHECK	Kevin Cheng	1:1	mm	1 OF 1	ES120MC1 PACKING
DESIGN	Maggie Chen	MTL.NO.		DWG.NO.	A4 SIZE