RELAY CONTROL CHART

CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

JUMPER TABLE

JP#	ON	OFF
1		
2		
3		
4		
5		

* SEE ASSEMBLY INSTRUCTIONS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

CUSTOMER NOTICE:

ANALOG DEVICES HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATION; HOWEVER IT REMAINS THE CUSTOMER RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT ANALOG DEVICES APPLICATIONS ENGINEERING FOR ASSISTANCE
THIS CIRCUIT IS PROPRIETARY TO ANALOG DEVICES AND SUPPLIED FOR USE WITH ANALOG DEVICES PARTS.

P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER

	DATE
TEMPLATE ENGINEER -	
HARDWARE SERVICES Pat Sheahan	
HARDWARE SYSTEMS -	
TEST ENGINEER -	
COMPONENT ENGINEER -	
TEST PROCESS -	
HARDWARE RELEASE -	
DESIGNER -	
PTD ENGINEER Cian McNamara	
CHECKER -	

SCHEMATIC

ANALOG DEVICES

Customer Evaluation: EVAL-AD4131-8WARDZ
-
-
<User Define>
<User Define>
<User Define>
TBD
Product(s): AD4131

MASTER PROJECT TEMPLATE: <MASTER_PROJECT_TEMPLATE>
TESTER TEMPLATE: <TESTER_TEMPLATE>

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES

DECIMALS	FRACTIONS	ANGLES
X.XX +-0.010 X.XXX +-0.005	+-1/32	+-2

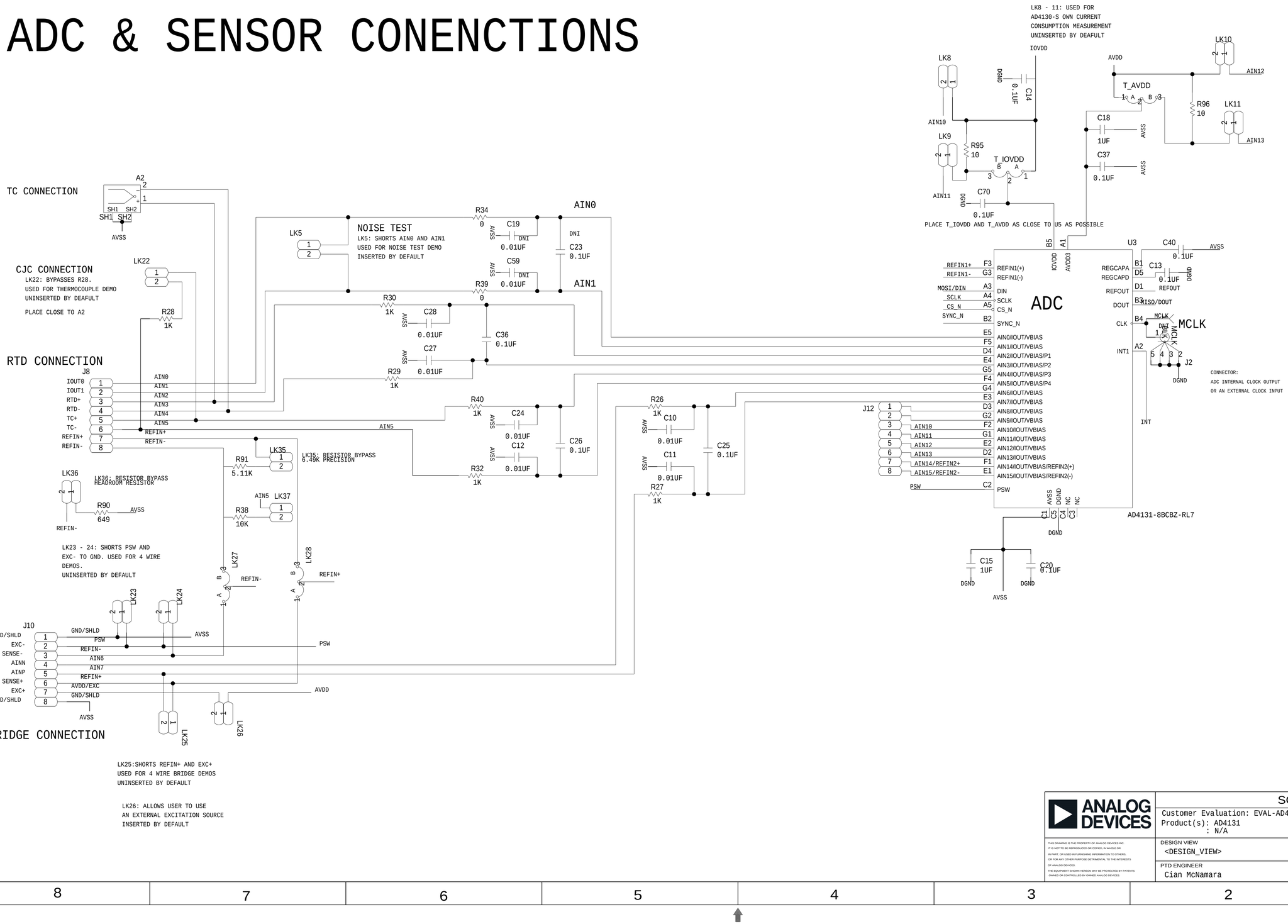
DRAWING NO. 02-065889
REV. C

SIZE	SCALE	CODE ID NO.	SHEET
C	1:1	CodeID	1 OF 6

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

AD4131-8 16-BIT 2.4KSPS (SETTLED) SD ADC

ADC & SENSOR CONENCTIONS



SCHEMATIC

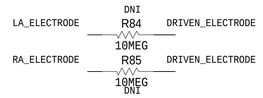
Customer Evaluation: EVAL-AD4131-8WARDZ
Product(s): AD4131
: N/A

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02-065889	C
PTD ENGINEER	SIZE / SCALE	SHEET 2 OF 6
Cian McNamara	D / 1:1	

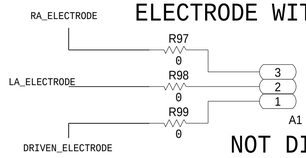
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

PAGE3:ECG CONNECTION

LK 30 - 32 ALLOW TO DISCONNECT
A! FROM THE ANALOG INPUTS



A1 ALLOWS THE USER TO CONNECT AN ECG
ELECTRODE WITH A 3.5MM JACK, AT THEIR OWN RISK



NOT DIFIBULATOR PROTECTED

ANALOG DEVICES

SCHEMATIC

Customer Evaluation: EVAL-AD4131-8WARDZ
Product(s): AD4131
: N/A

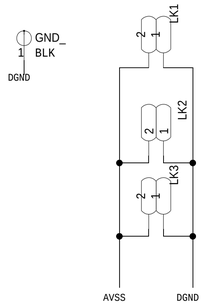
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02-065889	C

PTD ENGINEER	SIZE	SCALE	SHEET	OF
Cian McNamara	D	1:1	3	6

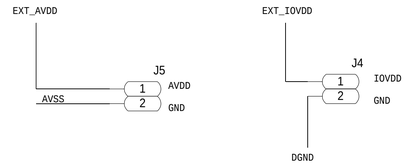
PAGE4: BOARD SUPPLIES

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

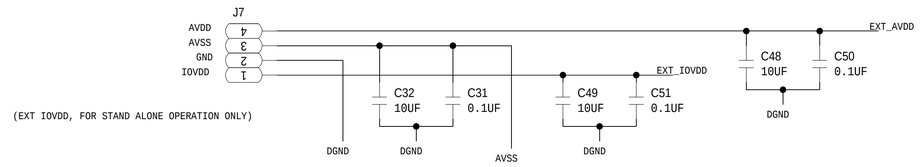
CONNECT AVSS AND AGND FOR 3.3V SUPPLY
DISCONNECT FOR +/- 1.8V OPERATION

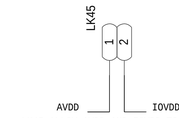


EXTERNAL VOLTAGE CONNECTOR FOR SCP BOARDS



EXTERNAL VOLTAGE CONNECTOR IF SEPARATE SUPPLY IS REQUIRED IN STAND ALONE CONFIGURATION
OR TO ALLOW FOR EXTERNAL SOLIT SUPPLY OPERATION +/-1.8V

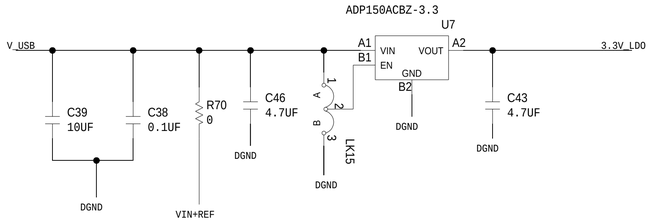




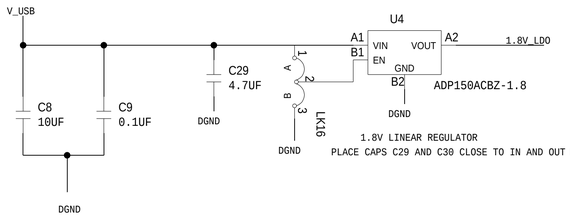
LK45 ALLOW AVDD AND IOVDD TO
BE POWERED OFF OF ONE SUPPLY

3.3V & 1.8V REGULATORS

3.3V LINEAR REGULATOR

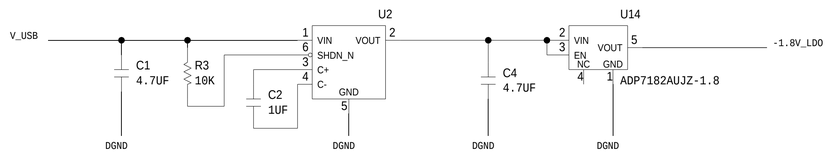


ON BOARD LDO 3.3V OR 1.8V

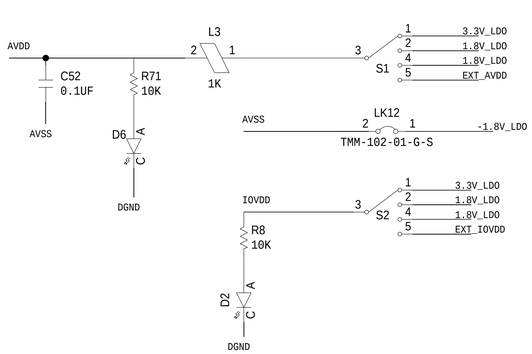


1.8V LINEAR REGULATOR
PLACE CAPS C29 AND C30 CLOSE TO IN AND OUT PINS

LTC1983ES6-3#TRMPBF



AVDD/AVSS/IOVDD



POS 1) AVDD: 3.3V, AVSS: 0V, IOVDD: 3.3V
POS 2) AVDD: 1.8V, AVSS: 0V, IOVDD: 1.8V
POS 3) AVDD: 1.8V, AVSS: -1.8V, IOVDD: 1.8V
POS 4) AVDD: EXT, AVSS: EXT, IOVDD: EXT

ANALOG DEVICES

SCHEMATIC

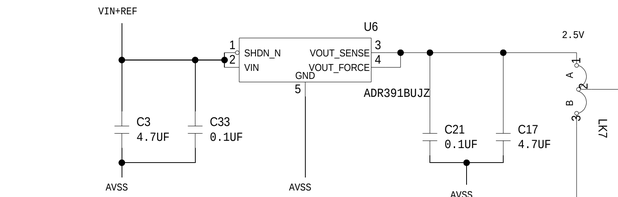
Customer Evaluation: EVAL-AD4131-8WARDZ
Product(s): AD4131
: N/A

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02-065889	C
PTD ENGINEER	SIZE / SCALE	SHEET 4 OF 6
Cian McNamara	D / 1:1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

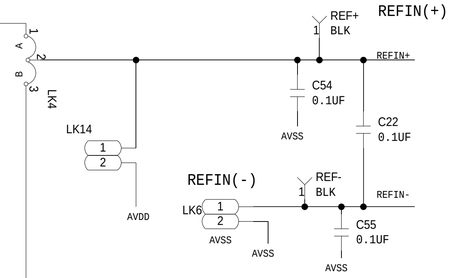
PAGE 5: VOLTAGE REFERENCE

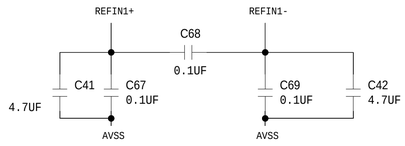
VOLTAGE REF

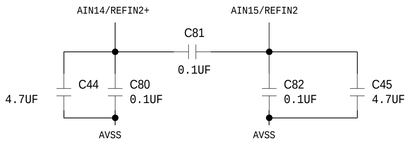


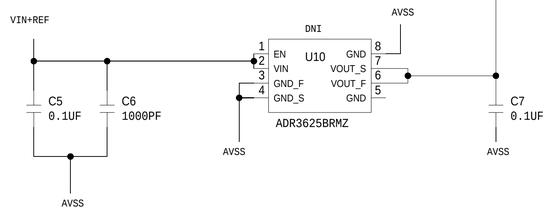
VOLTAGE REF

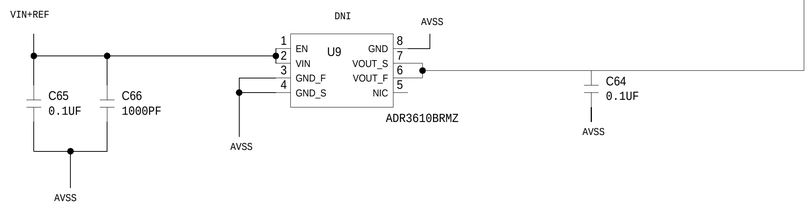
1) 2.5V FROM EITHER U6 (LK7 POS A) OR U10 (LK7 POS B)
2) 1.25V FROM U11 (LK4 POS B)



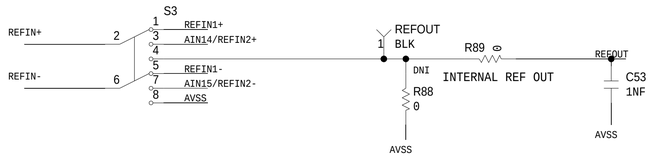








OS203012MU5QP1

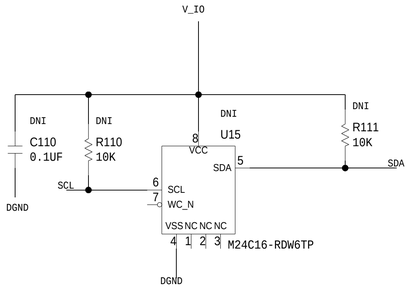


ANALOG DEVICES	SCHEMATIC			
	Customer Evaluation: EVAL-AD4131-8WARDZ Product(s): AD4131 : N/A			
DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02-065889		REV C
PTD ENGINEER Cian McNamara		SIZE D	SCALE 1:1	SHEET 5 OF 6

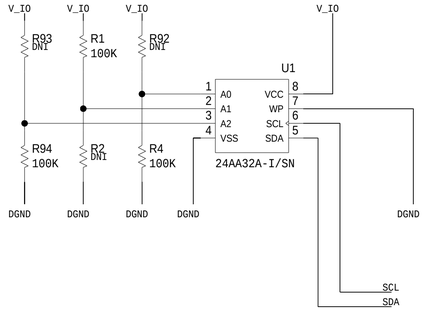
PAGE 6: MICRO HEADERS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

EEPROM DHC/VSM_M8 NRF

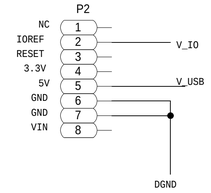


EEPROM SDP-K1

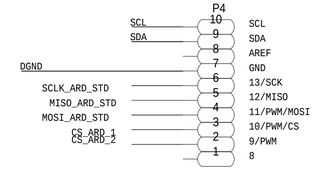


ARDUNIO HEADER

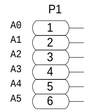
POWER



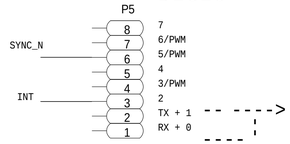
DIGI1



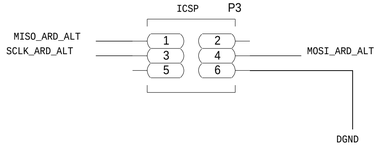
ANALOG IN

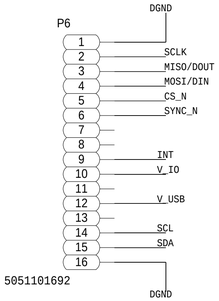


DIGI0



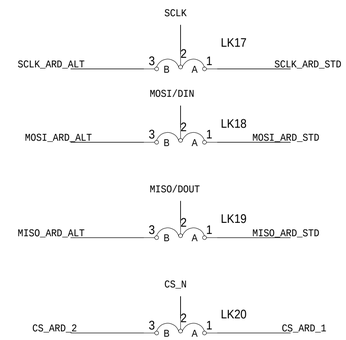
ICSP





SHORT TO ALLOW THE CLK PIN TO BE
USED AS A INTERRUPT FOR THE FIFO

LK29: PULL DOWN RESISTOR FOR THE MCLK PIN.
INSERTED: FOR CURRENT CONSUMPTION TEST.
UNINSERTED: FOR EXTERNAL USE OF CLK PIN OR IF
INT CLOCK WANTS TO BE CHECKED

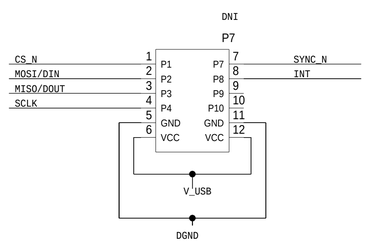


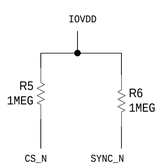
STD = STANDARD CONNECTION

ALT = ALTERNATE CONNECTION

DEFAULT A

PMOD 12 PIN HEADER





PULL UP RESISTORS FOR CHIP SELECT AND THE SYNC PIN

ANALOG DEVICES

SCHEMATIC

Customer Evaluation: EVAL-AD4131-8WARDZ
Product(s): AD4131
: N/A

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	02-065889	C

PTD ENGINEER	SIZE	SCALE	SHEET
Cian McNamara	D	1:1	6 OF 6