name:	Vince Rothenberg
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1. What is an Interrupt Service Routine (ISR)?

An interrupt handler, also known as an interrupt service routine or ISR, is a special block of code associated with a specific interrupt condition. Interrupt handlers are initiated by hardware interrupts, software interrupt instructions, or software exceptions, and are used for implementing device drivers or transitions between protected modes of operation, such as system calls.

2. What is an interrupt vector table?

An interrupt vector table (IVT) is a data structure that associates a list of interrupt handlers with a list of interrupt requests. Each entry of the interrupt vector table, called an interrupt vector, is the address of an interrupt handler.

3. Describe the ARM Cortex-M Nested Vector Interrupt Controller (NVIC).

Interrupts on the Cortex-M are controlled by the Nested Vectored Interrupt Controller (NVIC). Each exception has an associated 32-bit vector (pointer) that points to the memory location where the ISR that handles the exception is located. Vectors are stored in ROM at the beginning of memory, such as the vtable of interrupts in a pre-configured sequence which must be mapped to a specific handler label / function.

4. What are the hexadecimal addresses of (1) Reset_Handler and (2) UART0_Handler?

Reset_Handler 0x00000004

UART0_Handler 0x00000054

5. Thoroughly explain the ARM instructions bx and lr, and the invocation "bx lr".
BX dest dest: Register containing target address (R0..R15) The BX instruction branches to the specified dest containing an ARM* or Thumb* instruction and optionally executes it. A link register (LR) is a special-purpose register which holds the address to return to when a function call completes. To return from an interrupt, the ISR executes the typical function return BX LR.