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1. Define Instruction Set Architecture (ISA), emphasizing those aspects of an ISA most relevant to programmers.

An instruction set architecture (ISA) is an abstract model of a computer. It is also referred to as architecture or computer architecture. A realization of an ISA, such as a central processing unit (CPU), is called an implementation.

In general, an ISA defines the supported data types, the registers, the hardware support for managing main memory fundamental features (such as the memory consistency, addressing modes, virtual memory), and the input/output model of a family of implementations of the ISA.

2. Define central processing unit (CPU).

A central processing unit (CPU), also called a central processor or main processor, is the electronic circuitry within a computer that executes instructions that make up a computer program. The CPU performs basic arithmetic, logic, controlling, and input/output (I/O) operations specified by the instructions in the program. Traditionally, the term "CPU" refers to a processor, more specifically to its processing unit and control unit (CU), distinguishing these core elements of a computer from external components such as main memory and I/O circuitry. Principal components of a CPU include the arithmetic logic unit (ALU) that performs arithmetic and logic operations, processor registers that supply operands to the ALU and store the results of ALU operations, and a control unit that orchestrates the fetching (from memory) and execution of instructions by directing the coordinated operations of the ALU, registers and other components.

3. Define System on Chip (SoC).

A system on a chip (SoC) is an integrated circuit (also known as a "chip") that integrates all or most components of a computer or other electronic system. These components almost always include a central processing unit (CPU), memory, input/output ports and secondary storage â€“ all on a single substrate or microchip, the size of a coin. It must contain digital, analog, mixed-signal, and often radio frequency signal processing functions, otherwise it will only be considered as an application processor. As they are integrated on a single substrate, SoCs consume much less power and take up much less area than multi-chip designs with equivalent functionality. Because of this, SoCs are very common in the mobile computing (such as in smartphones) and edge computing markets. System on a chip are typically fabricated using metalâ€“oxideâ€“semiconductor (MOS) technology, and are commonly used in embedded systems and the Internet of Things. Higher-performance SoCs are often paired with dedicated and physically separate memory and secondary storage chips, that may be layered on top of the SoC in what's known as a Package on

4. What is ARM (the architecture)?

ARM is a family of reduced instruction set computing (RISC) architectures for computer processors, configured for various environments.

5. What is ARM (the company)?

Arm Holdings develops the architecture and licenses it to other companies, who design their own products that implement one of those architecturesâ€•â€”â€Œincluding systems-on-chips (SoC) and systems-on-modules (SoM) that incorporate memory, interfaces, radios, etc. It also designs cores that implement this instruction set and licenses these designs to a number of companies that incorporate those core designs into their own products.

6. What is a Reduced Instruction Set Computer (RISC)?

A reduced instruction set computer (RISC) is a computer instruction set that allows a computer's microprocessor to have fewer cycles per instruction (CPI) than a complex instruction set computer (CISC).

A RISC computer has a small set of simple and general instructions, rather than a large set of complex and specialized ones. The main distinguishing feature of RISC is that the instruction set is optimized for a highly regular instruction pipeline flow. Another common RISC trait is their load/store architecture, in which memory is accessed through specific instructions rather than as a part of most instructions.

7. What does it mean that the ARM instruction set is a load/store architecture?

In computer engineering, a loadâ€“store architecture is an instruction set architecture that divides instructions into two categories: memory access (load and store between memory and registers), and ALU operations (which only occur between registers).

For instance, in a loadâ€“store approach both operands and destination for an ADD operation must be in registers. This differs from a registerâ€“memory architecture (for example, a CISC instruction set architecture such as x86) in which one of the operands for the ADD operation may be in memory, while the other is in a register.

8. What are the ARM/bitwise logic instructions to (1) set a bit, (2) clear a bit, (3) toggle a bit, and (4) test a bit?

1) ORR
2) BIC
3) EOR
4) TST / AND

9. Implement an if statement in ARM assembly that adds one to r1 if the value in r0 is less than 10.

```
CMP r0, #10
IT LO
ADDLO r1, #1

// alternative without block

CMP r0, 10
BHS do_not_increment
add r1, 1

do_not_increment:
```

10. Implement a loop in ARM assembly that repeats nop 10 times.

```
// nop is "no operation"

mov r0, 1
nop_loop:
nop
add r0, 1
teq r0, #10
it lo
blo nop_loop
```