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1. What is ARM?

ARM, known as Advanced RISC Machines, is a family of reduced instruction set computing architectures for processors.

2. What is a Reduced Instruction Set Computer (RISC)?

A reduced instruction set computer allows the microprocessor to have fewer cycles per instruction than a complex instruction set computer. A RISC has a small set of simple and general instructions, rather than a large set of complex and specialized ones. The main distinguishing feature of RISC is that the instruction set is optimized for a highly regular instruction pipeline flow, as well as their load/store architecture in which memory is accessed through specific instructions rather than as a part of most instructions.

3. What is a load/store architecture?

A load/store architecture is an instruction set architecture that divides instructions into two categories, memory access operations such as loading data from memory into registers and storing results from registers into memory, and Arithmetic Logic Unit operations which only occur between registers.

4. Briefly describe the Harvard architecture, Von Neumann architecture, and modified Harvard architecture.

The Harvard architecture is a computer architecture with separate storage and signal pathways for instructions and data. These two memories can have varying characteristics such as different word width, timing, implementation technology, and memory address structure. In some systems, instructions for pre-programmed tasks can be stored in read-only memory while data memory generally requires read-write memory. In other systems, instruction addresses are wider than data addresses when there is much more instruction memory. A Harvard architecture machine also has distinct code and data address spaces, for example the instruction address zero is not the same as data address zero. Instruction address zero might identify a twenty-four-bit value, while data address zero might indicate an eight-bit byte that is not part of that twenty-four-bit value.

In contrast, the von Neumann architecture allows for program instructions and data to share the same memory and pathways. This means that a CPU cannot simultaneously read an instruction and read or write data from or to the memory. Whereas a CPU using the Harvard architecture can both read an instruction and perform a data memory access at the same time without a cache. Von Neumann CPUs can be slower than those implemented with the Harvard architecture computer because instruction fetches and data access can conflict on a single memory pathway.

A modified Harvard architecture machine relaxes the strict separation between

5. What does the company Arm Holdings do?
Arm Holdings designs semiconductor and software, primarily the design of ARM CPUs, some software development tools, as well as system-on-a-chip infrastructure and software. It has achieved market dominance in mobile and tablet processors. For example their processors range from the world's smallest computer to the processors in the largest and most energy efficient supercomputers. ARM processors are also used in microcontrollers for embedded systems, including real-time safety systems such as automobiles' automatic braking system, biometrics systems like fingerprint sensors, smart TVs, modern smartwatches, as well as general purpose desktops.

6. What are the stated advantages of RISC processors over CISC processors?
RISC processors have a smaller computer instruction set which enables fewer cycles per instruction than a complex instruction set computer. RISC processors are optimized for a highly regular instruction pipeline flow and are designed with a load/store architecture in which memory is accessed through specific instructions rather than as a part of most instructions.

7. List the members of the ARM Cortex-M family of processors.
The ARM Cortex-M cores consist of the Cortex-M0, Cortex-M0+, Cortex-M1, Cortex-M3, Cortex-M4, Cortex-M7, Cortex-M23, Cortex-M33, Cortex-M35P.

8. Describe the features of the Cortex-M4 processor (including the features shared with the Cortex-M3).

The Cortex-M4 core is designed with the ARMv7E-M architecture and supports 3-stage pipeline with branch speculation.

Instruction sets include:
Thumb-1 (entire).
Thumb-2 (entire).
32-bit hardware integer multiply with 32-bit or 64-bit result, signed or unsigned, add or subtract after the multiply. 32-bit Multiply and MAC are 1 cycle.
32-bit hardware integer divide (2â€“12 cycles).
Saturation arithmetic support.
DSP extension: Single cycle 16/32-bit MAC, single cycle dual 16-bit MAC, 8/16-bit SIMD arithmetic.

It also supports:
1 to 240 interrupts, plus NMI.
12 cycle interrupt latency.
Integrated sleep modes.

Silicon options include:
Optional floating-point unit (FPU): single-precision only IEEE-754 compliant. It is called the FPv4-SP extension.
Optional memory protection unit (MPU): 0 or 8 regions.

9. On what ARM processor are the STM32F401RE devices based?

STM32F401xD/xE devices are based on the high-performance ARM Cortex-M4 32-bit RISC core operating at a frequency of up to 84 MHz. It features a Floating Point Unit single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a Memory Protection Unit which enhances application security.

10. Does the STM32F401RE implement a Floating Point Unit (FPU)?

Yes it features a Floating Point Unit single precision which supports all ARM single-precision data-processing instructions and data types.