Vrunda Dave

Room No. 301, CFDVS Lab, New CC Building
Near SOM, IIT Bombay, Powai, Mumbai-400076, India
Phone: +91 7045331844
vrunda@cse.iitb.ac.in
www.cse.iitb.ac.in/~vrunda/

EDUCATION

Indian Institute of Technology, Bombay *Jan 2015 - Ongoing*
Ph. D., Computer Science and Engineering
CPI till now: 8.85/10

Dharamsinh Desai University, Gujarat *May 2014*
Bachelors in Technology, Computer Science and Engineering
Overall CPI: 9.18/10

H.S.C. (10 + 2) *May 2010*
Gujarat Higher Scondary Education Board
Percentage: 88.89%

S.S.C. (10) *May 2008*
Gujarat Scondary Education Board
Percentage: 92.31%

PHD THESIS TOPIC

I am currently working with Prof. Krishna S. on theoretical problems related to regular & aperiodic transformations. I am also planning to look at their applications in verification.

PUBLICATIONS

- Regular Transducer Expressions for Regular Transformations.
  Vrunda Dave, Paul Gastin, Krishna Shankara Narayanan. *33^{rd} Annual ACM/IEEE Symposium on Logic in Computer Science, LICS 2018.* https://dl.acm.org/citation.cfm?doid=3209108.3209182
- FO-Definable Transformations of Infinite Strings
  Vrunda Dave, Shankara Narayanan Krishna, Ashutosh Trivedi. *36^{th} IARCS Annual Conference on Foundations of Software Technology and Theoretical Computer Science, FSTTCS 2016.* http://drops.dagstuhl.de/opus/volltexte/2016/6847/
- A Logical Characterization for Dense-Time Visibly Pushdown Automata.
  Devendra Bhave, Vrunda Dave, Shankara Narayanan Krishna, Ramchandra Phawade, Ashutosh Trivedi. *10^{th} International Conference on Language and Automata Theory and Applications (LATA 2016).* https://link.springer.com/chapter/10.1007%2F978-3-319-30000-9_7
- A Perfect Class of Context-Sensitive Timed Languages.
  Devendra Bhave, Vrunda Dave, Shankara Narayanan Krishna, Ramchandra Phawade, Ashutosh Trivedi. *20^{th} International Conference on Developments in Language Theory (DLT 2016).* https://link.springer.com/chapter/10.1007%2F978-3-662-53132-7_4

EXPERIENCE

Ericsson Research Lab May '16 - June '16
Summer Intern *Bangalore, India*

- Worked in SAT based planning project.
- Explored various SAT based planners or model checking tool which can serve efficiently like SATPLAN, Madagascar, OPTIC planner, SAL model checking tool.

TCS Innovation Lab(TRDDC) September '14 - January '14
Assistant System Engineer Trainee *Pune, India*

- Worked in a project titled as Anomalies Detection in Business Rules which was focusing to represent the business rules in standard format and find the anomalies(like Conflict, Duplicacy and Subsumption) from them using z3 SMT solver.
- Detected Conflicting rules and Duplicate rules.

TCS Innovation Lab(TRDDC) December '13 - April '14
Project Trainee *Pune, India*

- Worked in same project and found conflicting rules from them using z3 SMT solver.
- explored several SMT solvers and verification techniques and built a prototype using Eclipse Plugin.

RESEARCH INTERESTS

Automata/Transducer Theory, Logic
Formal Verification
Reachability Games

RELEVANT COURSES

Logic for CS(Teaching Assistant), Discrete Structure(Teaching Assistant), Special Topics in Automata & Logic, Concepts, Algorithms and Tools for Model-Checking, Formal Models for Asynchronous and Concurrent Systems, Linear Optimization, Algorithms & complexity(Teaching Assistant), Probabilistic Models, Number theory & Cryptography

ACHIEVEMENTS/AWARDS

- Receiving CISCO PhD fellowship.
- Secured second position in Dharamsinh Desai University in B. Tech, Computer Engineering (2010-2014).
- Got Best Design Project award in Students' Day organized by TRDDC, Pune during Internship (April, 2014).
- Won 1st prize in encode-decode and bug detector competition organized during tech fest in team.
- Secured second position Chess tournament in School in 2010.