

# MPCA WEEK5 LAB

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Section:"I"

SRN:PES1UG20CS516

1. Write a program in ARM7TDMI-ISA to multiply 2 matrices of order3.

i.e., implement  $c[i][j]=c[i][j] + a[i][j] \times b[i][j]$ .

a. Use MLA instruction

b. Use MUL instruction

a.

**=>CODE:**

```
.DATA
A: .WORD 1,2,3,4,5,6,7,8,9
B: .WORD 9,8,7,6,5,4,3,2,1
C: .WORD 0,0,0,0,0,0,0,0,0
.TEXT
LDR R0,=A
LDR R1,=B
LDR R2,=C
MOV R12,#0
MOV R3,#0
MOV R4,#0
MOV R5,#0
MOV R8,#3
L1: MUL R6,R3,R8
    ADD R6,R6,R4
    MUL R7,R4,R8
```

```
ADD R7,R7,R5
LDR R10,[R0,R6,LSL #2]
LDR R11,[R1,R7,LSL #2]
MUL R7,R10,R11
ADD R12,R12,R7
ADD R4,R4,#1
CMP R4,#3
BNE L1
MUL R9,R3,R8
ADD R9,R9,R5
STR R12,[R2,R9,LSL #2]
MOV R4,#0
MOV R12,#0
ADD R5,R5,#1
CMP R5,#3
BNE L1
MOV R5,#0
ADD R3,R3,#1
CMP R3,#3
BNE L1
SWI 0X011
```

=>Output:

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 4236  
R1 : 4272  
R2 : 4308  
R3 : 3  
R4 : 0  
R5 : 0  
R6 : 8  
R7 : 9  
R8 : 3  
R9 : 8  
R10 (s1) : 9  
R11 (fp) : 1  
R12 (ip) : 0  
R13 (sp) : 21504  
R14 (lr) : 0  
R15 (pc) : 4220

CPSR Register  
Negative (N) : 0  
Zero (Z) : 1  
Carry (C) : 1  
Overflow (V) : 0  
IRQ Disable : 1  
FIQ Disable : 1  
Thumb (T) : 0  
CPU Mode : System

0x600000df

mul(a).s

```
.DATA
0000108C: A: .WORD 1,2,3,4,5,6,7,8,9
000010B0: B: .WORD 9,8,7,6,5,4,3,2,1
000010D4: C: .WORD 0,0,0,0,0,0,0,0,0
.TEXT
00001000:E59F0078 LDR R0,=A
00001004:E59F1078 LDR R1,=B
00001008:E59F2078 LDR R2,=C
0000100C:E3A0C000 MOV R12,#0
00001010:E3A03000 MOV R3,#0
00001014:E3A04000 MOV R4,#0
00001018:E3A05000 MOV R5,#0
0000101C:E3A08003 MOV R8,#3
00001020:E0060893 L1: MUL R6,R3,R8
00001024:E0866004 ADD R6,R6,R4
00001028:E0070894 MUL R7,R4,R8
0000102C:E0877005 ADD R7,R7,R5
00001030:E790A106 LDR R10,[R0,R6,LSL #2]
00001034:E791B107 LDR R11,[R1,R7,LSL #2]
00001038:E0070B9A MUL R7,R10,R11
0000103C:E08CC007 ADD R12,R12,R7
00001040:E2844001 ADD R4,R4,#1
00001044:E3540003 CMP R4,#3
```

MemoryView0

000010D4

000010D4	0000001E	00000018	00000012	00000054	00000045	00000036	0000008A	00000072	0000005A	81818
00001108	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818
0000113C	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818
00001170	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818
000011A4	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818

OutputView

Console Stdin/Stdout/Stderr

Loading assembly language file D:\RISHI\SEM4\MPCA\LAB\Week5\mul(a).s  
Execution starting ...

Execution ending, Instruction Count:390 Elapsed Time:00:00:00.0060013  
Instructions per second:64985

b.

=>CODE:

```
.DATA
A: .WORD 1,2,3,4,5,6,7,8,9
B: .WORD 9,8,7,6,5,4,3,2,1
C: .WORD 0,0,0,0,0,0,0,0,0
.TEXT
LDR R0,=A
LDR R1,=B
LDR R2,=C
MOV R12,#0
MOV R3,#0
MOV R4,#0
MOV R5,#0
MOV R8,#3
L1:
    MLA R6,R3,R8,R4
    MLA R7,R4,R8,R5
    LDR R10,[R0,R6,LSL #2]
    LDR R11,[R1,R7,LSL #2]
```

```

MLA R12,R10,R11,R12
ADD R4,R4,#1
CMP R4,#3
BNE L1
MLA R9,R3,R8,R5
STR R12,[R2,R9,LSL #2]
MOV R4,#0
MOV R12,#0
ADD R5,R5,#1
CMP R5,#3
BNE L1
MOV R5,#0
ADD R3,R3,#1
CMP R3,#3
BNE L1

```

SWI 0X11

=>Output:

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 4220  
R1 : 4256  
R2 : 4292  
R3 : 3  
R4 : 0  
R5 : 0  
R6 : 8  
R7 : 8  
R8 : 3  
R9 : 8  
R10 (s1) : 9  
R11 (fp) : 1  
R12 (ip) : 0  
R13 (sp) : 21504  
R14 (lr) : 0  
R15 (pc) : 4204

CPSR Register  
Negative (N) : 0  
Zero (Z) : 1  
Carry (C) : 1  
Overflow (V) : 0  
IRQ Disable : 1  
FIQ Disable : 1  
Thumb (T) : 0  
CPU Mode : System

0x600000df

mul(b).s

.DATA  
0000107C: A: .WORD 1,2,3,4,5,6,7,8,9  
000010A0: B: .WORD 9,8,7,6,5,4,3,2,1  
000010C4: C: .WORD 0,0,0,0,0,0,0,0

.TEXT  
00001000:E59F0068 LDR R0,=A  
00001004:E59F1068 LDR R1,=B  
00001008:E59F2068 LDR R2,=C  
0000100C:E3A0C000 MOV R12,#0  
00001010:E3A03000 MOV R3,#0  
00001014:E3A04000 MOV R4,#0  
00001018:E3A05000 MOV R5,#0  
0000101C:E3A08003 MOV R8,#3  
00001020: L1:  
00001020:E0264893 MLA R6,R3,R8,R4  
00001024:E0275894 MLA R7,R4,R8,R5  
00001028:E790A106 LDR R10,[R0,R6,LSL #2]  
0000102C:E791B107 LDR R11,[R1,R7,LSL #2]  
00001030:E02CCB9A MLA R12,R10,R11,R12  
00001034:E2844001 ADD R4,R4,#1  
00001038:E3540003 CMP R4,#3  
0000103C:1AFFFFF7 BNE L1  
00001040:E0295893 MLA R9,R3,R8,R5

MemoryView0

000010C4

Word  
8Bit

000010C4 0000001E 00000018 00000012 00000054 00000045 00000036 0000008A 00000072 0000005A 81818181 81818181 81818181  
000010F8 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181  
0000112C 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181  
00001160 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181  
00001194 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

OutputView

Console Stdin/Stdout/Stderr

Loading assembly language file D:\RISHI\SEM4\MPCA\LAB\Week5\mul(b).s  
Execution starting ...

Execution ending, Instruction Count:300 Elapsed Time:00:00:00.0060014  
Instructions per second:49988

2. Write a program in ARM7TDMI-ISA to find the NORM of a square matrix of order n

=>CODE:

```
.DATA
A: .WORD 1,2,7,6,9,5,4,3,8
SUM: .WORD

.TEXT

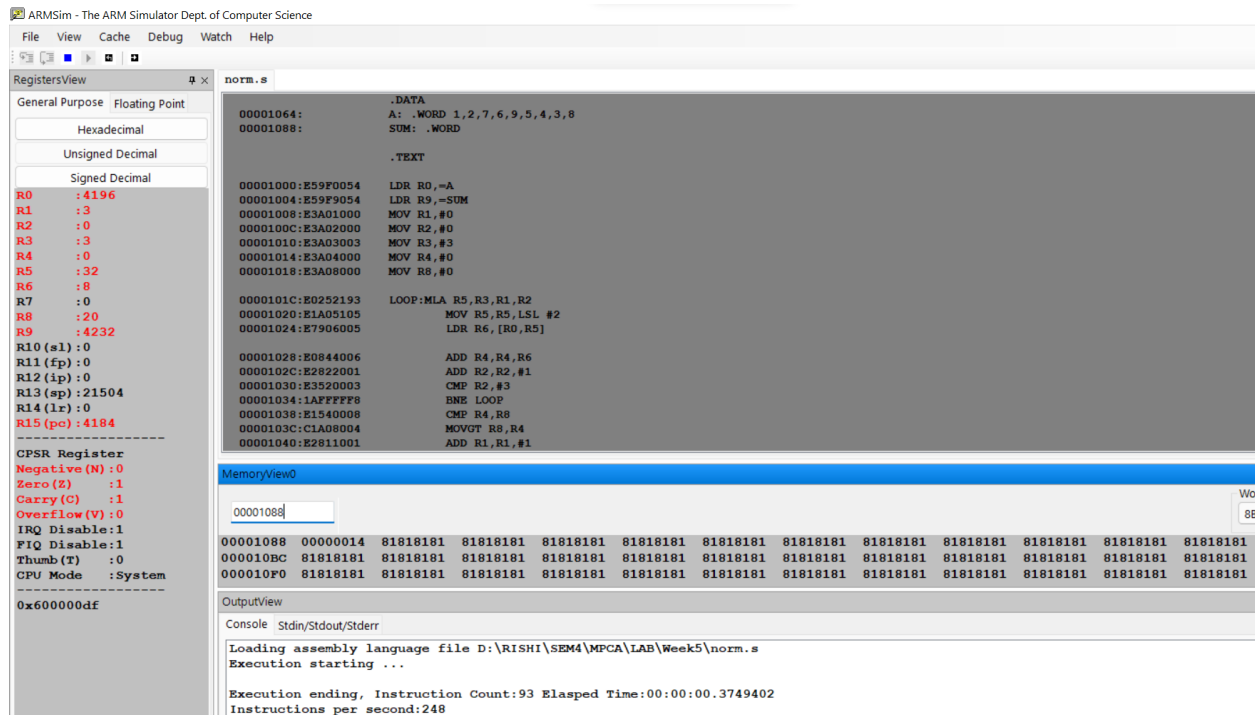
LDR R0,=A
LDR R9,=SUM
MOV R1,#0
MOV R2,#0
MOV R3,#3
MOV R4,#0
MOV R8,#0

LOOP:MLA R5,R3,R1,R2
      MOV R5,R5,LSL #2
      LDR R6,[R0,R5]

      ADD R4,R4,R6
      ADD R2,R2,#1
      CMP R2,#3
      BNE LOOP
      CMP R4,R8
      MOVGT R8,R4
      ADD R1,R1,#1
      MOV R2,#0
      MOV R4,#0
      CMP R1,#3
      BNE LOOP

      STR R8,[R9]
SWI 0X011
```

=>Output:



3. Write a program in ARM7TDMI-ISA to find the ROWSUM of a matrix.

=>CODE:

```
.DATA
A: .WORD 1,2,3,4,5,6,7,8,9
SUM: .WORD 0,0,0

.TEXT

LDR R0,=A
LDR R9,=SUM

MOV R1,#0

MOV R2,#0

MOV R3,#3

MOV R4,#0
```

```

LOOP:MLA R5,R3,R1,R2
      MOV R5,R5,LSL #2
      LDR R6,[R0,R5]

      ADD R4,R4,R6
      ADD R2,R2,#1
      CMP R2,#3
      BNE LOOP
      STR R4,[R9],#4
      ADD R1,R1,#1
      MOV R2,#0
      MOV R4,#0
      CMP R1,#3
      BNE LOOP

```

SWI 0X011

=>Output:

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 4184

R1 : 3

R2 : 0

R3 : 3

R4 : 0

R5 : 32

R6 : 9

R7 : 0

R8 : 0

R9 : 4232

R10 (s11) : 0

R11 (fp) : 0

R12 (ip) : 0

R13 (sp) : 21504

R14 (lr) : 0

R15 (pc) : 4172

CPSR Register

Negative (N) : 0

Zero (Z) : 1

Carry (C) : 1

Overflow (V) : 0

IRQ Disable: 1

FIQ Disable: 1

Thumb (T) : 0

CPU Mode : System

0x600000df

rowsum.s

.DATA

00001058: A: .WORD 1,2,3,4,5,6,7,8,9

0000107C: SUM: .WORD 0,0,0

.TEXT

00001000:E59F0048 LDR R0,=A

00001004:E59F9048 LDR R9,=SUM

00001008:E3A01000 MOV R1,#0

0000100C:E3A02000 MOV R2,#0

00001010:E3A03003 MOV R3,#3

00001014:E3A04000 MOV R4,#0

00001018:E0252193 LOOP:MLA R5,R3,R1,R2

0000101C:E1A05105 MOV R5,R5,LSL #2

00001020:E7906005 LDR R6,[R0,R5]

00001024:E0844006 ADD R4,R4,R6

00001028:E2822001 ADD R2,R2,#1

0000102C:E3520003 CMP R2,#3

MemoryView0

0000107d

0000107C 00000006 0000000F 00000018 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

000010B0 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

000010E4 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

OutputView

Console Stdin/Stdout/Stderr

Loading assembly language file D:\RISHI\SEM4\MPCA\LAB\Week5\rowsum.s

Execution starting ...

Execution ending, Instruction Count:88 Elapsed Time:00:00:00.1591282

Instructions per second:553