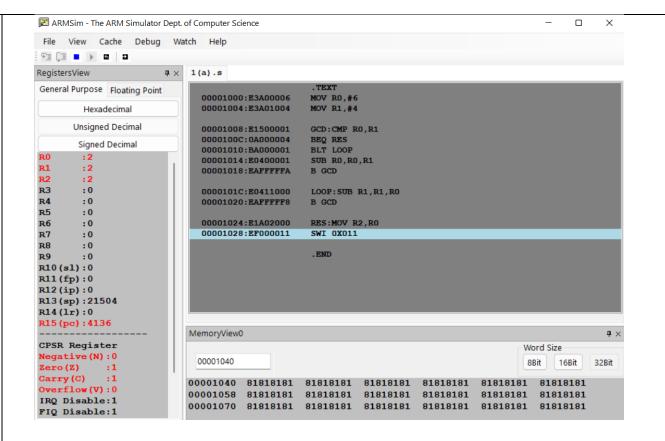


Department of Computer Science & Engineering Microprocessor & Computer Architecture MPCA-Laboratory/Assignment/Hands-on/Project UE20CS252

Vrushank G PES1UG20CS516 SEC-I

SI. No.	Programs
Week No. 3	Write a program in ARM7TDMI–ISA to find GCD of two numbers. a. Assume operands to be in the CPU registers.
	.TEXT MOV R0,#6 MOV R1,#4 GCD:CMP R0,R1 BEQ RES BLT LOOP SUB R0,R0,R1 B GCD LOOP:SUB R1,R1,R0
	B GCD RES:MOV R2,R0 SWI 0X011 .END
	Output:



b. Assume operands in the memory locations.

```
.TEXT
LDR R0,=A
LDR R1,=B
LDR R4,=C

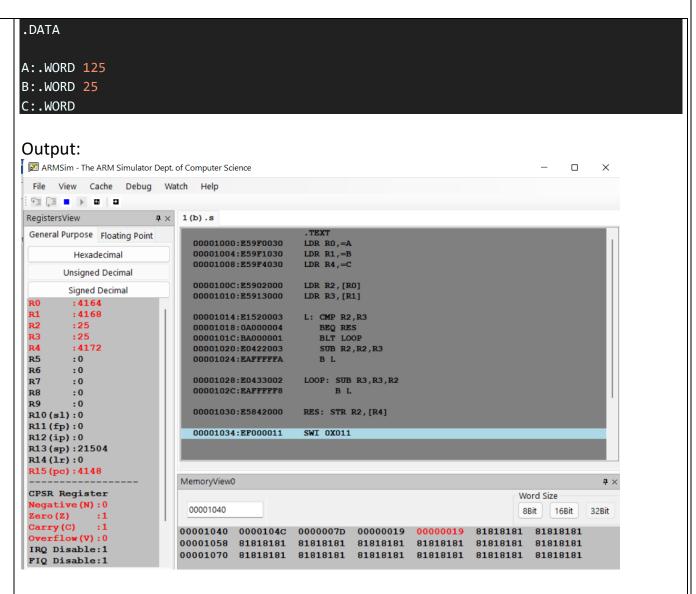
LDR R2,[R0]
LDR R3,[R1]

L: CMP R2,R3
BEQ RES
BLT LOOP
SUB R2,R2,R3
B L

LOOP: SUB R3,R3,R2
B L

RES: STR R2,[R4]

SWI 0X011
```



- 2. Write a program in ARM7TDMI–ISA to find the sum of N data items in the memory. Store the result in the memory location.
 - a. Use Pre-indexing addressing mode.

```
.DATA
A:.WORD 10,20,30,40,50,60,70,80,90,100
SUM:.WORD 0

.TEXT
LDR R0,=A
LDR R1,=SUM

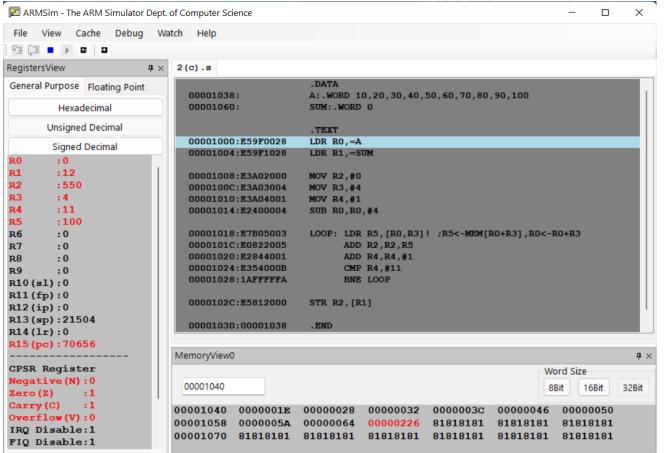
MOV R2,#0
MOV R3,#4
MOV R4,#1
SUB R0,R0,#4

LOOP: LDR R5,[R0,R3] ;R5<-MEM[R0+R3]
ADD R2,R2,R5
```

```
ADD R3, R3, #4
       ADD R4, R4, #1
       CMP R4,#11
       BNE LOOP
STR R2,[R1]
SWI 0X011
Output:
 ARMSim - The ARM Simulator Dept. of Computer Science
                                                                                                  ×
  File View Cache Debug Watch Help
 RegistersView
                        Д×
                            2(a).s
 General Purpose Floating Point
                              00001040:
                                                  A:.WORD 10,20,30,40,50,60,70,80,90,100
                              00001068:
                                                  SUM: .WORD 0
         Hexadecimal
       Unsigned Decimal
                                                  . TEXT
                              00001000:E3A00D41
                                                  LDR RO,=A
        Signed Decimal
                                                  LDR R1,=SUM
                              00001004:E59F102C
         :4156
         :4200
 R1
                              00001008:E3A02000
                                                  MOV R2,#0
         :550
                              0000100C:E3A03004
                                                  MOV R3,#4
 R3
         :44
                              00001010:E3A04001
                                                  MOV R4,#1
         :11
                              00001014:E2400004
                                                  SUB R0, R0, #4
         :100
                              00001018:E7905003
                                                  LOOP: LDR R5, [R0,R3] ; R5<-MEM[R0+R3], R0<-R0+R3
 R6
         : 0
                                                       ADD R2,R2,R5
                              0000101C:E0822005
 R7
         : 0
                              00001020:E2833004
                                                        ADD R3,R3,#4
 R8
         : 0
                              00001024:E2844001
                                                       ADD R4, R4, #1
 R9
         : 0
                              00001028:E354000B
                                                       CMP R4,#11
 R10(s1):0
                              0000102C:1AFFFFF9
                                                       BNE LOOP
 R11(fp):0
 R12(ip):0
                              00001030:E5812000
                                                  STR R2, [R1]
 R13(sp):21504
                                                  SWI 0X011
 R14(lr):0
 R15 (pc):4148
                            MemoryView0
                                                                                                       Д×
 CPSR Register
                                                                                        Word Size
 Negative(N):0
                             00001040
                                                                                         8Bit 16Bit
                                                                                                    32Bit
 Zero(Z)
             :1
 Carry (C)
             :1
                            00001040 0000000A
                                                 00000014
                                                           0000001E
                                                                      00000028
                                                                                00000032
                                                                                           0000003C
 Overflow(V):0
                            00001058
                                      00000046
                                                 00000050 0000005A
                                                                      00000064
                                                                                00000226
                                                                                           81818181
 IRQ Disable:1
                            00001070 81818181 81818181 81818181 81818181 81818181 81818181
 FIQ Disable:1
      b. Use Post-indexing addressing mode.
.DATA
A:.WORD 10,20,30,40,50,60,70,80,90,100
SUM:.WORD 0
.TEXT
LDR R0,=A
LDR R1,=SUM
MOV R2,#0
```

MOV R3,#4 MOV R4,#1

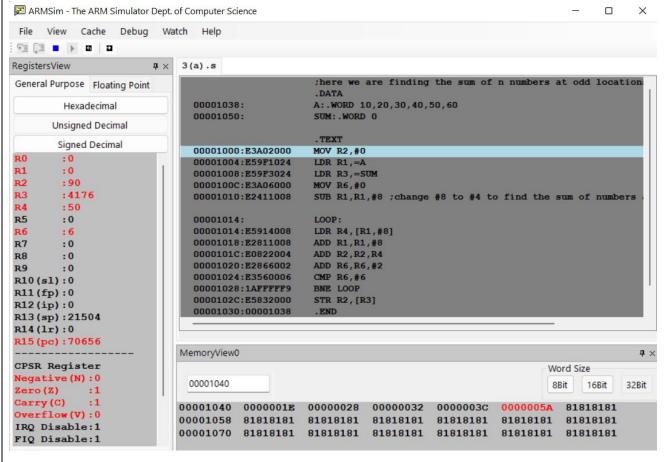
```
LOOP: LDR R5,[R0],#4
       ADD R2, R2, R5
       ADD R4, R4, #1
       CMP R4,#11
       BNE LOOP
STR R2,[R1]
.END
Output:
 ARMSim - The ARM Simulator Dept. of Computer Science
                                                                                                 ×
  File View Cache Debug Watch Help
 RegistersView
                            2 (b) .s
 General Purpose Floating Point
                              00001034:
                                                  A:.WORD 10,20,30,40,50,60,70,80,90,100
                                                  SUM: .WORD 0
                              0000105C:
         Hexadecimal
       Unsigned Decimal
                                                  . TEXT
                              00001000:E59F0024
                                                 LDR RO,=A
        Signed Decimal
                                                  LDR R1,=SUM
                              00001004:E59F1024
         : 0
         : 0
                                                 MOV R2,#0
                              00001008:E3A02000
 R2
         :550
                              0000100C:E3A03004
                                                 MOV R3,#4
                              00001010:E3A04001
                                                 MOV R4,#1
         :11
         :100
                              00001014:E4905004
                                                 LOOP: LDR R5, [R0], #4 ; R5<-MEM[R0+R3], R0<-R0+R3
 R6
                              00001018:E0822005
         : 0
                                                       ADD R2,R2,R5
                              0000101C:E2844001
                                                       ADD R4,R4,#1
 R7
         :0
                                                       CMP R4,#11
                              00001020:E354000B
         :0
                                                       BNE LOOP
                              00001024:1AFFFFFA
 R9
         : 0
 R10(s1):0
                                                 STR R2, [R1]
                              00001028:E5812000
 R11(fp):0
 R12(ip):0
                              0000102C:00001034
                                                  . END
 R13(sp):21504
                              00001030:0000105C
 R14(lr):0
 R15 (pc):70656
                            MemoryView0
                                                                                                       4 ×
 CPSR Register
                                                                                        Word Size
 Negative(N):0
                             00001040
                                                                                        8Bit
                                                                                             16Bit 32Bit
 Zero(Z)
            :1
 Carry(C)
                            00001040 00000028 00000032 0000003C 00000046 00000050 0000005A
 Overflow(V):0
                            00001058
                                      00000064
                                                00000226
                                                           81818181
                                                                      81818181
 IRQ Disable:1
                                      81818181 81818181 81818181 81818181 81818181 81818181
                            00001070
 FIQ Disable:1
      c. Use Auto-indexing addressing mode.
A:.WORD 10,20,30,40,50,60,70,80,90,100
SUM:.WORD 0
.TEXT
LDR R0,=A
LDR R1,=SUM
MOV R2,#0
MOV R3,#4
```



- 3. Write a program in ARM7TDMI–ISA to find the sum of N data items at alternate [**odd** or **even** positions] locations in the memory. Store the result in the memory location.
 - a. Use Pre-indexing addressing mode.

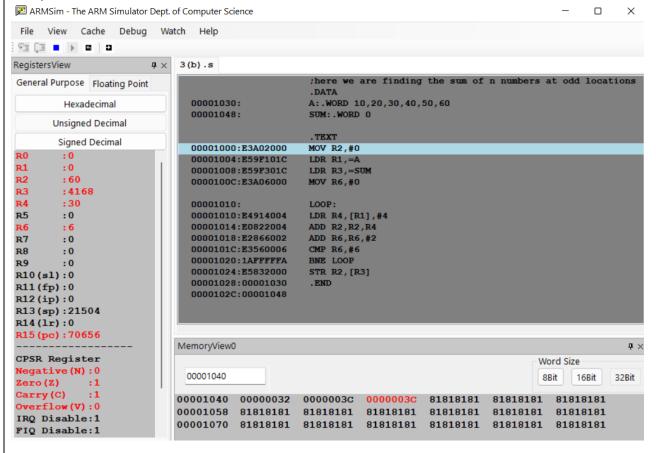
```
;here we are finding the sum of n numbers at odd locations
.DATA
A:.WORD 10,20,30,40,50,60
```

```
SUM:.WORD 0
.TEXT
MOV R2,#0
LDR R1,=A
LDR R3,=SUM
MOV R6,#0
SUB R1,R1,#8 ;change #8 to #4 to find the sum of numbers at even positions
LOOP:
LDR R4,[R1,#8]
ADD R1,R1,#8
ADD R2,R2,R4
ADD R6, R6, #2
CMP R6,#6
BNE LOOP
STR R2,[R3]
.END
```



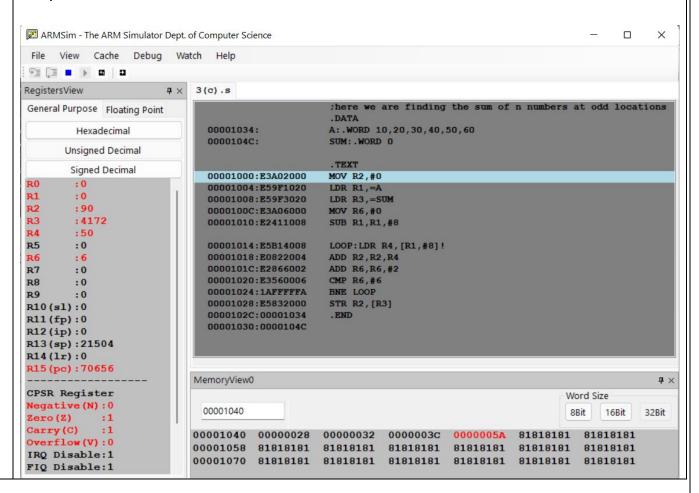
b. Use Auto-indexing addressing mode.

```
;here we are finding the sum of n numbers at odd locations
.DATA
A:.WORD 10,20,30,40,50,60
SUM:.WORD 0
.TEXT
MOV R2,#0
LDR R1,=A
LDR R3,=SUM
MOV R6,#0
LOOP:
LDR R4,[R1],#4
ADD R2,R2,R4
ADD R6, R6, #2
CMP R6,#6
BNE LOOP
STR R2,[R3]
.END
```



c. Use Post–indexing addressing mode.

```
;here we are finding the sum of n numbers at odd locations
.DATA
A:.WORD 10,20,30,40,50,60
SUM:.WORD 0
.TEXT
MOV R2,#0
LDR R1,=A
LDR R3,=SUM
MOV R6,#0
SUB R1,R1,#8
LOOP:LDR R4,[R1,#8]!
ADD R2,R2,R4
ADD R6, R6, #2
CMP R6,#6
BNE LOOP
STR R2,[R3]
.END
```



- 4. Write a program in ARM7TDMI–ISA to search for an element in an array. Store 00 if the search is unsuccessful and 01 if the search is successful in the register.
 - a. Use Linear Search Technique.

```
.TEXT
LDR R0,=A
LDR R1,=KEY
LDR R3,[R1]
MOV R4,#1
L:LDR R2,[R0]
  CMP R2,R3
  BEQ RES
  ADD R0, R0, #4
  ADD R4,R4,#1
  CMP R4,#6
  BNE L
MOV R5,#0
B LOOP
RES:MOV R5,#01
LOOP: SWI 0X011
.DATA
A:.WORD 10,20,30,40,50
KEY:.WORD 60
```

