



Department of Computer Science & Engineering
Microprocessor & Computer Architecture
MPCA-Laboratory/Assignment/Hands-on/Project

UE20CS252

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Sec-I

Sl. No.	Programs
Week No. 2	<p>1. Write a program in ARM7TDMI-ISA to copy a block of N data items from Location A to Location B. a) Use Full word (.word directive)</p> <pre>1(i).s - Notepad PREVIEW File Edit View .TEXT LDR R0, =A LDR R1, =B MOV R4, #1 L: LDR R2, [R0] ;LDR R3, [R1] MOV R3, R2 STR R3, [R1] ADD R0, R0, #4 ADD R1, R1, #4 ADD R4, R4, #1 CMP R4, #11 BNE L SWI 0X011 .DATA A: .WORD 10,20,30,40,50,60,70,80,90,100 B: .WORD 0,0,0,0,0,0,0,0,0,0</pre>

Output:

The screenshot displays the ARMSim interface. The 'RegistersView' window on the left shows the state of 16 registers (R0-R15) and the CPSR register. R0 is 4192, R1 is 4232, R2 is 100, R3 is 100, R4 is 11, and R15 (PC) is 4140. The CPSR register shows Negative (N) as 0, Zero (Z) as 1, Carry (C) as 1, Overflow (V) as 0, IRQ Disable as 1, and FIQ Disable as 1. The main assembly window shows the code for '1(i).s', including instructions like LDR, STR, MOV, ADD, CMP, BNE, and SWI. The 'OutputView' window at the bottom shows the console output, indicating the assembly file was loaded and execution started, ending with an instruction count of 84 and an elapsed time of 00:00:00.143.

```
ARMSim - The ARM Simulator Dept. of Computer Science
File View Cache Debug Watch Help

RegistersView
General Purpose Floating Point
Hexadecimal
Unsigned Decimal
Signed Decimal
R0 : 4192
R1 : 4232
R2 : 100
R3 : 100
R4 : 11
R5 : 0
R6 : 0
R7 : 0
R8 : 0
R9 : 0
R10 (sl) : 0
R11 (fp) : 0
R12 (ip) : 0
R13 (sp) : 21504
R14 (lr) : 0
R15 (pc) : 4140
-----
CPSR Register
Negative (N) : 0
Zero (Z) : 1
Carry (C) : 1
Overflow (V) : 0
IRQ Disable : 1
FIQ Disable : 1

0000100C: E5902000 L: LDR R2, [R0]
00001010: E1A03002 ;LDR R3, [R1]
00001014: E5813000 MOV R3, R2
00001018: E2800004 STR R3, [R1]
0000101C: E2811004 ADD R0, R0, #4
00001020: E2844001 ADD R1, R1, #4
00001024: E354000B ADD R4, R4, #1
00001028: 1AFFFFF7 CMP R4, #11
                                BNE L
0000102C: EF000011 SWI 0X011

.DATA
00001038: A: .WORD 10,20,30,40,50,60,70,80,90,100
00001060: B: .WORD 0,0,0,0,0,0,0,0,0,0

OutputView
Console Stdin/Stdout/Stderr
Loading assembly language file D:\RISHI\SEM4\MPCA\LAB\Week2\1(i)
Execution starting ...

Execution ending, Instruction Count:84 Elapsed Time:00:00:00.143
Instructions per second:584
```

b) Use Half word(.Hword directive)

```
1(ii).s - Notepad PREVIEW
File Edit View
.TEXT
LDR R0, =A
LDR R1, =B
MOV R4, #1

L:
    LDRH R2, [R0]
    ;LDRH R3, [R1]
    MOV R3, R2
    STRH R3, [R1]
    ADD R0, R0, #4
    ADD R1, R1, #4
    ADD R4, R4, #1
    CMP R4, #11
    BNE L

SWI 0X011

.DATA
A: .HWORD 10,20,30,40,50,60,70,80,90,100
B: .HWORD 0,0,0,0,0,0,0,0,0,0
```

Output:

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView 1(ii).s

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 4192
R1 : 4212
R2 : 90
R3 : 90
R4 : 11
R5 : 0
R6 : 0
R7 : 0
R8 : 0
R9 : 0
R10 (s1) : 0
R11 (fp) : 0
R12 (ip) : 0
R13 (sp) : 21504
R14 (lr) : 0
R15 (pc) : 4140

CPSR Register

Negative (N) : 0
Zero (Z) : 1
Carry (C) : 1
Overflow (V) : 0
IRQ Disable : 1
FIQ Disable : 1

```

0000100C:      L:
0000100C:E01020B0      LDRH R2,[R0]
                        ;LDRH R3,[R1]
00001010:E1A03002      MOV R3,R2
00001014:E00130B0      STRH R3,[R1]
00001018:E2800004      ADD R0,R0,#4
0000101C:E2811004      ADD R1,R1,#4
00001020:E2844001      ADD R4,R4,#1
00001024:E354000B      CMP R4,#11
00001028:1AFFFFF7      BNE L

0000102C:EF000011      SWI 0X011

      .DATA
00001038:      A: .HWORD 10,20,30,40,50,60,70,80,90,100
0000104C:      B: .HWORD 0,0,0,0,0,0,0,0,0,0

```

OutputView

Console Stdin/Stdout/Stderr

```

Loading assembly language file D:\RISHI\SEM4\MPCA\LAB\Week2\1(ii)
Execution starting ...

Execution ending, Instruction Count:84 Elapsed Time:00:00:00.110
Instructions per second:758

```

c) Use Byte wise (.Byte directive)

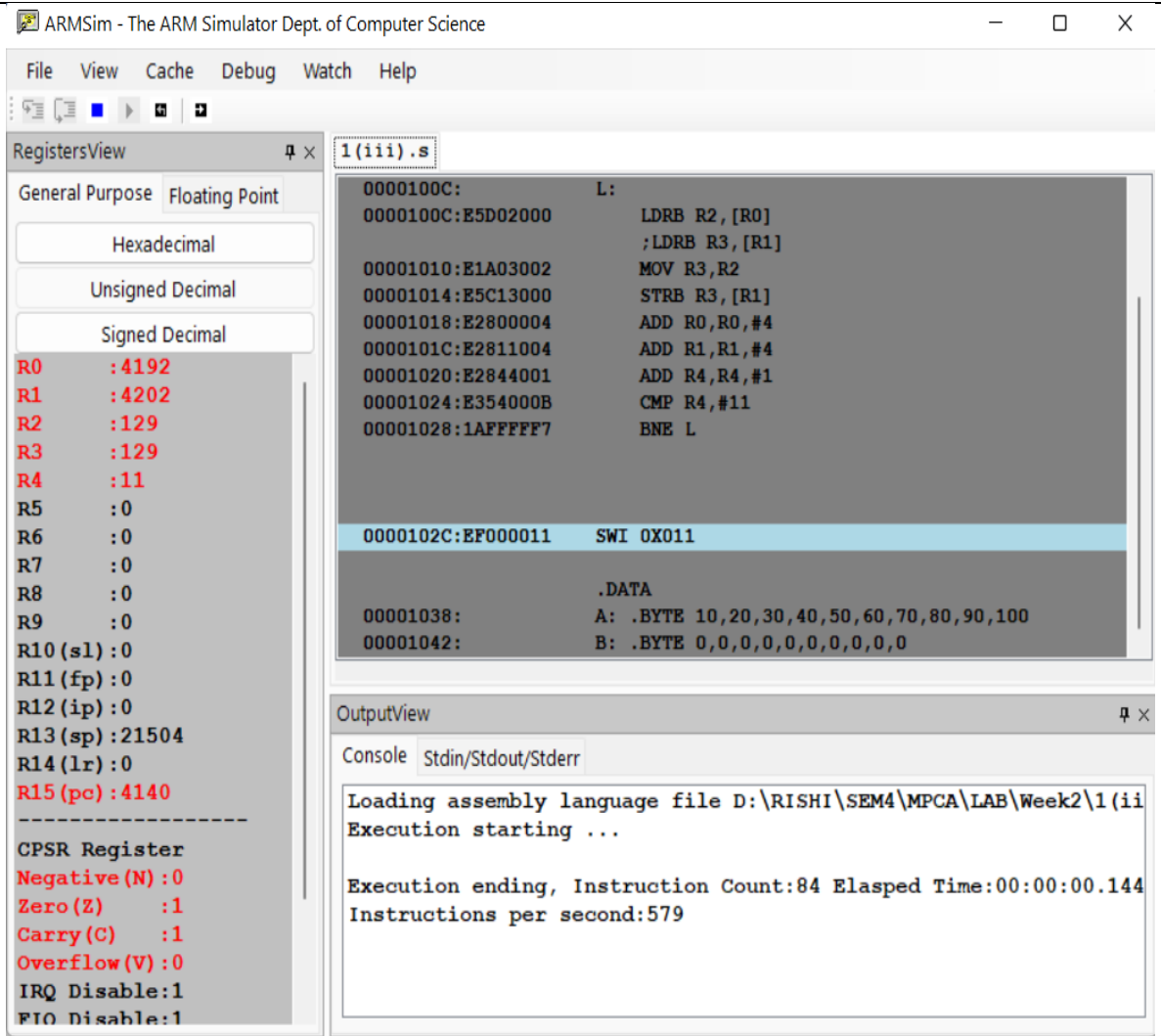
```
1(iii).s - Notepad PREVIEW
File Edit View
|.TEXT
LDR R0, =A
LDR R1, =B
MOV R4,#1

L:
    LDRB R2,[R0]
    ;LDRB R3,[R1]
    MOV R3,R2
    STRB R3,[R1]
    ADD R0,R0,#4
    ADD R1,R1,#4
    ADD R4,R4,#1
    CMP R4,#11
    BNE L

SWI 0X011

.DATA
A: .BYTE 10,20,30,40,50,60,70,80,90,100
B: .BYTE 0,0,0,0,0,0,0,0,0,0
```

Output:



2. Write a program in ARM7TDMI-ISA to find the sum of N data items in the memory. Store the result in the memory location.
 - a) Use Full word (.word directive)

2(i).s - Notepad PREVIEW

File Edit View

```
.TEXT
LDR R0, =A
LDR R1, =B
LDR R3, [R1]
MOV R4, #1

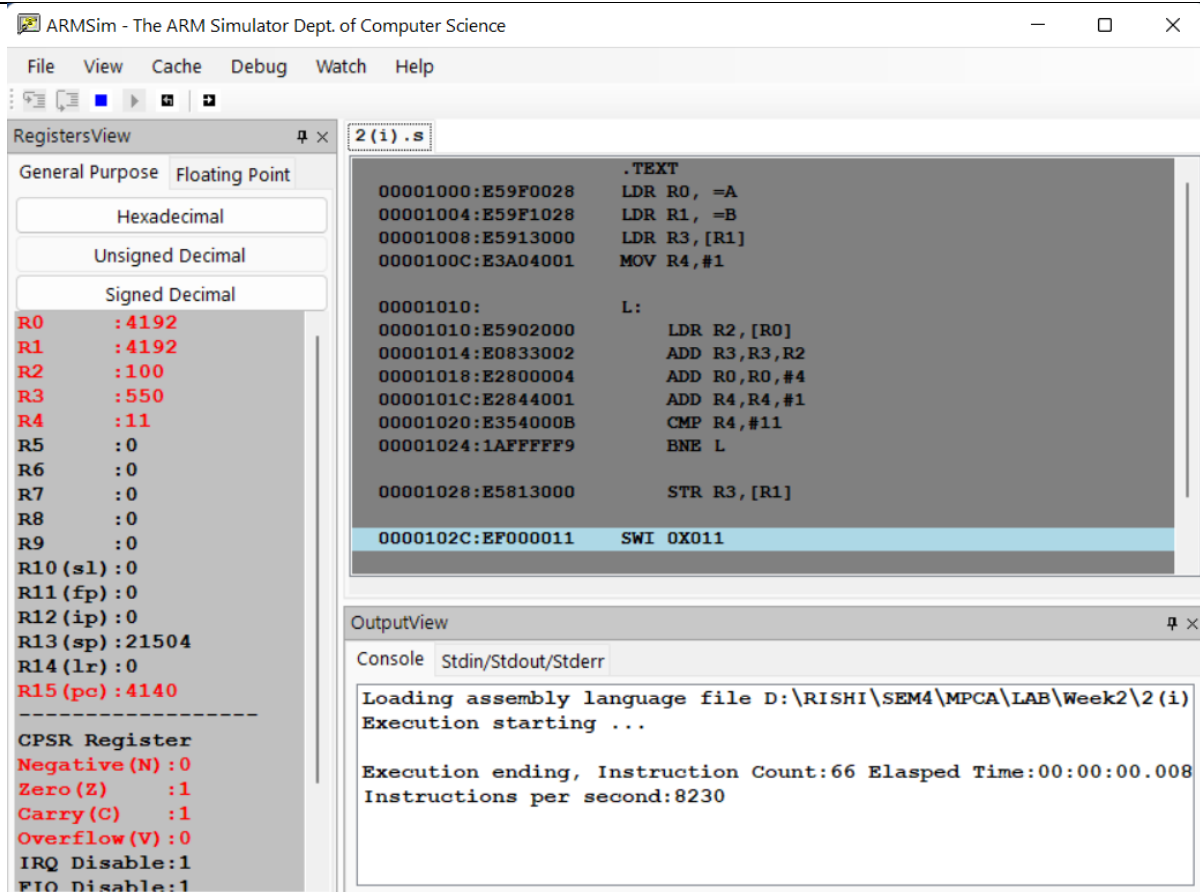
L:
    LDR R2, [R0]
    ADD R3, R3, R2
    ADD R0, R0, #4
    ADD R4, R4, #1
    CMP R4, #11
    BNE L

    STR R3, [R1]

SWI 0X011

.DATA
A: .WORD 10,20,30,40,50,60,70,80,90,100
B: .WORD 0
```

Output:



b) Use Half word(.Hword directive)


```
2(ii).s - Notepad PREVIEW
File Edit View
.TEXT
LDR R0, =A
LDR R1, =B
LDR R3,[R1]
MOV R4,#1

L:
    LDRH R2,[R0]
    ADD R3,R3,R2
    ADD R0,R0,#4
    ADD R4,R4,#1
    CMP R4,#11
    BNE L

    STRH R3,[R1]

SWI 0X011

.DATA
A: .HWORD 10,20,30,40,50,60,70,80,90,100
B: .HWORD 0
```

Output:

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView 2(ii).s

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 4192
R1 : 4172
R2 : 33153
R3 : 132862
R4 : 11
R5 : 0
R6 : 0
R7 : 0
R8 : 0
R9 : 0
R10 (s1) : 0
R11 (fp) : 0
R12 (ip) : 0
R13 (sp) : 21504
R14 (lr) : 0
R15 (pc) : 4140

CPSR Register

Negative (N) : 0
Zero (Z) : 1
Carry (C) : 1
Overflow (V) : 0
IRQ Disable : 1
FIQ Disable : 1

```

00001000:E59F0028    LDR R0, =A
00001004:E59F1028    LDR R1, =B
00001008:E5913000    LDR R3, [R1]
0000100C:E3A04001    MOV R4, #1

00001010:           L:
00001010:E01020B0        LDRH R2, [R0]
00001014:E0833002        ADD R3, R3, R2
00001018:E2800004        ADD R0, R0, #4
0000101C:E2844001        ADD R4, R4, #1
00001020:E354000B        CMP R4, #11
00001024:1AFFFFF9        BNE L

00001028:E00130B0        STRH R3, [R1]

0000102C:EF000011        SWI 0X011

```

OutputView

Console Stdin/Stdout/Stderr

Loading assembly language file D:\RISHI\SEM4\MPCA\LAB\Week2\2(ii).s
Execution starting ...

Execution ending, Instruction Count:66 Elapsed Time:00:00:00.006
Instructions per second:10997

c) Use Byte wise (.Byte directive)

```
.TEXT
LDR R0, =A
LDR R1, =B
LDR R3,[R1]
MOV R4,#1

L:
    LDRB R2,[R0]
    ADD R3,R3,R2
    ADD R0,R0,#4
    ADD R4,R4,#1
    CMP R4,#11
    BNE L

    STRB R3,[R1]

SWI 0X011

.DATA
A: .BYTE 10,20,30,40,50,60,70,80,90,100
B: .BYTE 0
```

Output:

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView 2(ii).s

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 4152
R1 : 4162
R2 : 0
R3 : 1683619840
R4 : 0
R5 : 0
R6 : 0
R7 : 0
R8 : 0
R9 : 0
R10 (s1) : 0
R11 (fp) : 0
R12 (ip) : 0
R13 (sp) : 21504
R14 (lr) : 0
R15 (pc) : 4108

CPSR Register

Negative (N) : 0
Zero (Z) : 0
Carry (C) : 0
Overflow (V) : 0
IRQ Disable : 1
FIQ Disable : 1

```

.TEXT
00001000:E59F0028 LDR R0, =A
00001004:E59F1028 LDR R1, =B
00001008:E5913000 LDR R3, [R1]
0000100C:E3A04001 MOV R4, #1

00001010: L:
00001010:E5D02000 LDRB R2, [R0]
00001014:E0833002 ADD R3, R3, R2
00001018:E2800004 ADD R0, R0, #4
0000101C:E2844001 ADD R4, R4, #1
00001020:E354000B CMP R4, #11
00001024:1AFFFFFF9 BNE L

00001028:E5C13000 STRB R3, [R1]

0000102C:EF000011 SWI 0X011

```

OutputView

Console Stdin/Stdout/Stderr

```

Loading assembly language file D:\RISHI\SEM4\MPCA\LAB\Week2\2(ii)
Execution starting ...
Access to unaligned memory location, bad address = 00001042

Execution ending, Instruction Count:3 Elapsed Time:00:00:00.0170
Instructions per second:176

```

- Write a program in ARM7TDMI-ISA to find the sum of N natural numbers. Store the result in the memory location.

```
3.s - Notepad PREVIEW

File Edit View

.TEXT
LDR R1, =A
LDR R2, =SUM
MOV R4,#0
MOV R5,#1
L1:LDR R3,[R1]
ADD R4,R4,R3
ADD R1,R1,#4
ADD R5,R5,#1
CMP R5,#15
BNE L1
STR R4,[R2]
SWI 0x011

.DATA
A: .WORD 10,25,30,45,50,65,70,85,90,100,105,120,135,140
SUM: .WORD 00
```

Output:

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView 3.s

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0	: 0
R1	: 4208
R2	: 4208
R3	: 140
R4	: 1070
R5	: 15
R6	: 0
R7	: 0
R8	: 0
R9	: 0
R10 (s1)	: 0
R11 (fp)	: 0
R12 (ip)	: 0
R13 (sp)	: 21504
R14 (lr)	: 0
R15 (pc)	: 4140

CPSR Register

Negative (N)	: 0
Zero (Z)	: 1
Carry (C)	: 1
Overflow (V)	: 0
IRQ Disable	: 1
FIQ Disable	: 1

.TEXT

00001000:E59F1028	LDR R1, =A
00001004:E59F2028	LDR R2, =SUM
00001008:E3A04000	MOV R4,#0
0000100C:E3A05001	MOV R5,#1
00001010:E5913000	L1:LDR R3,[R1]
00001014:E0844003	ADD R4,R4,R3
00001018:E2811004	ADD R1,R1,#4
0000101C:E2855001	ADD R5,R5,#1
00001020:E355000F	CMP R5,#15
00001024:1AFFFFF9	BNE L1
00001028:E5824000	STR R4,[R2]
0000102C:EF000011	SWI 0x011

.DATA

00001038:	A: .WORD 10,25,30,45,50,65,70,85,90,100,105,120,135,140
00001070:	SUM: .WORD 00

OutputView

Console Stdin/Stdout/Stderr

Loading assembly language file D:\RISHI\SEM4\MPCA\LAB\Week2\3.s
Execution starting ...

Execution ending, Instruction Count:90 Elapsed Time:00:00:00.031
Instructions per second:2902

4. Write a program in ARM7TDMI-ISA to find the product of two 32-bit numbers using barrel shifter.

```
4.s - Notepad PREVIEW
File Edit View

;multiplication by 9
.text
ldr r0, =a
ldr r1, [r0]
add r2, r1, r1, lsl #3
str r2,[r3]
swi 0x011

.data
a:.word 49
```

Output:

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 4120

R1 : 49

R2 : 441

R3 : 0

R4 : 0

R5 : 0

R6 : 0

R7 : 0

R8 : 0

R9 : 0

R10 (s1) : 0

R11 (fp) : 0

R12 (ip) : 0

R13 (sp) : 21504

R14 (lr) : 0

R15 (pc) : 4112

CPSR Register

Negative (N) : 0

Zero (Z) : 0

Carry (C) : 0

Overflow (V) : 0

IRQ Disable: 1

FIQ Disable: 1

4.s

```
;multiplication by 9
.text
00001000:E59F000C ldr r0, =a
00001004:E5901000 ldr r1, [r0]
00001008:E0812181 add r2, r1, r1, lsl #3
0000100C:E5832000 str r2,[r3]
00001010:EF000011 swi 0x011

.data
00001018: a:.word 49
```

OutputView

Console Stdin/Stdout/Stderr

Loading assembly language file D:\RISHI\SEM4\MPCA\LAB\Week2\4.s

Execution starting ...

Execution ending, Instruction Count:5 Elapsed Time:00:00:00.004

Instructions per second:1002

5. Convert the following statement in C language into an ALP using ARM7TDMI – ISA.

IF([A]==[B]) then C=[A]+[B];

ELSE IF ([B]==[C]) D=[A]-[B];

ELSE E=[A]*[B]

Where A,B, C, D & E are memory locations.

Case1:



5.s - Notepad PREVIEW

File Edit View

```
.text
ldr r0, =a
ldr r1, =b
ldr r2, =c
ldr r3, [r0]
ldr r4, [r1]
ldr r5, [r2]
;if(a==b)
cmp r3, r4
bne x
add r6, r3, r4
b endif

;else if(b==c)
x:
cmp r4, r5
bne y
sub r6, r3, r4
b endif

;else
y:
mul r7, r3, r4

endif:
swi 0x011

.data
a:.word 4
b:.word 4
c:.word 5
```


Output:

ARMSim - The ARM Simulator Dept. of Computer Science

FileViewCacheDebugWatchHelp

RegistersView

General PurposeFloating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0: 4172

R1: 4176

R2: 4180

R3: 4

R4: 4

R5: 5

R6: 8

R7: 0

R8: 0

R9: 0

R10 (s1): 0

R11 (fp): 0

R12 (ip): 0

R13 (sp): 21504

R14 (lr): 0

R15 (pc): 4156

CPSR Register

Negative (N): 0

Zero (Z): 1

Carry (C): 1

Overflow (V): 0

IRQ Disable: 1

FIQ Disable: 1

Thumb (T): 0

CPU Mode: System

0x600000df

5.s

.text

00001000:E59F0038ldr r0, =a

00001004:E59F1038ldr r1, =b

00001008:E59F2038ldr r2, =c

0000100C:E5903000ldr r3, [r0]

00001010:E5914000ldr r4, [r1]

00001014:E5925000ldr r5, [r2]

:if (a==b)

00001018:E1530004cmp r3, r4

0000101C:1A000001bne x

00001020:E0836004add r6, r3, r4

00001024:EA000004b endif

:else if (b==c)

00001028:x:

00001028:E1540005cmp r4, r5

0000102C:1A000001bne y

00001030:E0436004sub r6, r3, r4

00001034:EA000000b endif

:else

00001038:y:

00001038:E0070493mul r7, r3, r4

0000103C:endif:

0000103C:EF000011swi 0x011

.data

0000104C:a: word 4

00001050:b: word 4

00001054:c: word 5

MemoryView0

00001010

00001010	E5914000	E5925000	E1530004	1A000001	E0836004	EA000004	E1540005	1A000001	E0436004
00001044	00001050	00001054	00000004	00000004	00000005	81818181	81818181	81818181	81818181
00001078	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181	81818181

Case 2:

 5.s - Notepad PREVIEW

File Edit View

```
.text
ldr r0, =a
ldr r1, =b
ldr r2, =c
ldr r3, [r0]
ldr r4, [r1]
ldr r5, [r2]
;if(a==b)
cmp r3, r4
bne x
add r6, r3, r4
b endif

;else if(b==c)
x:
cmp r4, r5
bne y
sub r6, r3, r4
b endif

;else
y:
mul r7, r3, r4

endif:
swi 0x011

.data
a:.word 4
b:.word 5
c:.word 5
```

Output:

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView 5.s

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 4172
R1 : 4176
R2 : 4180
R3 : 4
R4 : 5
R5 : 5
R6 : -1
R7 : 0
R8 : 0
R9 : 0
R10 (s1) : 0
R11 (fp) : 0
R12 (ip) : 0
R13 (sp) : 21504
R14 (lr) : 0
R15 (pc) : 4156

CPSR Register
Negative (N) : 0
Zero (Z) : 1
Carry (C) : 1
Overflow (V) : 0
IRQ Disable: 1
FIQ Disable: 1
Thumb (T) : 0
CPU Mode : System

0x600000df

```

.text
00001000:E59F0038 ldr r0, =a
00001004:E59F1038 ldr r1, =b
00001008:E59F2038 ldr r2, =c
0000100C:E5903000 ldr r3, [r0]
00001010:E5914000 ldr r4, [r1]
00001014:E5925000 ldr r5, [r2]
; if (a==b)
00001018:E1530004 cmp r3, r4
0000101C:1A000001 bne x
00001020:E0836004 add r6, r3, r4
00001024:EA000004 b endif

; else if (b==c)
00001028:
x:
00001028:E1540005 cmp r4, r5
0000102C:1A000001 bne y
00001030:E0436004 sub r6, r3, r4
00001034:EA000000 b endif

; else
00001038:
y:
00001038:E0070493 mul r7, r3, r4

0000103C:
endif:
0000103C:EF000011 swi 0x011

.data
0000104C:
a:.word 4
00001050:
b:.word 5
00001054:
c:.word 5

```

MemoryView0

00001010

00001010	E5914000	E5925000	E1530004	1A000001	E0836004	EA000004
00001044	00001050	00001054	00000004	00000005	00000005	81818181
00001078	81818181	81818181	81818181	81818181	81818181	81818181

Case 3:



5.s - Notepad PREVIEW

File Edit View

```
.text
ldr r0, =a
ldr r1, =b
ldr r2, =c
ldr r3, [r0]
ldr r4, [r1]
ldr r5, [r2]
;if(a==b)
cmp r3, r4
bne x
add r6, r3, r4
b endif

;else if(b==c)
x:
cmp r4, r5
bne y
sub r6, r3, r4
b endif

;else
y:
mul r7, r3, r4

endif:
swi 0x011

.data
a:.word 4
b:.word 5
c:.word 6
```

Output:

FileViewCacheDebugWatchHelp

RegistersView

General PurposeFloating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0: 4172

R1: 4176

R2: 4180

R3: 4

R4: 5

R5: 6

R6: 0

R7: 20

R8: 0

R9: 0

R10 (s1): 0

R11 (fp): 0

R12 (ip): 0

R13 (sp): 21504

R14 (lr): 0

R15 (pc): 4156

CPSR Register

Negative (N): 1

Zero (Z): 0

Carry (C): 0

Overflow (V): 0

IRQ Disable: 1

FIQ Disable: 1

Thumb (T): 0

CPU Mode: System

0x800000df

5.s

```

.text
00001000:E59F0038    ldr r0, =a
00001004:E59F1038    ldr r1, =b
00001008:E59F2038    ldr r2, =c
0000100C:E5903000    ldr r3, [r0]
00001010:E5914000    ldr r4, [r1]
00001014:E5925000    ldr r5, [r2]
                    ;if(a==b)
00001018:E1530004    cmp r3, r4
0000101C:1A000001    bne x
00001020:E0836004    add r6, r3, r4
00001024:EA000004    b endif

                    ;else if(b==c)
00001028:          x:
00001028:E1540005    cmp r4, r5
0000102C:1A000001    bne y
00001030:E0436004    sub r6, r3, r4
00001034:EA000000    b endif

                    ;else
00001038:          y:
00001038:E0070493    mul r7, r3, r4

0000103C:          endif:
0000103C:EF000011    swi 0x011

.data
0000104C:          a:.word 4
00001050:          b:.word 5
00001054:          c:.word 6

```

MemoryView0

00001010

00001010	E5914000	E5925000	E1530004	1A000001	E0836004
00001044	00001050	00001054	00000004	00000005	00000006
00001078	81818181	81818181	81818181	81818181	81818181