CS2323- Final Project Proposal

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Project Topic: **RISC-V 32-bit or 64-bit processor design and demonstration on FPGA board**

Scope of the Project:

- The project aims to design and implement a configurable RISC-V processor in Verilog. The processor will support both RV32I and RV64I instruction sets through parameters.
- The following features will be implemented:
    a) Standard RISC-V machine encoding of instructions.
    b) Pipelined implementation along with hazard detection and forwarding.
    c) Implementation of the M extension for integer multiplication and division.

Implementation Timeline:

- Implement the base processor in Verilog. The design will be parameterized.
- Add pipeline stages, while implementing hazard detection and forwarding.
- Implementing the M extension in Verilog, and integrating it along with the base processor.
- Simulate and verify the working of the processor using testbenches.
- Deploy the design on an FPGA and debug.
- Demonstrate the correct operation on an FPGA.

Verification:

- Verification will be done using testbenches and pre-written RISC-V assembly codes.
- The hazard detection and pipelining correctness will be verified by checking the working for corner test-cases.

Final Project Deliverables:

- The final working codebase.
- A demonstration on an FPGA.
- A final report describing the implementation procedure, the timing analysis and resource utilization.

Team Members:

- This is an individual project; no additional team members.