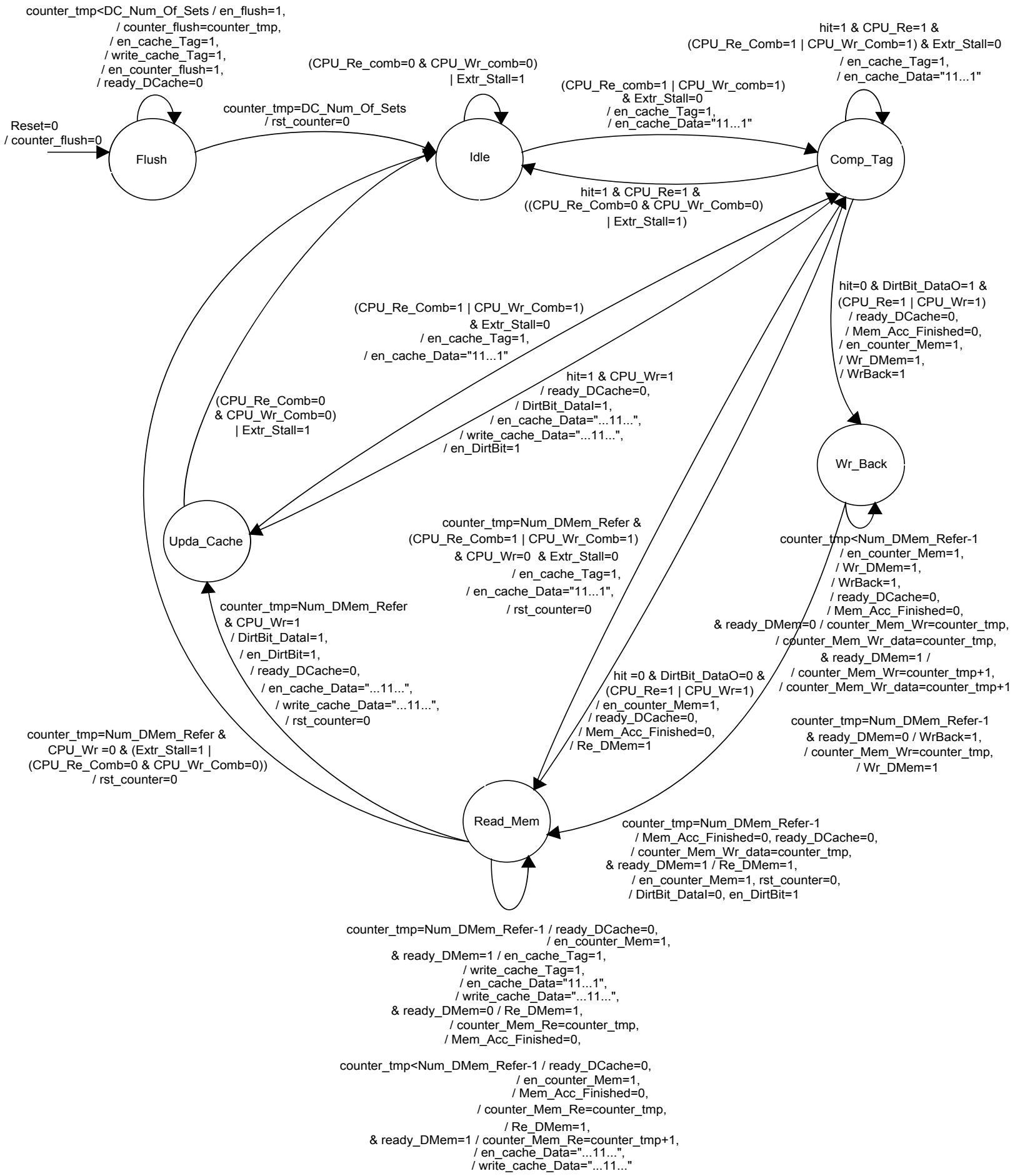
counter_tmp<DC_Num_Of_Sets / en_flush=1,
/ counter_flush=counter_tmp,
/ en_cache_Tag=1,
/ write_cache_Tag=1,
/ en_counter_flush=1,
/ ready_DCache=0
Reset=0
/ counter_flush=0
Flush
counter_tmp=DC_Num_Of_Sets
/ rst_counter=0
(CPU_Re_comb=0 & CPU_Wr_comb=0)
| Extr_Stall=1
Idle
(CPU_Re_comb=1 | CPU_Wr_comb=1)
& Extr_Stall=0
/ en_cache_Tag=1,
/ en_cache_Data="11...1"
hit=1 & CPU_Re=1 &
(CPU_Re_Comb=1 | CPU_Wr_Comb=1) & Extr_Stall=0
/ en_cache_Tag=1,
/ en_cache_Data="11...1"
Comp_Tag
hit=1 & CPU_Re=1 &
((CPU_Re_Comb=0 & CPU_Wr_Comb=0)
| Extr_Stall=1)
hit=0 & DirtBit_DataO=1 &
(CPU_Re=1 | CPU_Wr=1)
/ ready_DCache=0,
/ Mem_Acc_Finished=0,
/ en_counter_Mem=1,
/ Wr_DMem=1,
/ WrBack=1
(CPU_Re_Comb=1 | CPU_Wr_Comb=1)
& Extr_Stall=0
/ en_cache_Tag=1,
/ en_cache_Data="11...1"
hit=1 & CPU_Wr=1
/ ready_DCache=0,
/ DirtBit_DataI=1,
/ en_cache_Data="...11...",
/ write_cache_Data="...11...",
/ en_DirtBit=1
(CPU_Re_Comb=0
& CPU_Wr_Comb=0)
| Extr_Stall=1
Wr_Back
Upda_Cache
counter_tmp=Num_DMem_Refer &
(CPU_Re_Comb=1 | CPU_Wr_Comb=1)
& CPU_Wr=0 & Extr_Stall=0
/ en_cache_Tag=1,
/ en_cache_Data="11...1",
/ rst_counter=0
counter_tmp<Num_DMem_Refer-1
/ en_counter_Mem=1,
/ Wr_DMem=1,
/ WrBack=1,
/ ready_DCache=0,
/ Mem_Acc_Finished=0,
& ready_DMem=0 / counter_Mem_Wr=counter_tmp,
/ counter_Mem_Wr_data=counter_tmp,
& ready_DMem=1 /
/ counter_Mem_Wr=counter_tmp+1,
/ counter_Mem_Wr_data=counter_tmp+1
counter_tmp=Num_DMem_Refer
& CPU_Wr=1
/ DirtBit_DataI=1,
/ en_DirtBit=1,
/ ready_DCache=0,
/ en_cache_Data="...11...",
/ write_cache_Data="...11...",
/ rst_counter=0
hit =0 & DirtBit_DataO=0 &
(CPU_Re=1 | CPU_Wr=1)
/ en_counter_Mem=1,
/ ready_DCache=0,
/ Mem_Acc_Finished=0,
/ Re_DMem=1
counter_tmp=Num_DMem_Refer-1
& ready_DMem=0 / WrBack=1,
/ counter_Mem_Wr=counter_tmp,
/ Wr_DMem=1
counter_tmp=Num_DMem_Refer &
CPU_Wr =0 & (Extr_Stall=1 |
(CPU_Re_Comb=0 & CPU_Wr_Comb=0))
/ rst_counter=0
Read_Mem
counter_tmp=Num_DMem_Refer-1
/ Mem_Acc_Finished=0, ready_DCache=0,
/ counter_Mem_Wr_data=counter_tmp,
& ready_DMem=1 / Re_DMem=1,
/ en_counter_Mem=1, rst_counter=0,
/ DirtBit_DataI=0, en_DirtBit=1
counter_tmp=Num_DMem_Refer-1 / ready_DCache=0,
/ en_counter_Mem=1,
& ready_DMem=1 / en_cache_Tag=1,
/ write_cache_Tag=1,
/ en_cache_Data="11...1",
/ write_cache_Data="...11...",
& ready_DMem=0 / Re_DMem=1,
/ counter_Mem_Re=counter_tmp,
/ Mem_Acc_Finished=0,
counter_tmp<Num_DMem_Refer-1 / ready_DCache=0,
/ en_counter_Mem=1,
/ Mem_Acc_Finished=0,
/ counter_Mem_Re=counter_tmp,
/ Re_DMem=1,
& ready_DMem=1 / counter_Mem_Re=counter_tmp+1,
/ en_cache_Data="...11...",
/ write_cache_Data="...11..."