MADVLSI Mini Project 1
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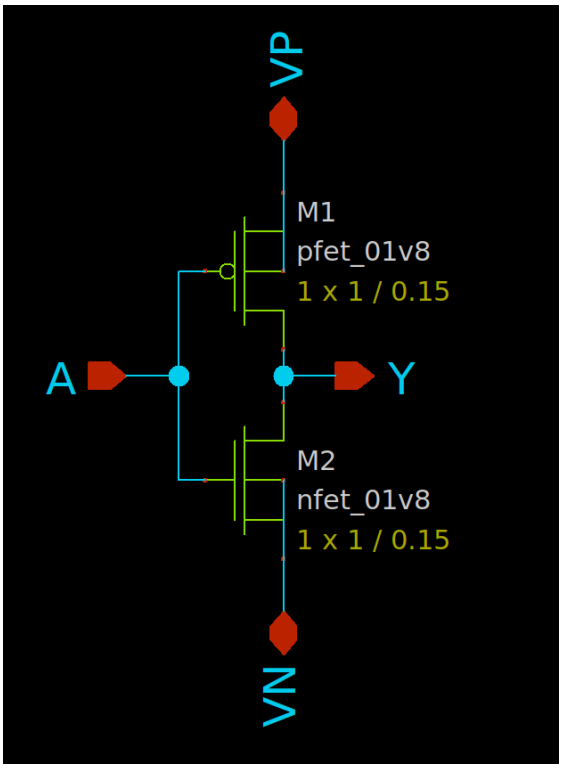
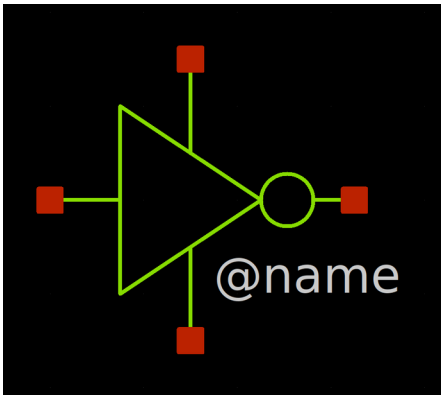
Github: https://github.com/vscheyer/MADVLSI

1. Schematic Capture and Simulation

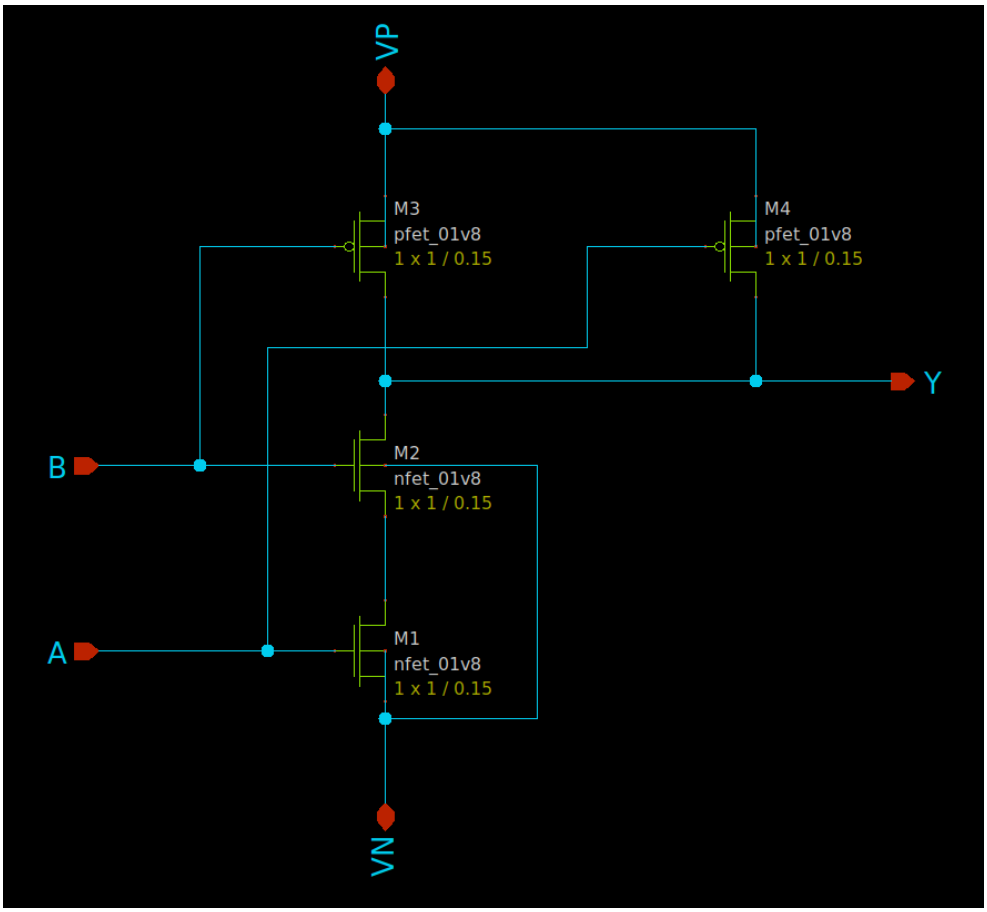
Inverter Schematic:



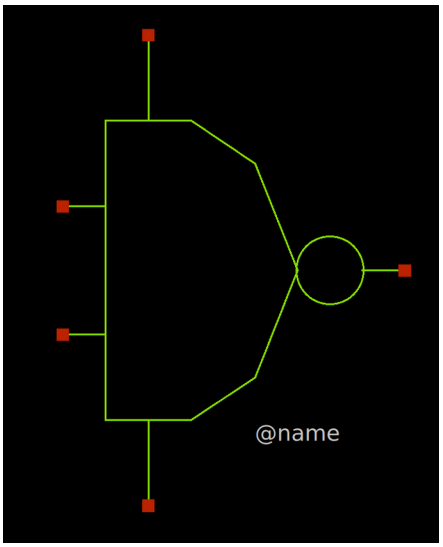
Inverter Symbol:



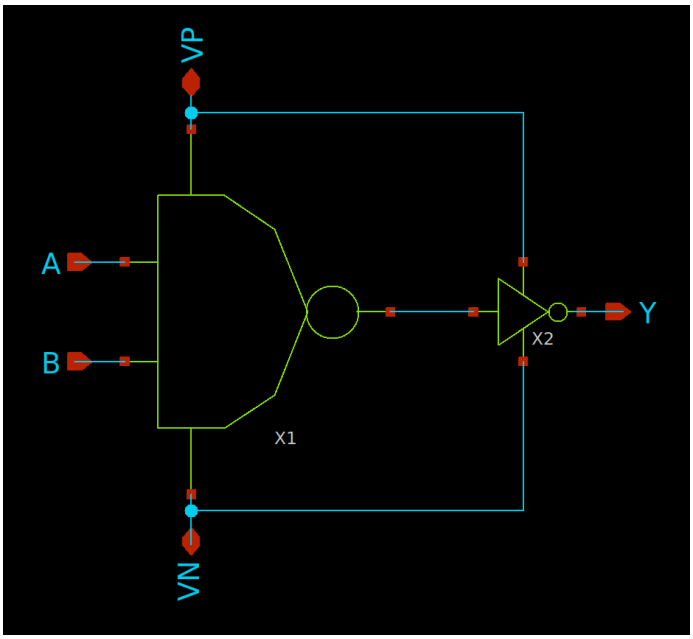
NAND Gate Schematic:



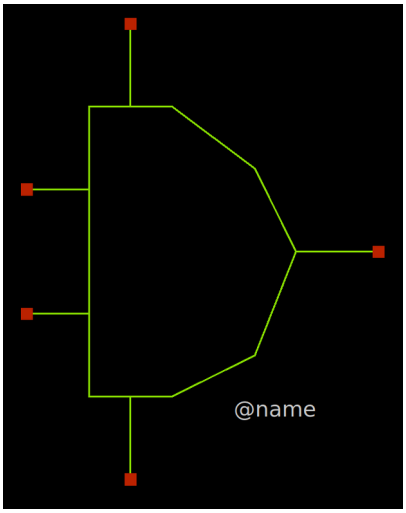
NAND Gate Symbol



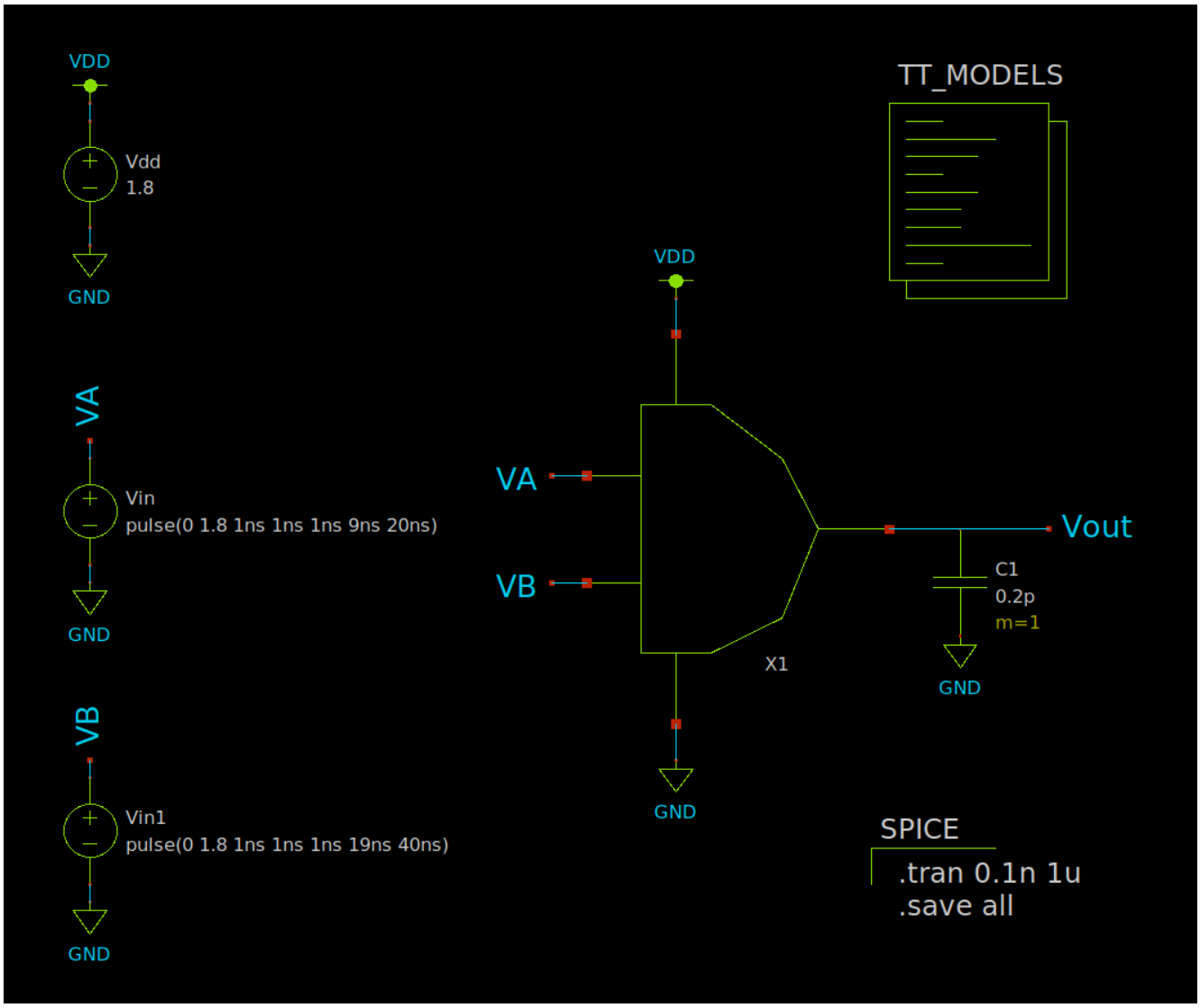
AND Gate Schematic:



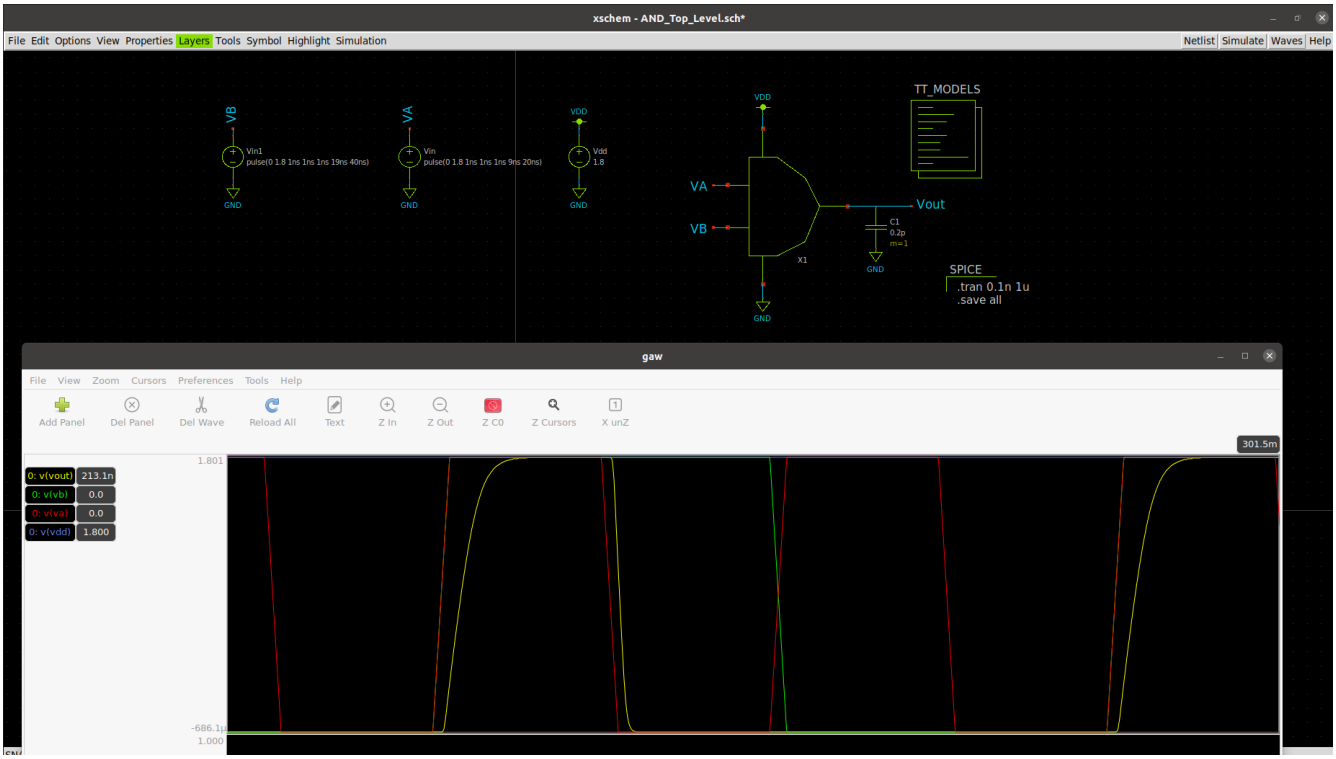
AND Gate Symbol:



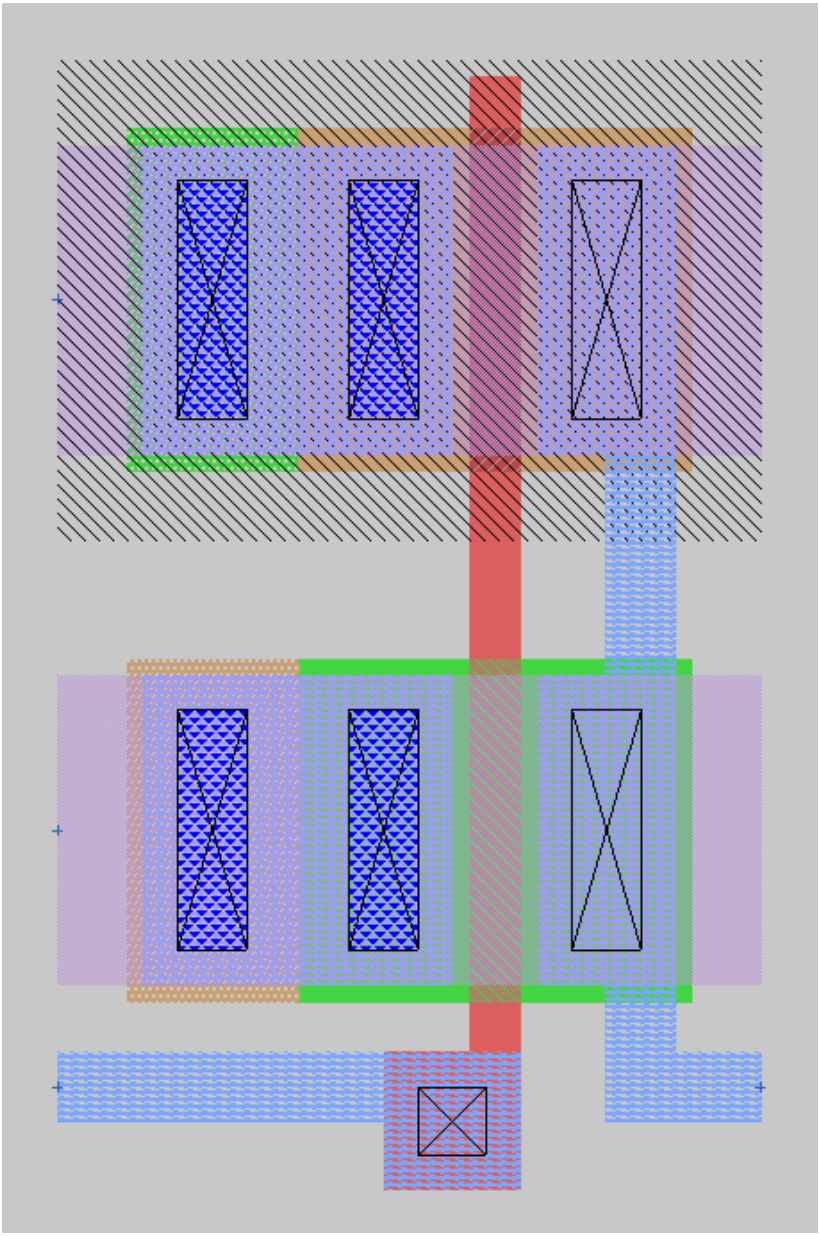
Top Level AND Gate Schematic For Simulation:



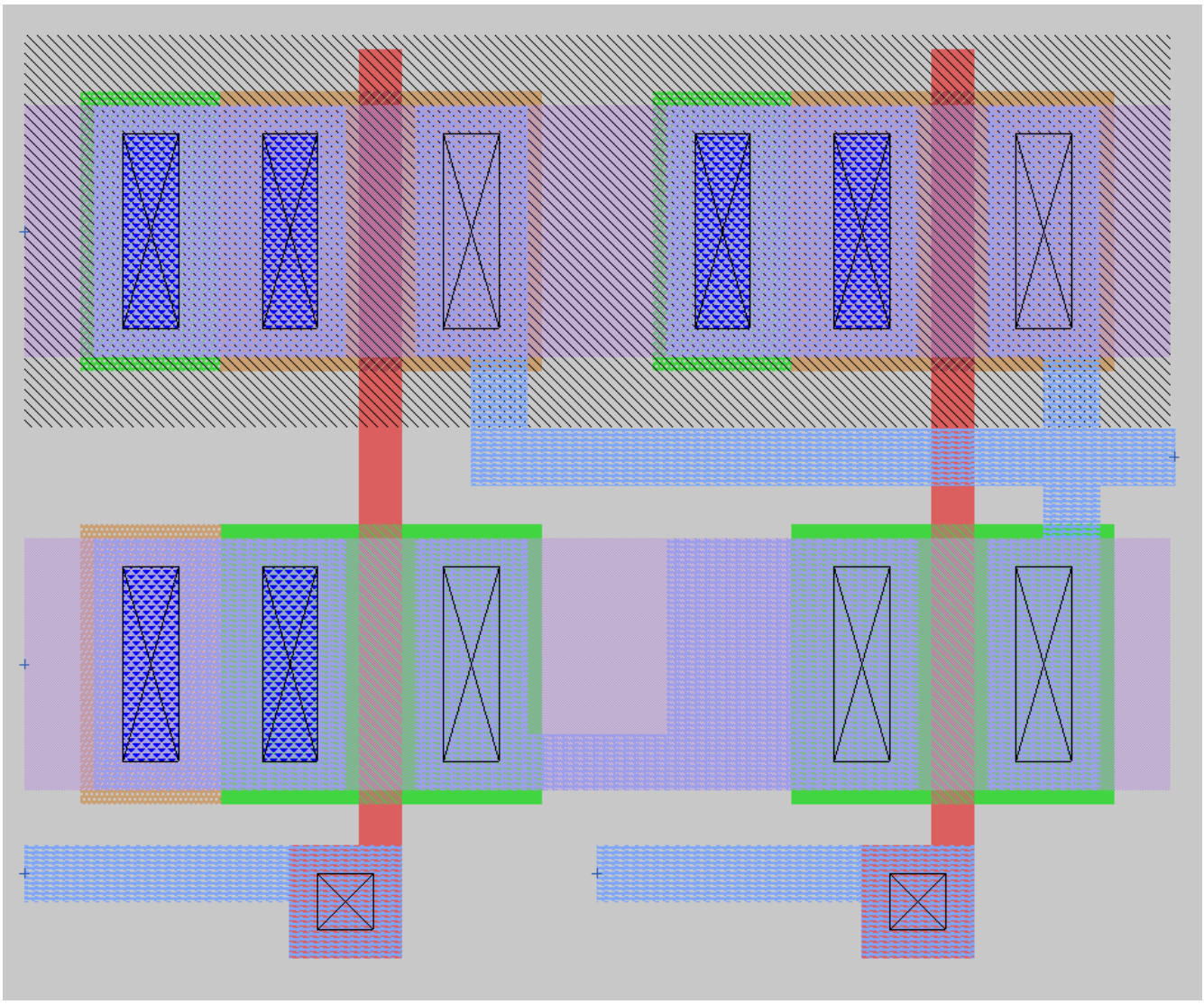
AND Gate Simulation Output:



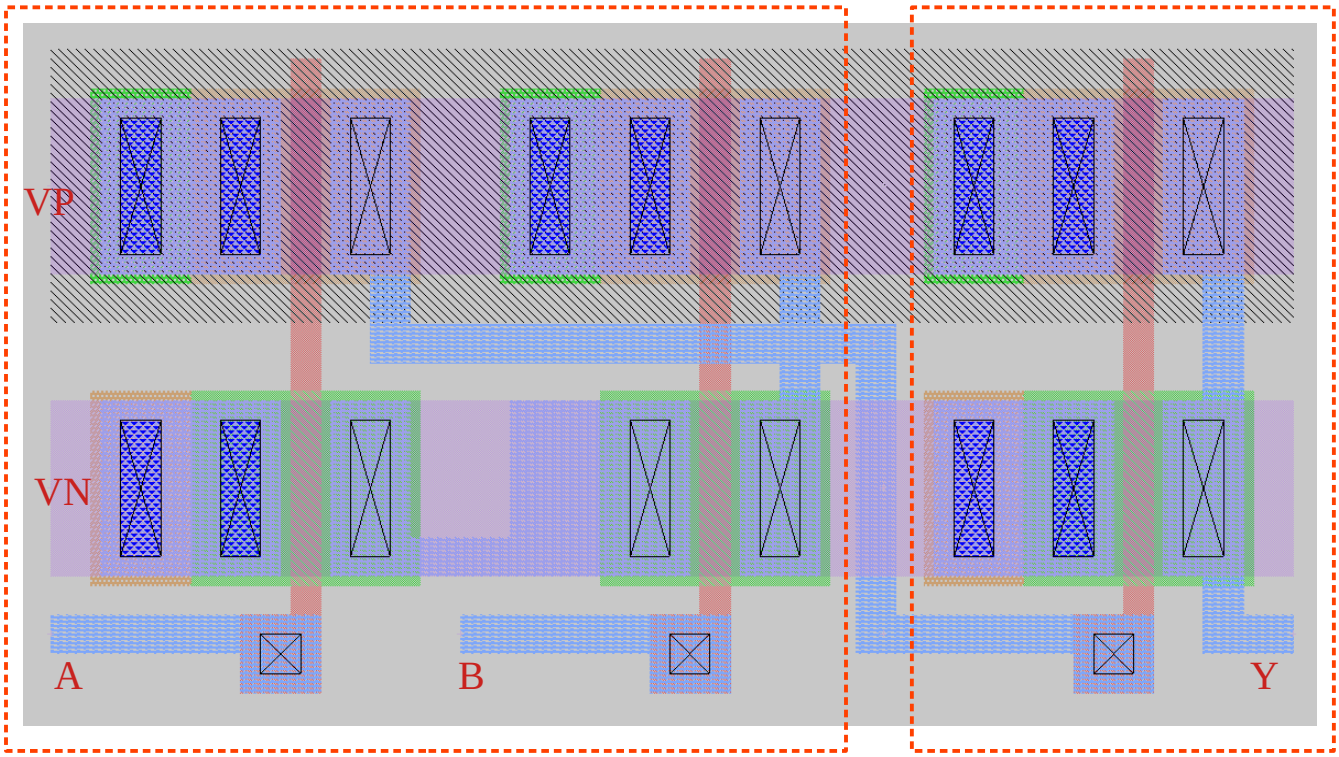
Inverter Subcircuit Layout:



NAND Gate Subcircuit Layout:



AND Gate Layout:



(NAND subsircuit on the left, inverter subcircuit on the right. Letters denote inputs and outputs.)

Layout Versus Schematic Comparison:

```
madvlsi@madvlsi-ubuntu:~/Documents/Mini_Project_1/lvs$ netgen -batch lvs
and_gate_lvs_xschem.spice and_gate_layout.spice ~/skywater/open_pdks/sky1
30/netgen/sky130_setup.tcl
Netgen 1.5.166 compiled on Mon 15 Feb 2021 11:47:17 PM EST
Warning: netgen command 'format' use fully-qualified name '::netgen::form
at'
Warning: netgen command 'global' use fully-qualified name '::netgen::glob
al'
Reading netlist file and_gate_lvs_xschem.spice
Call to undefined subcircuit AND_Gate
Creating placeholder cell definition.
Call to undefined subcircuit NAND_Gate
Creating placeholder cell definition.
Call to undefined subcircuit Inverter
Creating placeholder cell definition.
Call to undefined subcircuit sky130_fd_pr__nfet_01v8
Creating placeholder cell definition.
Call to undefined subcircuit sky130_fd_pr__pfet_01v8
Creating placeholder cell definition.
Reading netlist file and_gate_layout.spice
Call to undefined subcircuit sky130_fd_pr__nfet_01v8
Creating placeholder cell definition.
Call to undefined subcircuit sky130_fd_pr__pfet_01v8
Creating placeholder cell definition.
Reading setup file /home/madvlsi/skywater/open_pdks/sky130/netgen/sky130_
setup.tcl
Model sky130_fd_pr__nfet_01v8 pin 1 == 3
Model sky130_fd_pr__nfet_01v8 pin 1 == 3
No property mult found for device sky130_fd_pr__nfet_01v8
No property sa found for device sky130_fd_pr__nfet_01v8
No property sb found for device sky130_fd_pr__nfet_01v8
No property sd found for device sky130_fd_pr__nfet_01v8
No property nf found for device sky130_fd_pr__nfet_01v8
No property nrd found for device sky130_fd_pr__nfet_01v8
No property nrs found for device sky130_fd_pr__nfet_01v8
Model sky130_fd_pr__pfet_01v8 pin 1 == 3
Model sky130_fd_pr__pfet_01v8 pin 1 == 3
No property mult found for device sky130_fd_pr__pfet_01v8
No property sa found for device sky130_fd_pr__pfet_01v8
No property sb found for device sky130_fd_pr__pfet_01v8
No property sd found for device sky130_fd_pr__pfet_01v8
No property nf found for device sky130_fd_pr__pfet_01v8
No property nrd found for device sky130_fd_pr__pfet_01v8
No property nrs found for device sky130_fd_pr__pfet_01v8
Comparison output logged to file comp.out
Logging to file "comp.out" enabled
Contents of circuit 1:  Circuit: 'sky130_fd_pr__nfet_01v8'
Circuit sky130_fd_pr__nfet_01v8 contains 0 device instances.
Circuit contains 0 nets.
Contents of circuit 2:  Circuit: 'sky130_fd_pr__nfet_01v8'
Circuit sky130_fd_pr__nfet_01v8 contains 0 device instances.
Circuit contains 0 nets.
Circuit sky130_fd_pr__pfet_01v8 contains no devices.
Contents of circuit 1:  Circuit: 'NAND_Gate'
Circuit NAND_Gate contains 4 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   2
  Class: sky130_fd_pr__pfet_01v8 instances:   2
Circuit contains 6 nets.
Contents of circuit 2:  Circuit: 'nand_gate'
Circuit nand_gate contains 4 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   2
  Class: sky130_fd_pr__pfet_01v8 instances:   2
Circuit contains 6 nets.

Circuit 1 contains 4 devices, Circuit 2 contains 4 devices.
Circuit 1 contains 6 nets,    Circuit 2 contains 6 nets.

Netlists match uniquely.
Contents of circuit 1:  Circuit: 'Inverter'
Circuit Inverter contains 2 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   1
  Class: sky130_fd_pr__pfet_01v8 instances:   1
Circuit contains 4 nets.
Contents of circuit 2:  Circuit: 'inverter'
Circuit inverter contains 2 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   1
  Class: sky130_fd_pr__pfet_01v8 instances:   1
Circuit contains 4 nets.

Circuit 1 contains 2 devices, Circuit 2 contains 2 devices.
Circuit 1 contains 4 nets,    Circuit 2 contains 4 nets.

Netlists match uniquely.
Contents of circuit 1:  Circuit: 'and_gate_lvs_xschem.spice'
Circuit and_gate_lvs_xschem.spice contains 2 device instances.
  Class: NAND_Gate             instances:   1
  Class: Inverter              instances:   1
Circuit contains 6 nets.
Contents of circuit 2:  Circuit: 'and_gate_layout.spice'
Circuit and_gate_layout.spice contains 2 device instances.
  Class: nand_gate             instances:   1
  Class: inverter              instances:   1
Circuit contains 6 nets.

Circuit 1 contains 2 devices, Circuit 2 contains 2 devices.
Circuit 1 contains 6 nets,    Circuit 2 contains 6 nets.

Netlists match uniquely.
Result: Circuits match uniquely.
Logging to file "comp.out" disabled
LVS Done.
```