MADVLSI Miniproject 2
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github: https://github.com/vscheyer/MADVLSI/tree/master/Mini_Project_2

For this project, I made a 4-bit shift register based on complementary set-reset logic (CSRL) flip-flop stages. This type of cell behaves in a similar way to a D flip-flop, but the CSRL is not ratioless. In other words, the transistor ratios affect the operation of the device. I based my design on Massimo Antonio Sivilotti's California Institute of Technology PhD thesis paper.[1] The strength ratio of importance is that of the pass transistors, which are $M_8$ and $M_9$ in my schematic as shown in Figure 1.

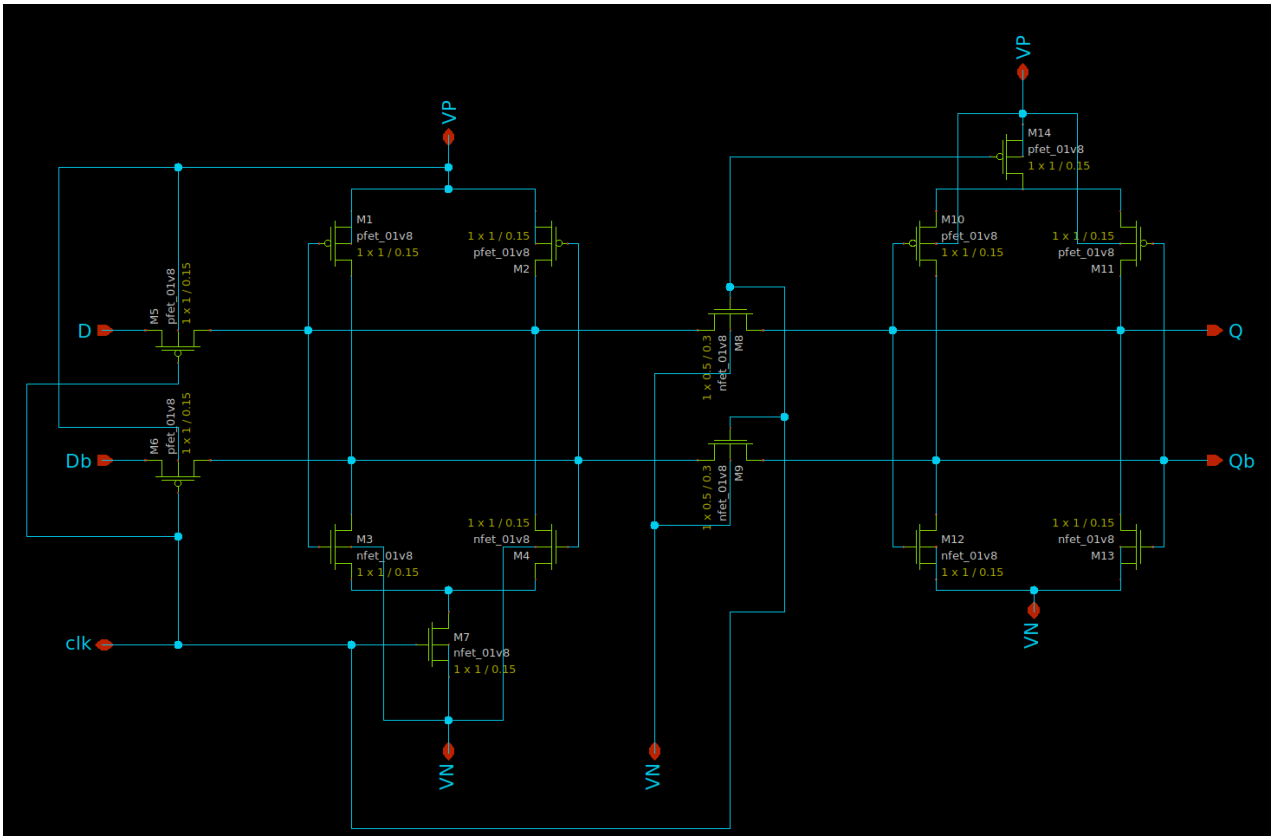

Figure 1: CSRL Schematic

It is desirable to achieve a strength ratio for the pass transistors such that the following ratio holds true:

$$\frac{\frac{W_{M7}}{L_{M7}}}{\frac{W_{M8}}{L_{M8}}} = 4$$

1 http://madvlsi.olin.edu/madvlsi/internal/Sivilotti91.pdf

In this case, $M_8$ is a pass transistor and $M_7$ is another transistor in the circuit. The strength ratios of the $M_8$ and $M_9$ pass transistors should match. Since I started with all my transistors at W=1 um and L=0.15 um, I calculated that I could change the widths of $M_8$ and $M_9$ to 0.25 um to achieve the suggested ratio of 4. However, when I went to implement this in my layout I ran into a design rule violation that specified the transistors may have a minimum width of 0.42 um. I changed the lengths of the pass transistors to 0.3 um to account for this, and so my pass transistors proportionally then had a width of W=0.5 um.

Figure 2 shows my CSRL layout. My CSRL has a cell width of 4.75um.

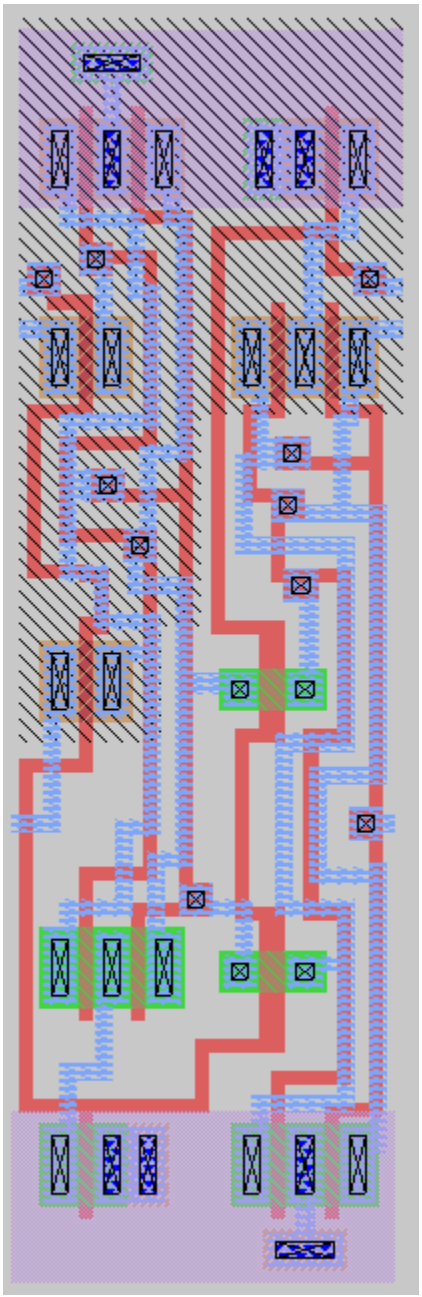

Figure 2: CSRL layout. Cell width = 4.75um.

Before moving on to the next step, I performed LVS on the CSRL cell to make sure those netlists matched. I checked that the transistor lengths and widths matched as well. Figure 3 shows the schematic I used to export a netlist for LVS. The output file from this LVS is in the *CSRL/lvs/* folder.

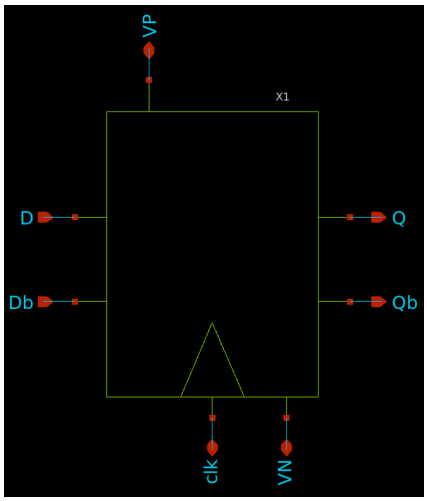


Figure 3: Top level schematic for exporting a CSRL netlist.

Next, I created a 4-bit shift register schematic by chaining together four CSRL latches. I also added an inverter to create the Db input from the D input. Figure 4 shows the shift register top level schematic that I used to export a netlist for LVS.

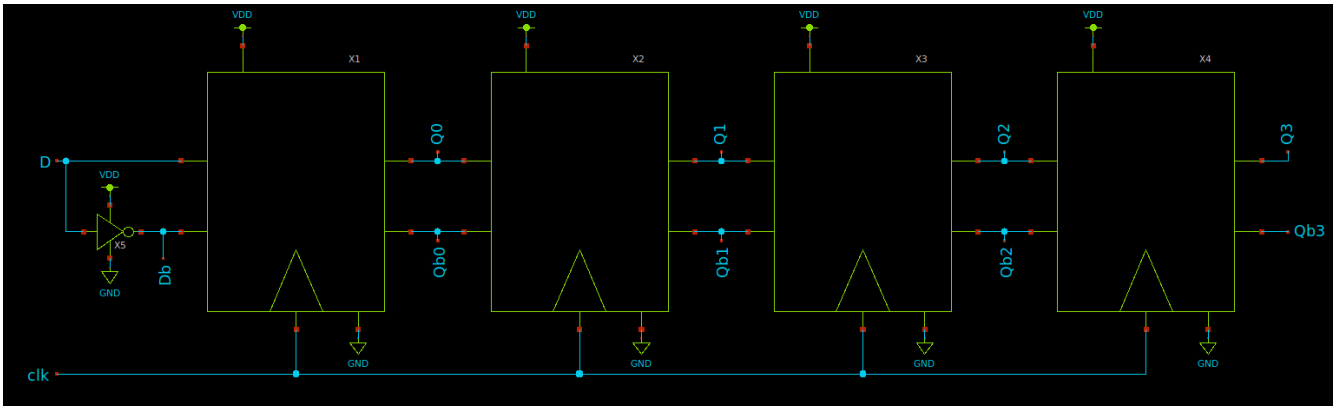


Figure 4: Top level schematic for exporting 4-bit shift register netlist.

I copied my shift register schematic over into a new file to create my transient simulation harness as shown in Figure 5.

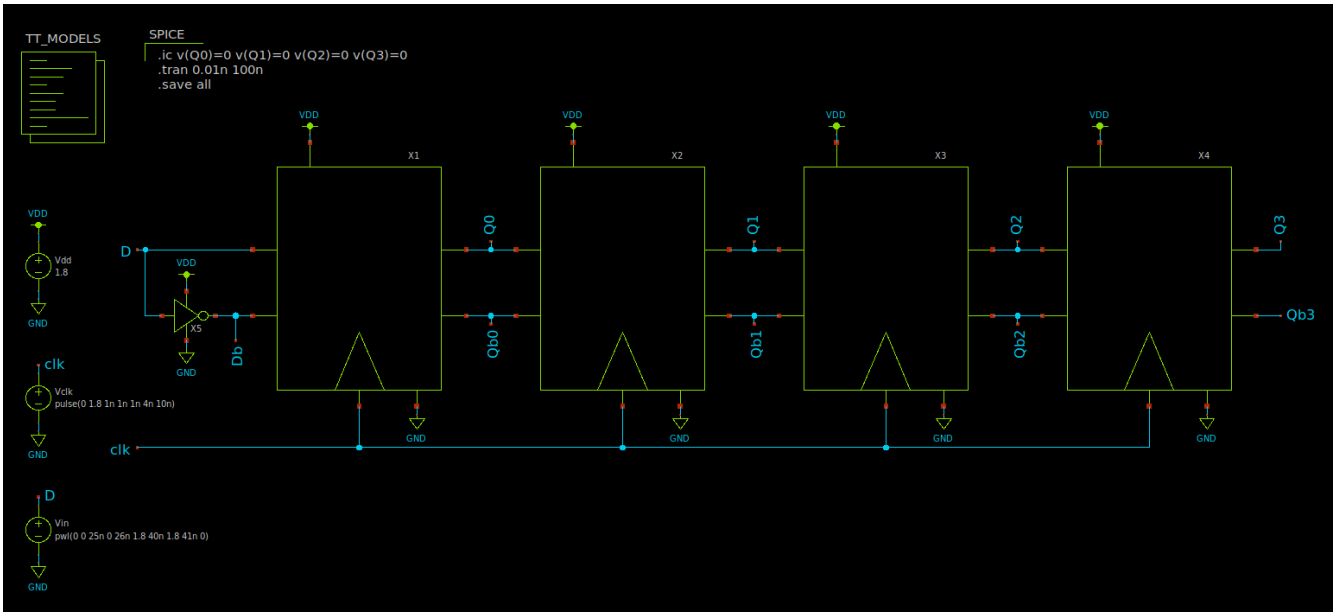

Figure 5: Test harness schematic for 4-bit shift register.

This simulation produced the waveforms shown in Figure 5. I was initially alarmed that the $Q_{\{0\text{-}3\}}$ rising edges did not reach the full 1.8 V, but after asking Brad I learned that this is because the CSRL latch can only pass one logic value strongly due to the type of the pass transistors.

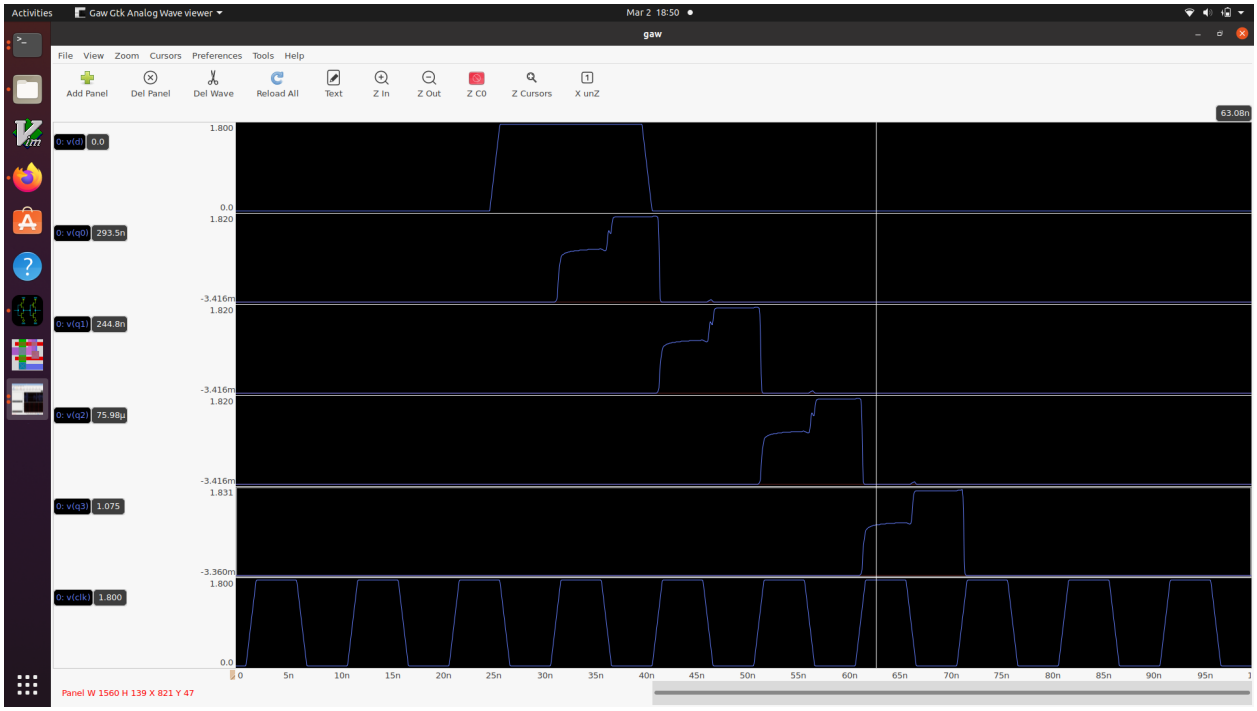

Figure 5: Waveforms for shift register transient simulation.

Once I had verified that my schematic worked, I implemented the shift register layout by importing four instances of the CSRL latch and one inverter cell as shown in Figure 6.

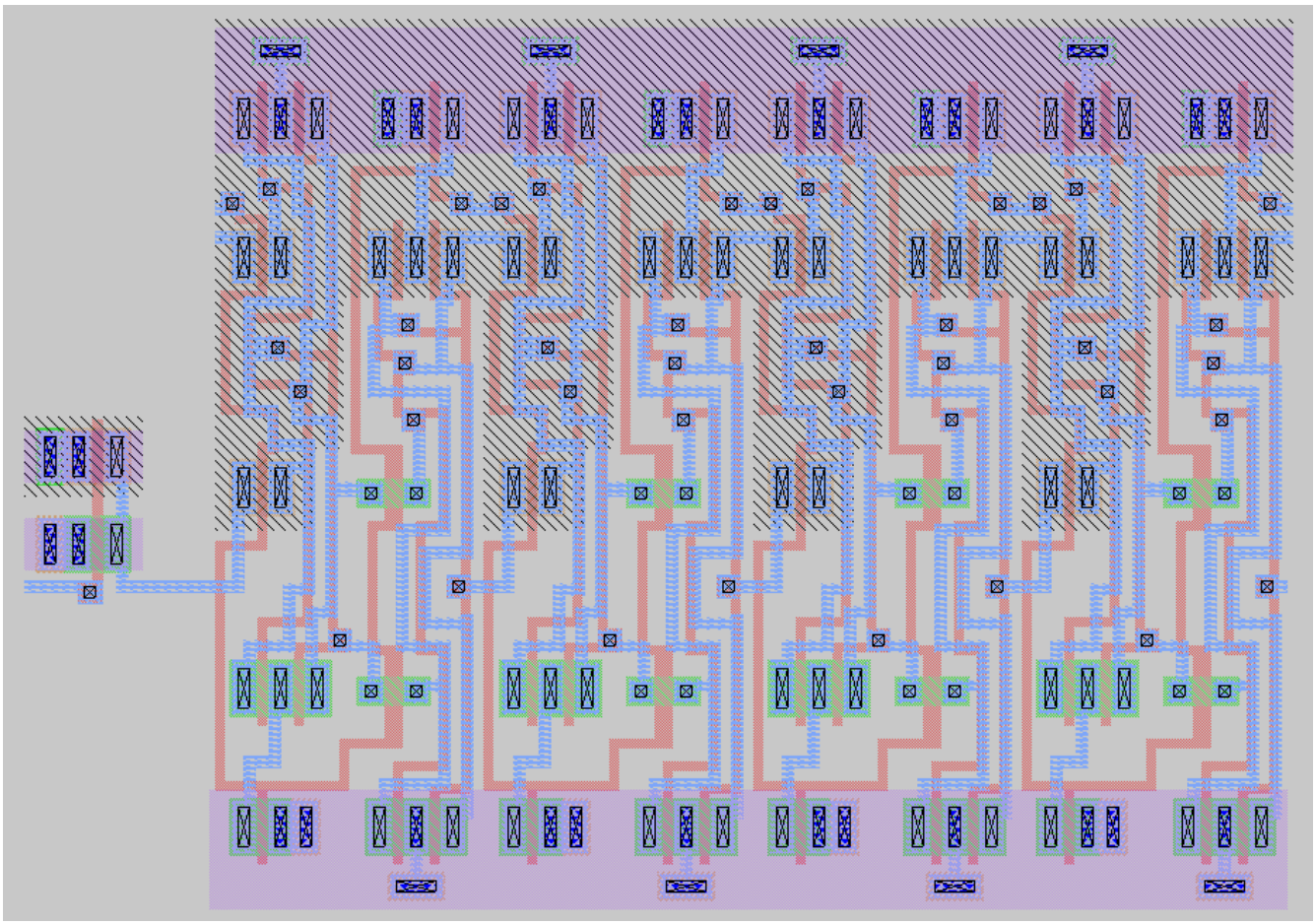

Figure 6: Shift register layout.

I probably could have edited my inverter to make it narrower, but I just ended up using the inverter from Miniproject 1.

I performed LVS on the shift register to ensure that the netlists matched which they did. The output file is in the *Shift_reg/lvs/* folder.

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