Lower power current programmable CMOS

Malay Marut Das
Portland, USA
malaydasat@gmail.com

***Abstract*—This document explains comparators, hysteresis and some comparator circuits.**

Keywords—Comparators

I. Introduction

A comparator is a device that compares two analog inputs and outputs a digital signal indicating which input is larger. So it has two analog input terminals and one binary digital output.

When the difference between two analog input signals approach zero, noise on the inputs will cause spurious switching of digital output. This rapid change in output due to noise can be prevented by hysteresis. Hysteresis is switching the output high or low at different input signal levels. In place of one switching point, hysteresis introduces two: one for rising edge, and one for falling edge of voltage or current. The difference between the higher-level trip value (VH) and the lower-level trip value (VL) equals the hysteresis voltage (HYST).

II. Comparator building blocks

A comparator can be divided into three distinctive pieces – a frontend differential amplifier, amplifier stage and output stage.

A. *Front-End differential amplifier*

A differential amplifier is used to amplify the difference voltage between two input signals. When both inputs change, that's called common mode input change. A differential change is called normal mode or sometimes differential mode. A good differential amplifier has a high Common Mode Rejection Ratio (CMRR), the ratio of response for a normal mode signal to the response for a common mode signal of same amplitude.

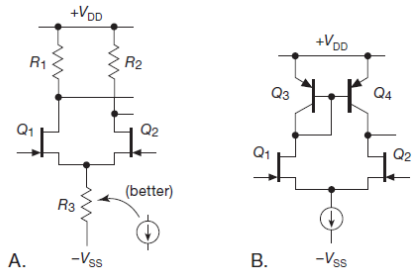

Fig 1: Sample differential amplifiers

The output can be single ended as in Fig 1B or differential output as in Fig 1A.

B. *Amplifier Stage*

The amplifier can be common source amplifier which will use single ended input from previous stage. It can be a multi-stage amplifier.

C. *Output Stage*

The output stage can be a CMOS inverter or a buffer or another circuit that can be used to improve slew rate, improve gain or change the output characteristics of a comparator.

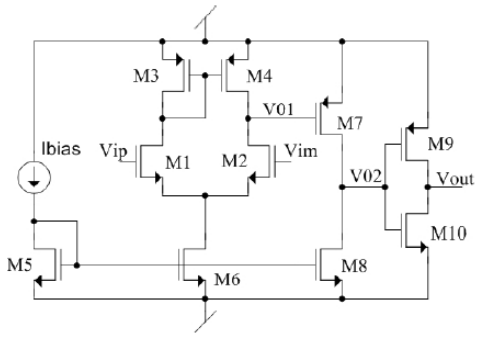

Fig 2: A sample comparator with a differential amplifier, a common-source amplifier and CMOS inverter.

III. Adding hysteresis

Hysteresis can be implemented by a resistive feedback network. In Fig 3 positive feedback increases the +ve differential voltage when output gets high thereby the +ve voltage has to go farther lower to assert output to low.

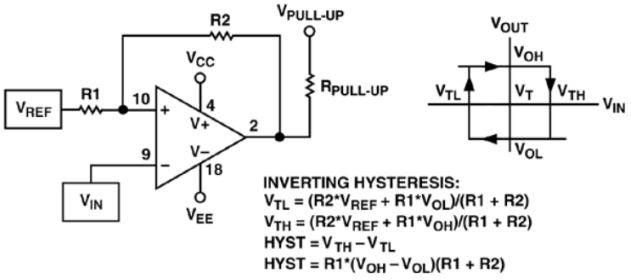

Fig 3: Hysteresis with positive feedback

For comparators having complementary (Q and $\bar{Q}$) outputs, positive feedback, and therefore hysteresis, can be implemented in multiple ways.

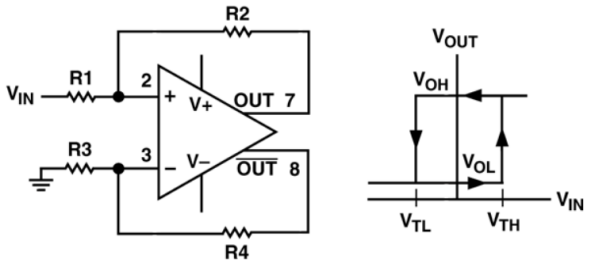

Fig 4: Feedback for comparator with complementary outputs.

The figures show feedback for a discreet comparator but can be implemented in internal circuitry.

IV. Comparator specifications

Propagation Delay - The time difference between the input crossing the reference voltage and the output changing the logic state. Generally, comparators are fast

Input Offset - The difference between the input voltages at the instance where output voltage equals zero volts

Gain – Ideal Comparator has infinite gain and output jumps from low to high at a specific difference in input voltage. Ideal comparators will have a linear transfer curve.

There are multiple other parameters like output swing, Output type, input and output current and impedance but we will focus on above including hysteresis.

V. Comparator circuits

This section shows some of the comparators circuits with programmable hysteresis. Hysteresis is achieved with an internal output feedback and an external current bias.

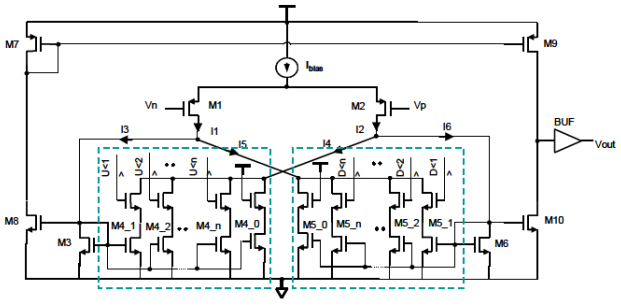

Fig 5: Feedback for comparator with complementary outputs.

They all have different trade-offs as in offset, propagation delay, bandwidth.

I understand the comparators in fig 5 and 6 to an extent. These comparators in their respective papers needs to be analyzed further before I select a circuit for implementation.

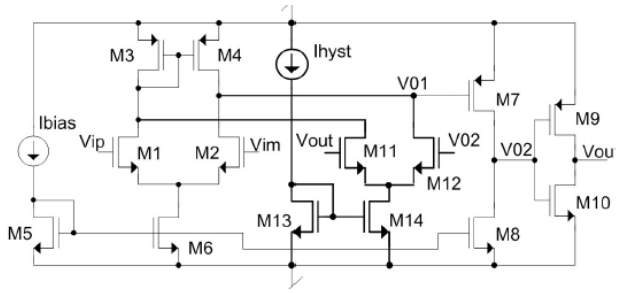

Fig 5: Programmable hysteresis with unbalanced differential pair.

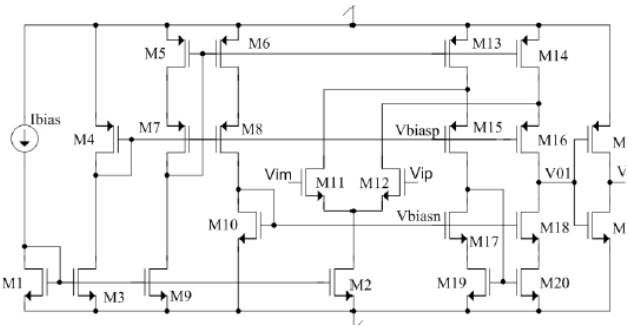

Fig 6: Programmable hysteresis with resistor and current

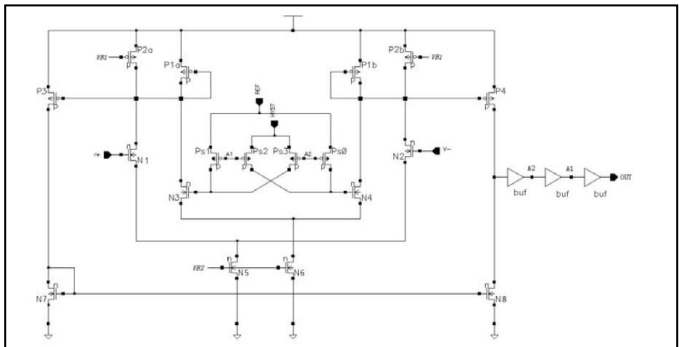

Fig 7: Programmable hysteresis from [6].

References

[1] P. Horowitz,and W. Hill, "The Art of Electronics," Cambridge Press University, 3rd ed *(references)*

[2] P. Furth, Y. Tsen, V. Kulkarni,and T. Raju, On the Design of Low-Power CMOS Comparators with Programmable Hysteresis., IEEE, 2010, pp.1077–1080.

[3] https://www.analog.com/en/analog-dialogue/articles/curing-comparator-instability-with-hysteresis.html#.

[4] https://en.wikipedia.org/

[5] X.Xian, T.Teo, "A Low-power Comparator with Programmable Hysteresis Level for Blood Pressure Peak Detection," IEEE, 2009.

[6] J. Tao, Y. Wang, J. Xing, "A comparator with flexible programming of the hysteresis," IEEE, 2010, pp. 105–107