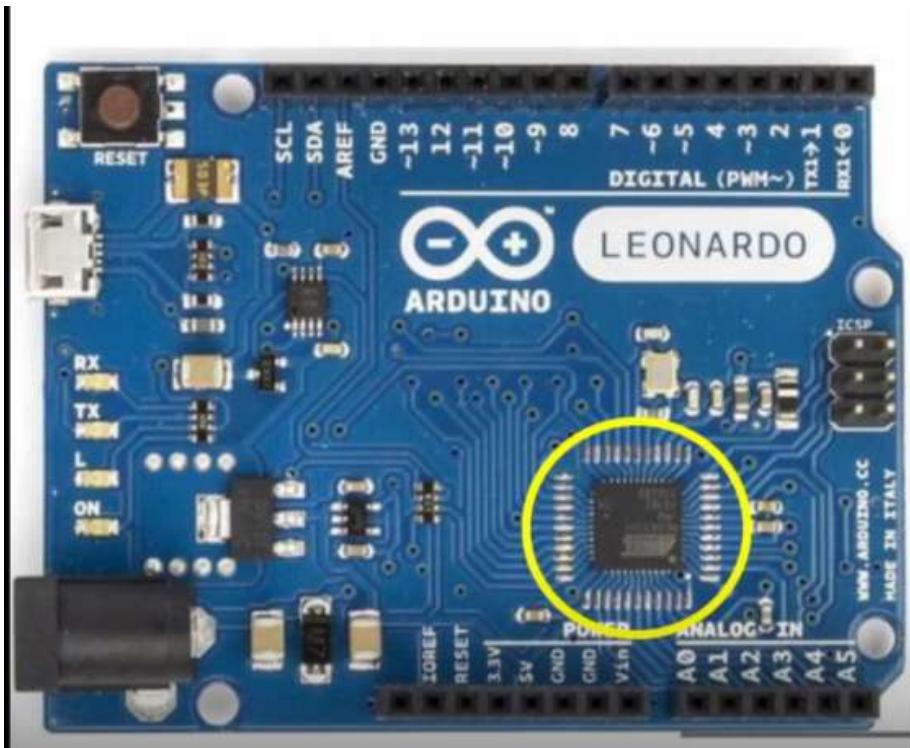


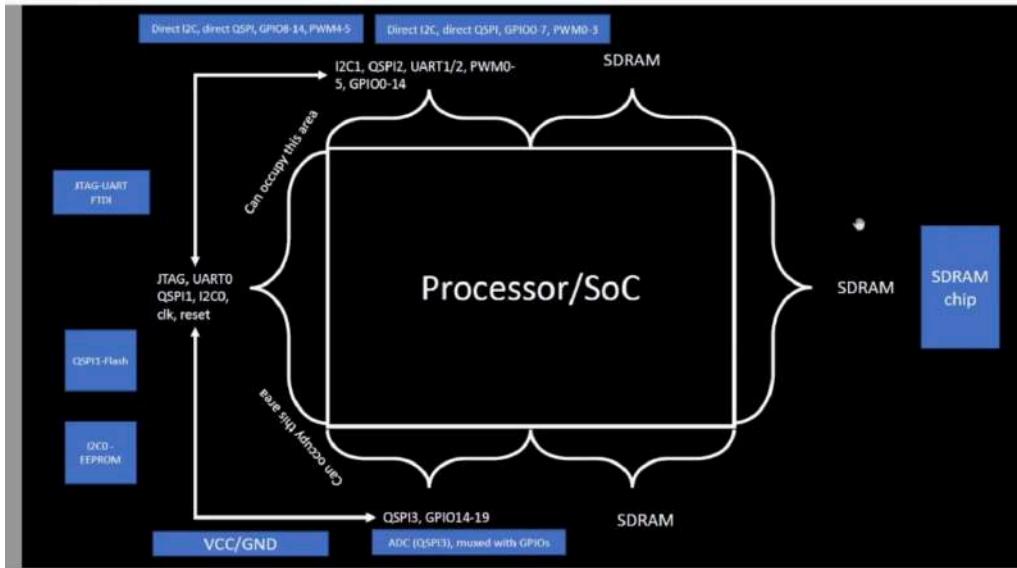
Summary of Asic design using openlane

Introduction to QFN - 48 package, chip, pads, core, die and IPs

A commonly and extensively used arduino circuit board can be seen in the below picture. The board has a processer or SoC i.e. System on a Chip. This is a central part of the chip and is encircled as can be seen below:



The encircled region, however is only a high level view, which can be represented through a block diagram, as shown below:



In the picture, we are able to see a large box which represents, as written a SoC. In layman's terms, this often called a "CHIP". However, in technicality it is termed as a "PACKAGE". One kind of package, which is used in the arduino board is a QFN - 48 package (Quad Flat No-Leads). A package can be schematically represented as below:

{IMAGE CREDITS - VSDIAT ; shared as part of lecture and subsequently hand drawn by author}

As seen, a chip is actually inside a package, and is connected to various "PINS" or inputs/outputs. The locations of the pins and what they are are usually driven by the design of the PCB. A chip is also a very complex system, and has various components such as :-

- **PADS** : They act as connectors between the integrated circuit and chip. Pads, simply are structures for sending electrical signals inside the chip. They are strategically placed and made with respect to the pins
- **CORE** : This is the digital logic (i.e. the various gates such as AND, OR, XOR etc and the MUXes) is placed. It carries out all processor functions.
- **DIE** : A die is a part of semiconductor wafer that can be used independently in various devices. It can contain more than one core.

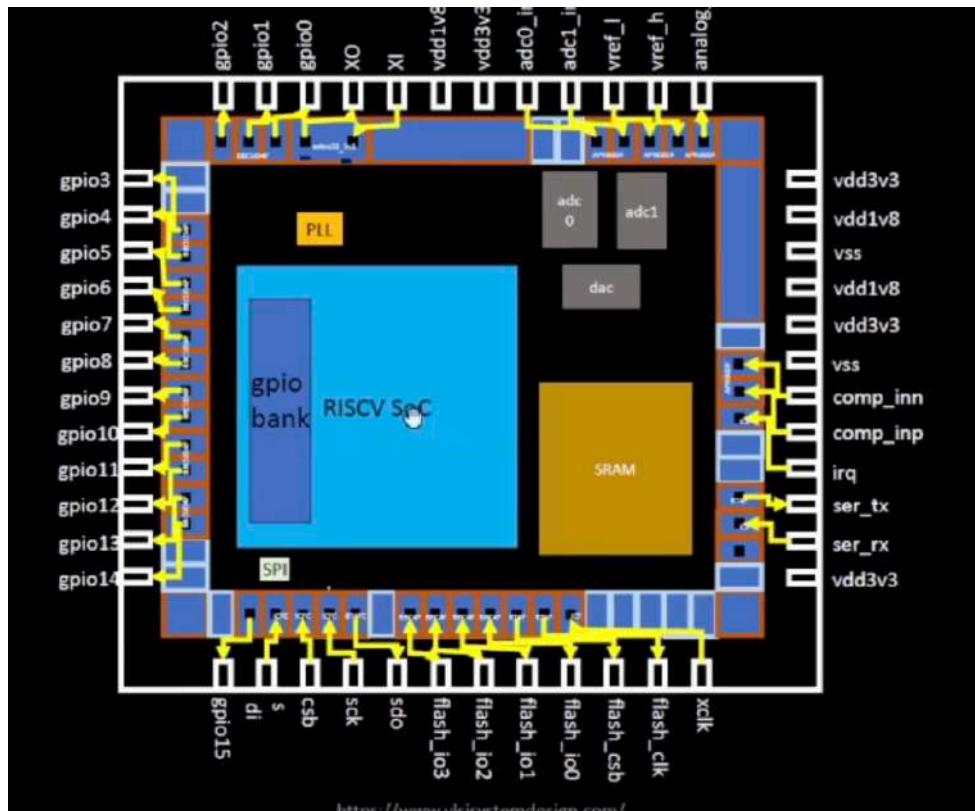
The core also has various components, which can mainly be segregated into :-

- **FOUNDRY IPs** : These are components that are provided to the designer of the SoC by the foundry (i.e. a factory where chips are produced). These components are usually pre-

designed and tested by the foundry. Foundry IPs can include PLLs, adco, adc1, SRAMs and various other components.

- **MACROs :** Macros are very similar to Foundry IPs, but consist of pure digital logic, that is pre-made for certain common use-cases and can be easily integrated into a SoC or Integrated Circuit (IC). Macros can be of various types such as a GPIO bank and SPI etc.

The schematic encompassing all of the above components can be seen below:



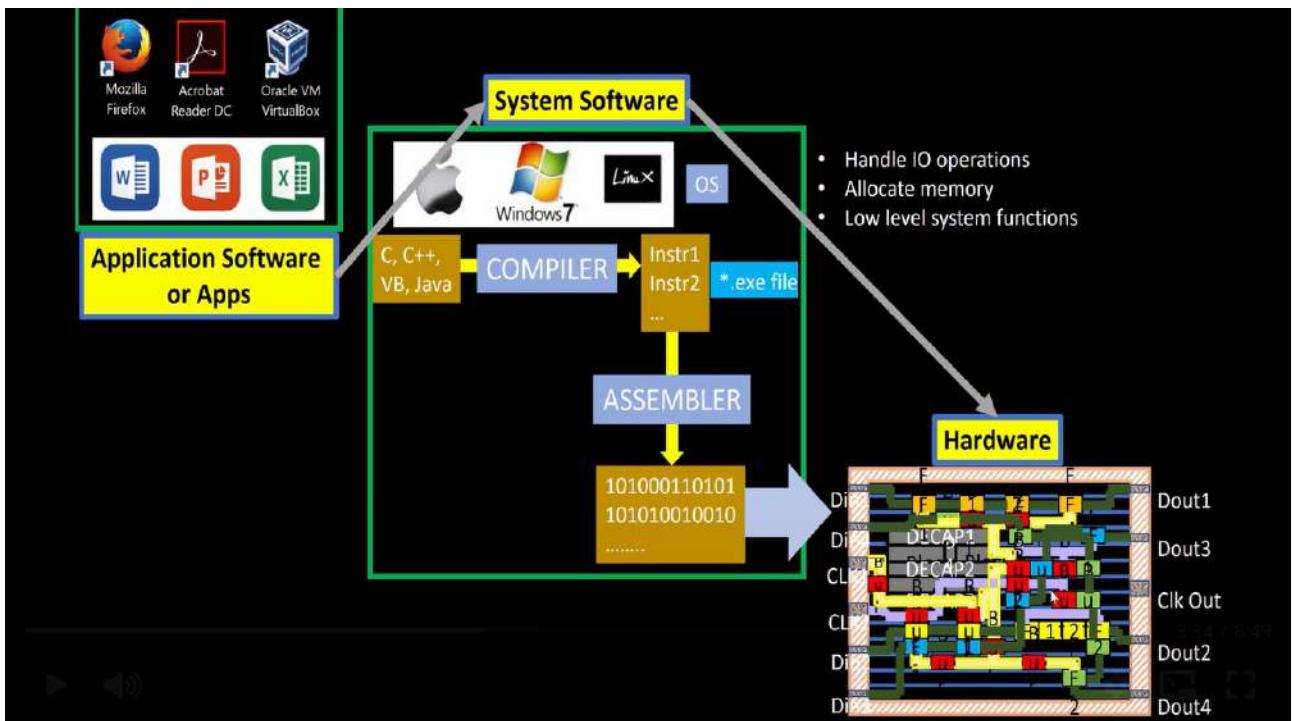
Introduction to RISC V

RISC-V Instruction Set Architecture, commonly called RISC V ISA, is the language of the computer. When a C program is to be run on a piece of hardware, it is first compiled in an assembly language program like RISC V. It is then converted to machine language i.e. binary and subsequently implemented in the form of a hardware description language such as picorv32 cpu core. A schematic is shown below, representing the same:

From Software Applications to Hardware

Application Software, or apps. They run on hardware such as laptops, mobile phones, tablets etc that are powered by chips. However, apps are coded in complex application programs that require conversion into binary or machine language for running. This is done through system software, which majorly consists of

- Operating systems - Operating Systems (OSs) perform a variety of functions such as I.O. operation, memory allocation and low level system function. They produce functions in languages such as C, C++, VB and Java, which are sent to the compiler.
 - Compilers - Compilers produce simple instructions (the format of which depends on the hardware) in the form of .exe documents, which are sent to the assemblers. These instructions are abstract interfaces between complex coding languages like C/C++ and hardware, and hence are called ISAs. They are known as the architecture of the computer.
 - Assemblers - Assemblers convert the instructions from the compilers into binary, and the function is implemented.



SoC Design and OpenLANE

Introduction to Components of Opensource Digital ASIC Design

ASIC requires mainly three components for design

- RTL IPs - they are building blocks written in a hardware description language. These blocks describe the functioning of the circuit at a basic level and are pre designed and verified.
- EDA Tools - EDA, which expands to Electronic Design Automation tools are used for design, simulation and verification and the analyzing of circuit designs. Common tools are OpenSTA, OpenRoad etc.
- PDK data - Process Design Kit data is a collection of files used to model the fabrication process for EDA tools. It is usually provided by a foundry and include Process Design Rules, Device Models, Digital Standard Cell Libraries and IO libraries.

However, until June of 2020, there was no OPEN SOURCE available PDK data, making it impossible to do ASIC design on opensource platforms. Nonetheless, this changed when Google and Skywater released PDK data on 130 nm chips. There is a unfortunate common misconception that 130 nm is not up to the industrial mark, with chips reaching Armstrong sizes in today's date. This is debunked due to the following two reasons :-

- several applications do not require such advanced nodes, and 130nm chips provide a good amount of power for those cases
 - fabrication costs are also much lesser for 130nm chips
- 130 nm chips are also not slow, as verified by intel and OSU:-

{IMAGE CREDITS - VSDIAT ; shared as part of lecture}

Is 130nm Fast?

- Yes!
 - Intel: P4EE @ 3.46 GHz (Q4'04)



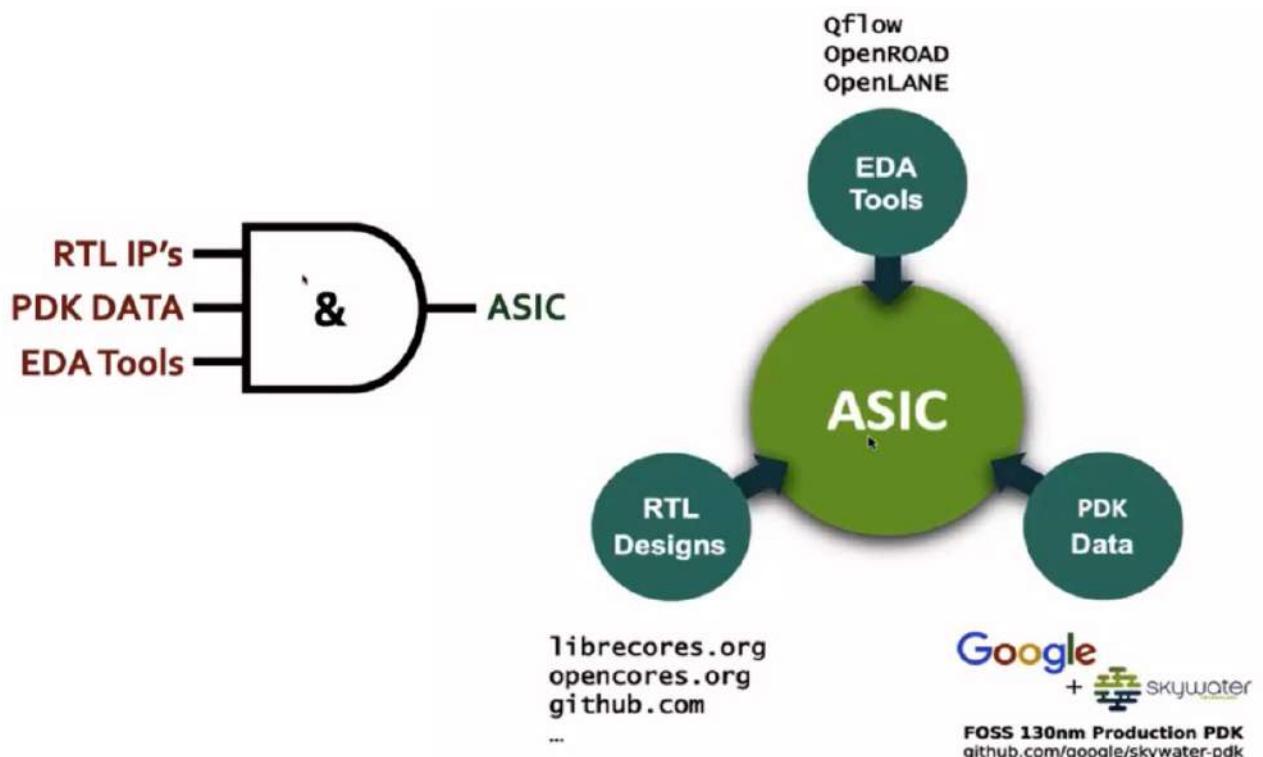
- OSU team reported 327 MHz post-layout clock frequency for a single cycle RV32i CPU
 - A pipelined version can achieve > 1 GHz clock!



Single-cycle RV32i design

Standard cell library	Synthesis			Place-and-route		
	Frequency [MHz]	Area [um^2]	PDP [pJ]	Frequency [MHz]	Area [um^2]	PDP [pJ]
sky130_osu_18T_hs	398	155,774	33.8	327	197,744	239.1

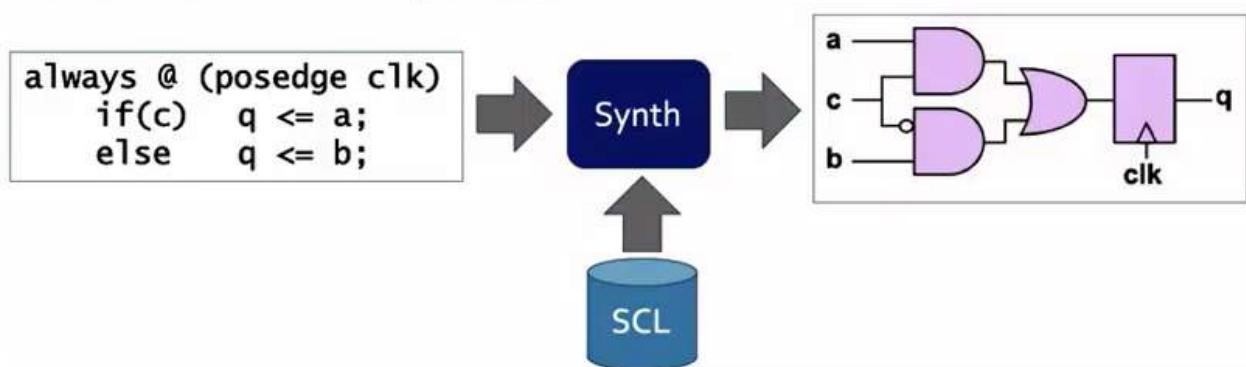
{IMAGE CREDITS - VSDIAT ; shared as part of lecture}



Simplified RTL to GDS flow

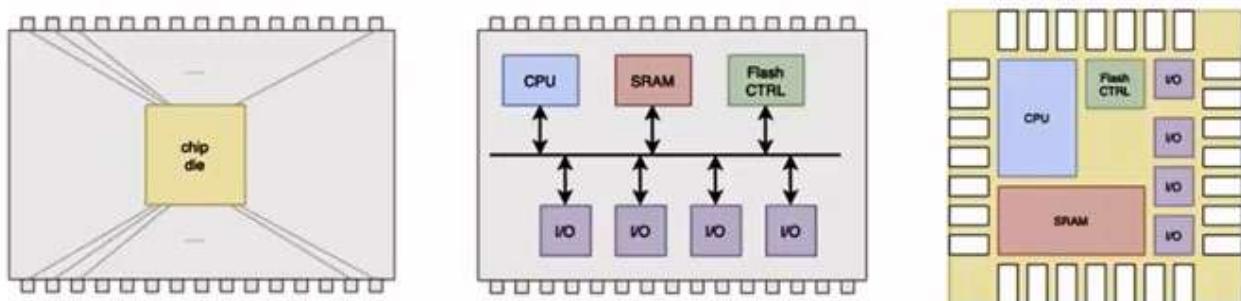
The RTL to GDSII (Register Transfer Level to Graphic Design System II) design process takes many steps, that are :-

- Synthesis - it converts hardware description languages such as VERILOG into gate-level representations part of a standard cell library. The cells part of this library have a regular layout. Each of these have different views/models such as Electrical, HDL, Spice etc.
- {IMAGE CREDITS - VSDIAT ; shared as part of lecture}
- Converts RTL to a circuit out of components from the standard cell library (SCL)



- Floor Planning involves optimizing chip performance, area utilization, and connectivity through spatial arrangements (i.e. the layout and placement of various components). The three main purposes of floor planning are firstly, minimizing wire lengths, secondly, reducing signal delays, thirdly, optimizing power distribution, and fourthly, ensuring efficient chip utilization. Power Planning aims to ensure stable and reliable power delivery to all components by effective distribution and design of power supplies and power distribution networks (PDN). The main purposes of this are minimizing voltage drop and noise, reducing power distribution network (PDN) resistances and capacitances, and ensuring uniform power distribution throughout. Usually the chip is powered through VDD pads which are connected to various components through parallel rectangular strips causing lesser resistance.

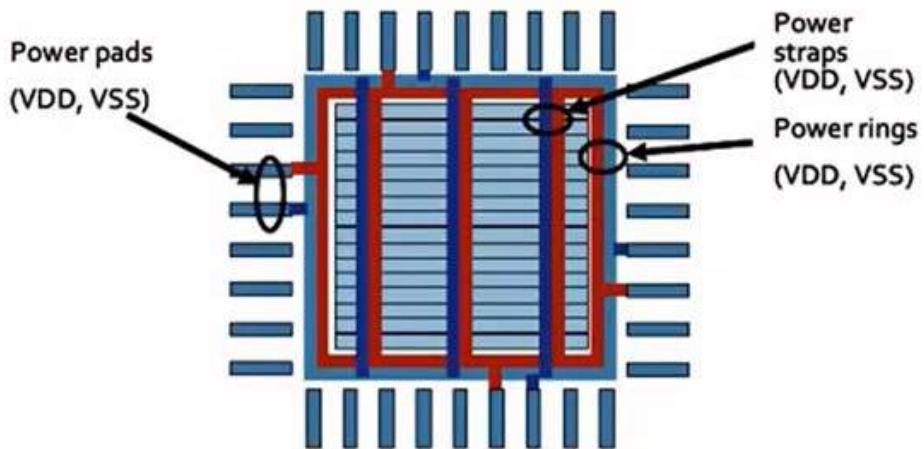
- Chip Floor-Planning: Partition the chip die between different system building blocks and place the I/O Pads



- Macro Floor-Planning: Dimensions, pin locations, rows definition



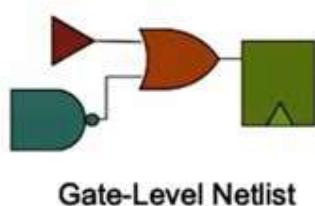
- Power Planning



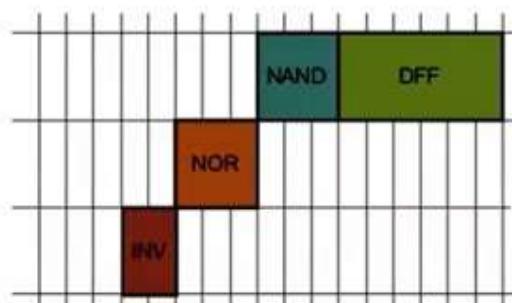
- Placement - it is the process of determining where a component will be placed on the chip. The components can include standard cells, macros, and I/O pads. The cells are usually placed on floorplan rows, and are aligned with the sites. There are majorly two steps - global and detailed.

{IMAGE CREDITS - VSIDIAT ; shared as part of lecture}

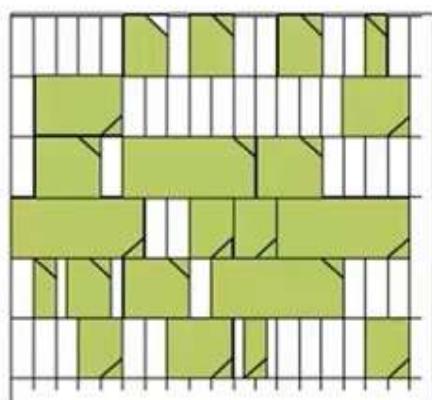
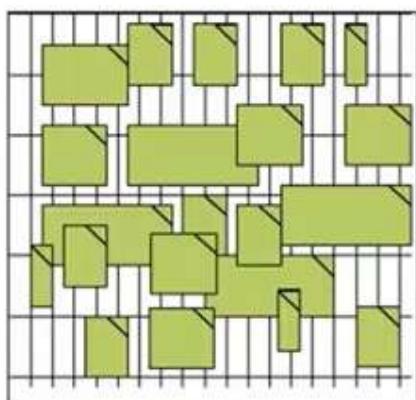
- Place the cells on the floorplan rows, aligned with the sites



Gate-Level Netlist



- Usually done in 2 steps: Global and Detailed

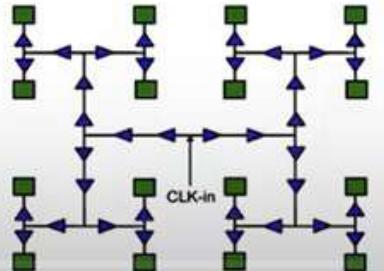


- Clock Tree Synthesis - This step is done before routing, because the clock needs to be routed by delivering the clock to all sequential elements.

{IMAGE CREDITS - VSDIAT ; shared as part of lecture}

• Create a clock distribution network

- To deliver the clock to all sequential elements (e.g., FF)
- With minimum skew (zero is hard to achieve)
- And in a good shape
- Usually a Tree (H, X, ...)



- Routing - The determination of the interconnections of the components through the various metal layers, whose thickness, pitch etc is detailed by the PDK. The SKY130 has 6 layers.
- Sign Off - this majorly has verification through three processes:
 - Design Rule Check (DRC) - this makes sure the design complies with manufacturing guidelines and is compatible for fabrication. It aims to detect and correct layout errors so that fabrication defects do not occur.
 - Layout vs. Schematic (LVS) - here the layout is contrasted against the schematic to ensure consistency. LVS tools extract netlists and compare them for differences, after which the design proceeds to physical design flow
 - Static Timing Analysis (STA) - it evaluates timing behaviour of a digital circuit to ensure design meets setup and hold time constraints, maximum clock frequency, and other timing requirements

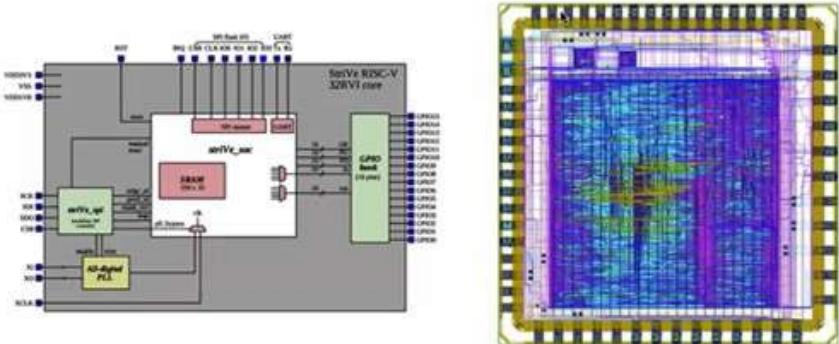
Introduction to OpenLANE and Strive Chipsets

OpenLANE is an open-source digital ASIC jointly developed by Efabless and Google, designed to automate the entire design process flow based on several components including OpenROAD, SPEF-Extractor, KLayout and a number of custom scripts for design exploration and optimization. It aims to create a clean GDSII (i.e. no LVS violations, no DRC violations, and no timing violations) with no human intervention. Strive is a family of SoCs created by Efabless.

{IMAGE CREDITS:VSDIAT ; shared as part of lecture}



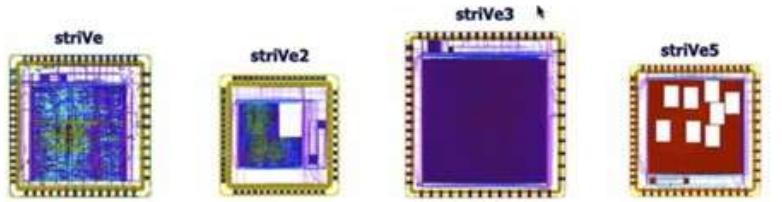
- Started as an Open-Source Flow for a True Open Source Tape-out Experiment
- striVe is a family of **open everything** SoCs
 - Open PDK, Open EDA, Open RTL



{IMAGE CREDITS - VSDIAT ; shared as part of lecture}

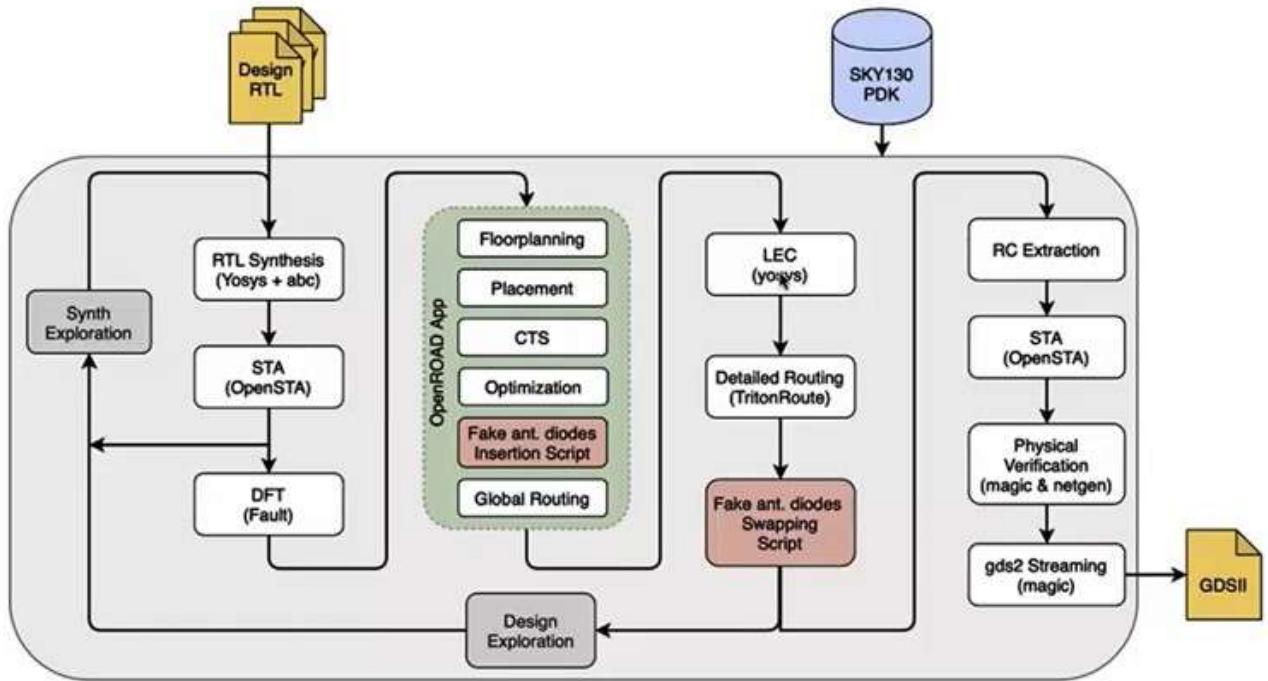


SoC	Features
striVe	Sky130 SCL + Synthesized 1 Kbytes SRAM
striVe 2	Sky130 SCL + 1 Kbytes OpenRAM block
striVe 2a	striVe 2 with a single chip core module
striVe 3	OSU SCL + Synthesized 1 Kbytes SRAM
striVe 5	Sky130 SCL + 8 x 1 Kbytes OpenRAM banks
striVe 6	striVe 2 with DFT



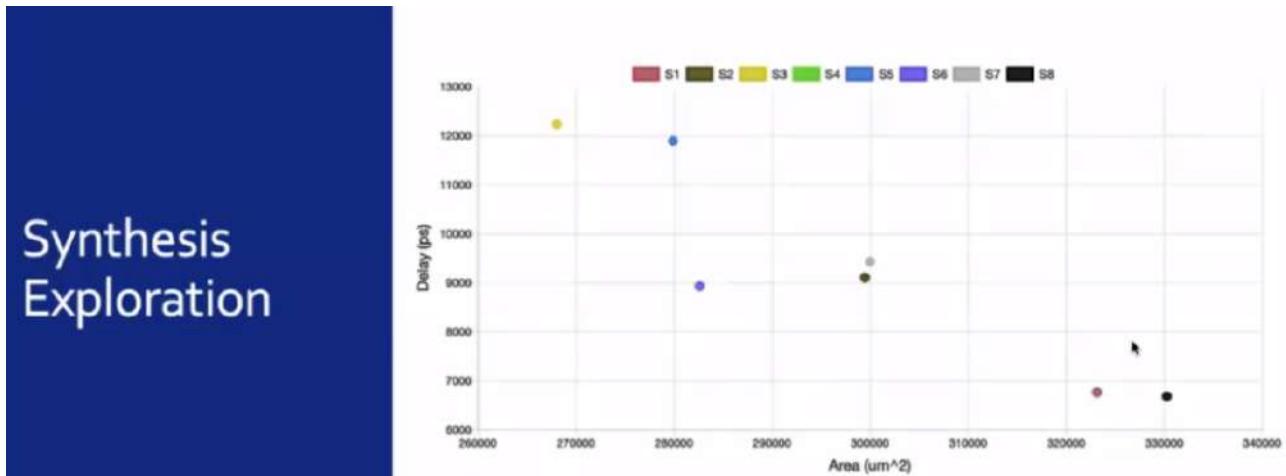
Introduction to OpenLANE detailed ASIC Design Flow

{IMAGE CREDITS - VSDIAT ; shared as part of lecture}



- Synthesis Exploration - it generates a delay vs area report

{IMAGE CREDITS - VSDIAT ; shared as part of lecture}



- Design Exploration - sweeps design configuration and subsequently find best configuration for any given design. It produces a report as shown:

{IMAGE CREDITS - VSDIAT ; shared as part of lecture}



Design	Runtime	Cell Count	TR Vios	FP_CORE_UTIL	ROUTING_STRATEGY	GLB_RT_ADJUSTMENT
aes	1h29m8s	22932	1	40	1	0.05
aes	1h34m31s	22932	2	30	1	0.05
aes	1h41m14s	22932	9	40	1	0.05
aes	1h47m14s	22932	1	45	1	0.05
aes	1h44m14s	22932	1	40	1	0.05
aes	1h47m59s	22932	1	45	1	0.05
aes	1h49m7s	22932	1	45	1	0.05
aes	1h43m54s	22932	2	30	1	0.05
aes	1h42m58s	22932	8	30	1	0.05
cordic	0h10m51s	8275	0	45	0	0.15
cordic	0h10m35s	8275	0	45	0	0.15
cordic	0h9m55s	8275	2	40	0	0.15
cordic	0h11m25s	8275	0	45	0	0.15
cordic	0h10m3s	8275	0	30	0	0.15
cordic	0h11m6s	8275	4	40	0	0.15
cordic	0h11m3s	8275	4	40	0	0.15
cordic	0h10m25s	8275	0	30	0	0.15
cordic	0h10m26s	8275	3	30	0	0.15

- OpenLane Regression Testing

{IMAGE CREDITS - VSDIAT ; shared as part of lecture}



- The design exploration utility is also used for regression testing (CI)
- We run OpenLane on ~70 designs and compare the results to the best known ones

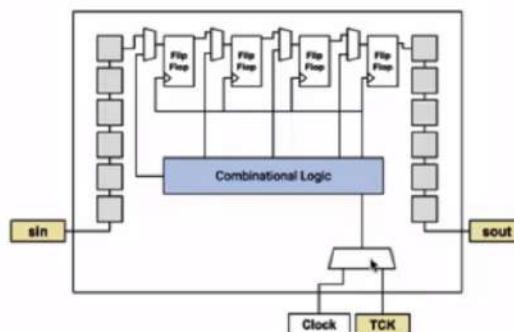
Design	Runtime	Cell Count	TR Vios
jpeg_encoder	3h16m7s	73624	0
strive_soc	3h14m0s	73271	0
aes256	1h35m51s	64435	0
genericfir	1h2m36s	48849	0
aes128	1h7m50s	44658	0
TEA	2h11m8s	44026	0
rc6_core	1h43m44s	35304	0
double_sqrt	1h14m18s	29252	0
lir5afix	1h14m5s	24950	0
y_huff	0h54m48s	16826	0
sha3	0h21m18s	16372	0
ocs_bitter	0h17m48s	10997	0
sub86	0h12m35s	7855	0
CPU	0h11m7s	7342	0
cordic	0h10m13s	7210	0

- Design for Test (also k/a DFT)

{IMAGE CREDITS - VSDIAT ; shared as part of lecture}

Design for Test (DFT)

- Scan Insertion
- Automatic Test Pattern Generation (ATPG)
- Test Patterns Compaction
- Fault Coverage
- Fault Simulation



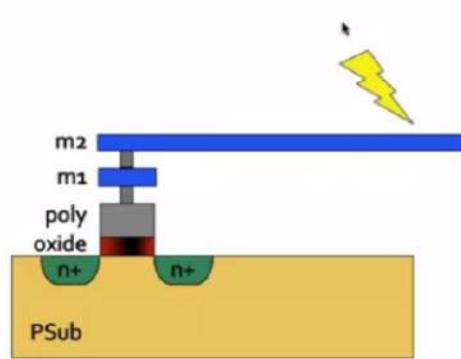
Fault

- Physical verification (DRC & LVS) - Magic is used for DRC and Magic and Netgen for LVS.
- Logic Equivalence Check (LEC) - checks that the physical implementation and the netlist have the same logic. It is performed each time netlist is modified and checks that changing netlist did not change function.
- Dealing with Antenna Rules violations

{IMAGE CREDITS - VSDIAT ; shared as part of lecture}

Dealing with Antenna Rules Violations

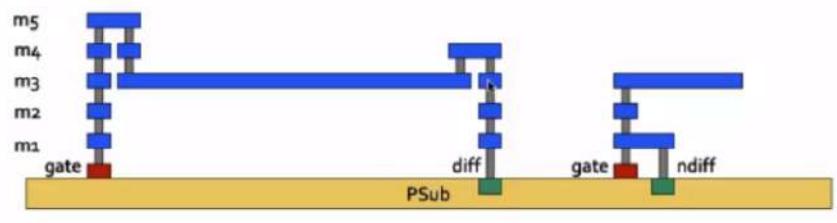
- When a metal wire segment is fabricated, it can act as an antenna.
 - Reactive ion etching causes charge to accumulate on the wire.
 - Transistor gates can be damaged during fabrication



{IMAGE CREDITS - VSDIAT ; shared as part of lecture}

Dealing with Antenna Rules Violations

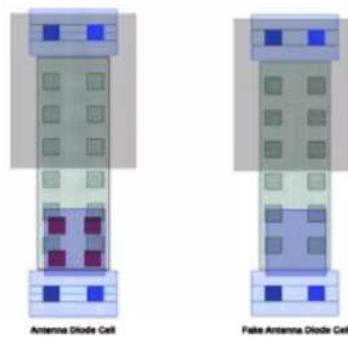
- Two solutions:
 - Bridging attaches a higher layer intermediary
 - Requires Router awareness (not there yet!)
 - Add antenna diode cell to leak away charges
 - Antenna diodes are provided by the SCL



{IMAGE CREDITS - VSDIAT ; shared as part of lecture}

Dealing with Antenna Rules Violations

- We took a preventive approach
 - Add a Fake Antenna Diode next to every cell input after placement
 - Run the Antenna Checker (Magic) on the routed layout
 - If the checker reports a violation on the cell input pin, replace the Fake Diode cell by a real one



- Timing Analysis (STA) - Here, the input also contains a synthesized netlist along with other data.

Theory

Expand or Collapse

Implementation

Section 1 tasks:-

1. Run 'picorv32a' design synthesis using OpenLANE flow and generate necessary outputs.
2. Calculate the flop ratio.

1. Run 'picorv32a' design synthesis using OpenLANE flow and generate necessary outputs.

Commands to invoke the OpenLANE flow and perform synthesis

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:vo.21'
```

```
# Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command
```

```
docker
```

```
# Now that we have entered the OpenLANE flow contained docker sub-system we can invoke the OpenLANE flow in the interactive mode using the following command
```

```
./flow.tcl -interactive
```

```
# Now that OpenLANE flow is open we have to input the required packages for proper functionality of the OpenLANE flow
```

```
package require openlane 0.9
```

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the design creating some necessary files and directories for running a specific design which in our case is 'picorv32a'
```

```
prep -design picorv32a
```

```
# Now that the design is prepped and ready, we can run synthesis using following command
```

```
run_synthesis
```

```
# Exit from OpenLANE flow
```

```
exit
```

```
# Exit from OpenLANE flow docker sub-system
```

```
exit
```

Screenshots of running each commands

Activities Terminal Fri 9:23 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
vsduser@vsdsquadron:~$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ docker
bash-4.2$ ./flow.tcl -interactive
[INFO]:
[INFO]: Version: v0.21
[INFO]: Running interactively
% package require openlane 0.9
0.9
% prep -design picorv32a
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/15-03_15-51
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane
```

Activities Terminal Fri 9:24 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/15-03_15-51
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.tlef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1l met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
[INFO]: % run_synthesis[]
```

```
Activities Terminal Fri 9:29 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -759.46
wns -24.89
[INFO]: Synthesis was successful
::: %
```

2. Calculate the flop ratio.

Screenshots of synthesis statistics report file with required values highlighted

Activities M GVim Fri 10:02 PM

File Edit Tools Syntax Buffers Window Help

1-yosys_4.stat.rpt (~/Desktop/work/tools/...uns/15-03_15-51/reports/synthesis) - GVIM

```
1
2 28. Printing statistics.
3
4 === picorv32a ===
5
6 Number of wires: 14596
7 Number of wire bits: 14978
8 Number of public wires: 1565
9 Number of public wire bits: 1947
10 Number of memories: 0
11 Number of memory bits: 0
12 Number of processes: 0
13 Number of cells: 14876
14 sky130_fd_sc_hd_a2111o_2 1
15 sky130_fd_sc_hd_a211o_2 35
16 sky130_fd_sc_hd_a211oi_2 60
17 sky130_fd_sc_hd_a21bo_2 149
18 sky130_fd_sc_hd_a21boi_2 8
19 sky130_fd_sc_hd_a21o_2 57
20 sky130_fd_sc_hd_a21oi_2 244
21 sky130_fd_sc_hd_a221o_2 86
22 sky130_fd_sc_hd_a22o_2 1013
23 sky130_fd_sc_hd_a2bb2o_2 1748
24 sky130_fd_sc_hd_a2bb2oi_2 81
25 sky130_fd_sc_hd_a311o_2 2
```

hlsearch 25, 38 Top

Activities M GVim Fri 10:03 PM

File Edit Tools Syntax Buffers Window Help

1-yosys_4.stat.rpt (~/Desktop/work/tools/...uns/15-03_15-51/reports/synthesis) - GVIM

```
25 sky130_fd_sc_hd_a311o_2 2
26 sky130_fd_sc_hd_a31o_2 49
27 sky130_fd_sc_hd_a31oi_2 7
28 sky130_fd_sc_hd_a32o_2 46
29 sky130_fd_sc_hd_a41o_2 1
30 sky130_fd_sc_hd_and2_2 157
31 sky130_fd_sc_hd_and3_2 58
32 sky130_fd_sc_hd_and4_2 345
33 sky130_fd_sc_hd_and4b_2 1
34 sky130_fd_sc_hd_buf_1 1656
35 sky130_fd_sc_hd_buf_2 8
36 sky130_fd_sc_hd_conb_1 42
37 sky130_fd_sc_hd_dfxtp_2 1613
38 sky130_fd_sc_hd_inv_2 1615
39 sky130_fd_sc_hd_mux2_1 1224
40 sky130_fd_sc_hd_mux2_2 2
41 sky130_fd_sc_hd_mux4_1 221
42 sky130_fd_sc_hd_nand2_2 78
43 sky130_fd_sc_hd_nor2_2 524
44 sky130_fd_sc_hd_nor2b_2 1
45 sky130_fd_sc_hd_nor3_2 42
46 sky130_fd_sc_hd_nor4_2 1
47 sky130_fd_sc_hd_o2111a_2 2
48 sky130_fd_sc_hd_o211a_2 69
49 sky130_fd_sc_hd_o211ai_2 6
```

search hit BOTTOM, continuing at TOP 49, 38 48%

Calculation of Flop Ratio and DFF % from synthesis statistics report file

Theory

Implementation

Section 2 tasks:-

1. Run 'picorv32a' design floorplan using OpenLANE flow and generate necessary outputs.
 2. Calculate the die area in microns from the values in floorplan def.
 3. Load generated floorplan def in magic tool and explore the floorplan.
 4. Run 'picorv32a' design congestion aware placement using OpenLANE flow and generate necessary outputs.
 5. Load generated placement def in magic tool and explore the placement.
- All section 2 logs, reports and results can be found in following run folder:
1. Run 'picorv32a' design floorplan using OpenLANE flow and generate necessary outputs.

Commands to invoke the OpenLANE flow and perform floorplan

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:vo.21'
```

```
# Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command
```

```
docker
```

```
# Now that we have entered the OpenLANE flow contained docker sub-system we can  
invoke the OpenLANE flow in the Interactive mode using the following command
```

```
./flow.tcl -interactive
```

```
# Now that OpenLANE flow is open we have to input the required packages for proper  
functionality of the OpenLANE flow
```

```
package require openlane 0.9
```

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the  
design creating some necessary files and directories for running a specific design which in  
our case is 'picorv32a'
```

```
prep -design picorv32a
```

```
# Now that the design is prepped and ready, we can run synthesis using following  
command
```

```
run_synthesis
```

```
# Now we can run floorplan
```

```
run_floorplan
```

Screenshot of floorplan run

```
Activities Terminal - Sun 6:06 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: Synthesis was successful
% run_floorplan
[INFO]: Running Floorplanning...
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 3
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/l
ib/sky130_fd_sc_hd_tt_025C_lv80.lib line 31, default_operating_condition tt_025C_lv80 not found.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/merged_unpadded.le
f
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 440 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/merged_unpadded.le
f
[INFO IFP-0001] Added 238 rows of 1412 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 660.685 671.405 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/reports/floorplan/3-verilog2def.die_area.rpt.
[INFO] Floorplanned on a core area of 5.52 10.88 655.04 658.24 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/reports/floorplan/3-verilog2def.core_area.rpt.
[INFO]: Core area width: 649.52
[INFO]: Core area height: 647.36
[INFO]: Changing layout from 0 to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/floorplan/3-verilog2def_openroad.def
[INFO]: Running IO Placement...
[INFO]: success! step index: 3
```

```
Activities Terminal - Sun 6:06 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
er stripe. Moving to closest stripe at (567.000um, 103.880um).
[WARNING PSM-0030] Vsrc location at (565.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 257.060um).
[WARNING PSM-0030] Vsrc location at (5.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (145.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
[WARNING PSM-0030] Vsrc location at (425.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 563.420um).
[INFO PSM-0031] Number of nodes on net VGND = 19223.
[INFO PSM-0037] G matrix created sucessfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/floorplan/picorv32a.floorplan.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/floorplan/7-pdn.def
1
% [ ]
```

2. Calculate the die area in microns from the values in floorplan def.

Screenshot of contents of floorplan def

```

1 VERSION 5.8 ;
2 DIVIDERCHAR "/";
3 BUSBITCHARS "[]";
4 DESIGN picorv32a ;
5 UNITS DISTANCE MICRONS 1000 ;
6 DIEAREA ( 0 0 ) ( 660685 671405 ) ;
7 ROW ROW_0 unithd 5520 10880 FS DO 1412 BY 1 STEP 460 0 ;
8 ROW ROW_1 unithd 5520 13600 N DO 1412 BY 1 STEP 460 0 ;
9 ROW ROW_2 unithd 5520 16320 FS DO 1412 BY 1 STEP 460 0 ;
10 ROW ROW_3 unithd 5520 19040 N DO 1412 BY 1 STEP 460 0 ;
11 ROW ROW_4 unithd 5520 21760 FS DO 1412 BY 1 STEP 460 0 ;
12 ROW ROW_5 unithd 5520 24480 N DO 1412 BY 1 STEP 460 0 ;
13 ROW ROW_6 unithd 5520 27200 FS DO 1412 BY 1 STEP 460 0 ;
14 ROW ROW_7 unithd 5520 29920 N DO 1412 BY 1 STEP 460 0 ;
15 ROW ROW_8 unithd 5520 32640 FS DO 1412 BY 1 STEP 460 0 ;
16 ROW ROW_9 unithd 5520 35360 N DO 1412 BY 1 STEP 460 0 ;
17 ROW ROW_10 unithd 5520 38080 FS DO 1412 BY 1 STEP 460 0 ;
18 ROW ROW_11 unithd 5520 40800 N DO 1412 BY 1 STEP 460 0 ;
19 ROW ROW_12 unithd 5520 43520 FS DO 1412 BY 1 STEP 460 0 ;
20 ROW ROW_13 unithd 5520 46240 N DO 1412 BY 1 STEP 460 0 ;
21 ROW ROW_14 unithd 5520 48960 FS DO 1412 BY 1 STEP 460 0 ;
22 ROW ROW_15 unithd 5520 51680 N DO 1412 BY 1 STEP 460 0 ;
23 ROW ROW_16 unithd 5520 54400 FS DO 1412 BY 1 STEP 460 0 ;
24 ROW ROW_17 unithd 5520 57120 N DO 1412 BY 1 STEP 460 0 ;
25 ROW ROW_18 unithd 5520 59840 FS DO 1412 BY 1 STEP 460 0 ;

```

According to floorplan def

3. Load generated floorplan def in magic tool and explore the floorplan.

Commands to load floorplan def in magic in another terminal

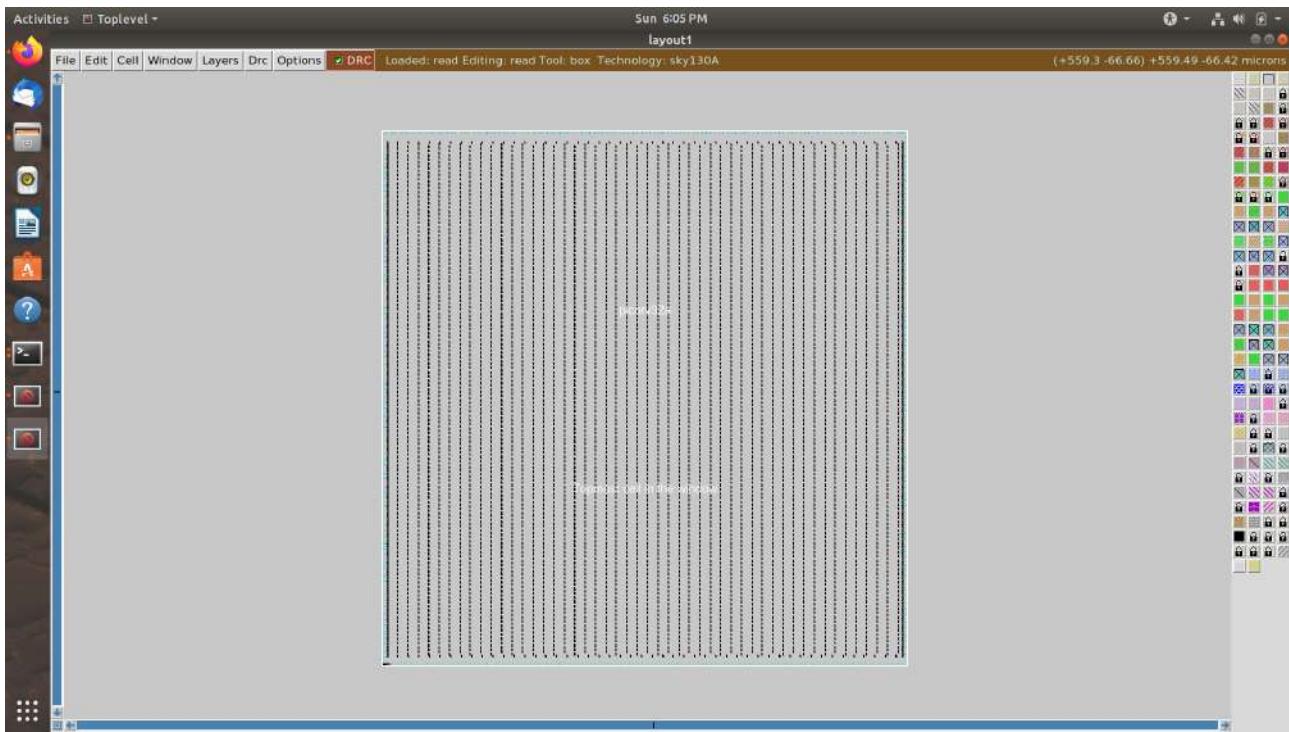
```
# Change directory to path containing generated floorplan def
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
17-03_12-06/results/floorplan/
```

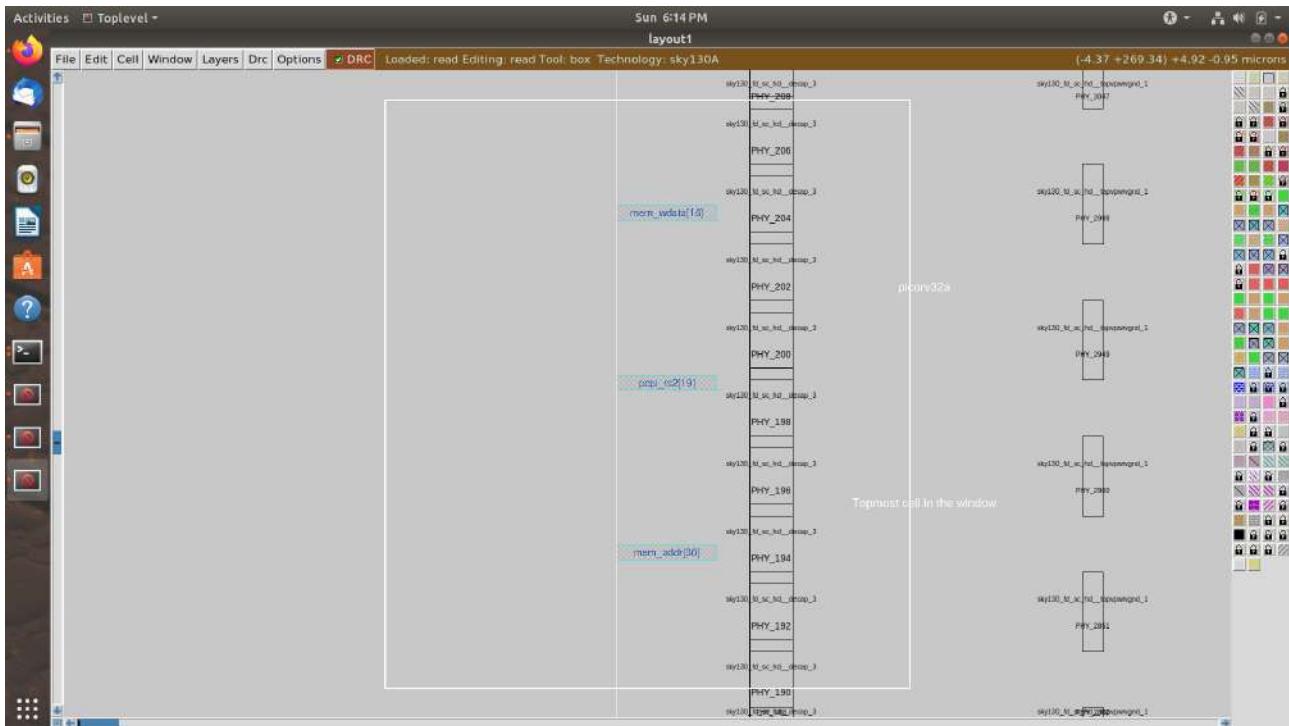
```
# Command to load the floorplan def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.floorplan.def &
```

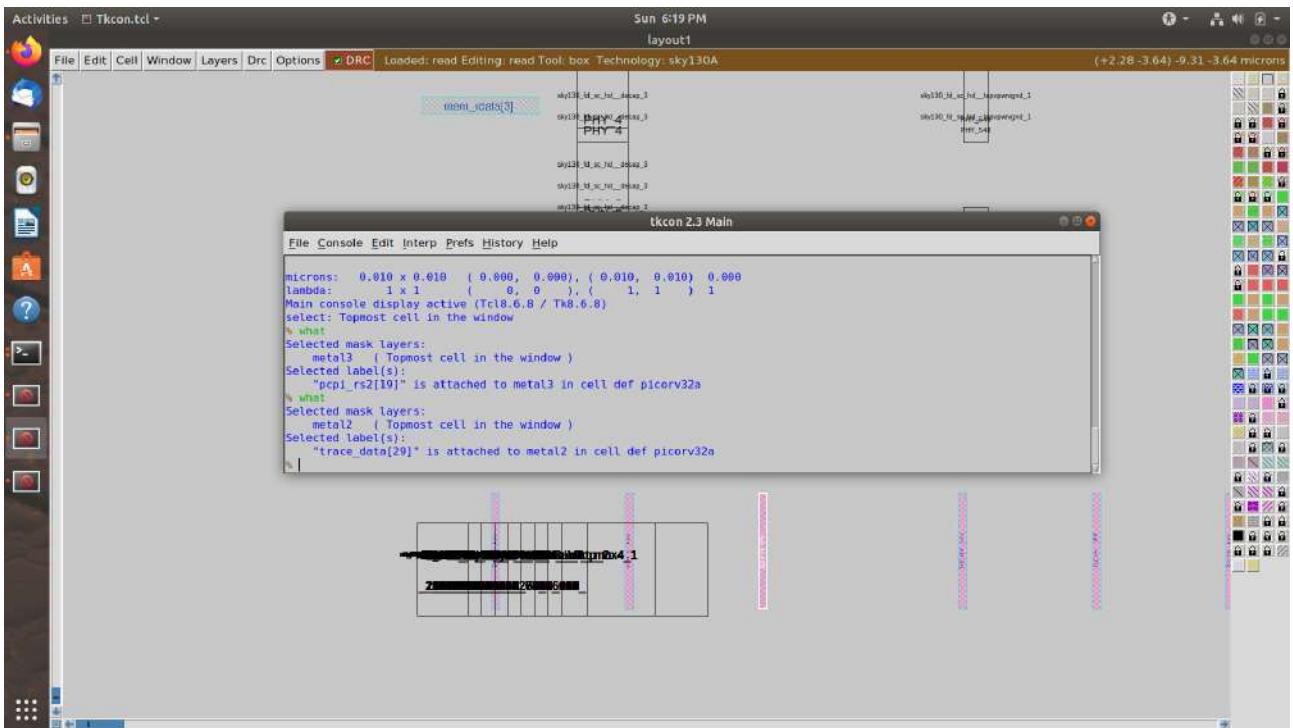
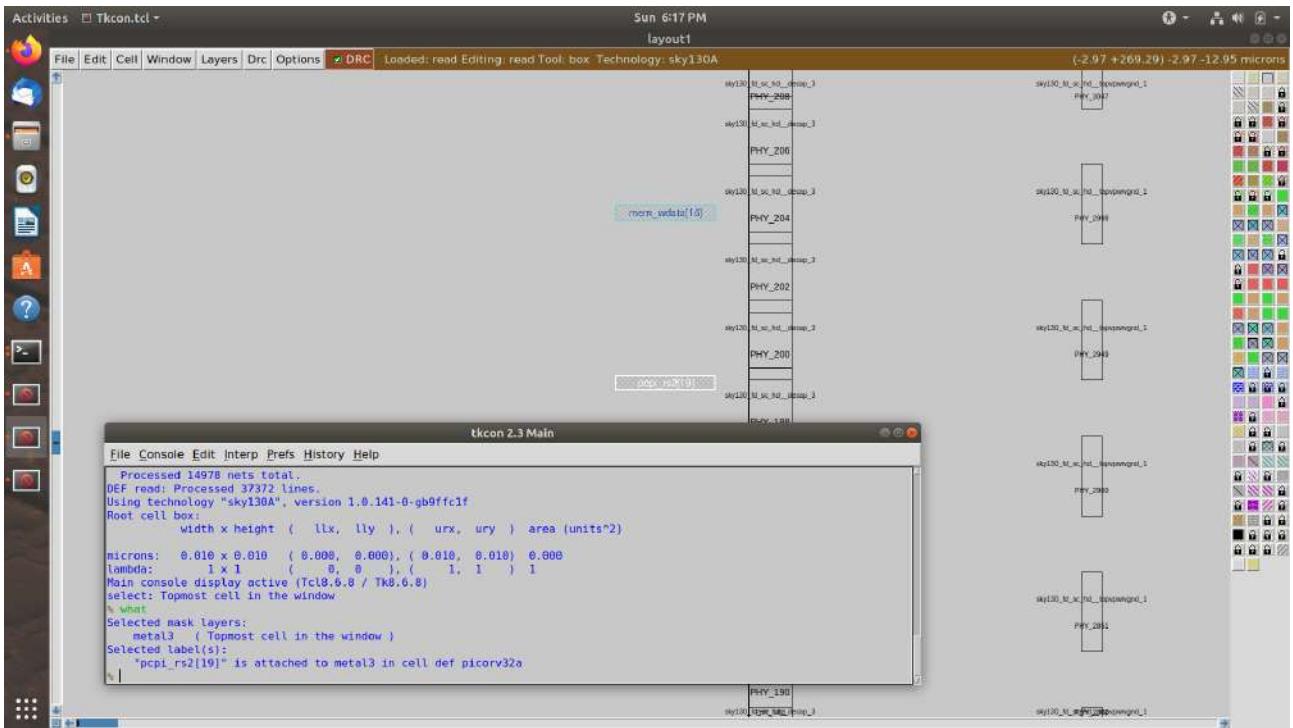
Screenshots of floorplan def in magic



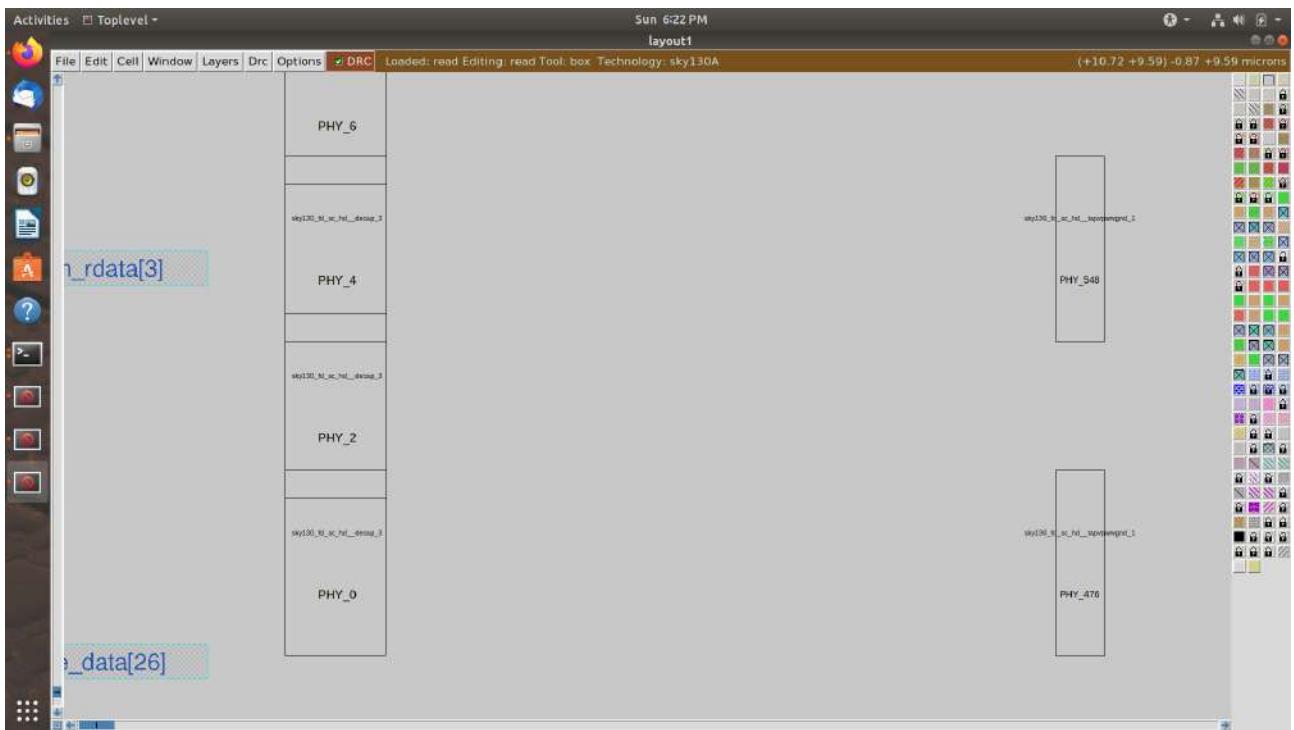
Equidistant placement of ports



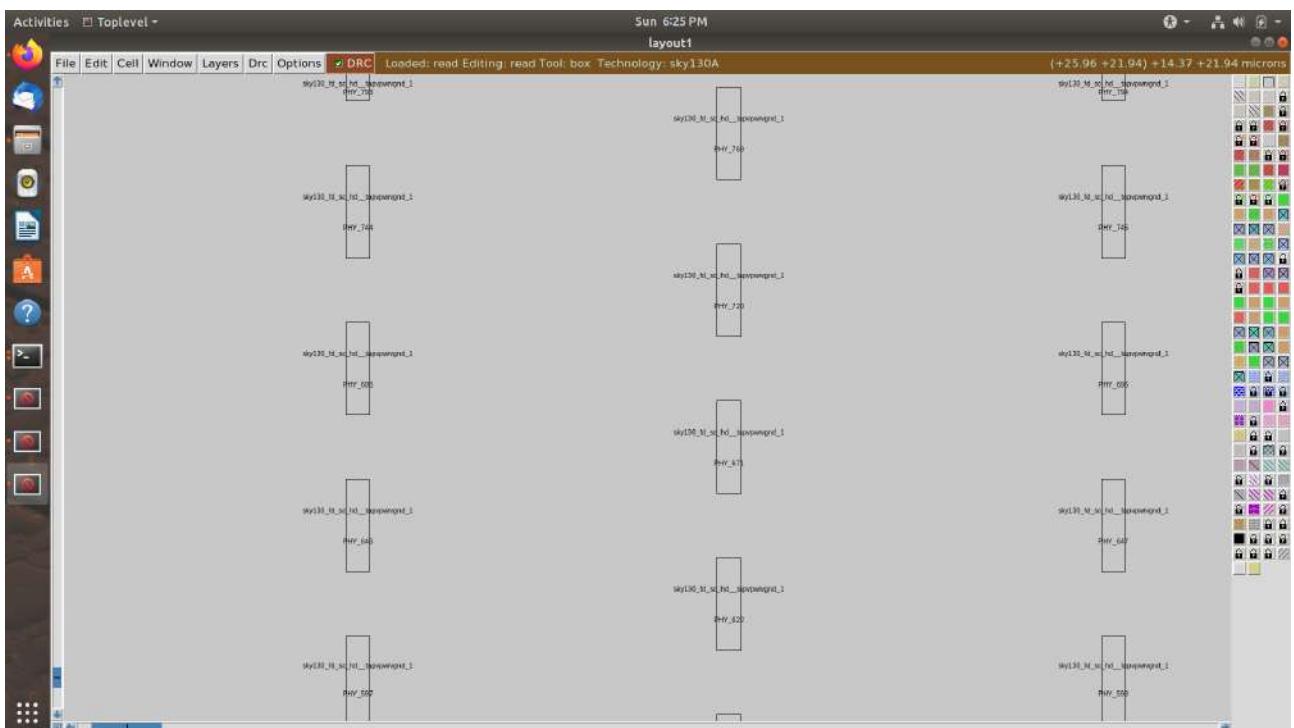
Port layer as set through config.tcl



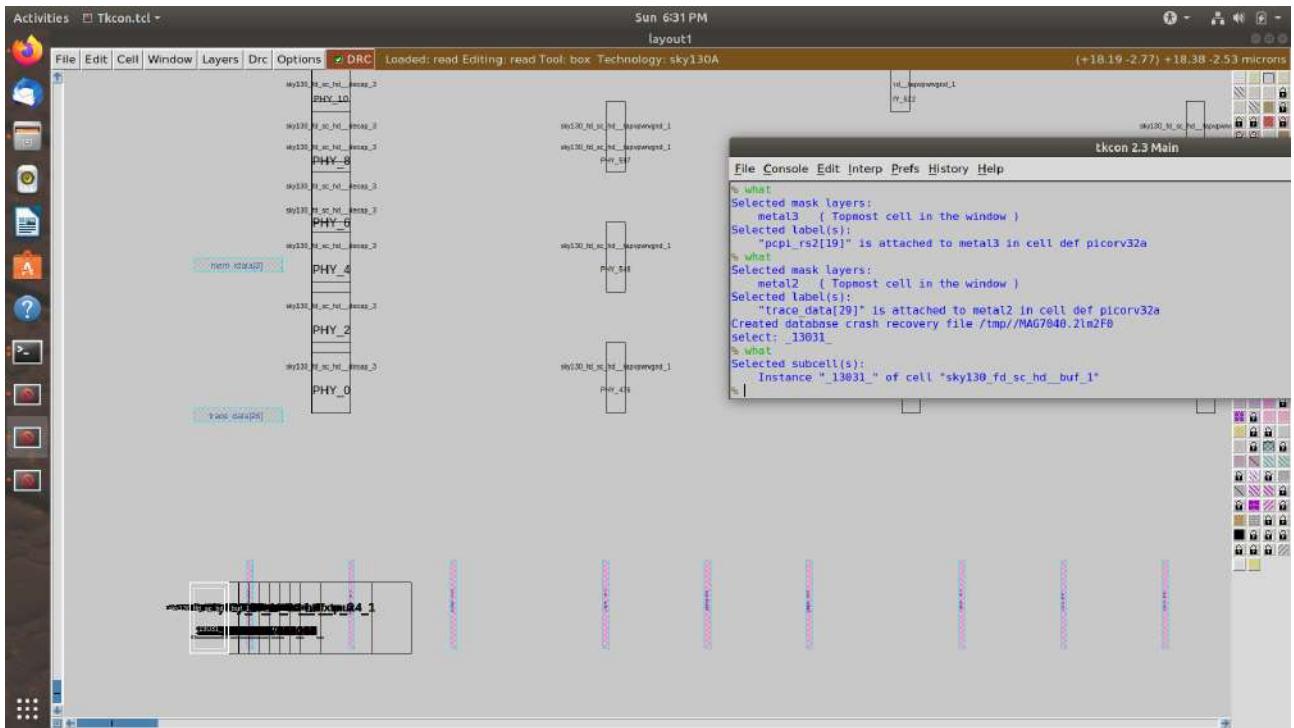
Decap Cells and Tap Cells



Diagonally equidistant Tap cells



Unplaced standard cells at the origin



4. Run 'picorv32a' design congestion aware placement using OpenLANE flow and generate necessary outputs.

Command to run placement

```
# Congestion aware placement by default
```

```
run_placement
```

Screenshots of placement run

```

Activities Terminal - Sun 10:44 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
er stripe. Moving to closest stripe at (567.000um, 103.880um).
[WARNING PSM-0030] Vsrc location at (565.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 257.060um).
[WARNING PSM-0030] Vsrc location at (5.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (145.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
[WARNING PSM-0030] Vsrc location at (425.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 563.420um).
[INFO PSM-0031] Number of nodes on net VGND = 19223.
[INFO PSM-0037] G matrix created sucessfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/floorplan/picorv32a.floorplan.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/floorplan/7-pdn.def
1
::: % run_placement

```

```

Activities Terminal - Sun 10:46 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
legalized HPWL      779196.5 u
delta HPWL          2 %
[INFO DPL-0020] Mirrored 6193 instances
[INFO DPL-0021] HPWL before      779196.5 u
[INFO DPL-0022] HPWL after       766080.0 u
[INFO DPL-0023] HPWL delta      -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/placement/8-resizer.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 12
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
::: %

```

5. Load generated placement def in magic tool and explore the placement.

Commands to load placement def in magic in another terminal

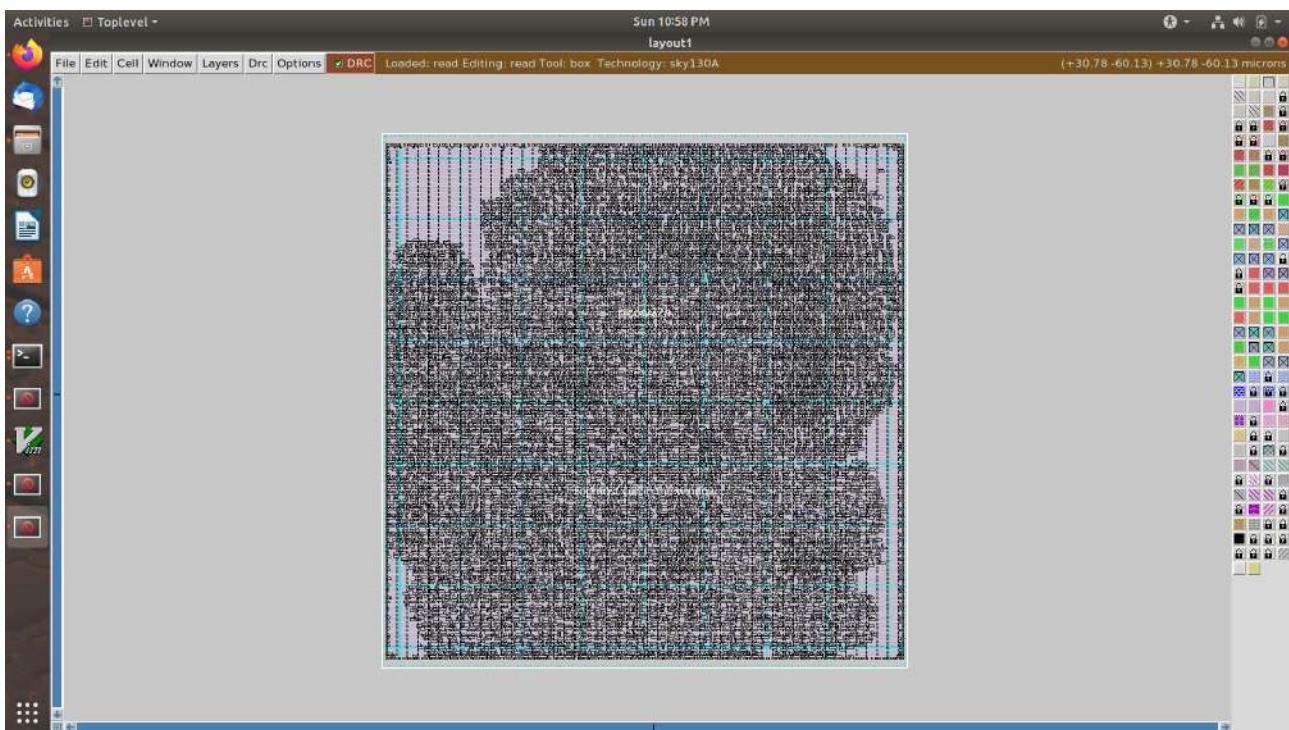
Change directory to path containing generated placement def

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/  
17-03_12-06/results/placement/
```

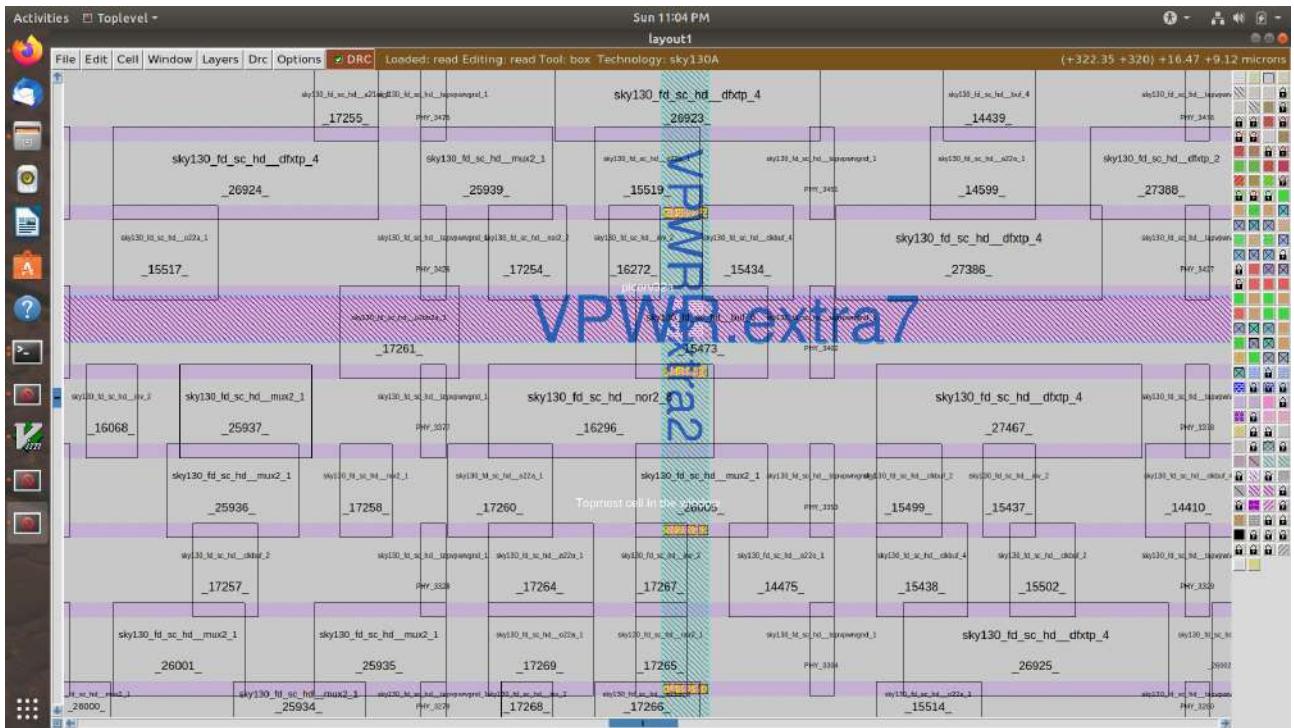
Command to load the placement def in magic tool

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def  
&
```

Screenshots of floorplan def in magic



Standard cells legally placed



Commands to exit from current run

```
# Exit from OpenLANE flow
```

```
exit
```

```
# Exit from OpenLANE flow docker sub-system
```

```
exit
```

Theory

Implementation

- **Section 3 tasks:-**

6. Clone custom inverter standard cell design from github repository: [Standard cell design and characterization using OpenLANE flow.](#)
 7. Load the custom inverter layout in magic and explore.
 8. Spice extraction of inverter in magic.
 9. Editing the spice model file for analysis through simulation.
 10. Post-layout ngspice simulations.
 11. Find problem in the DRC section of the old magic tech file for the skywater process and fix them.
- Section 3 - Tasks 1 to 5 files, reports and logs can be found in the following folder:

[Section 3 - Tasks 1 to 5 \(vsdstdcelldesign\)](#)

- Section 3 - Task 6 files, reports and logs can be found in the following folder:

[Section 3 - Task 6 \(drc_tests\)](#)

1. Clone custom inverter standard cell design from github repository

```
# Change directory to openlane
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# Clone the repository with custom inverter design
```

```
git clone https://github.com/nickson-jose/vsdstdcelldesign
```

```
# Change into repository directory
```

```
cd vsdstdcelldesign
```

```
# Copy magic tech file to the repo directory for easy access
```

```
cp /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic/sky130A.tech .
```

```
# Check contents whether everything is present
```

ls

```
# Command to open custom inverter layout in magic
```

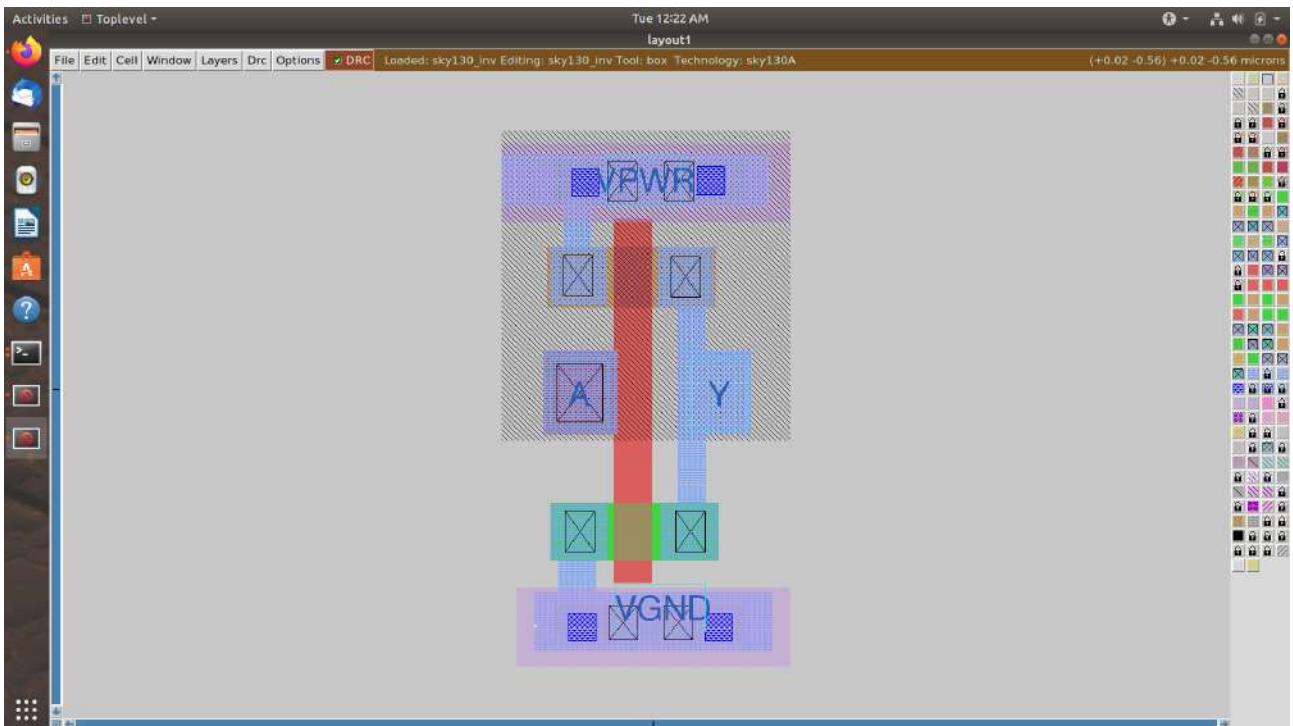
```
magic -T sky130A.tech sky130_inv.mag &
```

Screenshot of commands run

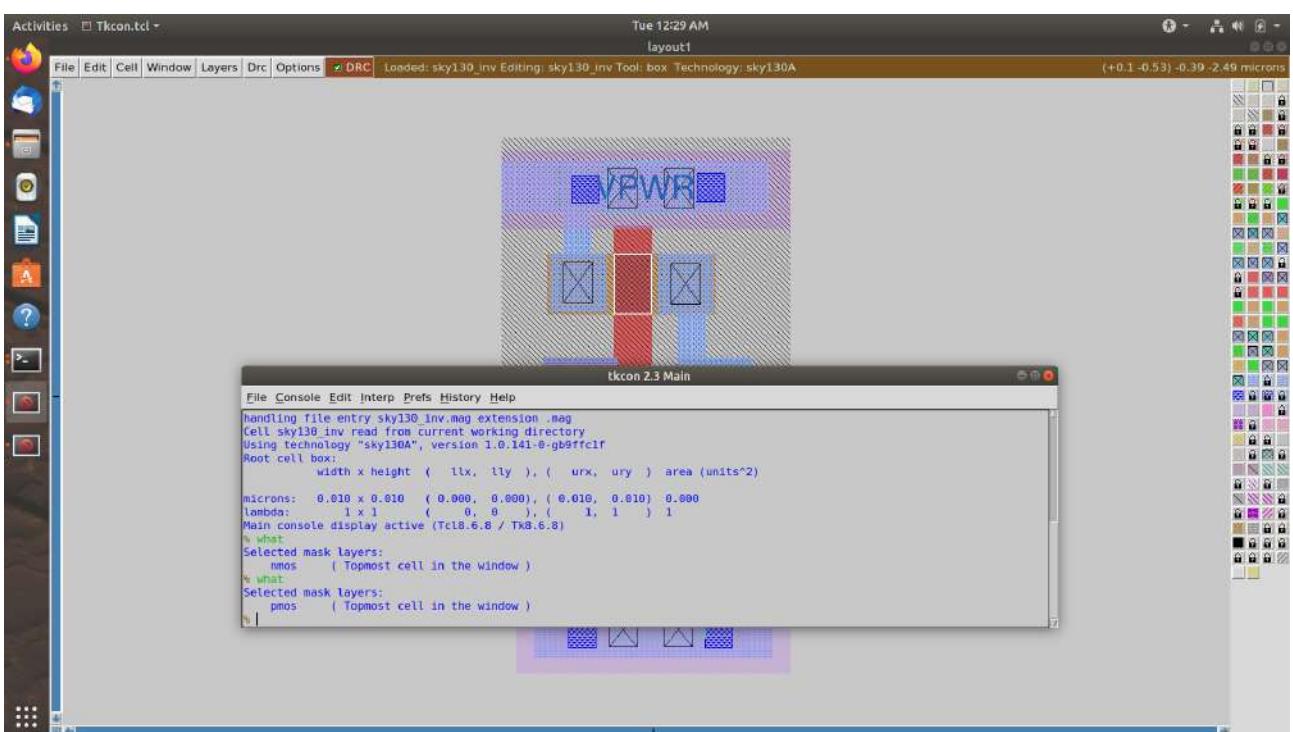
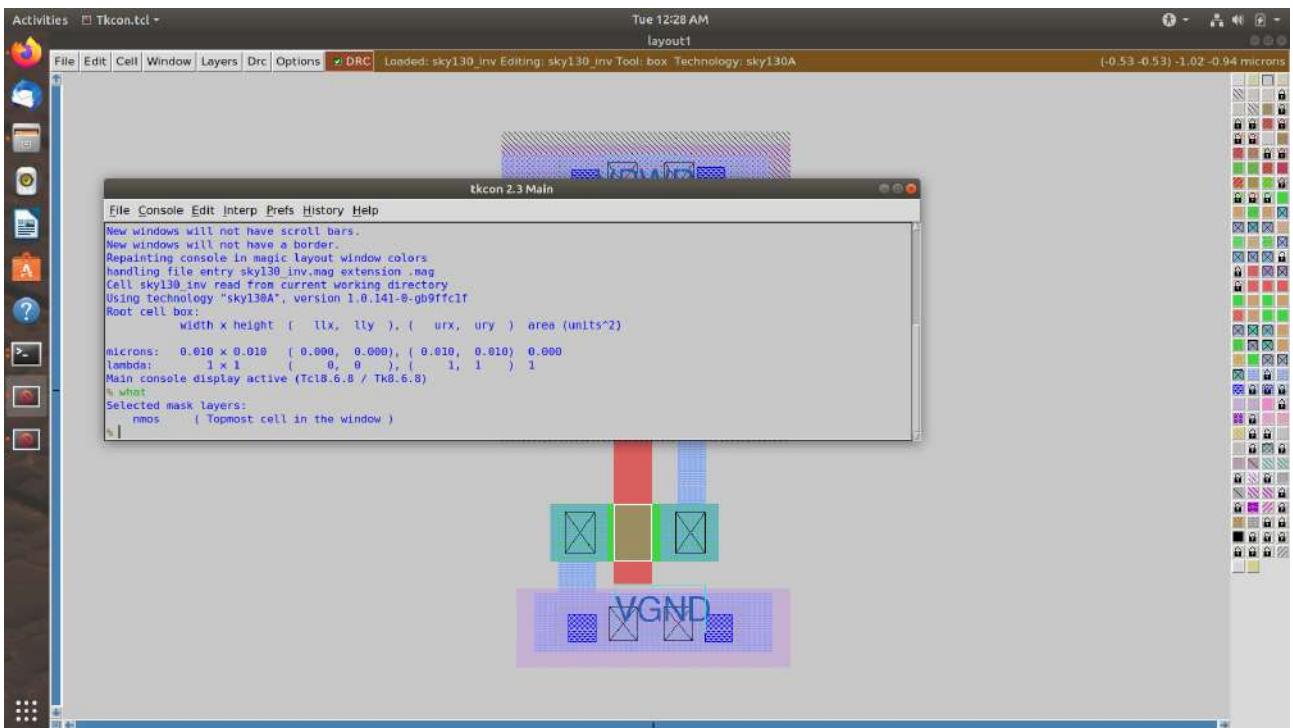
```
Activities Terminal Tue 12:22 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ git clone https://github.com/nickson-jose/vsdstdcelldesign
Cloning into 'vsdstdcelldesign'...
remote: Enumerating objects: 492, done.
remote: Counting objects: 100% (18/18), done.
remote: Compressing objects: 100% (18/18), done.
remote: Total 492 (delta 7), reused 0 (delta 0), pack-reused 474
Receiving objects: 100% (492/492), 24.08 MiB | 480.00 KiB/s, done.
Resolving deltas: 100% (210/210), done.
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd vsdstdcelldesign
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cp /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/magic/sky130A.tech .
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls
extras Images libs LICENSE README.md sky130A.tech sky130_inv.mag
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ magic -T sky130A.tech sky130_inv.mag &
[1] 4495
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```

2. Load the custom inverter layout in magic and explore.

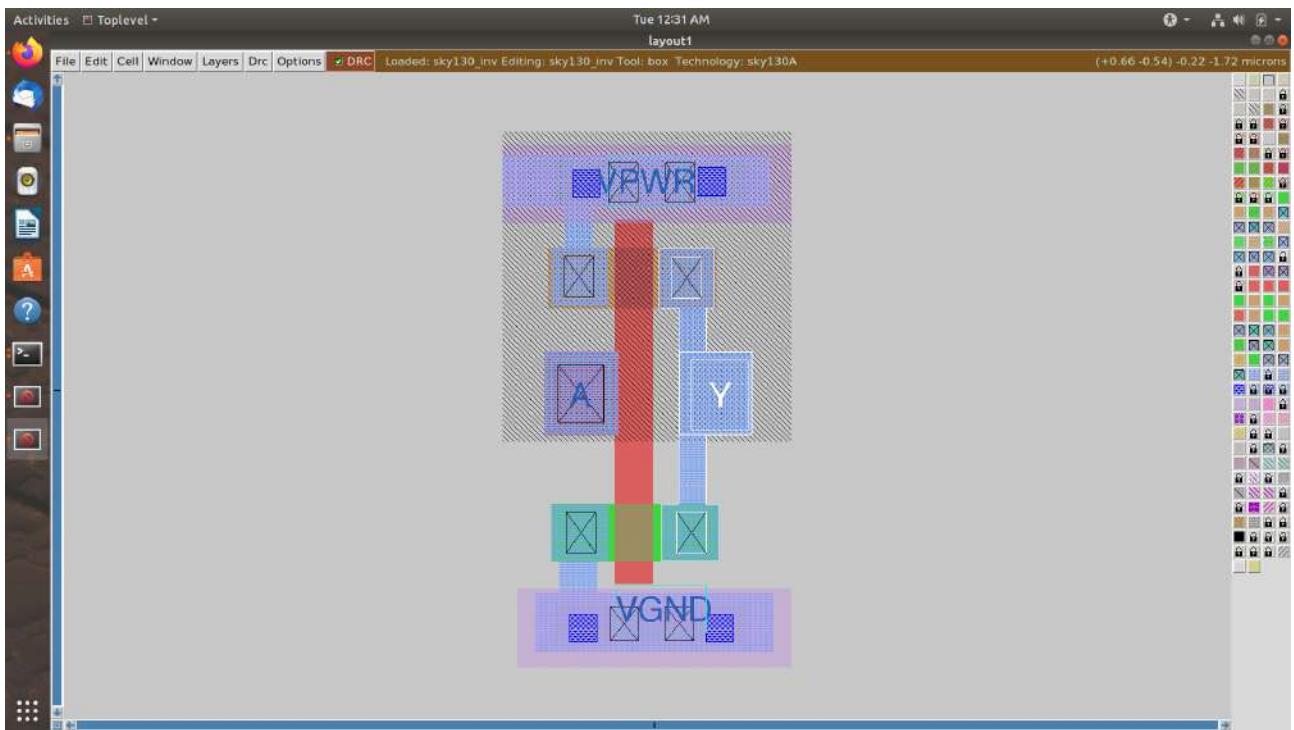
Screenshot of custom inverter layout in magic



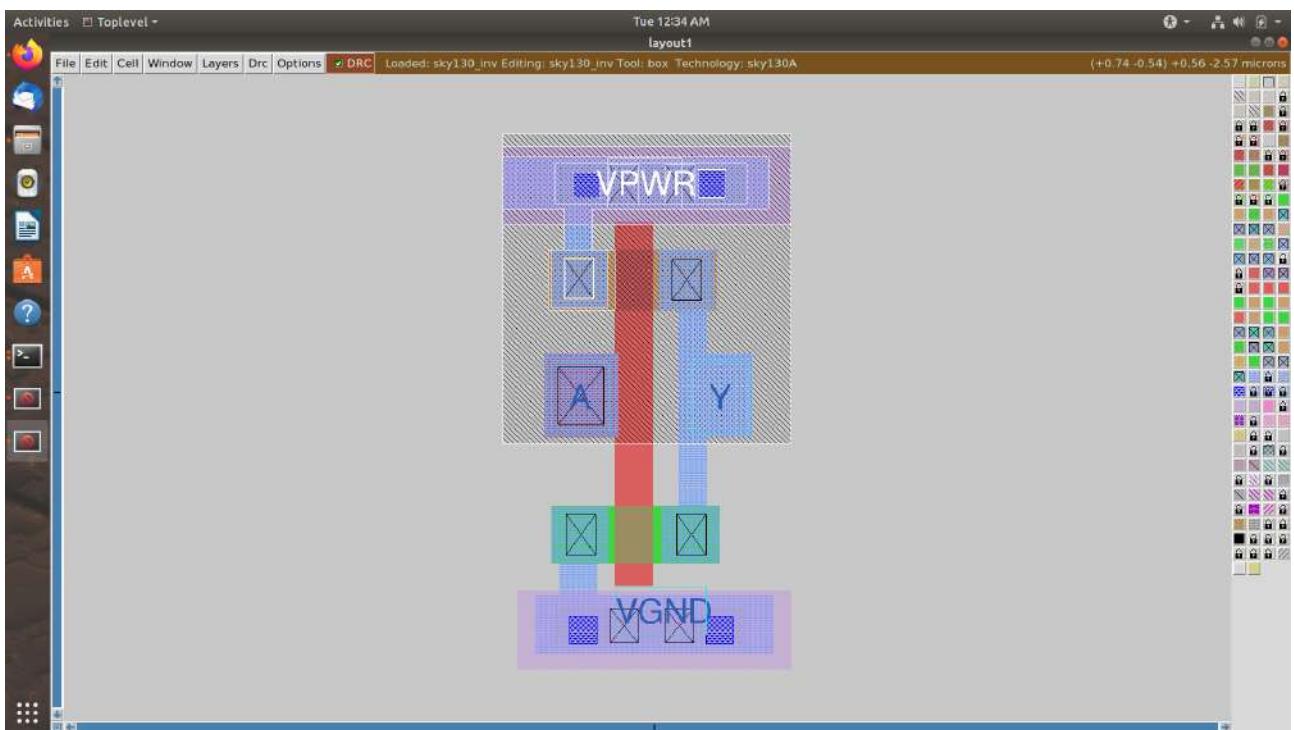
NMOS and PMOS identified



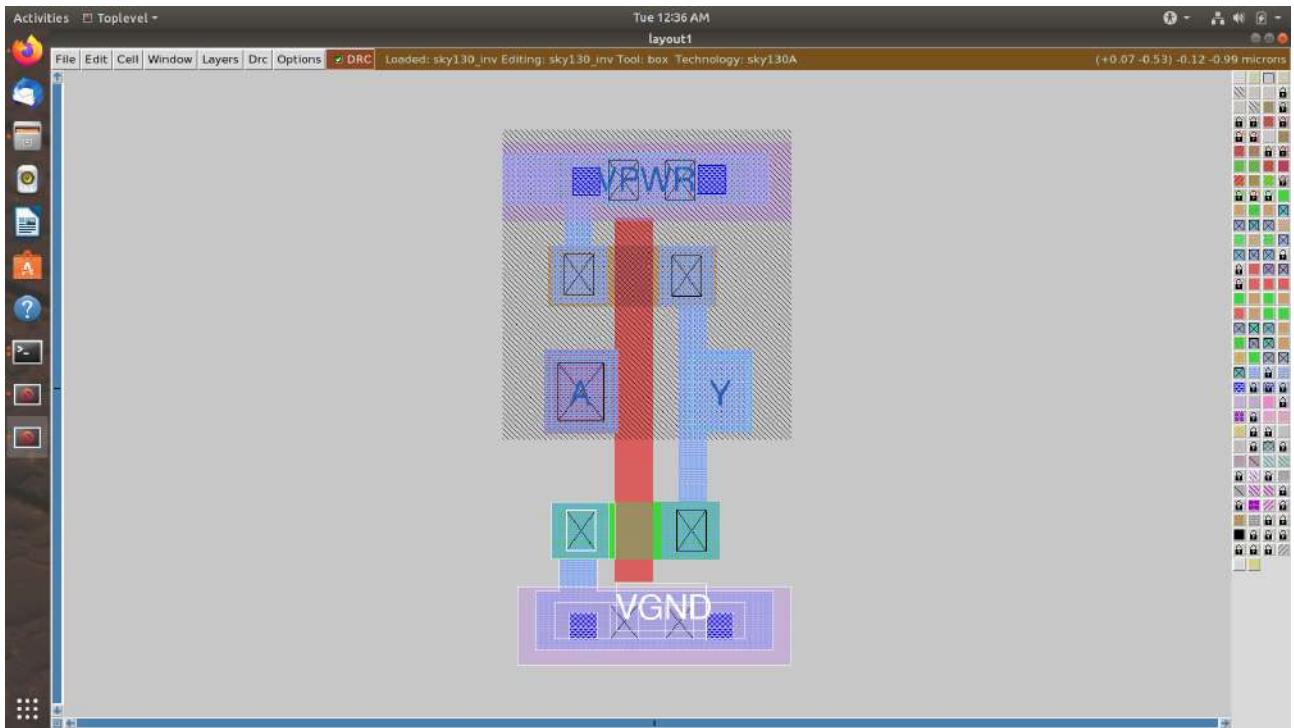
Output Y connectivity to PMOS and NMOS drain verified



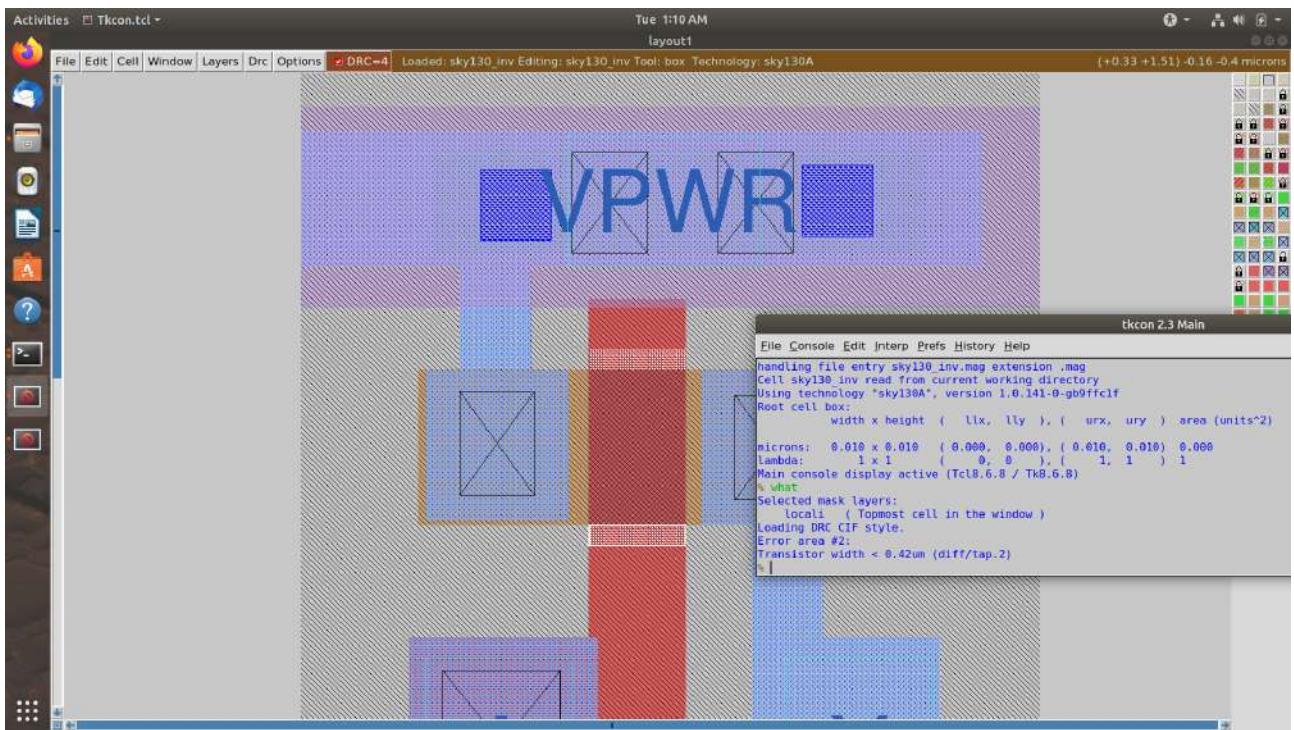
PMOS source connectivity to VDD (here VPWR) verified



NMOS source connectivity to VSS (here VGND) verified



Deleting necessary layout part to see DRC error



3. Spice extraction of inverter in magic.

Commands for spice extraction of the custom inverter layout to be used in tkcon window of magic

```
# Check current directory
```

pwd

```
# Extraction command to extract to .ext format
```

extract all

Before converting ext to spice this command enable the parasitic extraction also

`ext2splice cthresh 0 rthresh 0`

Converting to ext to spice

ext2spice

Screenshot of tkcon window after running above commands

```
Activities □ Tkcon.tcl - Tue 1:24 AM
tkcon 2.3 Main

File Console Edit Interp Prefs History Help
Loading history file ... 16 events added
Use openwrapper to create a new GUI-based layout window
Use closerwrapper to remove a new GUI-based layout window

Magic 8.3 revision 400 - Compiled on Mon May 22 20:58:24 IST 2023.
Starting magic under Tcl Interpreter
Using Tk console window
Using TrueColor, VisualID 0x21 depth 24
Input style sky130(): scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
    nmosc obsactive mvbsactive obsl11 obsm1 obsm2 obsm3 obsm4 obsm5 obsnrd1 ubm fillblock comment obscomment res0p35 res0p69 reslp41 res2p85 res5p73
Processing system .magicrc file
New windows will not have a title caption.
New windows will not have scroll bars.
New windows will not have a border.
Repainting console in magic layout window colors
handling file entry sky130_inv.mag extension .mag
Cell sky130_inv read from current working directory
Using technology "sky130A", version 1.0.141-0-gb9ffcf
Root cell box:
    width x height ( llx, lly ),( urx, ury ) area (units^2)
microns: 0.010 x 0.010 ( 0.000, 0.000 ),( 0.010, 0.010 ) 0.000
lambda: 1 x 1 ( 0, 0 ),( 1, 1 ) 1
Main console display active (Tcl8.6.8 / Tk8.6.8)
> .pmel
> /home/vsuser/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
> extract all
Extracting sky130_inv into sky130_inv.ext:
% ext2spice cthresh 0 rthresh 0
% ext2spice
ext2spice finished.
%
```

Screenshot of created spice file

Activities ▾ GVim ▾

Tue 1:27 AM

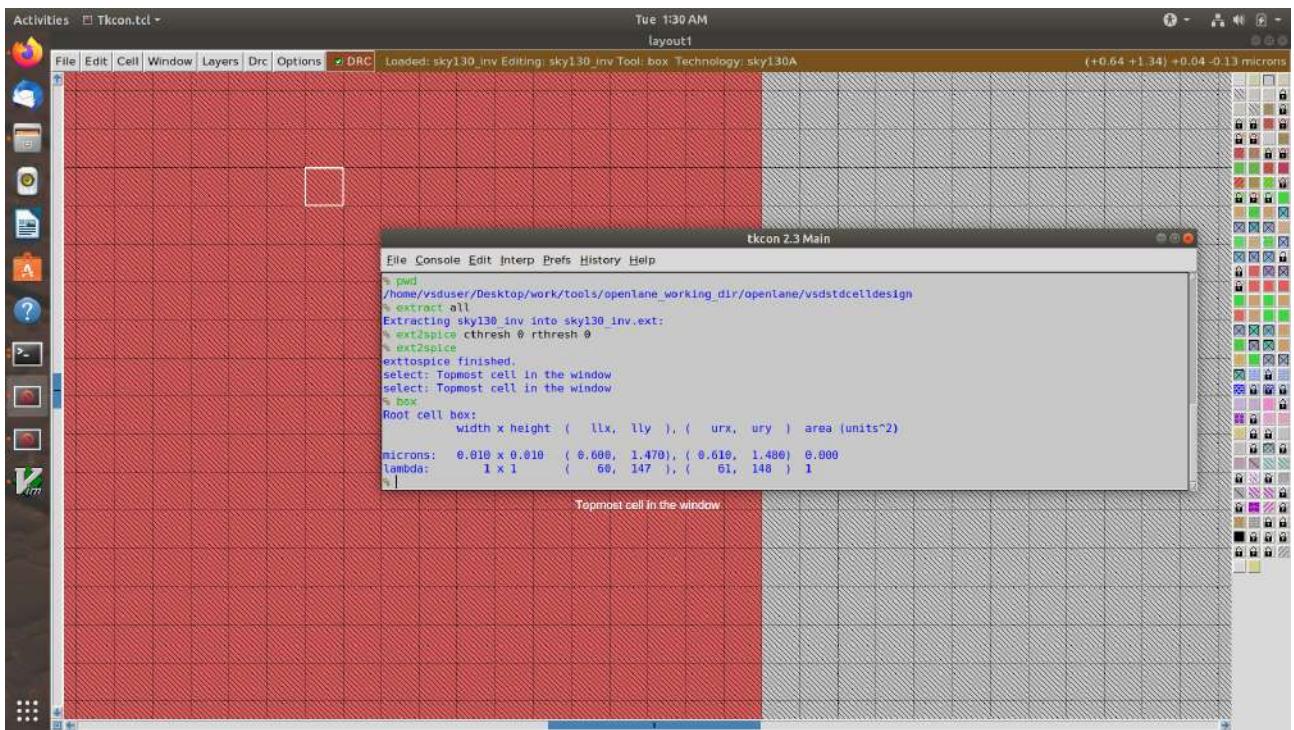
sky130_inv.spice (~/Desktop/work/tools/op...ng_dlr/openlane/vsdstdceldesign) - GVIM

File Edit Tools Syntax Buffers Window Help

```
1 * SPICE3 file created from sky130_inv.ext - technology: sky130A
2
3 .option scale=10m
4
5 .subckt sky130_inv A Y VPWR VGND
6 X0 Y A VGND VGND sky130_fd_pr_nfet_01v8 ad=1.44n pd=0.152m as=1.37n ps=0.148m w=35 l=23
7 X1 Y A VPWR VPWR sky130_fd_pr_pfet_01v8 ad=1.44n pd=0.152m as=1.52n ps=0.156m w=37 l=23
8 C0 A VPWR 0.0774f
9 C1 Y VPWR 0.117f
10 C2 A Y 0.0754f
11 C3 Y VGND 0.279f
12 C4 A VGND 0.45f
13 C5 VPWR VGND 0.781f
14 .ends
```

4. Editing the spice model file for analysis through simulation.

Measuring unit distance in layout grid



Final edited spice file ready for ngspice simulation

Activities M GVim Tue 2:50 PM

File Edit Tools Syntax Buffers Window Help

sky130_inv.spice (~/Desktop/work/tools/op...ing_dir/openlane/vsdstdcelldesign) - GVIM

```
1 * SPICE3 file created from sky130_inv.ext - technology: sky130A
2
3 * Scale adjusted as per magic layout grid unit distance
4 .option scale=0.01u
5
6 * Including our custom inverter pmos and nmos libs
7 .include ./libs/pshort.lib
8 .include ./libs/nshort.lib
9
10 // .subckt sky130_inv A Y VPWR VGND
11
12 * Changing pmos and nmos to included library model names and subckt names
13 M1000 Y A VPWR VPWR pshort_model.0 w=37 l=23
14 * ad=1.44n pd=0.152m as=1.52n ps=0.156m
15 M1001 Y A VGND VGND nshort_model.0 w=35 l=23
16 * ad=1.44n pd=0.152m as=1.37n ps=0.148m
17
18 * Adding VDD & VSS for simulation
19 VDD VPWR 0 3.3V
20 VSS VGND 0 0V
21 * Adding load capacitance to remove spikes in output
22 C6 Y 0 2fF
23
24 * Defining input pulse
25 Va A VGND PULSE(0V 3.3V 0 0.1ns 0.1ns 2ns 4ns)
```

25,47 Top

Activities M GVim Tue 2:51PM

File Edit Tools Syntax Buffers Window Help

sky130_inv.spice (~/Desktop/work/tools/op...ing_dir/openlane/vsdstdcelldesign) - GVIM

```
24 * Defining input pulse
25 Va A VGND PULSE(0V 3.3V 0 0.1ns 0.1ns 2ns 4ns)
26 C0 A VPWR 0.0774fF
27 C1 Y VPWR 0.117fF
28 C2 A Y 0.0754fF
29 C3 Y VGND 0.279fF
30 C4 A VGND 0.45fF
31 C5 VPWR VGND 0.781fF
32 // .ends
33
34 * Specifying the type of analysis to be performed
35 .tran 1n 20n
36 .control
37 run
38 .endc
39 .end
```

25,47 Bot

5. Post-layout ngspice simulations.

Commands for ngspice simulation

```
# Command to directly load spice file for simulation to ngspice
```

```
ngspice sky130_inv.spice
```

```
# Now that we have entered ngspice with the simulation spice file loaded we just have to  
load the plot
```

```
plot y vs time a
```

Screenshots of ngspice run

```

Activities Terminal - vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ngspice sky130_inv.spice
*****
** ngspice-27 : Circuit level simulation program
** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California.
** Please get your ngspice manual from http://ngspice.sourceforge.net/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Tue Dec 26 17:10:20 UTC 2017
*****
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node Voltage
-----
y 3.3
a 0
vpwr 3.3
vgnd 0
va#branch 0

```

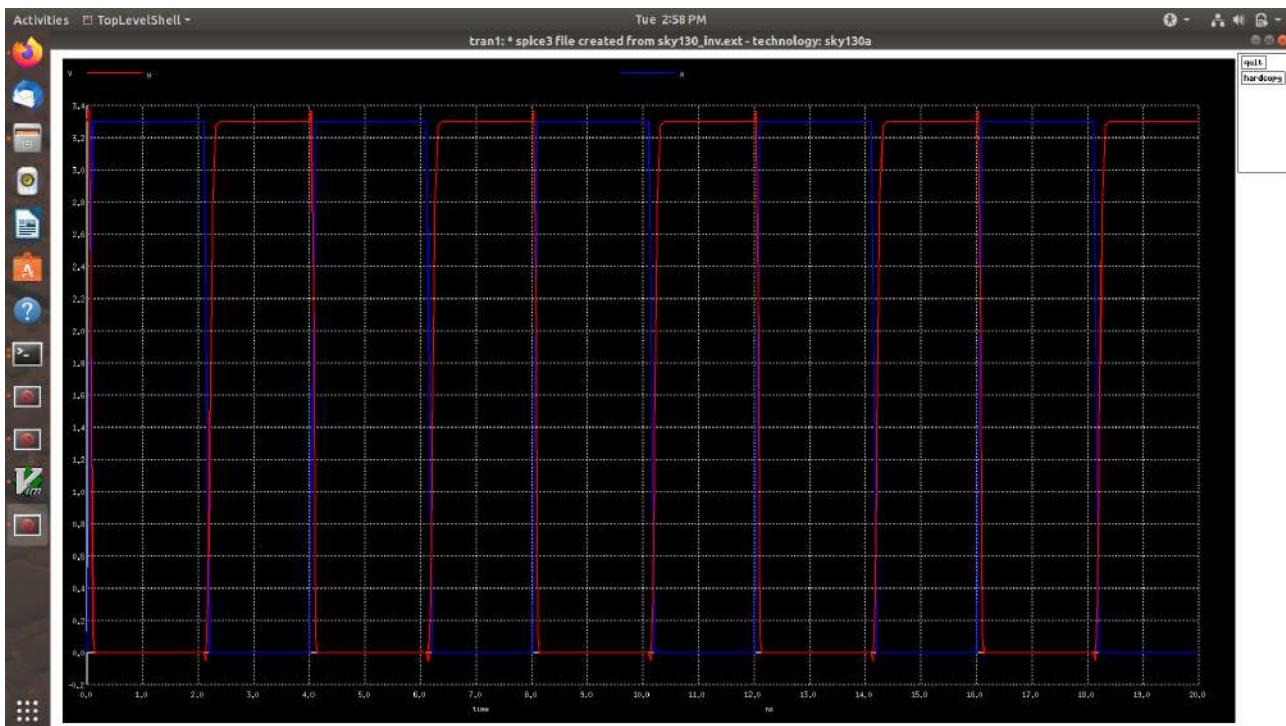
```

Activities TopLevelShell - vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ 
*****
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node Voltage
-----
y 3.3
a 0
vpwr 3.3
vgnd 0
va#branch 0
vss#branch 3.32351e-12
vdd#branch -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
::: ngspice 1 -> 

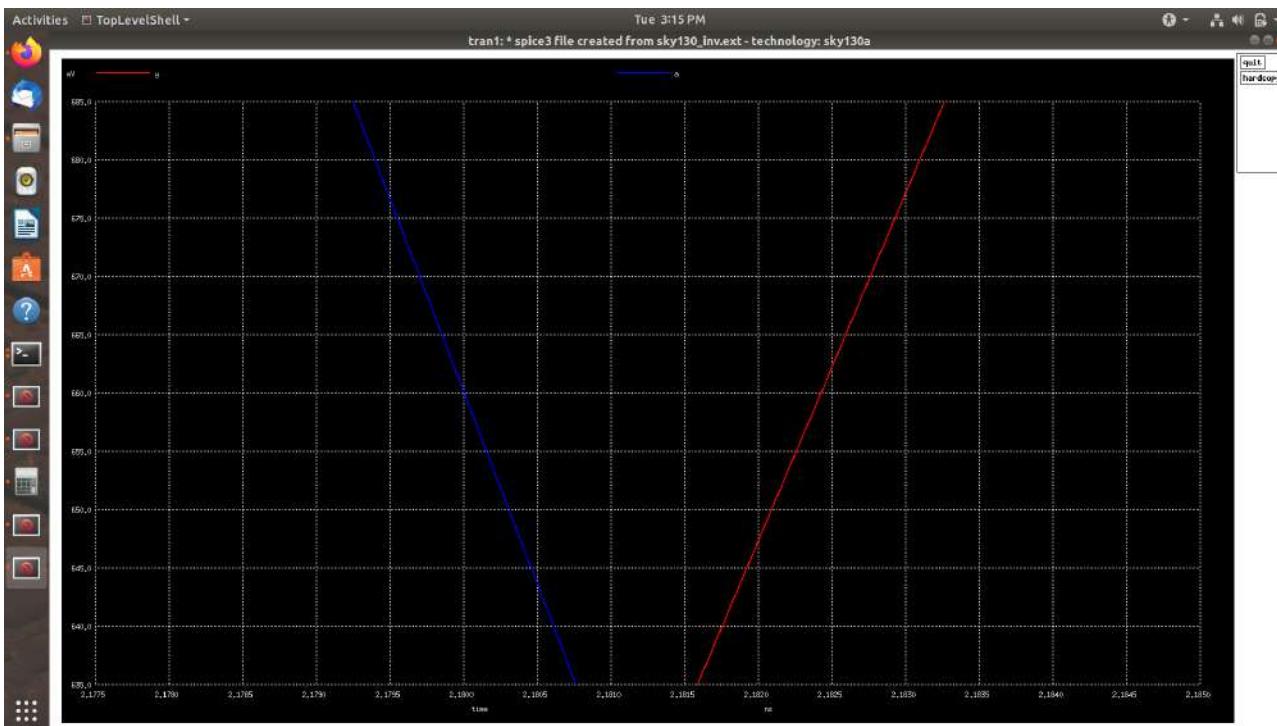
```

Screenshot of generated plot



Rise transition time calculation

20% Screenshots



Activities Terminal -

Tue 3:20 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign

```

File Edit View Search Terminal Help
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a

Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

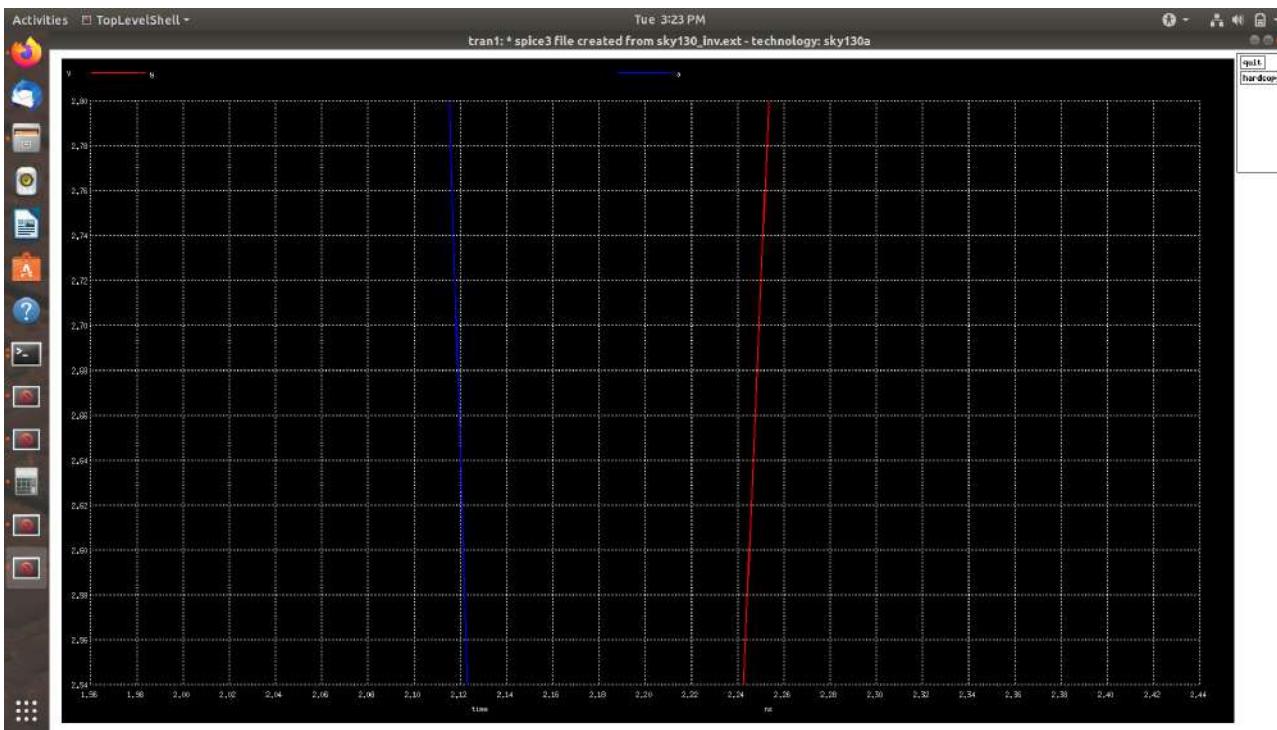
Warning: va: no DC value, transient time 0 value used

Initial Transient Solution
-----
Node          Voltage
---- 
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043

```

80% Screenshots



Activities Terminal Tue 3:24 PM

vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```

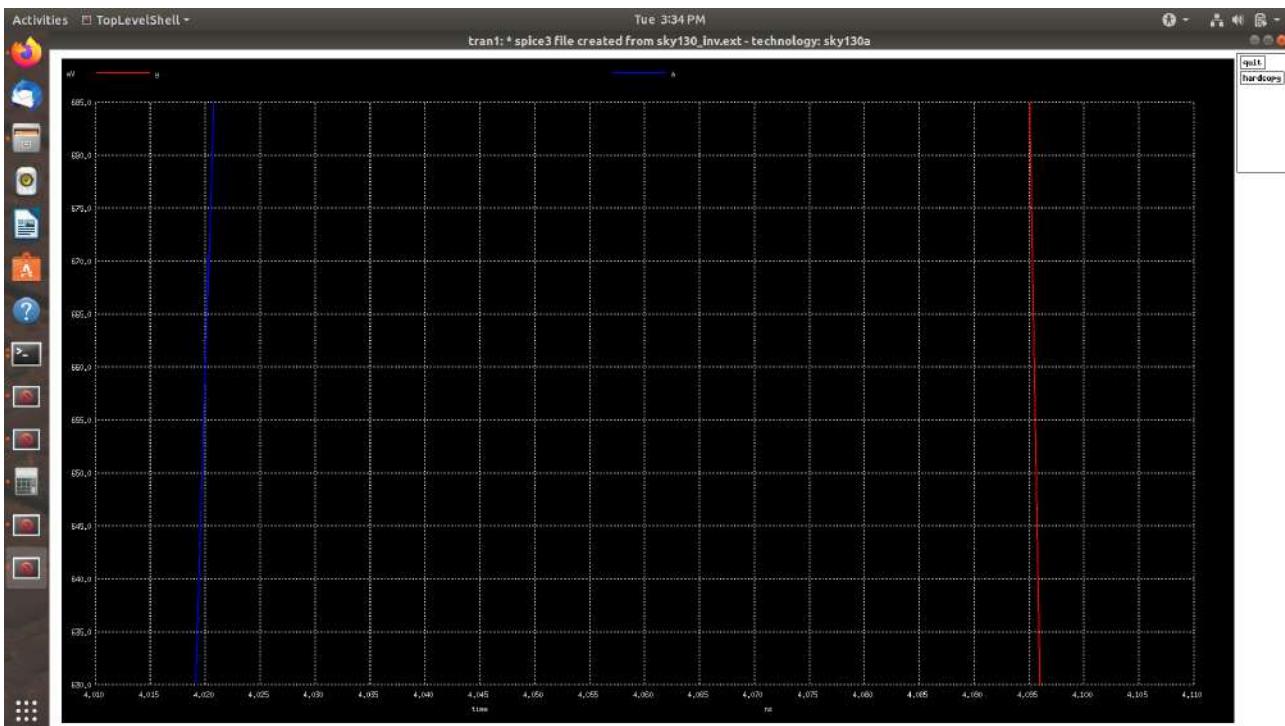
File Edit View Search Terminal Help
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node          Voltage
-----
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403

```

Fall transition time calculation

20% Screenshots



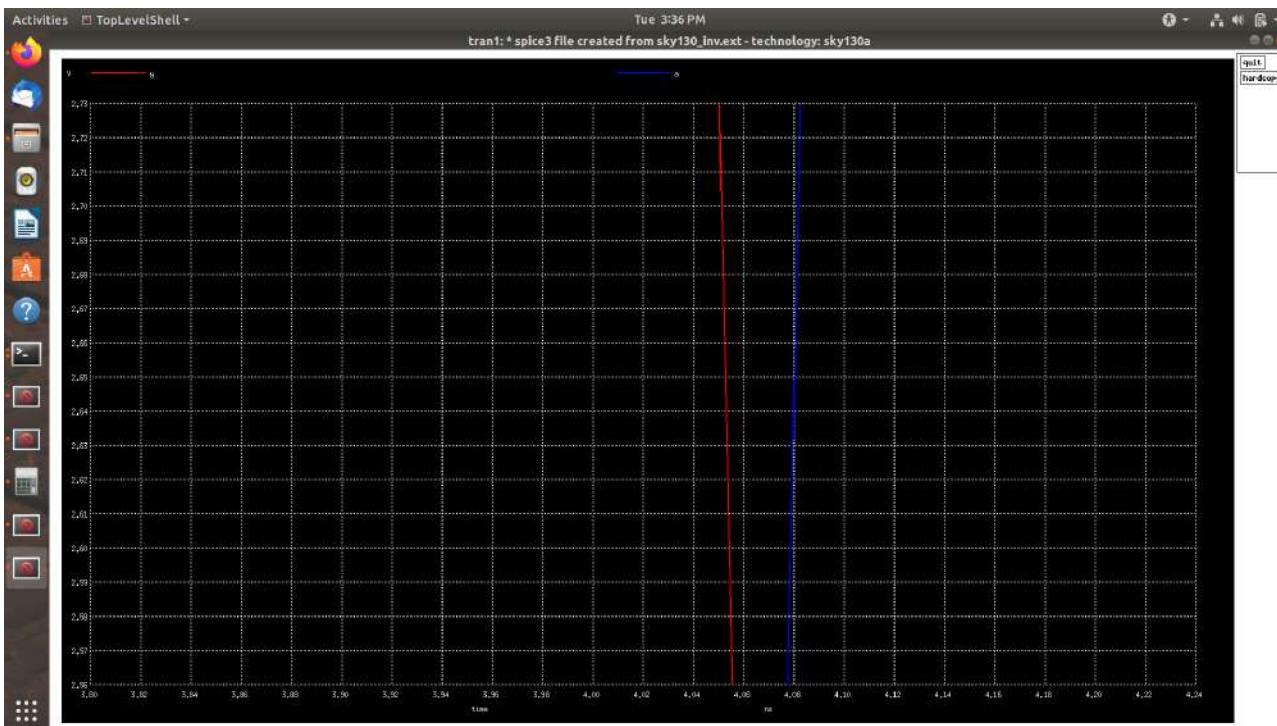
Activities Terminal -

Tue 3:34 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node          Voltage
-----
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
x0 = 4.09555e-09, y0 = 0.660127
```

80% Screenshots



Activities Terminal -

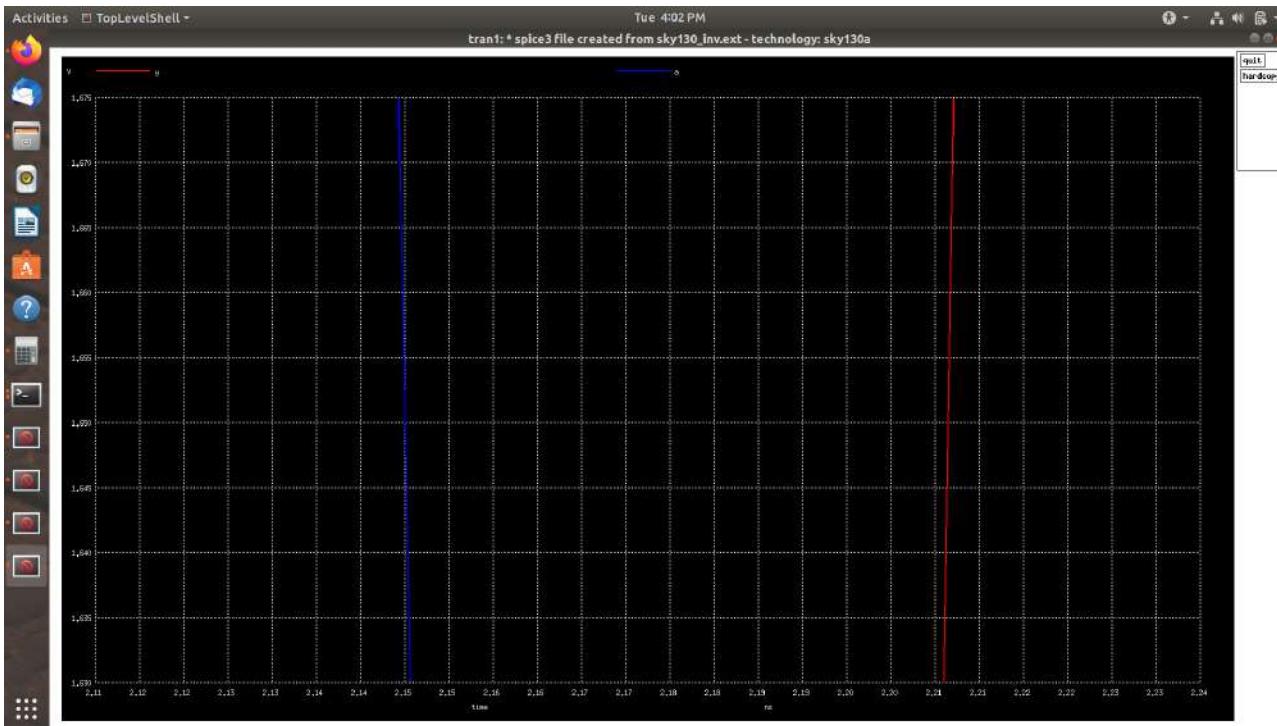
Tue 3:36 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```
Initial Transient Solution
-----
Node          Voltage
-----
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
x0 = 4.09555e-09, y0 = 0.660127
x0 = 4.0536e-09, y0 = 2.64
```

Rise Cell Delay Calculation

50% Screenshots



Activities Terminal

Tue 4:03 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```

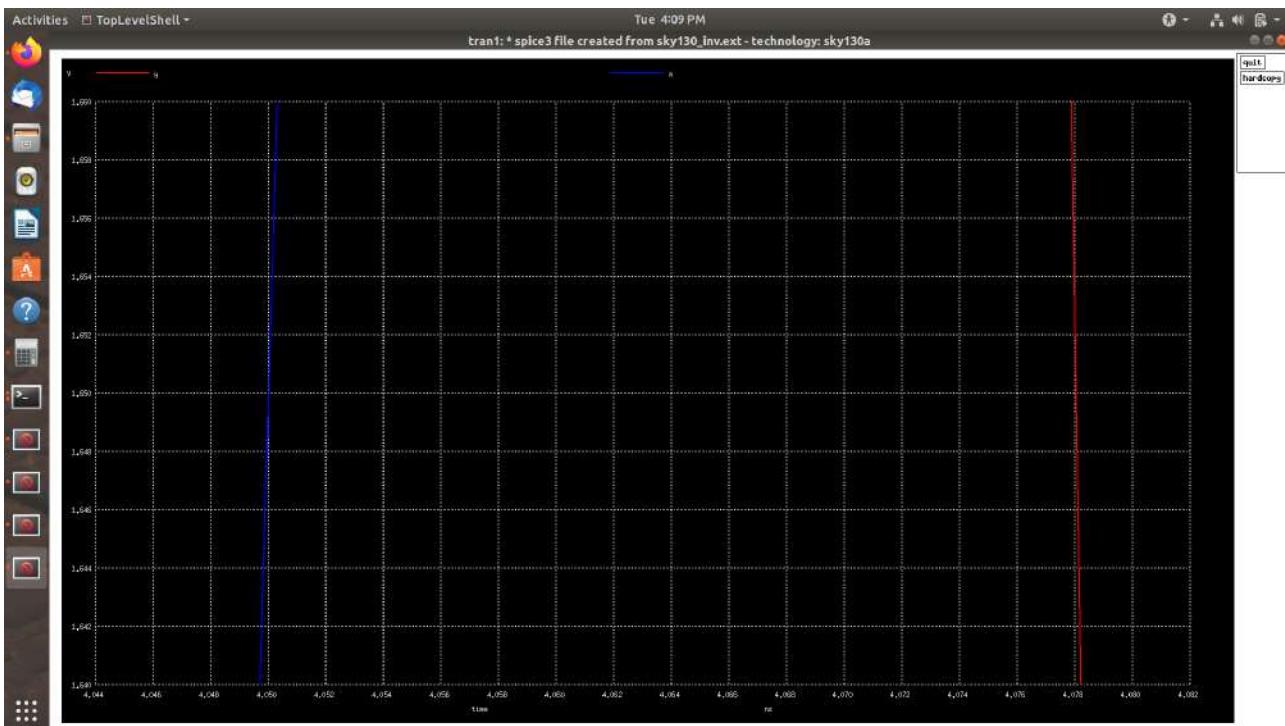
File Edit View Search Terminal Help
Node          Voltage
-----
y             3.3
a             0
vpwr          3.3
vgnd          0
va#branch     0
vss#branch    3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
x0 = 4.09555e-09, y0 = 0.660127
x0 = 4.0536e-09, y0 = 2.64
x0 = 2.21144e-09, y0 = 1.65
x0 = 2.15008e-09, y0 = 1.6501

```

Fall Cell Delay Calculation

50% Screenshots



Activities Terminal Tue 4:10 PM

vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```

File Edit View Search Terminal Help
vpwr          3.3
vgnd          0
va#branch     0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
> x0 = 2.24638e-09, y0 = 2.6403
> x0 = 4.09555e-09, y0 = 0.660127
> x0 = 4.0536e-09, y0 = 2.64
> x0 = 2.21144e-09, y0 = 1.65
> x0 = 2.15008e-09, y0 = 1.6501
> x0 = 4.07807e-09, y0 = 1.65005
> x0 = 4.05e-09, y0 = 1.65002

```

6. Find problem in the DRC section of the old magic tech file for the skywater process and fix them.

Link to Sky130 Periphery rules: <https://skywater-pdk.readthedocs.io/en/main/rules/periphery.html>

Commands to download and view the corrupted skywater process magic tech file and associated files to perform drc corrections

```
# Change to home directory
```

```
cd
```

```
# Command to download the lab files
```

```
wget http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
```

```
# Since lab file is compressed command to extract it
```

```
tar xfz drc_tests.tgz
```

```
# Change directory into the lab folder
```

```
cd drc_tests
```

```
# List all files and directories present in the current directory
```

```
ls -al
```

```
# Command to view .magicrc file
```

```
gvim .magicrc
```

```
# Command to open magic tool in better graphics
```

```
magic -d XR &
```

Screenshots of commands run

```
Activities Terminal Thu 10:33 PM
vsduser@vsdsquadron:~$ cd
vsduser@vsdsquadron:~$ wget http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
--2024-03-21 22:31:14-- http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
Resolving opencircuitdesign.com (opencircuitdesign.com)... 69.251.37.208
Connecting to opencircuitdesign.com (opencircuitdesign.com)|69.251.37.208|:80... connected.
HTTP request sent, awaiting response... 200 OK
Length: 41651 (41K) [application/x-gzip]
Saving to: 'drc_tests.tgz'

drc_tests.tgz          100%[=====] 40.67K 160KB/s in 0.3s

2024-03-21 22:31:15 (160 KB/s) - 'drc_tests.tgz' saved [41651/41651]

vsduser@vsdsquadron:~$ tar xfz drc_tests.tgz
vsduser@vsdsquadron:~$ cd drc_tests
vsduser@vsdsquadron:~/drc_tests$ ls -al
total 276
drwxrwxr-x 2 vsduser vsduser 4096 Sep 16 2020 .
drwxr-xr-x 22 vsduser vsduser 4096 Mar 21 22:31 ..
-rw-rw-r-- 1 vsduser vsduser 3178 Sep 15 2020 capm.mag
-rw-rw-r-- 1 vsduser vsduser 3610 Sep 16 2020 difftap.mag
-rw-rw-r-- 1 vsduser vsduser 1535 Sep 16 2020 dnwell.mag
-rw-rw-r-- 1 vsduser vsduser 1684 Sep 15 2020 hvtp.mag
-rw-rw-r-- 1 vsduser vsduser 897 Sep 15 2020 hvtr.mag
-rw-rw-r-- 1 vsduser vsduser 11586 Sep 15 2020 licon.mag
-rw-rw-r-- 1 vsduser vsduser 1480 Sep 15 2020 li.mag
-rw-rw-r-- 1 vsduser vsduser 4648 Sep 15 2020 lvtn.mag
-rw-rw-r-- 1 vsduser vsduser 2565 Sep 15 2020 .magicrc
```

```
Activities Terminal Thu 10:34 PM
vsduser@vsdsquadron:~/drc_tests$ vim .magicrc
vsduser@vsdsquadron:~/drc_tests$ magic -d XR
```

Screenshot of .magicrc file

```

Thu 10:35 PM
.magicrc (~/.drc_tests) - GVIM

File Edit Tools Syntax Buffers Window Help
1 puts stdout "Sourcing design .magicrc for technology sky130A ..."
2
3 # Put grid on 0.005 pitch. This is important, as some commands don't
4 # rescale the grid automatically (such as lef read?).
5
6 set scalefac [tech lambda]
7 if {[lindex $scalefac 1] < 2} {
8     scalegrid 1 2
9 }
10
11 # drc off
12 drc euclidean on
13
14 # Allow override of PDK path from environment variable PDKPATH
15 if {[catch {set PDKPATH $env(PDKPATH)}]} {
16     set PDKPATH "~/cad/pdk/sky130A"
17 }
18
19 # loading technology
20 # tech load $PDKPATH/libs.tech/magic/sky130A.tech
21 tech load sky130A.tech
22
23 # load device generator
24 # source $PDKPATH/libs.tech/magic/sky130A.tcl
25

".magicrc" 74L, 2565C

```

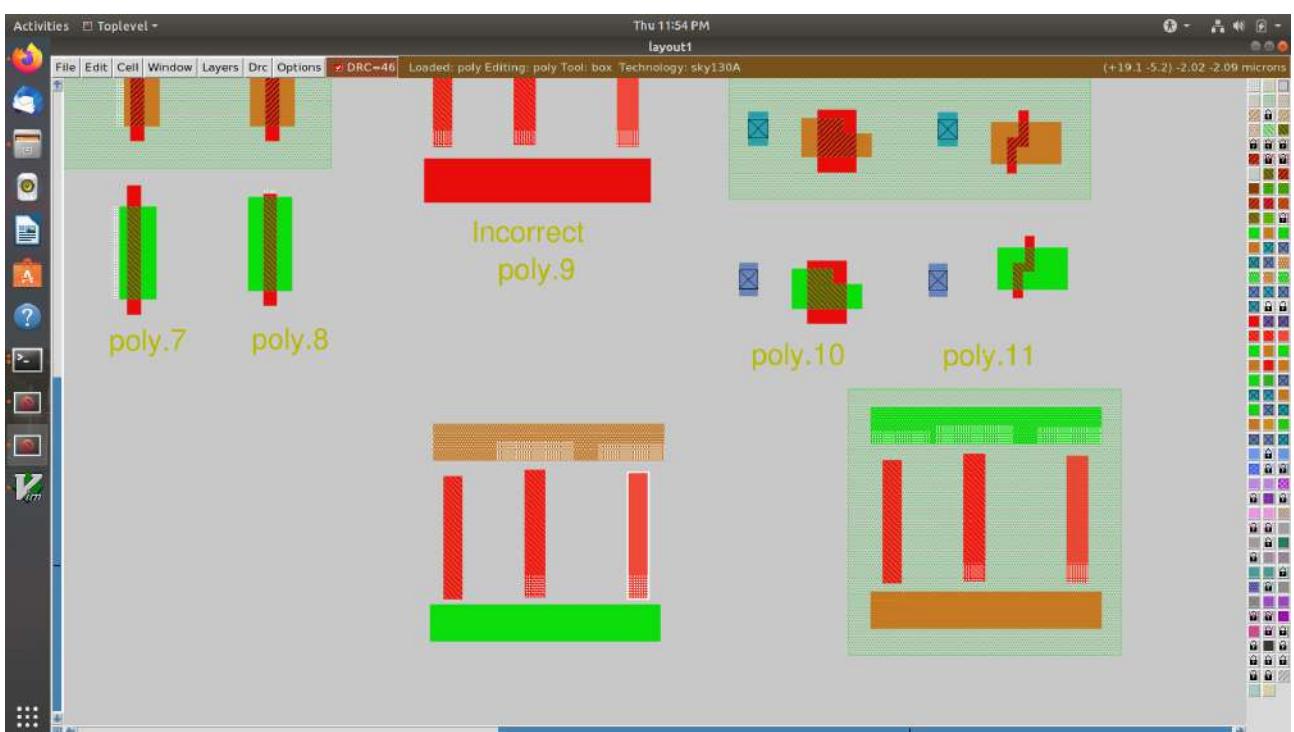
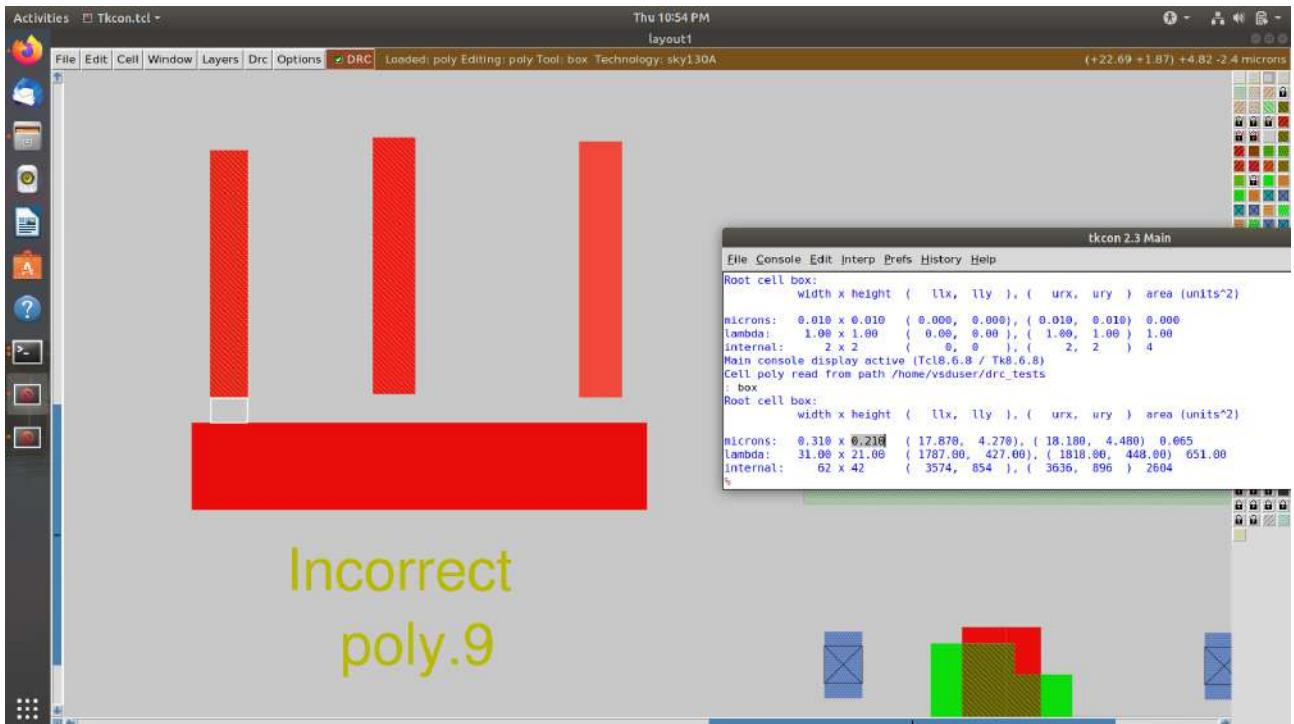
1,1 Top

Incorrectly implemented poly.9 simple rule correction

Screenshot of poly rules

Periphery Rules		Search	google/skywater-pdk
SkyWater SKY130 PDK	(poly.1a)	Width of poly	0.150 μm
Versioning Information	(poly.1b)	Min channel length (poly width) for peft overlapping lvtn (exempt rule for dummy_poly in cells listed on Table H3)	0.350 μm
Current Status	(poly.2)	Spacing of poly to poly except for poly.c2 and poly.c3. Exempt cell: sr_bld_eq where it is same as poly.c2	0.210 μm
Known Issues	(poly.3)	Min poly resistor width	0.330 μm
Design Rules	(poly.4)	Spacing of poly on field to diff (parallel edges only)	P 0.075 μm
PDK Contents	(poly.5)	Spacing of poly on field to tap	P 0.055 μm
Analog Design	(poly.6)	Spacing of poly on diff to abutting tap (min source)	P 0.300 μm
Digital Design	(poly.7)	Extension of diff beyond poly (min drain)	P 0.250
Simulation	(poly.8)	Extension of poly beyond diffusion (endcap)	P 0.130
Physical & Design Verification	(poly.9)	Poly resistor spacing to poly or spacing (no overlap) to diff/tap	0.480 μm
Python API	(poly.10)	Poly can't overlap inner corners of diff	
Previous Nomenclature	(poly.11)	No 90 deg turns of poly on diff	
Glossary	(poly.12)	(Poly NOT (inwell NOT hv)) may not overlap tap: Rule exempted for cell name "g8tge_n_fq2" and gated_rgn and inside UHVL.	P
How to Contribute	(poly.13)	Poly must not overlap diff/rs	
Partners	(poly.14)		
References	(poly.15)		

Incorrectly implemented poly.9 rule no drc violation even though spacing < 0.48μ



New commands inserted in sky130A.tech file to update drc

Activities M GVim Thu 11:58 PM
sky130A.tech (~/.drc_tests) - GVIM

```

4803
4804 variants *
4805
4806 #-----
4807 # POLY
4808 #-----
4809
4810 width allpoly 150 "poly.width < %d (poly.1a)"
4811 spacing allpoly allpoly 210 touching_ok "poly.spacing < %d (poly.2)"
4812 spacing allpolynonfet alldiffvnonfet 75 corner_ok allfets \
    "poly.spacing to Diffusion < %d (poly.4a)"
4813 spacing npres alldiff 480 touching_illegal \
    "poly.resistor spacing to alldiff < %d (poly.9)"
4814 spacing npres allpolynonres 480 touching_illegal \
    "poly.resistor spacing to allpolynonres < %d (poly.9)"
4815 overhang *ndiff,rndiff nfet,scnfet,npd,npass 250 "N-Diffusion overhang of nmos < %d (poly.7)"
4816 overhang *mvndiff,mvrndiff mvnfet,mvnnfet 250 \
    "N-Diffusion overhang of nmos < %d (poly.7)"
4817 overhang *pdifff,rdifff pfet,scpfet,ppu 250 "P-Diffusion overhang of pmos < %d (poly.7)"
4818 overhang *mvpdiff,mvrpdifff mvpfet 250 "P-Diffusion overhang of pmos < %d (poly.7)"
4819 overhang *poly allfets 130 "poly.overhang of transistor < %d (poly.8)"
4820 rect_only allfets "No bends in transistors (poly.11)"
4821 rect_only xhrpoly,uhrpoly "No bends in poly resistors (poly.11)"
4822 extend xpc/a xhrpoly,uhrpoly 2160 \
    "poly.contact extends poly resistor by < %d (lcon.1c + li.5)"
4823
4824 -- VISUAL --
4817,56-63 81%

```

Activities M GVim Thu 11:09 PM
sky130A.tech (~/.drc_tests) - GVIM

```

5168 # xhrpoly (P+ poly resistor)
5169 #-----
5170
5171 width xhrpoly 350 "xhrpoly resistor width < %d (P+ poly.1a)"
5172 # NOTE: xhrpoly resistor requires choice of discrete widths 0.35, 0.69, ... up to 1.27.
5173
5174 #-----
5175 # uhrpoly (P+ poly resistor, 2kOhm/sq)
5176 #-----
5177
5178 width uhrpoly 350 "uhrpoly resistor width < %d"
5179 spacing xhrpoly,uhrpoly,xpc alldiff 480 touching_illegal \
    "xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
5180 spacing xhrpoly,uhrpoly,xpc allpolynonres 480 touching_illegal \
    "xhrpoly/uhrpoly resistor spacing to allpolynonres < %d (poly.9)"
5181
5182
5183
5184
5185 #-----
5186 # MOS Varactor device rules
5187 #-----
5188
5189 overhang *nsd var,varhvt 250 \
    "N-Tap overhang of Varactor < %d (var.4)"
5190
5191
5192 overhang *mvnsd mvvar 250 \
-- VISUAL --
5182,67-74 87%

```

Commands to run in tkcon window

```
# Loading updated tech file
```

```
tech load sky130A.tech
```

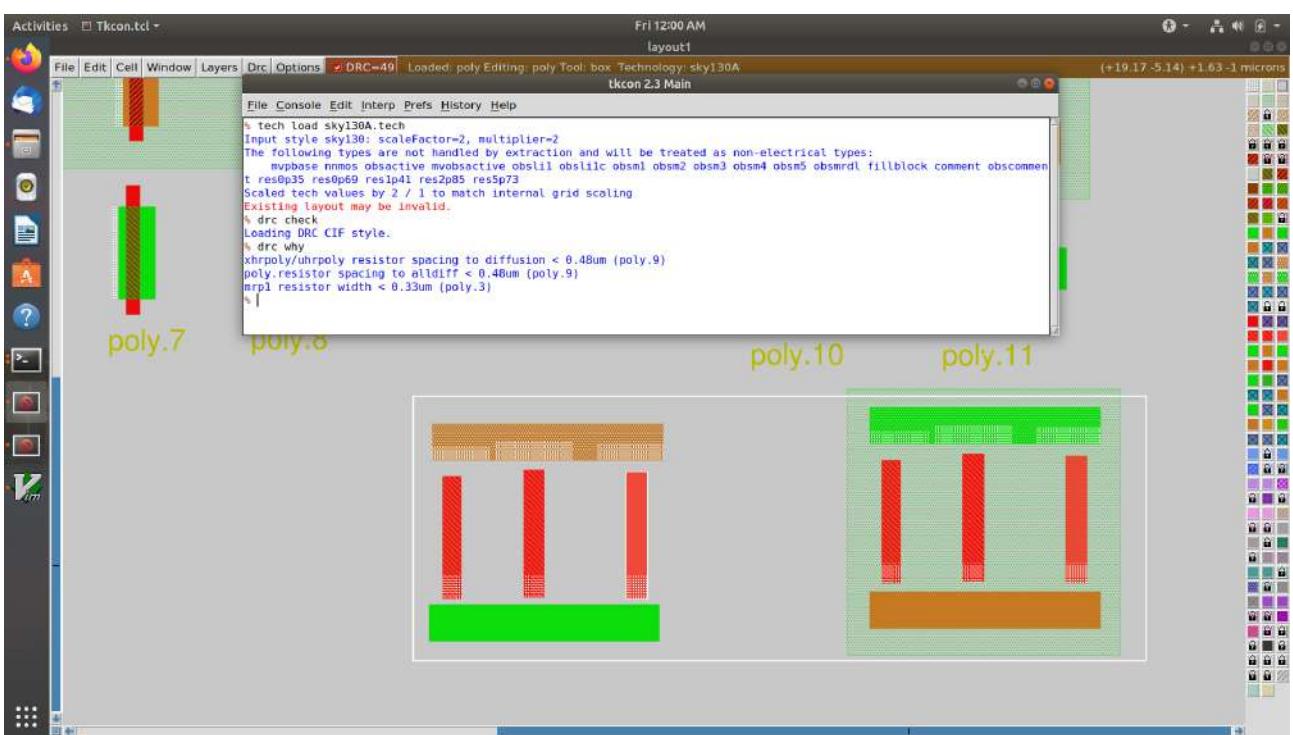
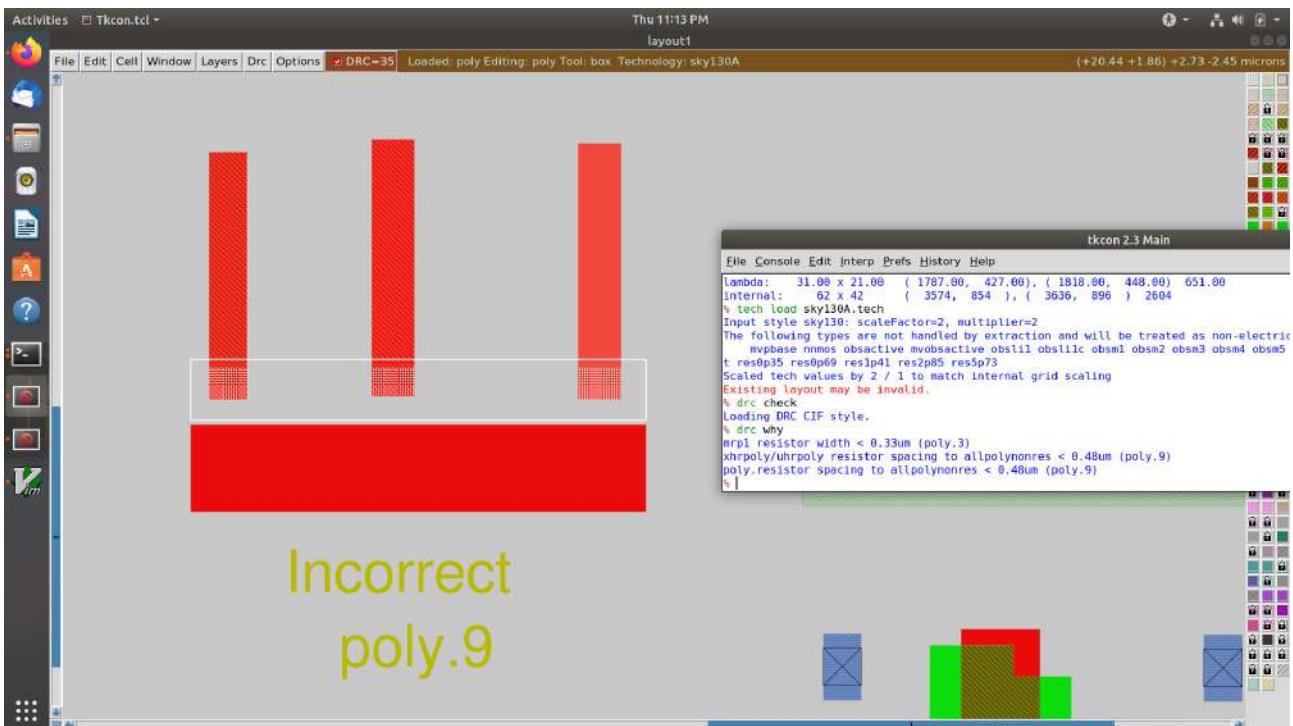
```
# Must re-run drc check to see updated drc errors
```

```
drc check
```

```
# Selecting region displaying the new errors and getting the error messages
```

```
drc why
```

Screenshot of magic window with rule implemented



Incorrectly implemented difftap.2 simple rule correction

Screenshot of difftap rules

Activities Firefox Web Browser Fri 12:14 AM

Editing soc-design-and... yosys-tcl-ui-report/RE... nickson-jose/vsdstdce... Online Clipboard Periphery Rules — Sky... Magic VLSI

<https://skywater-pdk.readthedocs.io/en/main/rules/periphery.html#difftap>

Periphery Rules Search google@skywater-pdk

SkyWater SKY130 PDK

Versioning Information Current Status Known Issues Design Rules PDK Contents Analog Design Digital Design Simulation Physical & Design Verification Python API Previous Nomenclature Glossary How to Contribute Partners References

Name Description Flags Value Unit

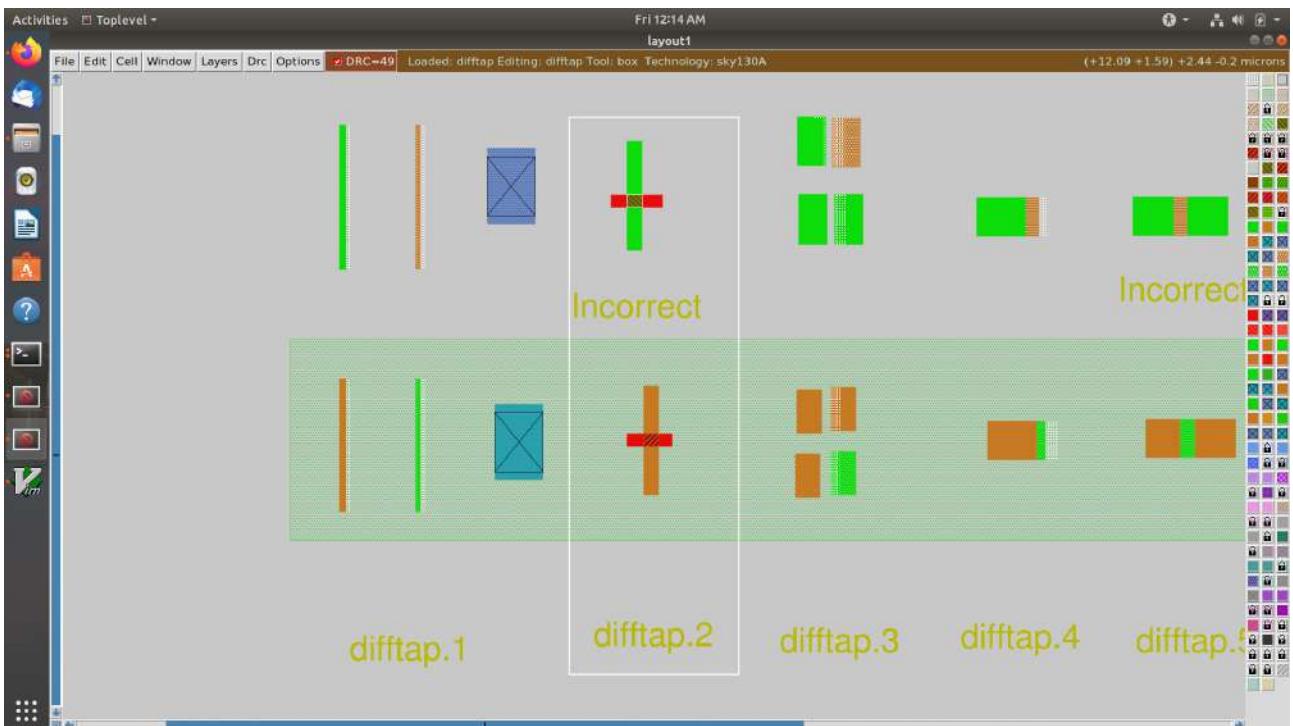
Table 38 Function: Defines active regions and contacts to substrate

Name	Description	Flags	Value	Unit
(difftap.1)	Width of diff or tap	P	0.150	μm
(difftap.2)	Minimum channel width (Diff And Poly) except for FETs inside areaid.sc: Rule exempted in the SP8* flows only, for the cells listed in rule difftap.2a	P	0.420	μm
(difftap.2a)	Minimum channel width (Diff And Poly) for cell names "s8cell_ee_plus_ssein_a", "s8cell_ee_plus_ssein_b", "s8cell_ee_plus_sseip_a", "s8cell_ee_plus_sseip_b", "s8lpls_pl8", "s8lpls_rdrv4", "s8lpls_rdrv4f" and "s8lpls_rdrv8"	P, NA	NA	μm
(difftap.2b)	Minimum channel width (Diff And Poly) for FETs inside areaid.sc	P	0.360	μm
(difftap.3)	Spacing of diff to diff, tap to tap, or non-abutting diff to tap		0.270	μm
(difftap.4)	Min tap bound by one diffusion		0.290	
(difftap.5)	Min tap bound by two diffusions	P	0.400	
(difftap.6)	Diff and tap are not allowed to extend beyond their abutting edge			
(difftap.7)	Spacing of difftap abutting edge to a non-conciding diff or tap edge	NE	0.130	μm
(difftap.8)	Enclosure of (p+) diffusion by N-well. Rule exempted inside UHVI.	DE NE P	0.180	μm
(difftap.9)	Spacing of (n+) diffusion to N-well outside UHVI	DE NE P	0.340	μm
(difftap.10)	Enclosure of (n+) tap by N-well. Rule exempted inside UHVI.	NE P	0.180	μm
Difftap.11	Creation of resistors in N-well. Only recommended inside UHVI	NE P	0.190	μm

Contents

- Periphery Rules (x,-) (dnwell,-) (nwell,-) (pwell,-) (pudem,-) (hvtp,-) (hvtr,-) (lvtn,-) (ncm,-) (difftap,-) (tunn,-) (poly,-) (rpm,-) (varac,-) (photo,-) (npc,-) (n/ psd,-) (licon,-) (li,-) (ct,-) (capm,-) (vpp,-) /m1 -

Incorrectly implemented difftap.2 rule no drc violation even though spacing < 0.42μ



New commands inserted in sky130A.tech file to update drc

```
5178 width uhrpoly 350 "uhrpoly resistor width < %d"
5179 spacing xhrpoly,uhrpoly,xpc alldiff 480 touching_illegal \
      "xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
5180 spacing xhrpoly,uhrpoly,xpc allpolynonres 480 touching_illegal \
      "xhrpoly/uhrpoly resistor spacing to allpolynonres < %d (poly.9)"
5181
5182
5183
5184
5185 #-----
5186 # MOS Varactor device rules
5187 #-----
5188
5189 width pmos 420 \
      "mos transistor formed should have minimum width of < %d (difftap.2)"
5190 width nmos 420 \
      "mos transistor formed should have minimum width of < %d (difftap.2)"
5191
5192
5193 overhang *nsd var,varhvt 250 \
      "N-Tap overhang of Varactor < %d (var.4)"
5194
5195 overhang *mvnsd mvvar 250 \
      "N-Tap overhang of Varactor < %d (var.4)"
5196
5197 width var,varhvt,mvvar 180 "Varactor length < %d (var.1)"
5198 extend var,varhvt,mvvar *poly 1000 "Varactor width < %d (var.2)"
5199
5200
5201
5202
```

-- VISUAL --

5192, 71 88%

Commands to run in tkcon window

```
# Loading updated tech file
```

```
tech load sky130A.tech
```

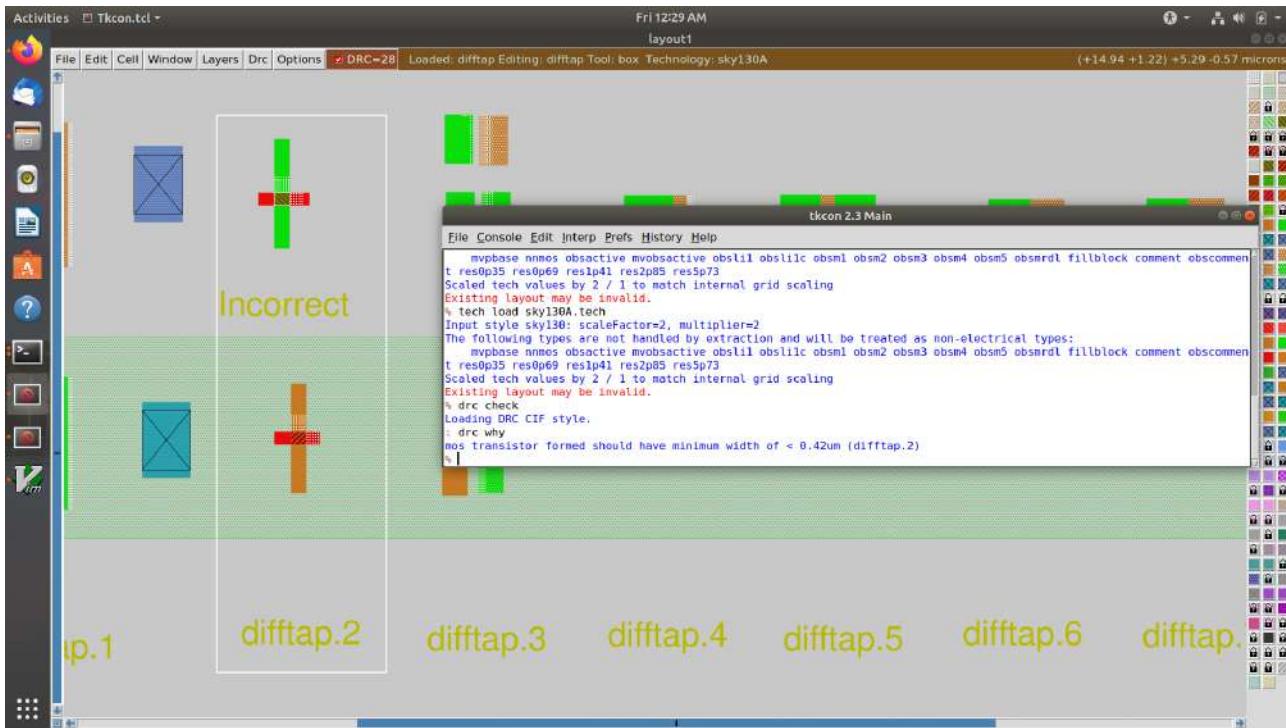
```
# Must re-run drc check to see updated drc errors
```

```
drc check
```

```
# Selecting region displaying the new errors and getting the error messages
```

```
drc why
```

Screenshot of magic window with rule implemented

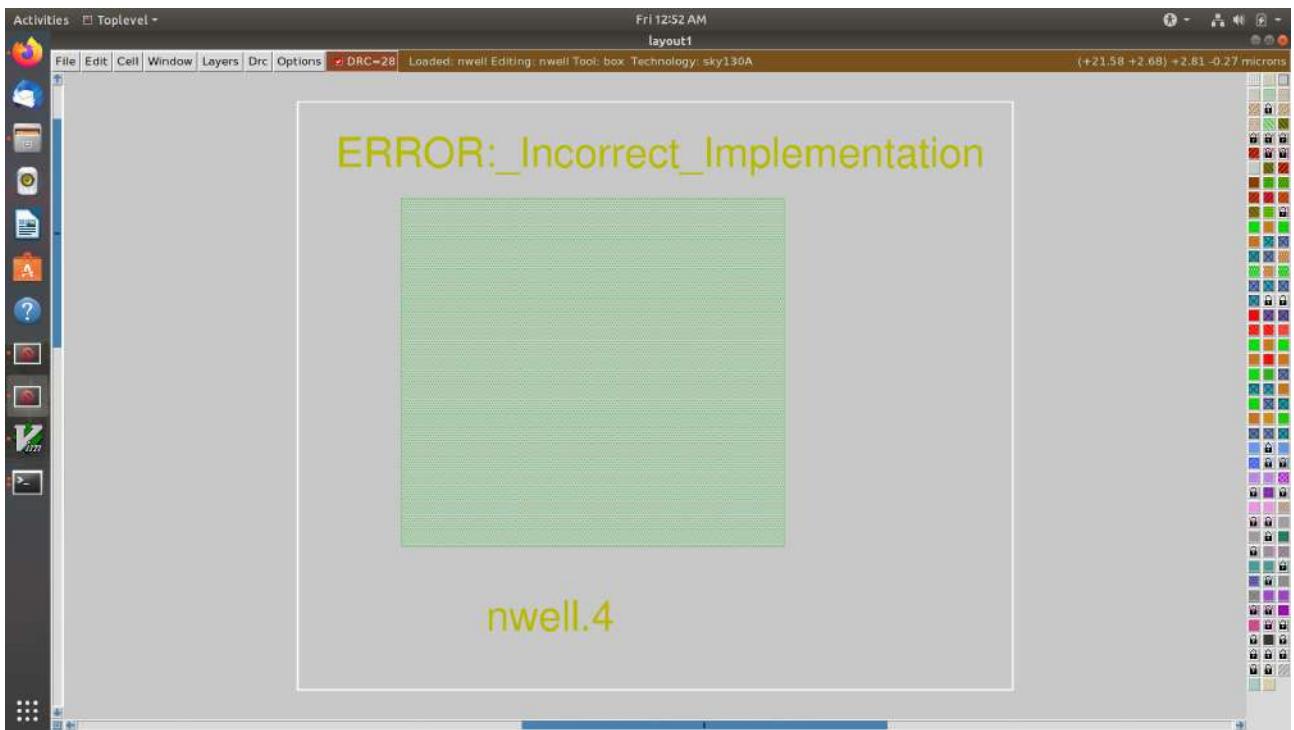


Incorrectly implemented nwell.4 complex rule correction

Screenshot of nwell rules

Name	Description	Flags	Value	Unit
(nwell.1)	Width of nwell		0.840	μm
(nwell.2a)	Spacing between two n-wells		1.270	μm
(nwell.2b)	Manual merge wells if less than minimum			
(nwell.4)	All n-wells will contain metal-contacted tap (rule checks only for icon on top) . Rule exempted from high voltage cells inside UHVI			
(nwell.5)	Deep nwell must be enclosed by nwell by atleast... Exempted inside UHVI or areaid, lw Nwells can merge over deep nwell if spacing too small (as in rule nwell.2)	TC	0.400	μm
(nwell.5a)	min enclosure of nwell by dnwell inside UHVI		N/A	N/A
(nwell.5b)	nwell inside UHVI must not be on the same net as nwell outside UHVI		N/A	N/A
(nwell.6)	Min enclosure of nwell hole by deep nwell outside UHVI	TC	1.030	μm
(nwell.7)	Min spacing between nwell and deep nwell on separate nets Spacing between nwell and deep nwell on the same net is set by the sum of the rules nwell.2 and nwell.5. By default, DRC run on a cell checks for the separate-net spacing, when nwell and deep nwell nets are separate within the cell hierarchy and are joined in the upper hierarchy. To allow net names to be joined and make the same-net rule applicable in this case, the "joinNets" switch should be turned on. waffle_chip	TC	4.500	μm

Incorrectly implemented nwell.4 rule no drc violation even though no tap present in nwell



New commands inserted in sky130A.tech file to update drc

Activities M GVim

Fri 1:03 AM
sky130A.tech (~/.drc_tests) - GVIM

```
File Edit Tools Syntax Buffers Window Help
1230 options calma-permissive-labels
1231
1232 # Ensure nwell overlaps dnwell at least 0.4um outside and 1.03um inside
1233 templayer dnwell_shrink dnwell
1234 shrink 1030
1235
1236 templayer nwell_missing dnwell
1237 grow 400
1238 and-not dnwell_shrink
1239 and-not nwell
1240
1241 templayer nwell_tapped
1242 bloat-all nsc nwell
1243
1244 templayer nwell_untapped nwell
1245 and-not nwell_tapped
1246
1247 # SONOS nFET devices must be in deep nwell
1248 templayer dnwell_missing nsonos
1249 and-not dnwell
1250
1251 # Define MiM cap bottom plate for spacing rule
1252 templayer mim_bottom
1253 bloat-all *mimcap *metal3
1254
-- VISUAL --
```

1245, 22 20%

Activities M GVIM

Fri 1:04 AM
sky130A.tech (~/.drc_tests) - GVIM

```
File Edit Tools Syntax Buffers Window Help
4721 spacing dnwell dnwell 6300 touching_ok "Deep N-well spacing < %d (dnwell.3)"
4722 spacing dnwell allnwell 4500 surround_ok \
4723 "Deep N-well spacing to N-well < %d (nwell.7)"
4724 cifmaxwidth nwell_missing 0 bend_illegal \
4725 "N-well overlap of Deep N-well < 0.4um outside, 1.03um inside (nwell.5a, 7)"
4726 cifmaxwidth dnwell_missing 0 bend_illegal \
4727 "SONOS nFET must be in Deep N-well (tunm.6a)"
4728
4729 #-----
4730 # NWELL
4731 #-----
4732
4733 width allnwell 840 "N-well width < %d (nwell.1)"
4734 spacing allnwell allnwell 1270 touching_ok "N-well spacing < %d (nwell.2a)"
4735
4736 variants (full)
4737 cifmaxwidth nwell_untapped 0 bend_illegal \
4738 "Nwell missing tap (nwell.4)"
4739 variants *
4740
4741 #-----
4742 # DIFF
4743 #-----
@ -- VISUAL --
```

4739, 11 80%

Commands to run in tkcon window

```
# Loading updated tech file
```

```
tech load sky130A.tech
```

```
# Change drc style to drc full
```

```
drc style drc(full)
```

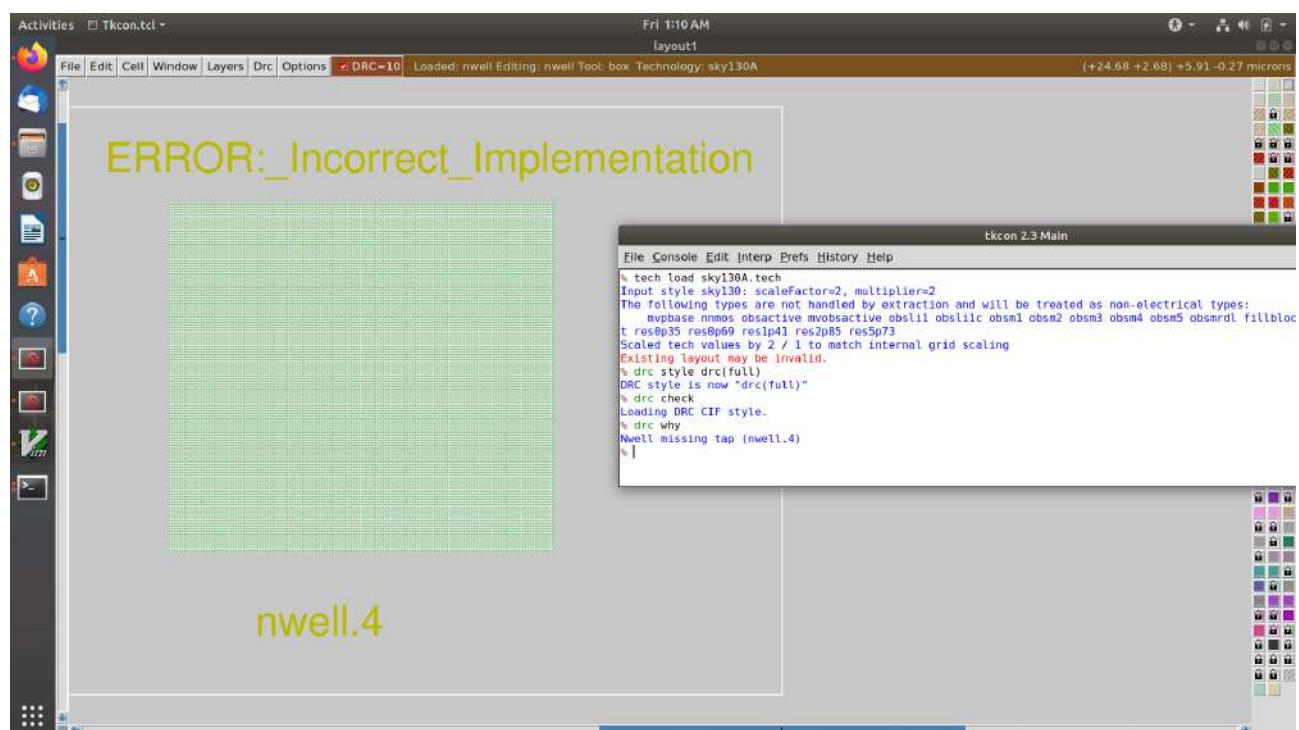
```
# Must re-run drc check to see updated drc errors
```

```
drc check
```

```
# Selecting region displaying the new errors and getting the error messages
```

```
drc why
```

Screenshot of magic window with rule implemented



Section 4 - Pre-layout timing analysis and importance of good clock tree (22/03/2024 - 24/03/2024)

Theory

Implementation

- Section 4 tasks:-
 12. Fix up small DRC errors and verify the design is ready to be inserted into our flow.
 13. Save the finalized layout with custom name and open it.
 14. Generate lef from the layout.
 15. Copy the newly generated lef and associated required lib files to 'picorv32a' design 'src' directory.
 16. Edit 'config.tcl' to change lib file and add the new extra lef into the openlane flow.
 17. Run openlane flow synthesis with newly inserted custom inverter cell.
 18. Remove/reduce the newly introduced violations with the introduction of custom inverter cell by modifying design parameters.
 19. Once synthesis has accepted our custom inverter we can now run floorplan and placement and verify the cell is accepted in PnR flow.
 20. Do Post-Synthesis timing analysis with OpenSTA tool.
 21. Make timing ECO fixes to remove all violations.

22. Replace the old netlist with the new netlist generated after timing ECO fix and implement the floorplan, placement and cts.
 23. Post-CTS OpenROAD timing analysis.
 24. Explore post-CTS OpenROAD timing analysis by removing 'sky130_fd_sc_hd_clkbuf_1' cell from clock buffer list variable 'CTS_CLK_BUFFER_LIST'.
1. Fix up small DRC errors and verify the design is ready to be inserted into our flow.

Conditions to be verified before moving forward with custom designed cell layout:

- Condition 1: The input and output ports of the standard cell should lie on the intersection of the vertical and horizontal tracks.
- Condition 2: Width of the standard cell should be odd multiples of the horizontal track pitch.
- Condition 3: Height of the standard cell should be even multiples of the vertical track pitch.

Commands to open the custom inverter layout

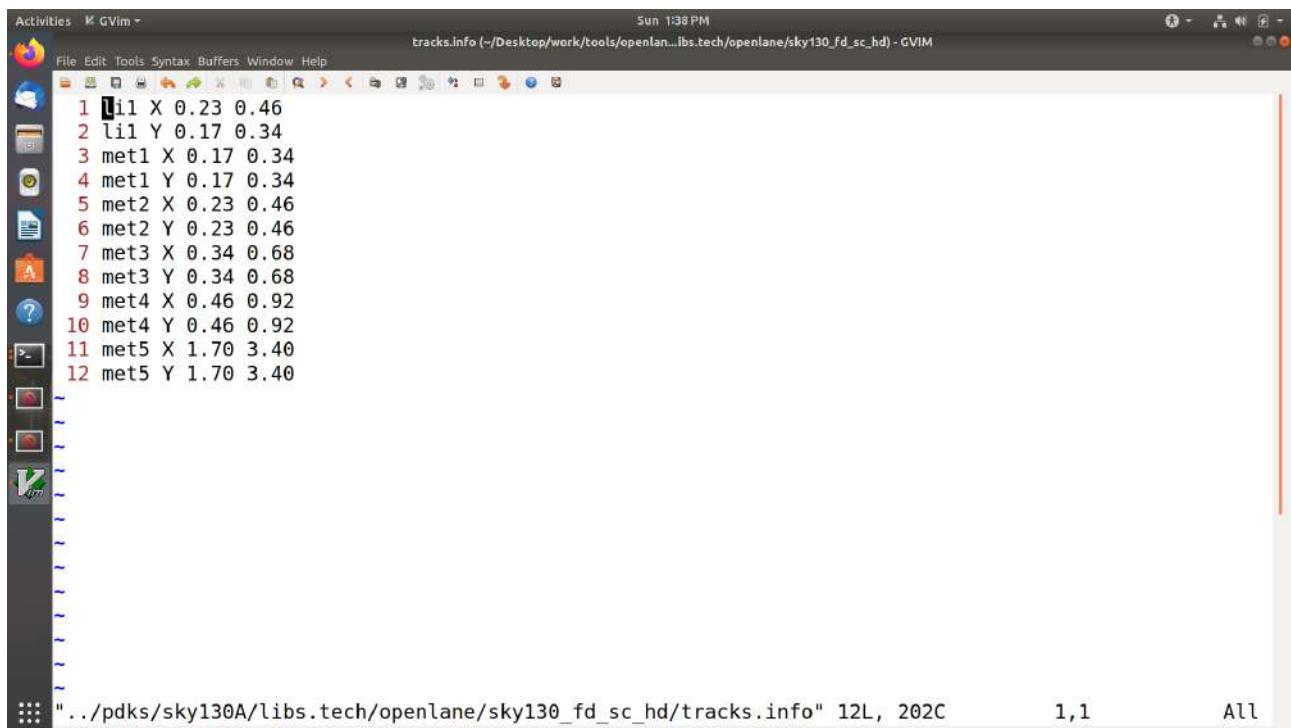
```
# Change directory to vsdstdcelldesign
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
```

```
# Command to open custom inverter layout in magic
```

```
magic -T sky130A.tech sky130_inv.mag &
```

Screenshot of tracks.info of sky130_fd_sc_hd



```
1 l1l X 0.23 0.46
2 l1l Y 0.17 0.34
3 met1 X 0.17 0.34
4 met1 Y 0.17 0.34
5 met2 X 0.23 0.46
6 met2 Y 0.23 0.46
7 met3 X 0.34 0.68
8 met3 Y 0.34 0.68
9 met4 X 0.46 0.92
10 met4 Y 0.46 0.92
11 met5 X 1.70 3.40
12 met5 Y 1.70 3.40
```

Commands for tkcon window to set grid as tracks of locali layer

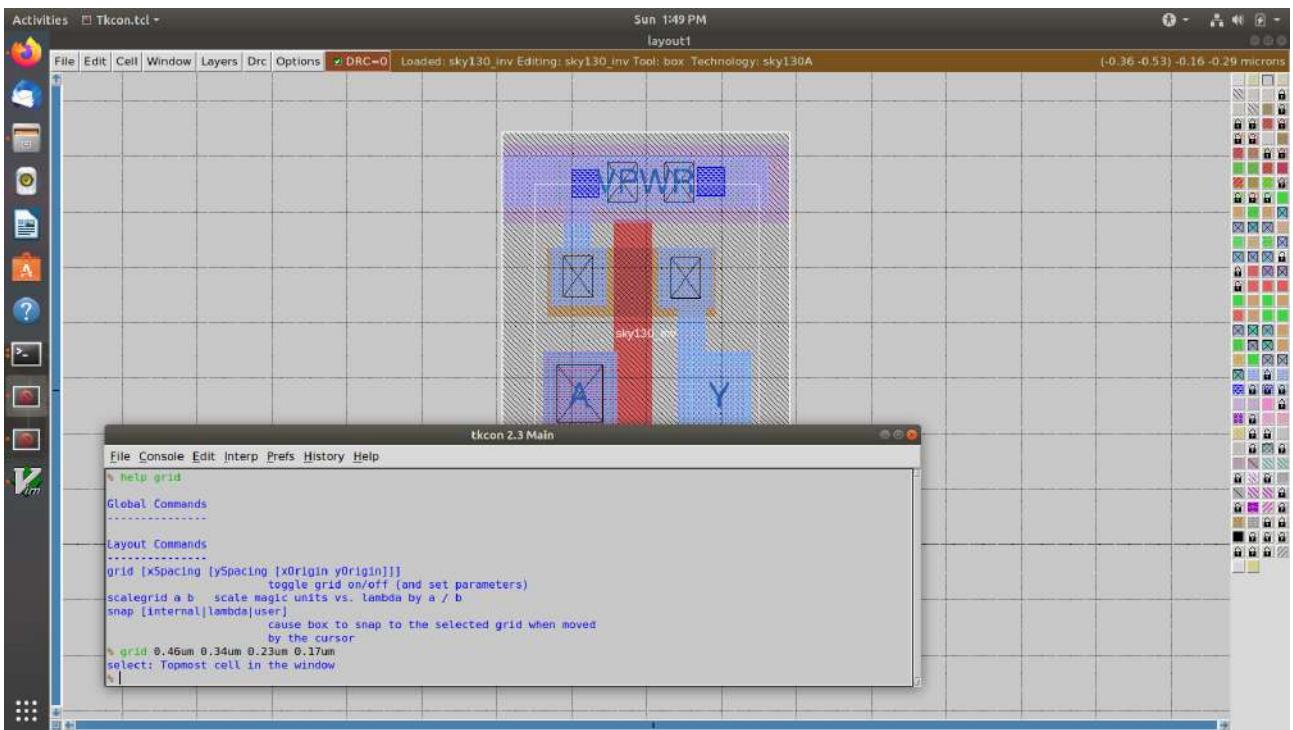
```
# Get syntax for grid command
```

```
help grid
```

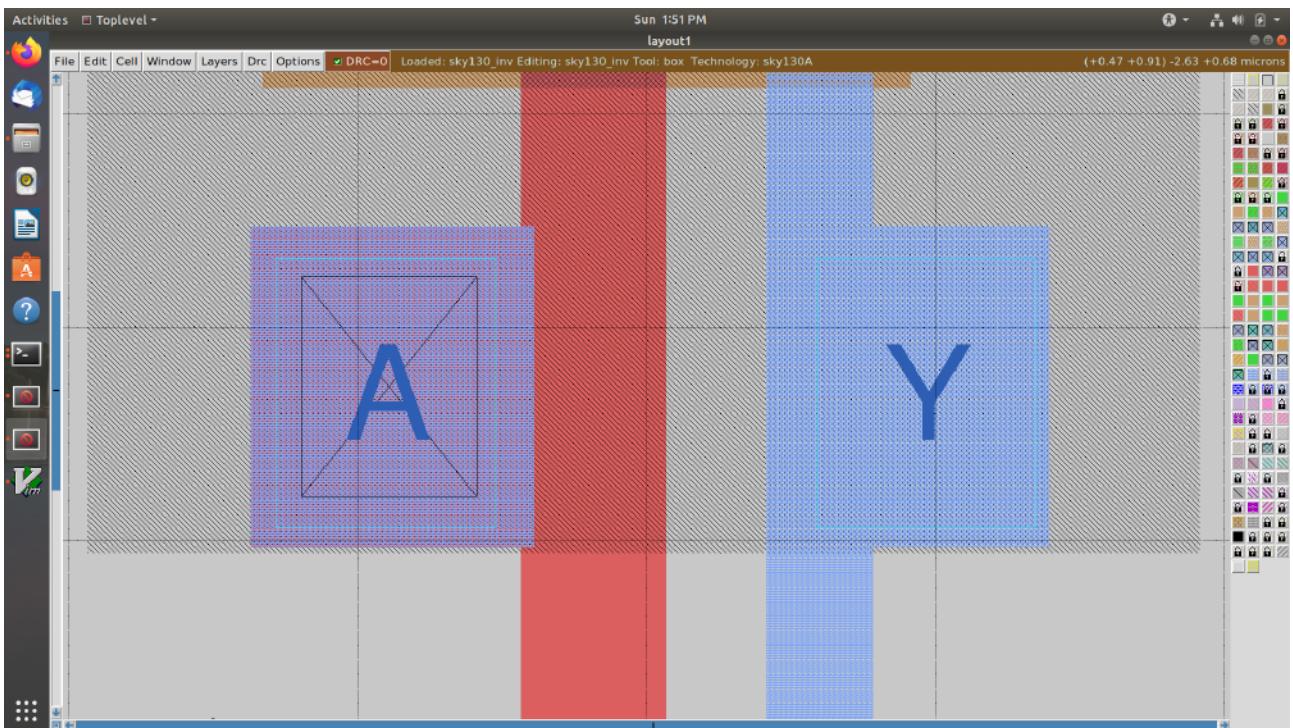
```
# Set grid values accordingly
```

```
grid 0.46um 0.34um 0.23um 0.17um
```

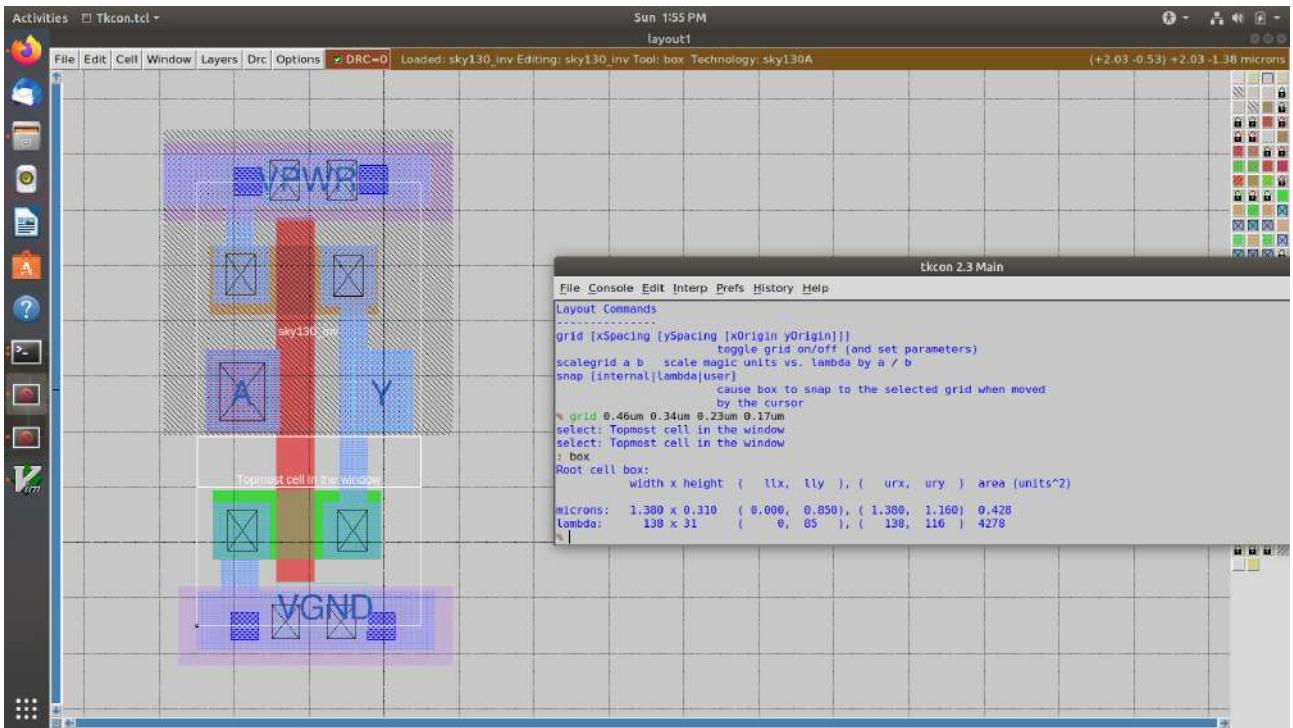
Screenshot of commands run



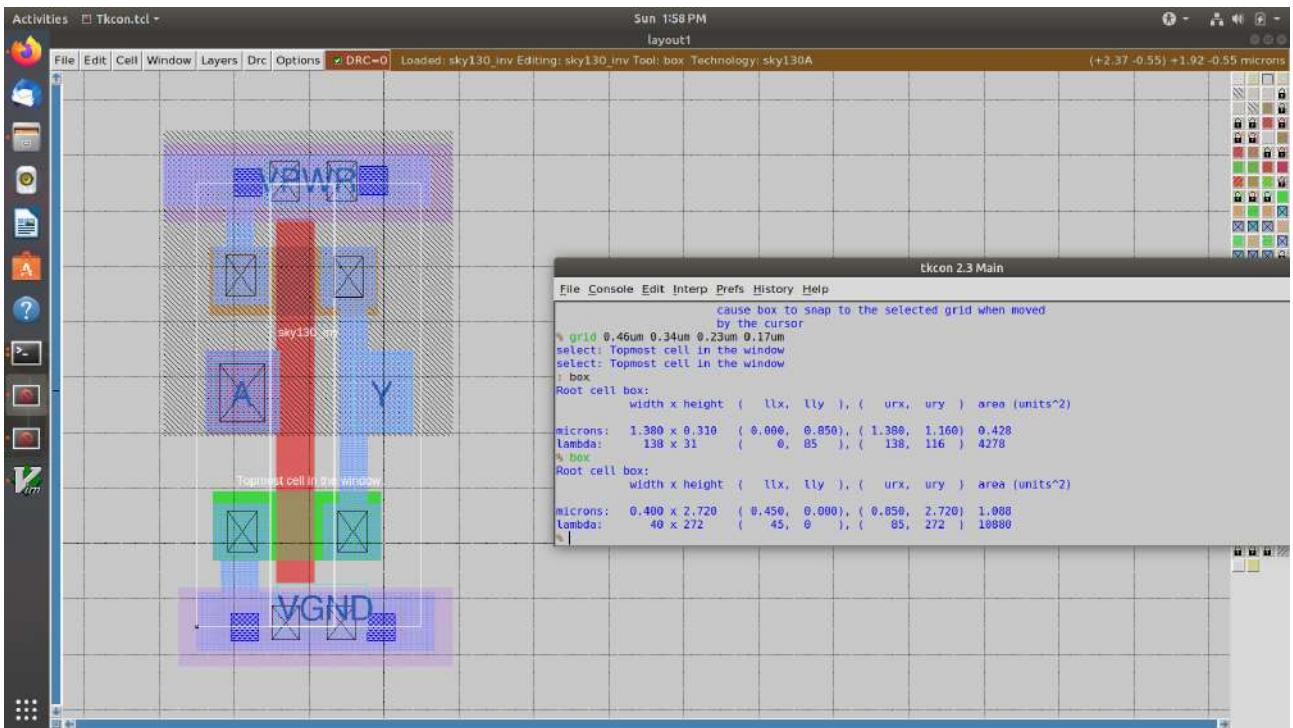
Condition 1 verified



Condition 2 verified



Condition 3 verified



2. Save the finalized layout with custom name and open it.

Command for tkcon window to save the layout with custom name

```
# Command to save as
```

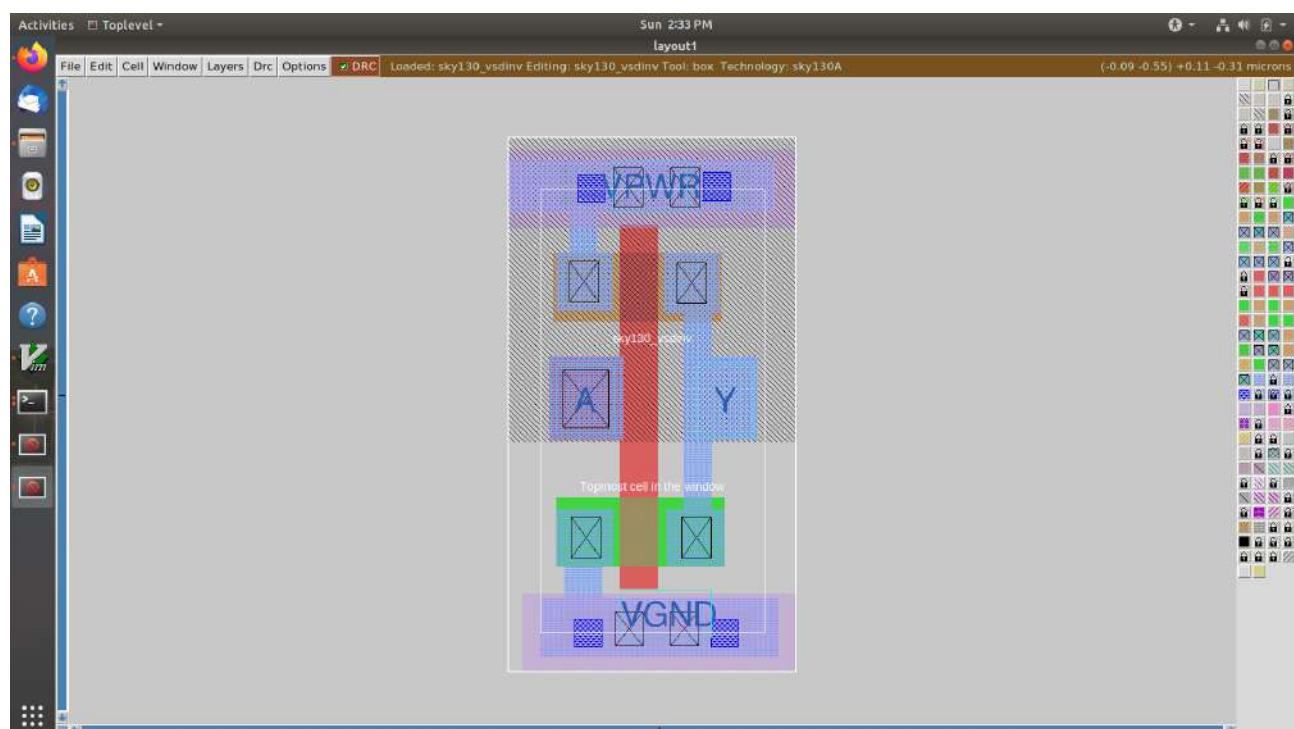
```
save sky130_vsdinv.mag
```

Command to open the newly saved layout

```
# Command to open custom inverter layout in magic
```

```
magic -T sky130A.tech sky130_vsdinv.mag &
```

Screenshot of newly saved layout



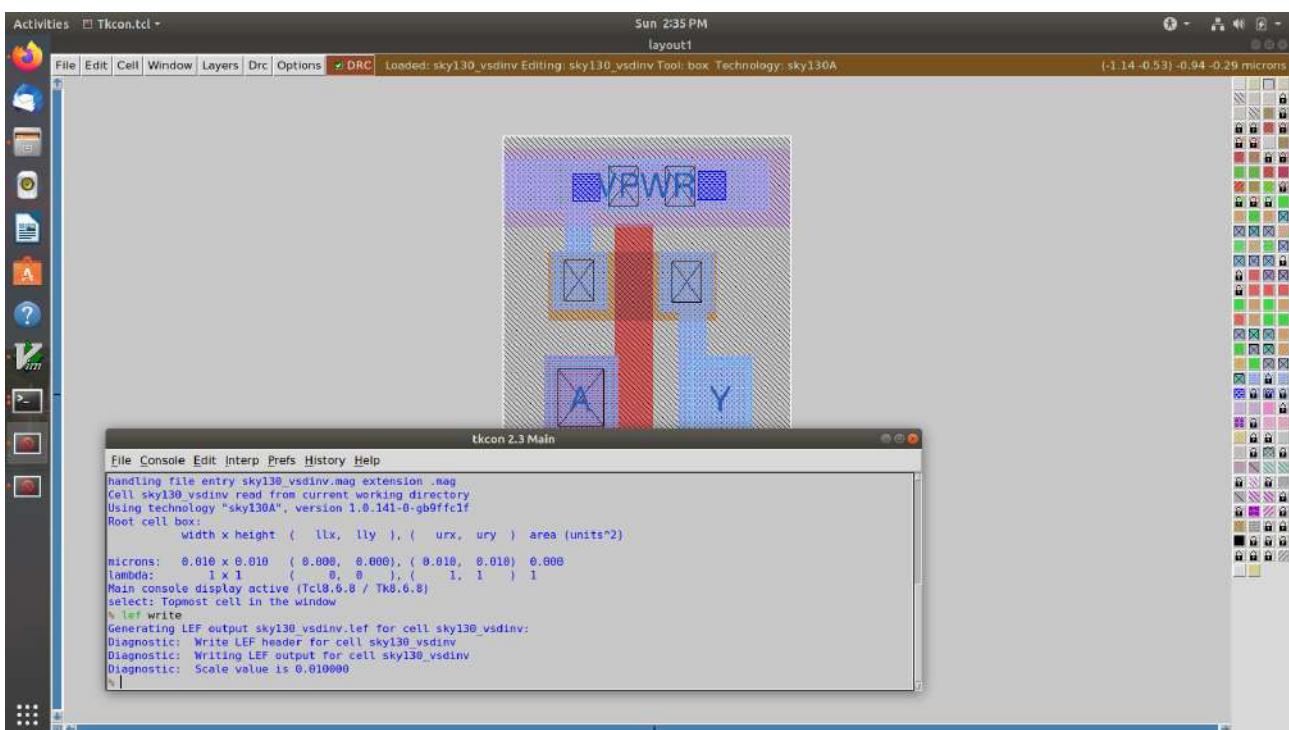
3. Generate lef from the layout.

Command for tkcon window to write lef

```
# lef command
```

```
lef write
```

Screenshot of command run



Screenshot of newly created lef file

The screenshot shows a GVIM window with the title 'sky130_vsdinv.lef (~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a) - GVIM'. The file contains a LEF (Liberty Cell Format) script with the following content:

```
1 VERSION 5.7 ;
2 NOWIREEXTENSIONATPIN ON ;
3 DIVIDERCHAR "/" ;
4 BUSBITCHARS "[]" ;
5 MACRO sky130_vsdinv
6 CLASS CORE ;
7 FOREIGN sky130_vsdinv ;
8 ORIGIN 0.000 0.000 ;
9 SIZE 1.380 BY 2.720 ;
10 SITE unithd ;
11 PIN A
12     DIRECTION INPUT ;
13     USE SIGNAL ;
14     ANTENNAGATEAREA 0.193200 ;
15     PORT
16         LAYER li1 ;
17         RECT 0.060 1.180 0.510 1.690 ;
18     END
19 END A
20 PIN Y
21     DIRECTION OUTPUT ;
22     USE SIGNAL ;
23     ANTENNADIFFAREA 0.336000 ;
24     PORT
25         LAYER li1 ;
```

4. Copy the newly generated lef and associated required lib files to 'picorv32a' design 'src' directory.

Commands to copy necessary files to 'picorv32a' design 'src' directory

```
# Copy lef file
```

```
cp sky130_vsdinv.lef ~/Desktop/work/tools/openlane_working_dir/openlane/designs/
picorv32a/src/
```

```
# List and check whether it's copied
```

```
ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
```

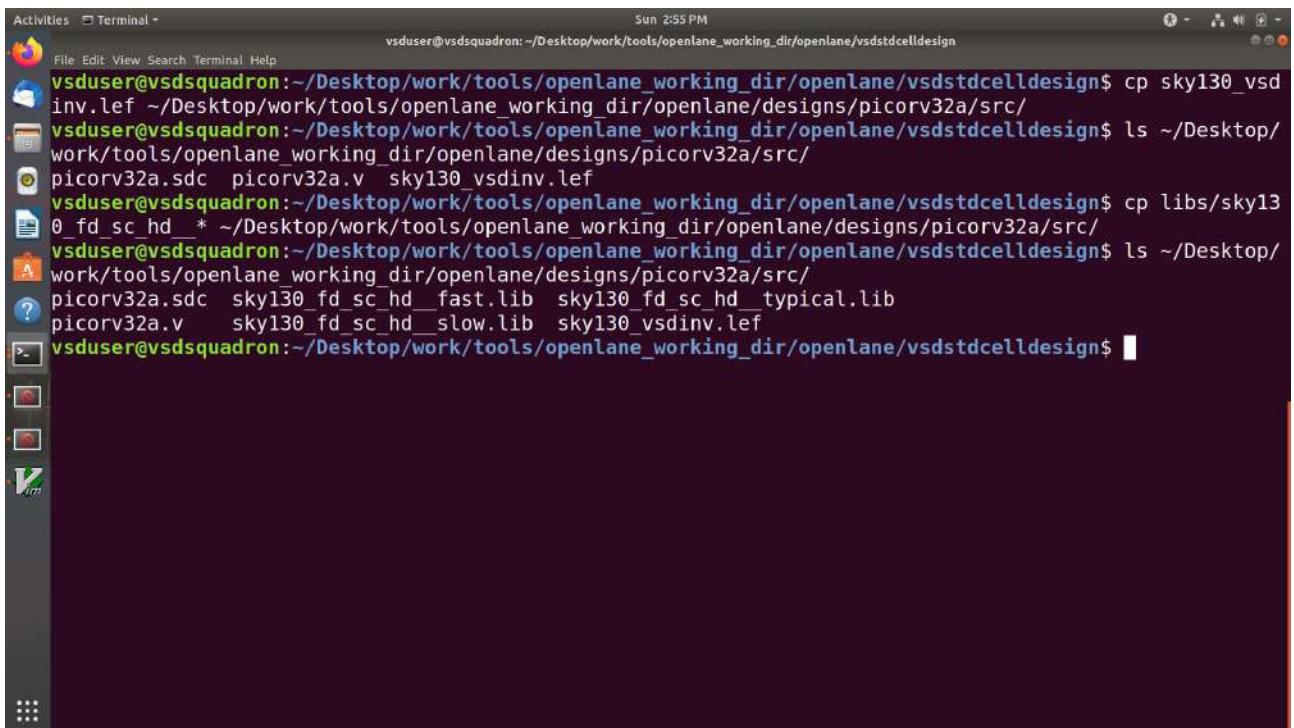
```
# Copy lib files
```

```
cp libs/sky130_fd_sc_hd_* ~/Desktop/work/tools/openlane_working_dir/openlane/designs/
picorv32a/src/
```

```
# List and check whether it's copied
```

```
ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
```

Screenshot of commands run



```
Activities Terminal Sun 2:55 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cp sky130_vsdinv.lef ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
picorv32a.sdc picorv32a.v sky130_vsdinv.lef
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cp libs/sky130_fd_sc_hd_* ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
picorv32a.sdc sky130_fd_sc_hd_fast.lib sky130_fd_sc_hd_typical.lib
picorv32a.v sky130_fd_sc_hd_slow.lib sky130_vsdinv.lef
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```

5. Edit 'config.tcl' to change lib file and add the new extra lef into the openlane flow.

Commands to be added to config.tcl to include our custom cell in the openlane flow

```
set ::env(LIB_SYNTH) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib"

set ::env(LIB_FASTEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib"

set ::env(LIB_SLOWEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib"
```

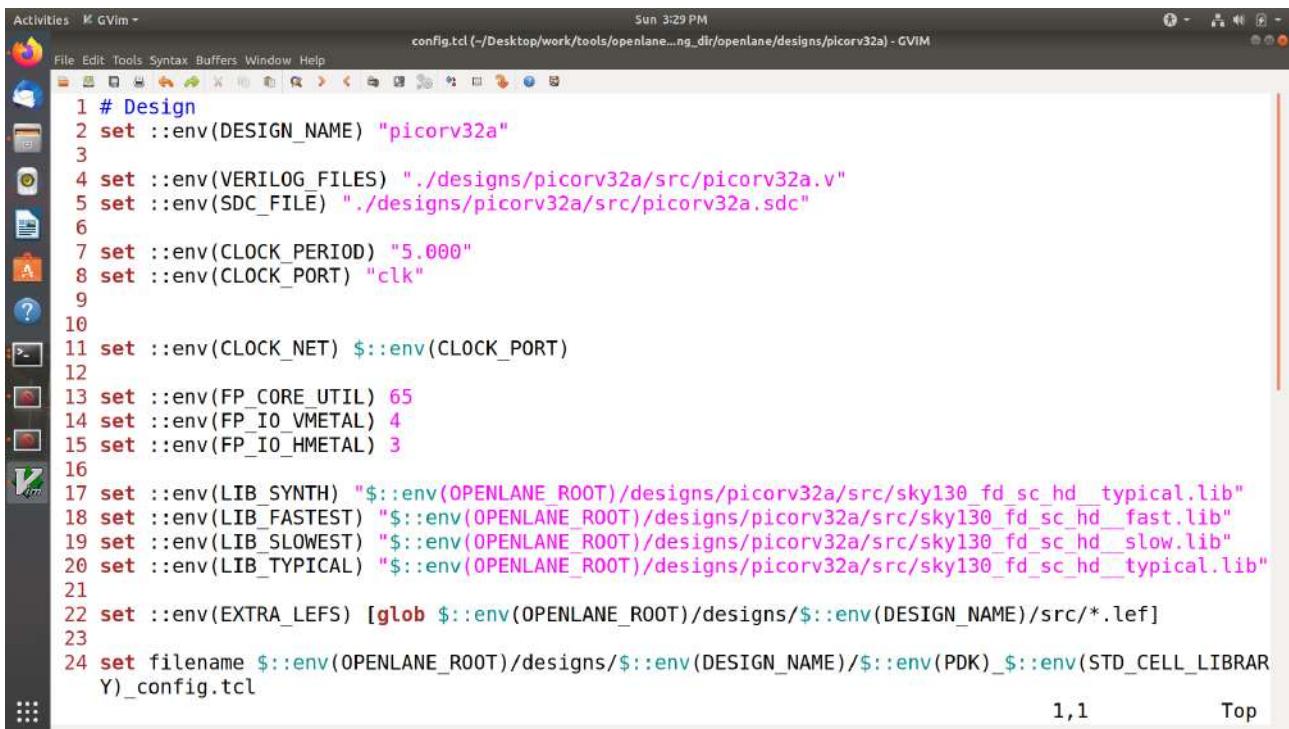
```

set ::env(LIB_TYPICAL) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/
sky130_fd_sc_hd_typical.lib"

set ::env(EXTRA_LEFS) [glob $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/
src/*.lef]

```

Edited config.tcl to include the added lef and change library to ones we added in src directory



```

Activities  M GVIM - Sun 3:29 PM config.tcl (-/Desktop/work/tools/openlane...ng_dir/openlane/designs/picorv32a) - GVIM
File Edit Tools Syntax Buffers Window Help
1 # Design
2 set ::env(DESIGN_NAME) "picorv32a"
3
4 set ::env(VERILOG_FILES) "./designs/picorv32a/src/picorv32a.v"
5 set ::env(SDC_FILE) "./designs/picorv32a/src/picorv32a.sdc"
6
7 set ::env(CLOCK_PERIOD) "5.000"
8 set ::env(CLOCK_PORT) "clk"
9
10
11 set ::env(CLOCK_NET) $::env(CLOCK_PORT)
12
13 set ::env(FP_CORE_UTIL) 65
14 set ::env(FP_IO_VMETAL) 4
15 set ::env(FP_IO_HMETAL) 3
16
17 set ::env(LIB_SYNTH) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib"
18 set ::env(LIB_FASTEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib"
19 set ::env(LIB_SLOWEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib"
20 set ::env(LIB_TYPICAL) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib"
21
22 set ::env(EXTRA_LEFS) [glob $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/src/*.lef]
23
24 set filename $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/$::env(PDK)_$::env(STD_CELL_LIBRARY)_config.tcl
1,1 Top

```

6. Run openlane flow synthesis with newly inserted custom inverter cell.

Commands to invoke the OpenLANE flow include new lef and perform synthesis

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:v0.21'
```

```
# Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command
```

```
docker
```

```
# Now that we have entered the OpenLANE flow contained docker sub-system we can invoke the OpenLANE flow in the Interactive mode using the following command
```

```
./flow.tcl -interactive
```

```
# Now that OpenLANE flow is open we have to input the required packages for proper functionality of the OpenLANE flow
```

```
package require openlane 0.9
```

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the design creating some necessary files and directories for running a specific design which in our case is 'picorv32a'
```

```
prep -design picorv32a
```

```
# Additional commands to include newly added lef to openlane flow
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

Now that the design is prepped and ready, we can run synthesis using following command

`run_synthesis`

Screenshots of commands run

Activities Terminal Sun 3:36 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
vsduser@vsdsquadron:~$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ docker
bash-4.2$ ./flow.tcl -interactive
[INFO]:

[INFO]: Version: v0.21
[INFO]: Running interactively
% package require openlane 0.9
% prep -design picorv32a
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
```

Activities Terminal Sun 3:37 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
? sky130_fd_sc_hd.lef: SITEs matched found: 0
? sky130_fd_sc_hd.lef: MACROs matched found: 437
? sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
? sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
? sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
? sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
? sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
? sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
```

```
Activities Terminal - Sun 3:37 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
::: % run_synthesis
```

```
Activities Terminal - Sun 3:45 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
::: %
```

7. Remove/reduce the newly introduced violations with the introduction of custom inverter cell by modifying design parameters.

Noting down current design values generated before modifying parameters to improve timing

```

Activities Terminal - Sun 4:00 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
sky130_fd_sc_hd_o31la_2 8
sky130_fd_sc_hd_o31a_2 19
sky130_fd_sc_hd_o31ai_2 1
sky130_fd_sc_hd_o32a_2 109
sky130_fd_sc_hd_o41a_2 2
sky130_fd_sc_hd_or2_2 1088
sky130_fd_sc_hd_or2b_2 25
sky130_fd_sc_hd_or3_2 68
sky130_fd_sc_hd_or3b_2 5
sky130_fd_sc_hd_or4_2 93
sky130_fd_sc_hd_or4b_2 6
sky130_fd_sc_hd_or4bb_2 2
sky130_vsdinv 1554

Chip area for module '\picorv32a': 147712.918400

29. Executing Verilog backend.
Dumping module '\picorv32a'.

Warnings: 307 unique messages, 307 total
End of script. Logfile hash: ea6f91c309, CPU: user 11.69s system 3.17s, MEM: 95.95 MB peak
Yosys 0.9+3621 (git sha1 84e9fa7, gcc 8.3.1 -fPIC -Os)
Time spent: 57% 2x abc (18 sec), 12% 33x opt_expr (4 sec), ...
[INFO]: Changing netlist from 0 to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis
/picorv32a.synthesis.v
[INFO]: Running Static Timing Analysis...
[INFO]: current step index: 2
OpenSTA 2.2.0-28b40207a8 Copyright (c) 2019, Parallever Software, Inc.

```

```

Activities Terminal - Sun 4:13 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.9460000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.9460000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
[INFO]: % 

```

Commands to view and change parameters to improve timing and run synthesis

Now once again we have to prep design so as to update variables

prep -design picorv32a -tag 24-03_10-03 -overwrite

```
# Addiitional commands to include newly added lef to openlane flow merged.lef
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to display current value of variable SYNTH_STRATEGY
```

```
echo $::env(SYNTH_STRATEGY)
```

```
# Command to set new value for SYNTH_STRATEGY
```

```
set ::env(SYNTH_STRATEGY) "DELAY 3"
```

```
# Command to display current value of variable SYNTH_BUFFERING to check whether it's  
enabled
```

```
echo $::env(SYNTH_BUFFERING)
```

```
# Command to display current value of variable SYNTH_SIZING
```

```
echo $::env(SYNTH_SIZING)
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Command to display current value of variable SYNTH_DRIVING_CELL to check whether it's the proper cell or not
```

```
echo $::env(SYNTH_DRIVING_CELL)
```

```
# Now that the design is prepped and ready, we can run synthesis using following command
```

```
run_synthesis
```

Screenshot of merged.lef in tmp directory with our custom inverter as macro

```
68236 MACRO Sky130_vsdinv
68237   CLASS CORE ;
68238   FOREIGN sky130_vsdinv ;
68239   ORIGIN 0.000 0.000 ;
68240   SIZE 1.380 BY 2.720 ;
68241   SITE unithd ;
68242   PIN A
68243     DIRECTION INPUT ;
68244     USE SIGNAL ;
68245     ANTENNAGATEAREA 0.193200 ;
68246     PORT
68247       LAYER l1l ;
68248       RECT 0.060 1.180 0.510 1.690 ;
68249     END
68250   END A
68251   PIN Y
68252     DIRECTION OUTPUT ;
68253     USE SIGNAL ;
68254     ANTENNADIFFAREA 0.336000 ;
68255     PORT
68256       LAYER l1l ;
68257       RECT 0.760 1.960 1.100 2.330 ;
68258       RECT 0.880 1.690 1.050 1.960 ;
68259       RECT 0.880 1.180 1.330 1.690 ;
68260       RECT 0.880 0.760 1.050 1.180 ;
```

Screenshots of commands run

```
Activities Terminal Sun 5:09 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% prep -design picorv32a -tag 24-03_10-03 -overwrite
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[WARNING]: Removing existing run /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
::: mergeLef.py : Merging LEFs
::: mergeLef.py : Merging LEFs
```

```
Activities Terminal Sun 5:09 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add lefs -src $lefs
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% echo $::env(SYNTH_STRATEGY)
AREA 0
% set ::env(SYNTH_STRATEGY) "DELAY 3"
DELAY 3
% echo $::env(SYNTH_BUFFERING)
1
% echo $::env(SYNTH_SIZING)
0
% set ::env(SYNTH_SIZING) 1
1
% echo $::env(SYNTH_DRIVING_CELL)
sky130_fd_sc_hd_inv_8
::: % run_synthesis
```

```
Activities Terminal - Sun 5:10 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
::: %
```

Comparing to previously noted run values area has increased and worst negative slack has become 0

```

Activities Terminal - Sun 5:11 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
sky130_fd_sc_hd_o32a_2 9
sky130_fd_sc_hd_o32ai_2 3
sky130_fd_sc_hd_o41ai_2 18
sky130_fd_sc_hd_or2_2 80
sky130_fd_sc_hd_or2b_2 264
sky130_fd_sc_hd_or3_2 6
sky130_fd_sc_hd_or3b_2 5
sky130_fd_sc_hd_or4_2 68
sky130_fd_sc_hd_or4b_2 4
sky130_fd_sc_hd_xnor2_2 700
sky130_fd_sc_hd_xor2_2 1164
sky130_vsdinv 1434

Chip area for module '\picorv32a': 181730.544000

29. Executing Verilog backend.
Dumping module '\picorv32a'.

Warnings: 307 unique messages, 307 total
End of script. Logfile hash: befd735e75, CPU: user 12.56s system 2.87s, MEM: 97.45 MB peak
Yosys 0.9+3621 (git sha1 84e9fa7, gcc 8.3.1 -fPIC -Os)
Time spent: 64% 2x abc (26 sec), 10% 33x opt_expr (4 sec), ...
[INFO]: Changing netlist from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis.v to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis.v
[INFO]: Running Static Timing Analysis...
[INFO]: current step index: 11
OpenSTA 2.2.0-28b10207a8 Copyright (c) 2019, Parallever Software, Inc.

```

```

Activities Terminal - Sun 5:11 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk $all_inputs_wo_clk

# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
[INFO]: % 

```

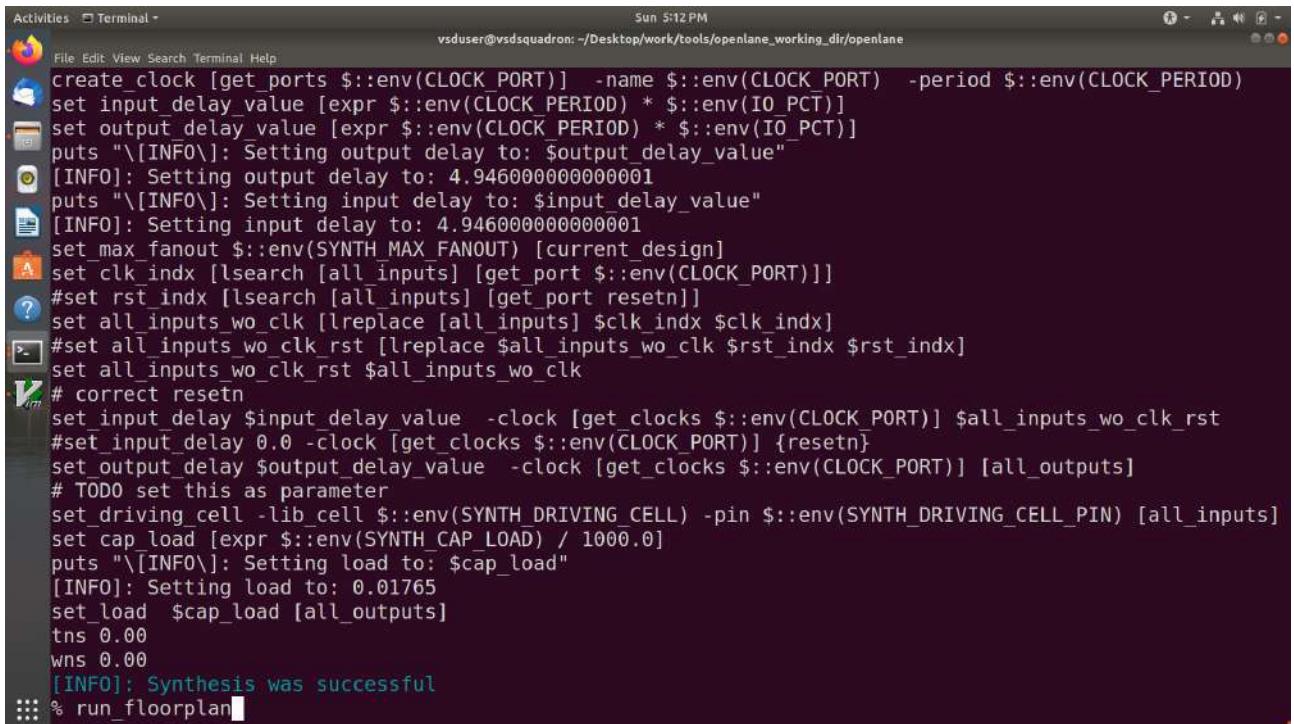
8. Once synthesis has accepted our custom inverter we can now run floorplan and placement and verify the cell is accepted in PnR flow.

Now that our custom inverter is properly accepted in synthesis we can now run floorplan using following command

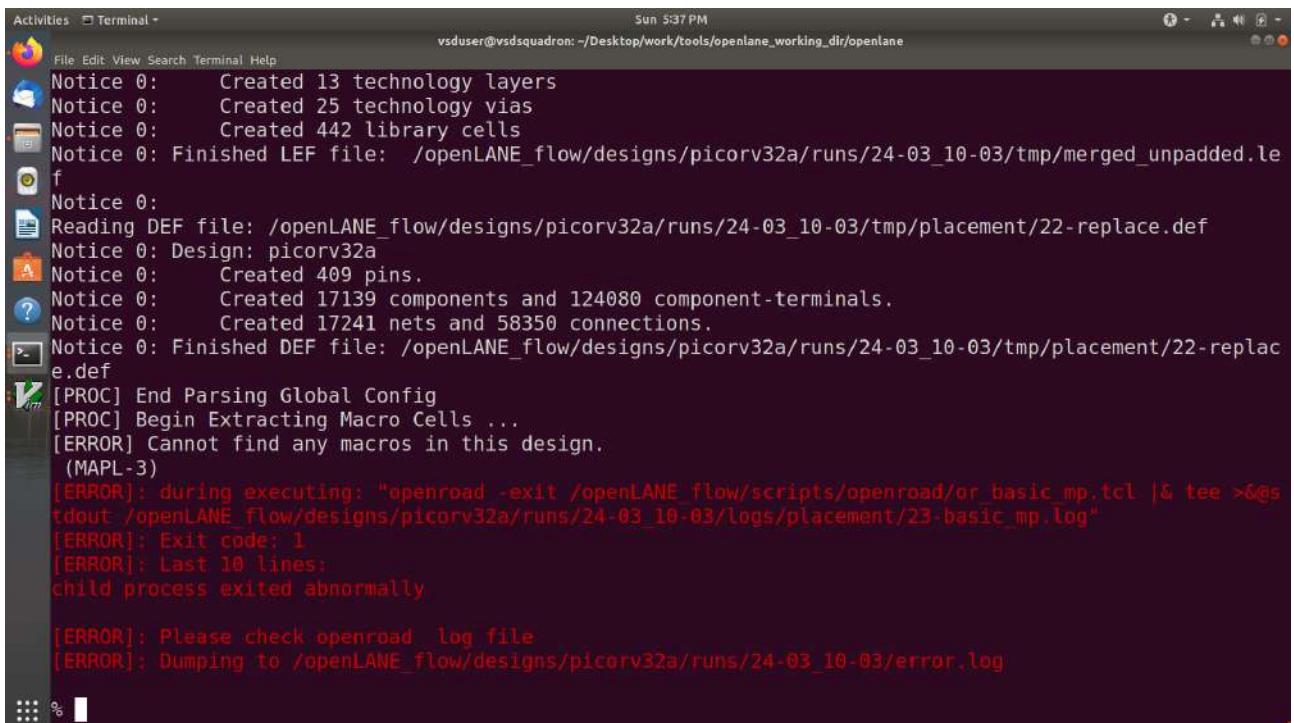
Now we can run floorplan

run_floorplan

Screenshots of command run



```
Activities Terminal Sun 5:12 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
:: % run_floorplan
```



```
Activities Terminal Sun 5:37 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/22-replace.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/22-replace.def
[PROC] End Parsing Global Config
[PROC] Begin Extracting Macro Cells ...
[ERROR] Cannot find any macros in this design.
(MAPL-3)
[ERROR]: during executing: "openroad -exit /openLANE_flow/scripts/openroad/or_basic_mp.tcl |& tee >& stdout /openLANE_flow/designs/picorv32a/runs/24-03_10-03/logs/placement/23-basic_mp.log"
[ERROR]: Exit code: 1
[ERROR]: Last 10 lines:
child process exited abnormally

[ERROR]: Please check openroad log file
[ERROR]: Dumping to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/error.log
:: %
```

Since we are facing unexpected un-explainable error while using run_floorplan command, we can instead use the following set of commands available based on information from Desktop/work/tools/openlane_working_dir/openlane/scripts/tcl_commands/floorplan.tcl and also based on Floorplan Commands section in Desktop/work/tools/openlane_working_dir/openlane/docs/source/OpenLANE_commands.md

Following commands are altogether sourced in "run_floorplan" command

init_floorplan

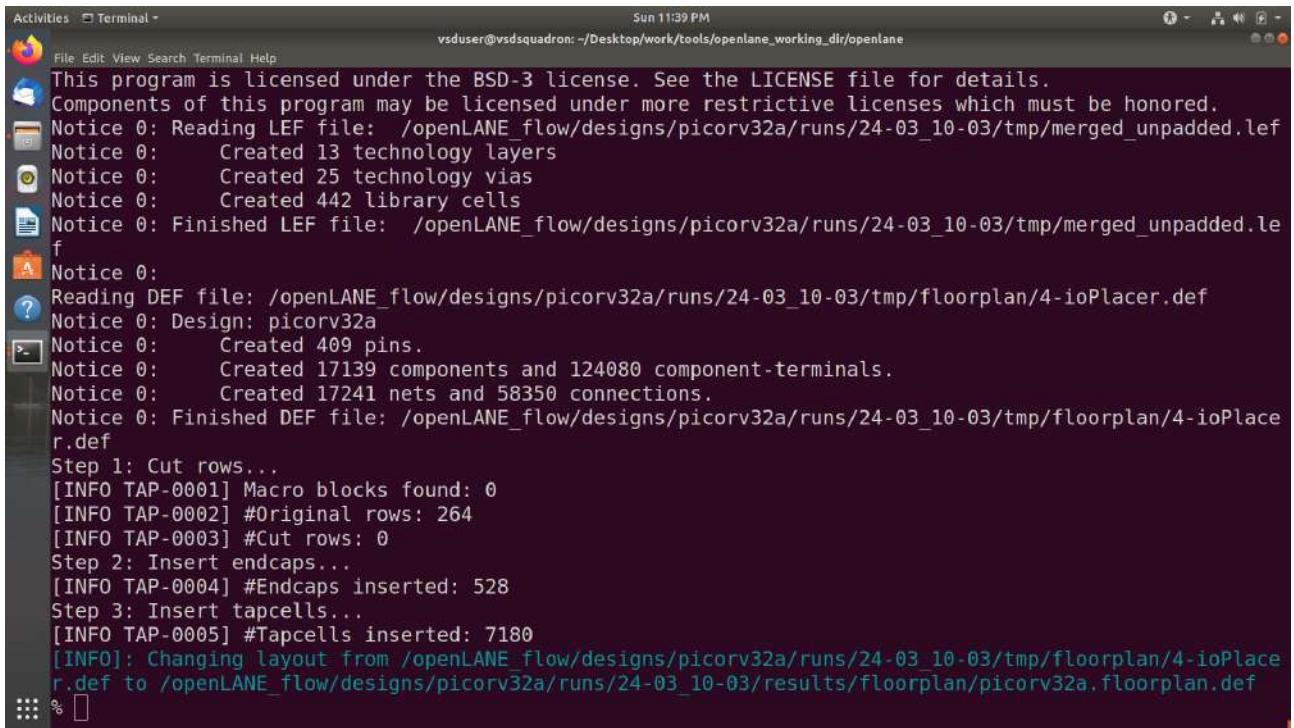
place_io

tap_decap_or

Screenshots of commands run

```
Activities Terminal Sun 11:38 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
% init_floorplan
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 3
OpenROAD 0.9.0 1415572a73
A This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
[INFO IFP-0001] Added 264 rows of 1566 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 731.615 742.335 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/3-verilog2def.die_area.rpt.
[INFO] Floorplanned on a core area of 5.52 10.88 725.88 728.96 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/3-verilog2def.core_area.rpt.
[INFO]: Core area width: 720.36
[INFO]: Core area height: 718.08
[INFO]: Changing layout from 0 to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def
::: % place_io
```

```
Activities Terminal Sun 11:38 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% place_io
[INFO]: Running IO Placement...
[INFO]: current step index: 4
OpenROAD 0.9.0 1415572a73
A This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def
#Macro blocks found: 0
Using 5u default boundaries offset
Random pin placement
RandomMode Even
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
::: % tap_decap_or
```



```
Sun 11:39 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

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Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 17139 components and 124080 component-terminals.
Notice 0:     Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Step 1: Cut rows...
[INFO TAP-0001] Macro blocks found: 0
[INFO TAP-0002] #Original rows: 264
[INFO TAP-0003] #Cut rows: 0
Step 2: Insert endcaps...
[INFO TAP-0004] #Endcaps inserted: 528
Step 3: Insert tapcells...
[INFO TAP-0005] #Tapcells inserted: 7180
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/floorplan/picorv32a.floorplan.def
```

Now that floorplan is done we can do placement using following command

Now we are ready to run placement

run_placement

Screenshots of command run

```
Activities Terminal Sun 11:49 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 17139 components and 124080 component-terminals.
Notice 0:     Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Step 1: Cut rows...
[INFO TAP-0001] Macro blocks found: 0
[INFO TAP-0002] #Original rows: 264
[INFO TAP-0003] #Cut rows: 0
Step 2: Insert endcaps...
[INFO TAP-0004] #Endcaps inserted: 528
Step 3: Insert tapcells...
[INFO TAP-0005] #Tapcells inserted: 7180
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/floorplan/picorv32a.floorplan.def
::: % run_placement
```

```
Activities Terminal Sun 11:51 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
legalized HPWL      910806.5 u
delta HPWL          2 %

[INFO DPL-0020] Mirrored 6650 instances
[INFO DPL-0021] HPWL before      910806.5 u
[INFO DPL-0022] HPWL after       895297.0 u
[INFO DPL-0023] HPWL delta       -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/6-resizer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 10
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
::: %
```

Commands to load placement def in magic in another terminal

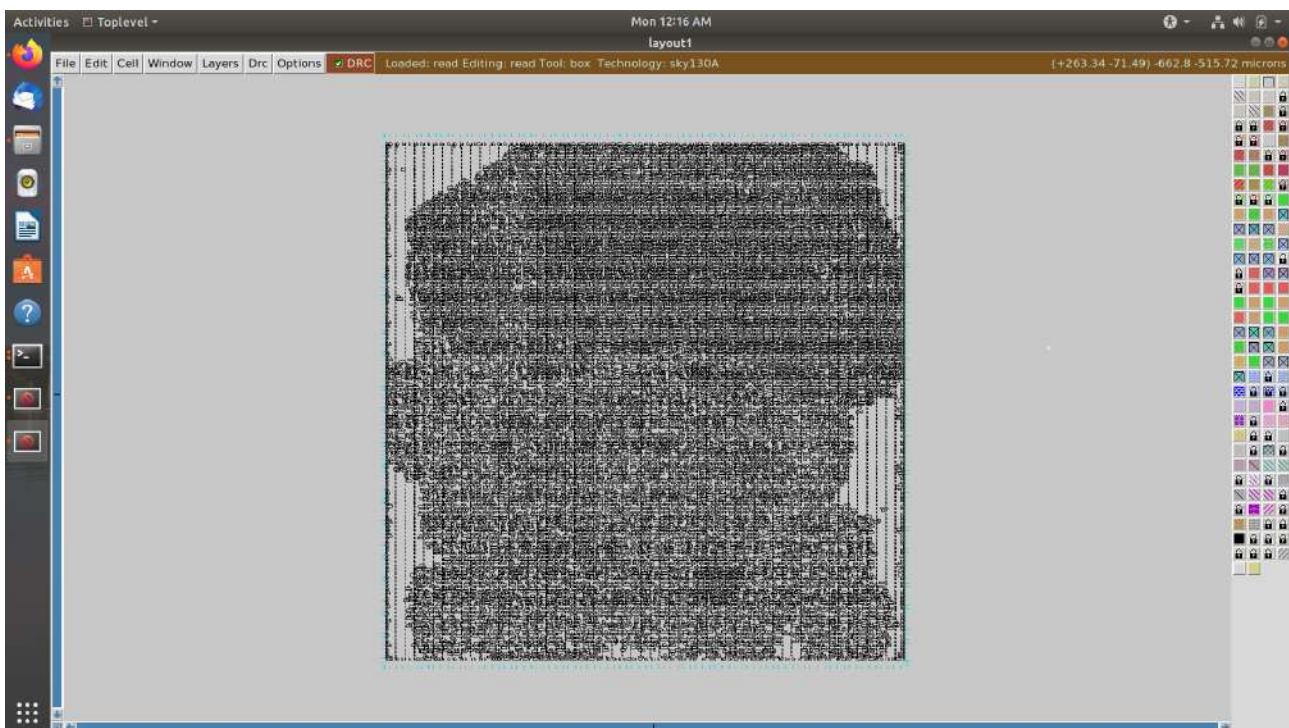
```
# Change directory to path containing generated placement def
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
24-03_10-03/results/placement/
```

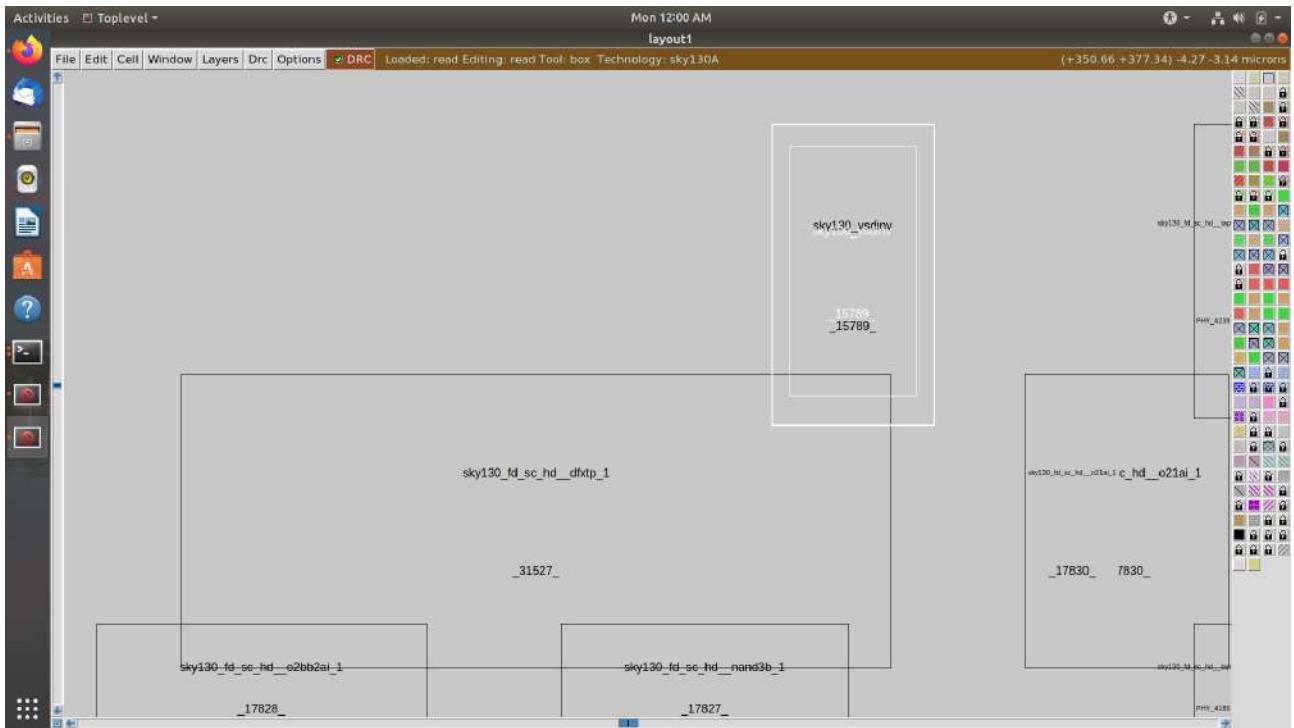
```
# Command to load the placement def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def  
&
```

Screenshot of placement def in magic



Screenshot of custom inverter inserted in placement def with proper abutment

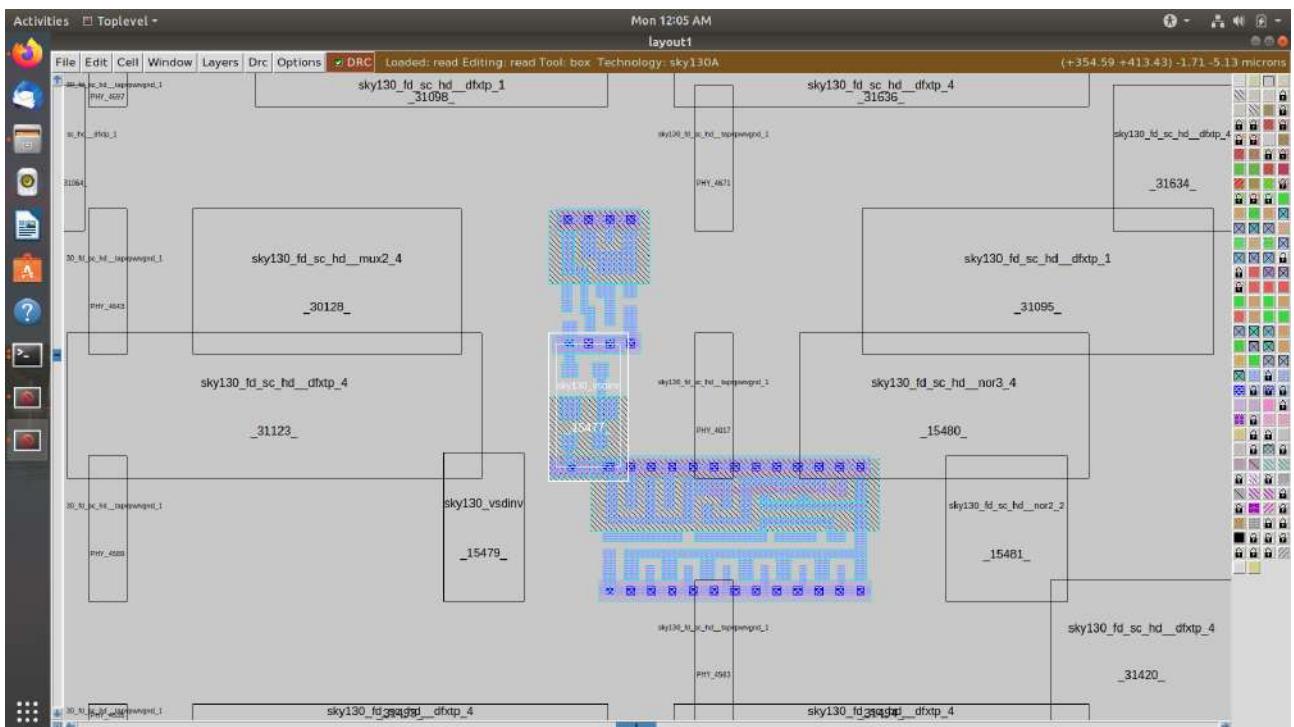
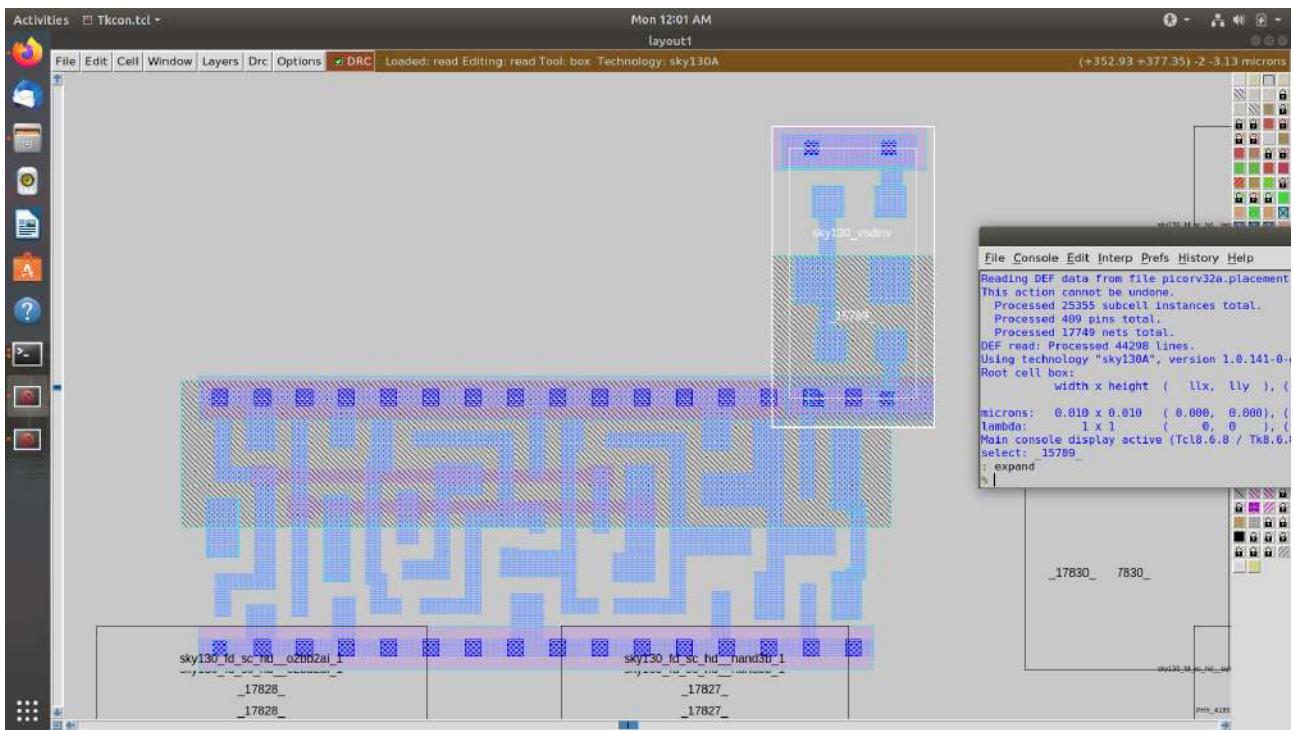


Command for tkcon window to view internal layers of cells

```
# Command to view internal connectivity layers
```

```
expand
```

Abutment of power pins with other cell from library clearly visible



9. Do Post-Synthesis timing analysis with OpenSTA tool.

Since we are having own after improved timing run we are going to do timing analysis on initial run of synthesis which has lots of violations and no parameters were added to improve timing

Commands to invoke the OpenLANE flow include new lef and perform synthesis

Change directory to openlane flow directory

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:vo.21'
```

Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command

```
docker
```

Now that we have entered the OpenLANE flow contained docker sub-system we can invoke the OpenLANE flow in the Interactive mode using the following command

```
./flow.tcl -interactive
```

Now that OpenLANE flow is open we have to input the required packages for proper functionality of the OpenLANE flow

```
package require openlane 0.9
```

Now the OpenLANE flow is ready to run any design and initially we have to prep the design creating some necessary files and directories for running a specific design which in our case is 'picorv32a'

```
prep -design picorv32a
```

```
# Additional commands to include newly added lef to openlane flow
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Now that the design is prepped and ready, we can run synthesis using following command
```

```
run_synthesis
```

Commands run final screenshot

Activities Terminal Tue 5:52 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
```

Newly created pre_sta.conf for STA analysis in openlane directory

Newly created `my_base.sdc` for STA analysis in `openlane/designs/picorv32a/src` directory based on the file `openlane/scripts/base.sdc`

```
Activities  M GVim - Tue 5:55 AM my_base.sdc (~/Desktop/work/tools/openlane/r/openlane/designs/picorv32a/src) - GVIM1
File Edit Tools Syntax Buffers Window Help
1 set ::env(CLOCK_PORT) cLK
2 set ::env(CLOCK_PERIOD) 24.73
3 #set ::env(SYNTH_DRIVING_CELL) sky130_vsdinv
4 set ::env(SYNTH_DRIVING_CELL) sky130_fd_sc_hd_inv_8
5 set ::env(SYNTH_DRIVING_CELL_PIN) Y
6 set ::env(SYNTH_CAP_LOAD) 17.653
7 set ::env(IO_PCT) 0.2
8 set ::env(SYNTH_MAX_FANOUT) 6
9
10 create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
11 set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
12 set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
13 puts "\[INFO\]: Setting output delay to: $output_delay_value"
14 puts "\[INFO\]: Setting input delay to: $input_delay_value"
15
16 set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
17
18 set clk_idx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
19 #set rst_idx [lsearch [all_inputs] [get_port resetn]]
20 set all_inputs_wo_clk [lreplace [all_inputs] $clk_idx $clk_idx]
21 #set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_idx $rst_idx]
22 set all_inputs_wo_clk_rst $all_inputs_wo_clk
23
24 # correct resetn
```

24,16

Top

```
Activities  M GVim - Tue 5:55 AM my_base.sdc (~/Desktop/work/tools/openlane/r/openlane/designs/picorv32a/src) - GVIM1
File Edit Tools Syntax Buffers Window Help
24 # correct resetn
25 set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
26 #set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
27 set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
28
29 # TODO set this as parameter
30 set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
31 set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
32 puts "\[INFO\]: Setting load to: $cap_load"
33 set_load $cap_load [all_outputs]
```

25,16

Bot

Commands to run STA in another terminal

```
# Change directory to openlane
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# Command to invoke OpenSTA tool with script
```

```
sta pre_sta.conf
```

Screenshots of commands run

```
Activities Terminal Tue 6:04 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
vsduser@vsdsquadron:~$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ sta pre_sta.conf
OpenSTA 2.4.0 ac3479bc24 Copyright (c) 2021, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type `show copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type `show warranty'.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib line 24, default_fanout_load is 0.0.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib line 23, default_fanout_load is 0.0.
[INFO]: Setting output delay to: 4.946000000000001
[INFO]: Setting input delay to: 4.946000000000001
[INFO]: Setting load to: 0.017653
Startpoint: _26669_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _26669_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _26669/_0 (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.00  0.00  cpuregs[0][0] (net)
          0.03  0.00  0.00 ^ _15938/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _15938/_X (sky130_fd_sc_hd_buf_1)
          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _26669/_D (sky130_fd_sc_hd_dfxtp_2)
          0.02  0.00  0.23  data arrival time
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data arrival time
          -0.02 -0.02  0.00  slack (MET)
```

```
Activities Terminal Tue 6:05 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _26669/_0 (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.00  0.00  cpuregs[0][0] (net)
          0.03  0.00  0.00 ^ _15938/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _15938/_X (sky130_fd_sc_hd_buf_1)
          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _26669/_D (sky130_fd_sc_hd_dfxtp_2)
          0.02  0.00  0.23  data arrival time
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data arrival time
          -0.02 -0.02  0.00  slack (MET)
```

```

Activities Terminal - Tue 6:05 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
Startpoint: _27860_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _27762_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
-----
          0.00 0.00 0.00 clock clk (rise edge)
          0.00 0.00 0.00 clock network delay (ideal)
          0.00 0.00 0.00 ^ _27860/_CLK (sky130_fd_sc_hd_dfxtp_2)
          0.10 0.64 0.64 ^ _27860/_Q (sky130_fd_sc_hd_dfxtp_2)
          4   0.01      irq_mask[1] (net)
          0.10 0.00 0.64 ^ _13108/_A (sky130_vsdinv)
          0.13 0.15 0.79 v _13108/_Y (sky130_vsdinv)
          6   0.01      _10510_ (net)
          0.13 0.00 0.79 v _13113/_A1 (sky130_fd_sc_hd_a221o_2)
          0.08 0.65 1.44 v _13113/_X (sky130_fd_sc_hd_a221o_2)
          1   0.00      _10515_ (net)
          0.08 0.00 1.44 v _13132/_A (sky130_fd_sc_hd_or4_2)
          0.21 1.53 2.98 v _13132/_X (sky130_fd_sc_hd_or4_2)
          1   0.00      _10534_ (net)
          0.21 0.00 2.98 v _13160/_A1 (sky130_fd_sc_hd_o2111a_2)
          0.07 0.54 3.52 v _13160/_X (sky130_fd_sc_hd_o2111a_2)
          2   0.00      _10562_ (net)
          0.07 0.00 3.52 v _13161/_C (sky130_fd_sc_hd_or3_2)
          0.17 0.97 4.48 v _13161/_X (sky130_fd_sc_hd_or3_2)
          2   0.00      _10563_ (net)
          0.17 0.00 4.48 v _13164/_A (sky130_fd_sc_hd_or2_2)

```

```

Activities Terminal - Tue 6:08 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
          0.14 0.68 47.22 v _13750/_X (sky130_fd_sc_hd_or2_2)
          3   0.01      10970_ (net)
          0.14 0.00 47.22 v _13751/_B (sky130_fd_sc_hd_or2_2)
          0.12 0.66 47.88 v _13751/_X (sky130_fd_sc_hd_or2_2)
          2   0.00      10971_ (net)
          0.12 0.00 47.88 v _13754/_B2 (sky130_fd_sc_hd_o221a_2)
          0.07 0.44 48.32 v _13754/_X (sky130_fd_sc_hd_o221a_2)
          1   0.00      03928_ (net)
          0.07 0.00 48.32 v _27762/_D (sky130_fd_sc_hd_dfxtp_2)
          48.32 data arrival time
          0.00 24.73 24.73 clock clk (rise edge)
          0.00 24.73 24.73 clock network delay (ideal)
          0.00 24.73 24.73 clock reconvergence pessimism
          24.73 ^ _27762/_CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.29 24.44 library setup time
          24.44 data required time
          24.44 data required time
          -48.32 data arrival time
          -23.89 slack (VIOLATED)

tns -711.59
wns -23.89
%
```

Since more fanout is causing more delay we can add parameter to reduce fanout and do synthesis again

Commands to include new lef and perform synthesis

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the  
design creating some necessary files and directories for running a specific design which in  
our case is 'picorv32a'
```

```
prep -design picorv32a -tag 25-03_18-52 -overwrite
```

```
# Additional commands to include newly added lef to openlane flow
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Command to set new value for SYNTH_MAX_FANOUT
```

```
set ::env(SYNTH_MAX_FANOUT) 4
```

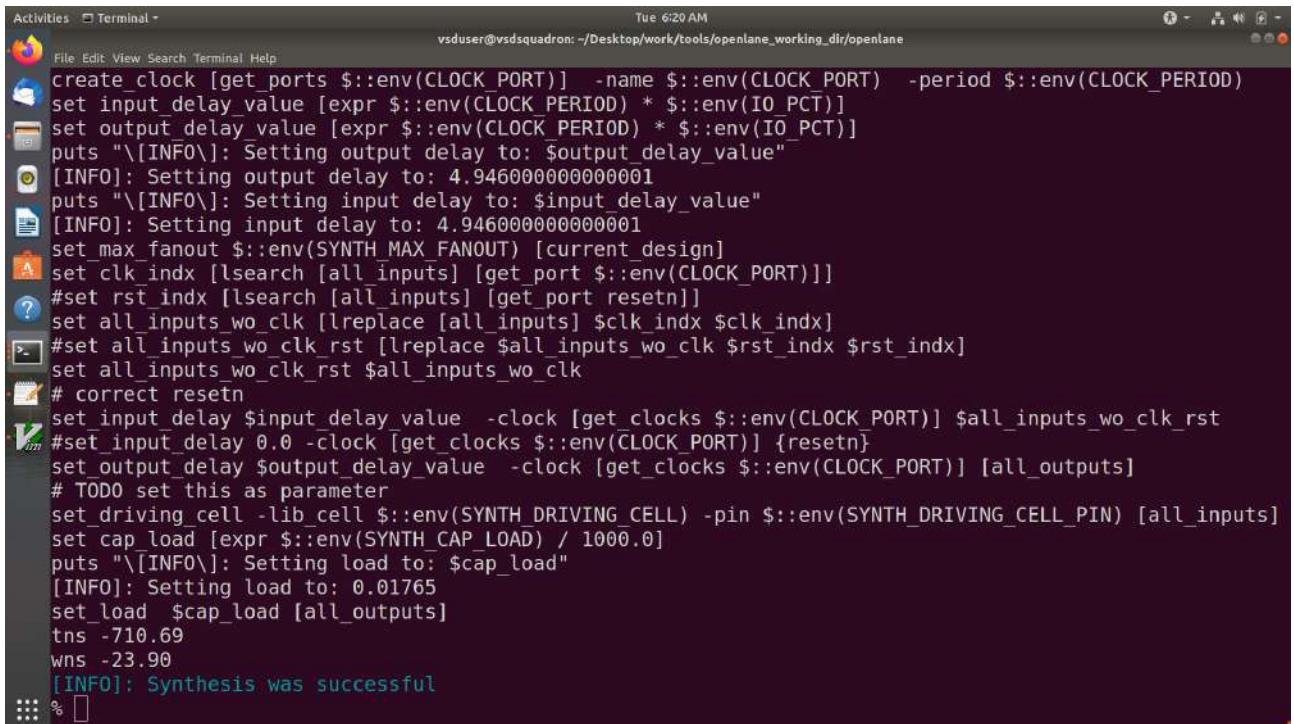
```
# Command to display current value of variable SYNTH_DRIVING_CELL to check whether  
it's the proper cell or not
```

```
echo $::env(SYNTH_DRIVING_CELL)
```

```
# Now that the design is prepped and ready, we can run synthesis using following  
command
```

run_synthesis

Commands run final screenshot



A screenshot of a terminal window titled "Terminal". The window shows a series of commands being run and their corresponding output. The commands relate to setting clock ports, input and output delays, and driving cell parameters. The output includes several "[INFO]" messages indicating the progress of the synthesis process, such as "Setting output delay to: 4.946000000000001" and "Synthesis was successful". The terminal window has a dark background with light-colored text.

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -710.69
wns -23.90
[INFO]: Synthesis was successful
```

Commands to run STA in another terminal

```
# Change directory to openlane
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# Command to invoke OpenSTA tool with script
```

```
sta pre_sta.conf
```

Screenshots of commands run

```

Activities Terminal - Tue 6:22 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ sta pre_sta.conf
OpenSTA 2.4.0 ac3479bc24 Copyright (c) 2021, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type `show copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type `show warranty'.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib line 24, default_fanout_load is 0.0.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib line 23, default_fanout_load is 0.0.
[INFO]: Setting output delay to: 4.9460000000000001
[INFO]: Setting input delay to: 4.9460000000000001
[INFO]: Setting load to: 0.017653
Startpoint: _29347_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _29347_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _29347_/Q (sky130_fd_sc_hd_dfxtp_2)
          2   0.00          cpuregs[0][0] (net)
          0.02  0.00  0.10 ^ _17885/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _17885/_X (sky130_fd_sc_hd_buf_1)
          1   0.00          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _29347/_D (sky130_fd_sc_hd_dfxtp_2)
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data required time
          -0.23 -0.23  0.00  data arrival time
          0.24  slack (MET)

```

```

Activities Terminal - Tue 6:22 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _29347_/Q (sky130_fd_sc_hd_dfxtp_2)
          2   0.00          cpuregs[0][0] (net)
          0.03  0.00  0.18 ^ _17885/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _17885/_X (sky130_fd_sc_hd_buf_1)
          1   0.00          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _29347/_D (sky130_fd_sc_hd_dfxtp_2)
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data required time
          -0.23 -0.23  0.00  data arrival time
          0.24  slack (MET)

```

Activities Terminal - Tue 6:22 AM
 vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```

Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00 ^ _29052_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.06  0.58  0.58 v _29052/_Q (sky130_fd_sc_hd_dfxtp_2)
          4   0.01           irq_pending[3] (net)
          0.06  0.00  0.58 v _14460/_A (sky130_vsdinv)
          0.19  0.17  0.75 ^ _14460/_Y (sky130_vsdinv)
          3   0.01           _11622_ (net)
          0.19  0.00  0.75 ^ _14461/_B2 (sky130_fd_sc_hd_o22ai_2)
          0.09  0.14  0.89 v _14461/_Y (sky130_fd_sc_hd_o22ai_2)
          1   0.00           _11623_ (net)
          0.09  0.00  0.89 v _14462/_C1 (sky130_fd_sc_hd_a221o_2)
          0.08  0.55  1.44 v _14462/_X (sky130_fd_sc_hd_a221o_2)
          1   0.00           _11624_ (net)
          0.08  0.00  1.44 v _14481/_A (sky130_fd_sc_hd_or4_2)
          0.21  1.53  2.97 v _14481/_X (sky130_fd_sc_hd_or4_2)
          1   0.00           _11643_ (net)
          0.21  0.00  2.97 v _14509/_A1 (sky130_fd_sc_hd_o2111a_2)
          0.07  0.54  3.51 v _14509/_X (sky130_fd_sc_hd_o2111a_2)
          2   0.00
  
```

Activities Terminal - Tue 6:23 AM
 vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```

          0.14  0.68  47.23 v _15226/_X (sky130_fd_sc_hd_or2_2)
          3   0.01           _12208_ (net)
          0.14  0.00  47.23 v _15227/_B (sky130_fd_sc_hd_or2_2)
          0.12  0.66  47.89 v _15227/_X (sky130_fd_sc_hd_or2_2)
          2   0.00           _12209_ (net)
          0.12  0.00  47.89 v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
          0.07  0.44  48.33 v _15230/_X (sky130_fd_sc_hd_o221a_2)
          1   0.00           _03928_ (net)
          0.07  0.00  48.33 v _30440/_D (sky130_fd_sc_hd_dfxtp_2)
          48.33 data arrival time
          0.00  24.73  24.73  clock clk (rise edge)
          0.00  24.73  24.73  clock network delay (ideal)
          0.00  24.73  24.73  clock reconvergence pessimism
          24.73 ^ _30440_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.29 24.44  24.44  library setup time
          24.44 24.44  24.44  data required time
          24.44 data required time
          -48.33 data arrival time
  ----- -23.90 slack (VIOLATED)

tns -710.69
wns -23.90
  
```

10. Make timing ECO fixes to remove all violations.

OR gate of drive strength 2 is driving 4 fanouts

Activities Terminal Tue 6:55 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

		0.19	0.00	0.75	^ _14461 /B2 (sky130_fd_sc_hd_o22ai_2)
1	0.00	0.09	0.14	0.89 v	_14461 /Y (sky130_fd_sc_hd_o22ai_2)
					11623 (net)
		0.09	0.00	0.89 v	_14462 /C1 (sky130_fd_sc_hd_a22lo_2)
1	0.00	0.08	0.55	1.44 v	_14462 /X (sky130_fd_sc_hd_a22lo_2)
					11624 (net)
		0.08	0.00	1.44 v	_14481 /A (sky130_fd_sc_hd_or4_2)
1	0.00	0.21	1.53	2.97 v	_14481 /X (sky130_fd_sc_hd_or4_2)
					11643 (net)
		0.21	0.00	2.97 v	_14509 /A1 (sky130_fd_sc_hd_o2111a_2)
2	0.00	0.07	0.54	3.51 v	_14509 /X (sky130_fd_sc_hd_o2111a_2)
					11671 (net)
		0.07	0.00	3.51 v	_14510 /C (sky130_fd_sc_hd_or3_2)
4	0.01	0.21	1.04	4.55 v	_14510 /X (sky130_fd_sc_hd_or3_2)
					11672 (net)
		0.21	0.00	4.55 v	_14513 /A (sky130_fd_sc_hd_or2_2)
2	0.00	0.11	0.71	5.26 v	_14513 /X (sky130_fd_sc_hd_or2_2)
					11674 (net)
		0.11	0.00	5.26 v	_14514 /C (sky130_fd_sc_hd_or3_2)
4	0.01	0.20	1.03	6.29 v	_14514 /X (sky130_fd_sc_hd_or3_2)
					11675 (net)
		0.20	0.00	6.29 v	_15166 /B (sky130_fd_sc_hd_or2_2)
2	0.00	0.11	0.67	6.96 v	_15166 /X (sky130_fd_sc_hd_or2_2)
					12148 (net)
		0.11	0.00	6.96 v	_15167 /C (sky130_fd_sc_hd_or3_2)
2	0.00	0.17	0.98	7.94 v	_15167 /X (sky130_fd_sc_hd_or3_2)
					12149 (net)
		0.17	0.00	7.94 v	_15168 /B (sky130_fd_sc_hd_or2_2)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

report_net -connections _11672_

Checking command syntax

help replace_cell

Replacing cell

replace_cell _14510_ sky130_fd_sc_hd_or3_4

Generating custom timing report

```
report_checks -fields {net cap slew input_pins} -digits 4
```

Result - slack reduced

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
----- [-23.90 slack (VIOLATED)]
tns -710.69
wns -23.90
% report_net -connections _11672_
Net _11672_
Driver pins
_14510 /X output (sky130_fd_sc_hd_or3_2)
Load pins
_14513 /A input (sky130_fd_sc_hd_or2_2)
_15505 /B input (sky130_fd_sc_hd_or2_2)
_18231 /A input (sky130_fd_sc_hd_buf_1)
_18326 /B input (sky130_fd_sc_hd_nand2_2)

% help replace_cell
replace_cell instance lib_cell
% replace_cell _14510_ sky130_fd_sc_hd_or3_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
----- Fanout Cap Slew Delay Time Description

```

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
----- Fanout Cap Slew Delay Time Description
----- 0.0000 0.0000 0.0000 0.0000 clock clk (rise edge)
----- 0.0000 0.0000 0.0000 0.0000 clock network delay (ideal)
----- 0.0000 0.0000 0.0000 ^ _29052/_CLK (sky130_fd_sc_hd_dfxtp_2)
----- 0.0572 0.5830 0.5830 v _29052/_Q (sky130_fd_sc_hd_dfxtp_2)
----- 4 0.0067 0.0572 0.0000 0.5830 v _14460/_A (sky130_vsdinv)
----- 0.1856 0.1667 0.7497 ^ _14460/_Y (sky130_vsdinv)
----- 3 0.0138 0.1856 0.0000 0.7497 ^ _14461/_B2 (sky130_fd_sc_hd_o22ai_2)
----- 0.0878 0.1436 0.8933 v _14461/_Y (sky130_fd_sc_hd_o22ai_2)
----- 1 0.0021 0.0878 0.0000 0.8933 v _14462/_C1 (sky130_fd_sc_hd_a221o_2)
----- 0.0784 0.5469 1.4402 v _14462/_X (sky130_fd_sc_hd_a221o_2)
----- 1 0.0013 0.0784 0.0000 1.4402 v _14481/_A (sky130_fd_sc_hd_or4_2)
----- 0.2106 1.5344 2.9746 v _14481/_X (sky130_fd_sc_hd_or4_2)
----- 1 0.0024 0.2106 0.0000 2.9746 v _14509/_A1 (sky130_fd_sc_hd_o2111a_2)
----- 0.0792 0.5466 3.5212 v _14509/_X (sky130_fd_sc_hd_o2111a_2)
----- 2 0.0044
----- 11623_ (net)
----- 11624_ (net)
----- 11643_ (net)
----- 11671_ (net)
```

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

Tue 9:42 AM

3	0.0138	0.1856	0.0000	0.7497	^ _11622_ (net)
		0.0878	0.1436	0.8933	v _14461/_B2 (sky130_fd_sc_hd_o22ai_2)
1	0.0021	0.0878	0.0000	0.8933	v _14461/_Y (sky130_fd_sc_hd_o22ai_2)
		0.0784	0.5469	1.4402	v _11623_ (net)
1	0.0013	0.0784	0.0000	1.4402	v _14462/_C1 (sky130_fd_sc_hd_a221o_2)
		0.2106	1.5344	2.9746	v _14462/_X (sky130_fd_sc_hd_a221o_2)
1	0.0024	0.2106	0.0000	2.9746	v _11624_ (net)
		0.0792	0.5466	3.5212	v _14481/_A (sky130_fd_sc_hd_or4_2)
2	0.0044	0.0792	0.0000	3.5212	v _14481/_X (sky130_fd_sc_hd_or4_2)
		0.1349	0.6755	4.1967	v _11643_ (net)
4	0.0089	0.1349	0.0000	4.1967	v _14509/_A1 (sky130_fd_sc_hd_o2111a_2)
		0.1121	0.6770	4.8737	v _14509/_X (sky130_fd_sc_hd_o2111a_2)
2	0.0025	0.1121	0.0000	4.8737	v _11671_ (net)
		0.1967	1.0321	5.9057	v _14514/_C (sky130_fd_sc_hd_or3_2)
4	0.0070	0.1967	0.0000	5.9057	v _14514/_X (sky130_fd_sc_hd_or3_2)
		0.1148	0.6684	6.5742	v _11675_ (net)
2	0.0032	0.1148	0.0000	6.5742	v _15166/_B (sky130_fd_sc_hd_or2_2)
		0.1692	0.9831	7.5573	v _15166/_X (sky130_fd_sc_hd_or2_2)
2	0.0025	0.0000	0.0000	7.5573	v _12148_ (net)
		0.0000	0.0000	7.5573	v _15167/_C (sky130_fd_sc_hd_or3_2)
		0.0000	0.0000	7.5573	v _15167/_X (sky130_fd_sc_hd_or3_2)
		0.0000	0.0000	7.5573	v _12149_ (net)

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

Tue 7:07 AM

2	0.0035	0.1162	0.0000	46.1648	v _12207_ (net)
		0.1421	0.6813	46.8462	v _15226/_B (sky130_fd_sc_hd_or2_2)
3	0.0079	0.1421	0.0000	46.8462	v _15226/_X (sky130_fd_sc_hd_or2_2)
		0.1228	0.6610	47.5072	v _12208_ (net)
2	0.0044	0.1228	0.0000	47.5072	v _15227/_B (sky130_fd_sc_hd_or2_2)
		0.0713	0.4381	47.9453	v _15227/_X (sky130_fd_sc_hd_or2_2)
1	0.0016	0.0713	0.0000	47.9453	v _12209_ (net)
		0.0000	24.7300	24.7300	v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
		0.0000	24.7300	24.7300	v _15230/_X (sky130_fd_sc_hd_o221a_2)
		0.0000	24.7300	24.7300	v _03928_ (net)
		0.0000	24.7300	24.7300	v _30440/_D (sky130_fd_sc_hd_dfxtip_2)
		0.0000	24.7300	24.7300	v data arrival time
		0.0000	24.7300	24.7300	v clock clk (rise edge)
		0.0000	24.7300	24.7300	v clock network delay (ideal)
		0.0000	24.7300	24.7300	v clock reconvergence pessimism
		24.7300	24.7300	24.7300	v ^ _30440/_CLK (sky130_fd_sc_hd_dfxtip_2)
		-0.2939	24.4361	24.4361	v library setup time
		-0.2939	24.4361	24.4361	v data required time
		24.4361	24.4361	24.4361	v data arrival time
		24.4361	24.4361	24.4361	v slack (VIOLATED)
		-47.9453	-47.9453	-47.9453	v -23.5092 slack (VIOLATED)

OR gate of drive strength 2 is driving 4 fanouts

Activities Terminal Tue 9:46 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

		0.2106	1.5344	2.9746 v	_14481/_X (sky130_fd_sc_hd_or4_2)
1	0.0024				11643 (net)
		0.2106	0.0000	2.9746 v	_14509/_A1 (sky130_fd_sc_hd_o2111a_2)
		0.0792	0.5466	3.5212 v	_14509/_X (sky130_fd_sc_hd_o2111a_2)
2	0.0044				11671 (net)
		0.0792	0.0000	3.5212 v	_14510/_C (sky130_fd_sc_hd_or3_4)
		0.1349	0.6755	4.1967 v	_14510/_X (sky130_fd_sc_hd_or3_4)
4	0.0089				11672 (net)
		0.1349	0.0000	4.1967 v	_14513/_A (sky130_fd_sc_hd_or2_2)
		0.1121	0.6770	4.8737 v	_14513/_X (sky130_fd_sc_hd_or2_2)
2	0.0025				11674 (net)
		0.1121	0.0000	4.8737 v	_14514/_C (sky130_fd_sc_hd_or3_2)
		0.1967	1.0321	5.9057 v	_14514/_X (sky130_fd_sc_hd_or3_2)
4	0.0070				11675 (net)
		0.1967	0.0000	5.9057 v	_15166/_B (sky130_fd_sc_hd_or2_2)
		0.1148	0.6684	6.5742 v	_15166/_X (sky130_fd_sc_hd_or2_2)
2	0.0032				12148 (net)
		0.1148	0.0000	6.5742 v	_15167/_C (sky130_fd_sc_hd_or3_2)
		0.1692	0.9831	7.5573 v	_15167/_X (sky130_fd_sc_hd_or3_2)
2	0.0035				12149 (net)
		0.1692	0.0000	7.5573 v	_15168/_B (sky130_fd_sc_hd_or2_2)
		0.1422	0.7026	8.2599 v	_15168/_X (sky130_fd_sc_hd_or2_2)
3	0.0079				12150 (net)
		0.1422	0.0000	8.2599 v	_15169/_B (sky130_fd_sc_hd_or2_2)
		0.1162	0.6492	8.9091 v	_15169/_X (sky130_fd_sc_hd_or2_2)
2	0.0035				12151 (net)
		0.1162	0.0000	8.9091 v	_15170/_B (sky130_fd_sc_hd_or2_2)
		0.1422	0.6817	9.5904 v	_15170/_X (sky130_fd_sc_hd_or2_2)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

```
# Reports all the connections to a net
```

```
report_net -connections _11675_
```

```
# Replacing cell
```

```
replace_cell _14514_ sky130_fd_sc_hd_or3_4
```

```
# Generating custom timing report
```

```
report_checks -fields {net cap slew input_pins} -digits 4
```

Result - slack reduced

```

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Tue 9:49 AM
-47.9453  data arrival time
-----
-23.5092  slack (VIOLATED)

% report_net -connections _11675_
Net _11675_
Driver pins
_14514/_X output (sky130_fd_sc_hd_or3_2)
Load pins
_14515/_A input (sky130_vsdinv)
_14521/_B2 input (sky130_fd_sc_hd_o221a_2)
_14662/_B input (sky130_fd_sc_hd_or2_2)
_15166/_B input (sky130_fd_sc_hd_or2_2)

% replace_cell _14514_ sky130_fd_sc_hd_or3_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout      Cap      Slew      Delay      Time      Description
-----      -----      -----      -----      -----      -----
          0.0000  0.0000  0.0000  clock clk (rise edge)
          0.0000  0.0000  slack network delay (ideal)

```

Tue 9:50 AM						
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane						
Fanout	Cap	Slew	Delay	Time	Description	
1	0.0013				11624_ (net)	
		0.0784	0.0000	1.4402	v 14481/_A (sky130_fd_sc_hd_or4_2)	
		0.2106	1.5344	2.9746	v 14481/_X (sky130_fd_sc_hd_or4_2)	
1	0.0024				11643_ (net)	
		0.2106	0.0000	2.9746	v 14509/_A1 (sky130_fd_sc_hd_o2111a_2)	
		0.0792	0.5466	3.5212	v 14509/_X (sky130_fd_sc_hd_o2111a_2)	
2	0.0044				11671_ (net)	
		0.0792	0.0000	3.5212	v 14510/_C (sky130_fd_sc_hd_or3_4)	
		0.1349	0.6755	4.1967	v 14510/_X (sky130_fd_sc_hd_or3_4)	
4	0.0089				11672_ (net)	
		0.1349	0.0000	4.1967	v 14513/_A (sky130_fd_sc_hd_or2_2)	
		0.1182	0.6880	4.8847	v 14513/_X (sky130_fd_sc_hd_or2_2)	
2	0.0034				11674_ (net)	
		0.1182	0.0000	4.8847	v 14514/_C (sky130_fd_sc_hd_or3_4)	
		0.1290	0.6794	5.5641	v 14514/_X (sky130_fd_sc_hd_or3_4)	
4	0.0070				11675_ (net)	
		0.1290	0.0000	5.5641	v 15166/_B (sky130_fd_sc_hd_or2_2)	
		0.1148	0.6414	6.2055	v 15166/_X (sky130_fd_sc_hd_or2_2)	
2	0.0032				12148_ (net)	
		0.1148	0.0000	6.2055	v 15167/_C (sky130_fd_sc_hd_or3_2)	
		0.1692	0.9831	7.1886	v 15167/_X (sky130_fd_sc_hd_or3_2)	
2	0.0035				12149_ (net)	
		0.1692	0.0000	7.1886	v 15168/_B (sky130_fd_sc_hd_or2_2)	
		0.1422	0.7026	7.8912	v 15168/_X (sky130_fd_sc_hd_or2_2)	
3	0.0079				12150_ (net)	
		0.1422	0.0000	7.8912	v 15169/_B (sky130_fd_sc_hd_or2_2)	
		0.1162	0.6492	8.5404	v 15169/_X (sky130_fd_sc_hd_or2_2)	
2	0.0025				12151_ (net)	

```
Activities Terminal Tue 9:50 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
2 0.0035
          0.1162  0.0000  45.7962 v _12207_(net)
          0.1421  0.6813  46.4775 v _15226/_B (sky130_fd_sc_hd_or2_2)
          0.1421  0.0000  46.4775 v _15226/_X (sky130_fd_sc_hd_or2_2)
3 0.0079
          0.1228  0.6610  47.1385 v _15227/_B (sky130_fd_sc_hd_or2_2)
          0.1228  0.0000  47.1385 v _15227/_X (sky130_fd_sc_hd_or2_2)
2 0.0044
          0.1228  0.0000  47.1385 v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
          0.0713  0.4381  47.5766 v _15230/_X (sky130_fd_sc_hd_o221a_2)
1 0.0016
          0.0713  0.0000  47.5766 v _30440/_D (sky130_fd_sc_hd_dfxtp_2)
          0.0713  0.0000  47.5766 v data arrival time

          0.0000  24.7300  24.7300  clock clk (rise edge)
          0.0000  24.7300  24.7300  clock network delay (ideal)
          0.0000  24.7300  24.7300  clock reconvergence pessimism
          -0.2939 24.4361  ^ _30440/_CLK (sky130_fd_sc_hd_dfxtp_2)
          24.4361  library setup time
          24.4361  data required time
          24.4361  data required time
          -47.5766  data arrival time
          -23.1405  slack (VIOLATED)
```

OR gate of drive strength 2 driving OA gate has more delay

vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane					
Fanout	Cap	Slew	Delay	Time	Description
			0.0000	0.0000	clock clk (rise edge)
			0.0000	0.0000	clock network delay (ideal)
			0.0000	0.0000	^ _29052_/_CLK (sky130_fd_sc_hd_dfxtp_2)
			0.0572	0.5830	v _29052_/_Q (sky130_fd_sc_hd_dfxtp_2)
4	0.0067				irq_pending[3] (net)
			0.0572	0.0000	v _14460_/_A (sky130_vsdinv)
			0.1856	0.1667	^ _14460_/_Y (sky130_vsdinv)
3	0.0138				_11622_ (net)
			0.1856	0.0000	^ _14461_/_B2 (sky130_fd_sc_hd_o22ai_2)
			0.0878	0.1436	v _14461_/_Y (sky130_fd_sc_hd_o22ai_2)
1	0.0021				_11623_ (net)
			0.0878	0.0000	v _14462_/_C1 (sky130_fd_sc_hd_a221o_2)
			0.0784	0.5469	v _14462_/_X (sky130_fd_sc_hd_a221o_2)
1	0.0013				_11624_ (net)
			0.0784	0.0000	v _14481_/_A (sky130_fd_sc_hd_or4_2)
			0.2106	1.5344	v _14481_/_X (sky130_fd_sc_hd_or4_2)
1	0.0024				_11643_ (net)
			0.2106	0.0000	v _14509_/_A1 (sky130_fd_sc_hd_o2111a_2)
			0.0792	0.5466	v _14509_/_X (sky130_fd_sc_hd_o2111a_2)
2	0.0044				_11671_ (net)
			0.0792	0.0000	v _14510_/_C (sky130_fd_sc_hd_or3_4)
			0.1349	0.6755	v _14510_/_X (sky130_fd_sc_hd_or3_4)
4	0.0089				_11672_ (net)
			0.1349	0.0000	v _14513_/_A (sky130_fd_sc_hd_or2_2)
			0.1182	0.6880	v _14513_/_X (sky130_fd_sc_hd_or2_2)
3	0.0034				_11674_ (net)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

```
report_net -connections _11643_
```

```
# Replacing cell
```

```
replace_cell _14481_ sky130_fd_sc_hd__or4_4
```

```
# Generating custom timing report
```

```
report_checks -fields {net cap slew input_pins} -digits 4
```

Result - slack reduced

```
Activities Terminal - Tue 10:29 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
-47.5766  data arrival time
-----  
-23.1405  slack (VIOLATED)

% report net -connections _11643_
Net _11643_
Driver pins
_14481/_X output (sky130_fd_sc_hd_or4_2)
Load pins
_14509/_A1 input (sky130_fd_sc_hd_o2111a_2)

% replace_cell _14481_ sky130_fd_sc_hd_hd_or4_4
1

% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29043_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout      Cap      Slew      Delay      Time      Description
-----  
0.0000      0.0000      0.0000      0.0000  clock clk (rise edge)
0.0000      0.0000      0.0000      0.0000  clock network delay (ideal)
0.0000      0.0000      0.0000 ^ _29043_/_CLK (sky130_fd_sc_hd_dfxtp_2)
0.0581      0.5838      0.5838 v _29043_/_Q (sky130_fd_sc_hd_dfxtp_2)
```

```
Activities Terminal + Tue 10:29 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
2 0.0035
          0.1162  0.0000  45.7918 v _12207_(net)
          0.1421  0.6813  46.4731 v _15226/_B (sky130_fd_sc_hd_or2_2)
          0.1421  0.0000  46.4731 v _15226/_X (sky130_fd_sc_hd_or2_2)
3 0.0079
          0.1228  0.6610  47.1341 v _15227/_B (sky130_fd_sc_hd_or2_2)
          0.1228  0.0000  47.1341 v _15227/_X (sky130_fd_sc_hd_or2_2)
2 0.0044
          0.0713  0.4381  47.5723 v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
          0.0713  0.0000  47.5723 v _15230/_X (sky130_fd_sc_hd_o221a_2)
          0.0016
          0.0713  0.0000  47.5723 v _30440/_D (sky130_fd_sc_hd_dfxtp_2)
          0.0713  0.0000  47.5723 data arrival time
          0.0000  24.7300  24.7300  clock clk (rise edge)
          0.0000  24.7300  24.7300  clock network delay (ideal)
          0.0000  24.7300  24.7300  clock reconvergence pessimism
          -0.2939  24.4361 ^ _30440/_CLK (sky130_fd_sc_hd_dfxtp_2)
          24.4361  library setup time
          24.4361  data required time
          24.4361  data required time
          -47.5723  data arrival time
-----
          -23.1362  slack (VIOLATED)
```

OR gate of drive strength 2 driving OA gate has more delay

Activities Terminal Tue 10:32 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

				irq_pending[12] (net)
4	0.0069	0.0581	0.0000	0.5838 v _14484 /A (sky130_vsdinv)
		0.1864	0.1676	0.7515 ^ _14484 /Y (sky130_vsdinv)
3	0.0139	0.1864	0.0000	11646_ (net)
		0.0878	0.1674	0.7515 ^ _14486 /A2 (sky130_fd_sc_hd_o22ai_2)
1	0.0021	0.0878	0.0000	0.9189 v _14486 /Y (sky130_fd_sc_hd_o22ai_2)
		0.0784	0.5469	11648_ (net)
1	0.0013	0.0784	0.0000	1.4658 v _14487 /C1 (sky130_fd_sc_hd_a22lo_2)
		0.2092	1.5317	1.4658 v _14487 /X (sky130_fd_sc_hd_a22lo_2)
1	0.0023	0.2092	0.0000	11649_ (net)
		0.0792	0.5193	2.9975 v _14506 /A (sky130_fd_sc_hd_or4_2)
2	0.0044	0.0792	0.0000	3.5168 v _14506 /X (sky130_fd_sc_hd_or4_2)
		0.1349	0.6755	11668_ (net)
4	0.0089	0.1349	0.0000	3.5168 v _14509 /A2 (sky130_fd_sc_hd_o2111a_2)
		0.1182	0.6880	4.1923 v _14509 /X (sky130_fd_sc_hd_o2111a_2)
2	0.0034	0.1182	0.0000	11671_ (net)
		0.1290	0.6794	4.8803 v _14510 /C (sky130_fd_sc_hd_or3_4)
4	0.0070	0.1290	0.0000	5.5597 v _14510 /X (sky130_fd_sc_hd_or3_4)
		0.1148	0.6414	11672_ (net)
2	0.0022	0.1148	0.0000	4.8803 v _14513 /A (sky130_fd_sc_hd_or2_2)
		0.1290	0.6794	5.5597 v _14513 /X (sky130_fd_sc_hd_or2_2)
4	0.0070	0.1290	0.0000	11674_ (net)
		0.1148	0.6414	6.2011 v _15166 /B (sky130_fd_sc_hd_or2_2)
2	0.0022	0.1148	0.0000	11675_ (net)
		0.1290	0.6794	5.5597 v _15166 /X (sky130_fd_sc_hd_or2_2)
4	0.0070	0.1290	0.0000	11676_ (net)
		0.1148	0.6414	6.2011 v _15166 /B (sky130_fd_sc_hd_or2_2)
2	0.0022	0.1148	0.0000	11677_ (net)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

report_net -connections _11668_

Replacing cell

replace_cell _14506_ sky130_fd_sc_hd_or4_4

Generating custom timing report

report_checks -fields {net cap slew input_pins} -digits 4

Result - slack reduced

```

Activities Terminal - Tue 10:36 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
-47.5723  data arrival time
-----  

-23.1362  slack (VIOLATED)

% report_net -connections _11668_
Net _11668
Driver pins
_14506 /X output (sky130_fd_sc_hd_or4_2)
Load pins
_14509 /A2 input (sky130_fd_sc_hd_o2111a_2)

% replace_cell _14506_ sky130_fd_sc_hd_or4_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout      Cap      Slew      Delay      Time      Description
-----  

          0.0000  0.0000  0.0000  clock clk (rise edge)
          0.0000  0.0000  0.0000  clock network delay (ideal)
          0.0000  0.0000  0.0000 ^ _29052 /CLK (sky130_fd_sc_hd_dfxtp_2)
          0.0572  0.5830  0.5830 v _29052 /Q (sky130_fd_sc_hd_dfxtp_2)
           0.0067  


```

```

Activities Terminal - Tue 10:37 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
2  0.0035
          0.1162  0.0000  45.2729 v _12207_(net)
          0.1421  0.6813  45.9542 v _15226 /B (sky130_fd_sc_hd_or2_2)
          0.1421  0.0000  45.9542 v _15226 /X (sky130_fd_sc_hd_or2_2)
          0.1228  0.6610  46.6153 v _12208_(net)
          0.1228  0.0000  46.6153 v _15227 /B (sky130_fd_sc_hd_or2_2)
          0.1228  0.0000  46.6153 v _15227 /X (sky130_fd_sc_hd_or2_2)
          0.0713  0.4381  47.0534 v _12209_(net)
          0.0713  0.0000  47.0534 v _15230 /B2 (sky130_fd_sc_hd_o221a_2)
          0.0713  0.0000  47.0534 v _15230 /X (sky130_fd_sc_hd_o221a_2)
          0.0713  0.0000  47.0534 v _03928_(net)
          0.0713  0.0000  47.0534 v _30440 /D (sky130_fd_sc_hd_dfxtp_2)
          0.0713  0.0000  47.0534 v data arrival time
          0.0000  24.7300  24.7300  clock clk (rise edge)
          0.0000  24.7300  24.7300  clock network delay (ideal)
          0.0000  24.7300  24.7300  clock reconvergence pessimism
          0.0000  24.7300  24.7300 ^ _30440 /CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.2939  24.4361  library setup time
          24.4361  data required time
          24.4361  data arrival time
-----  

-22.6173  slack (VIOLATED)

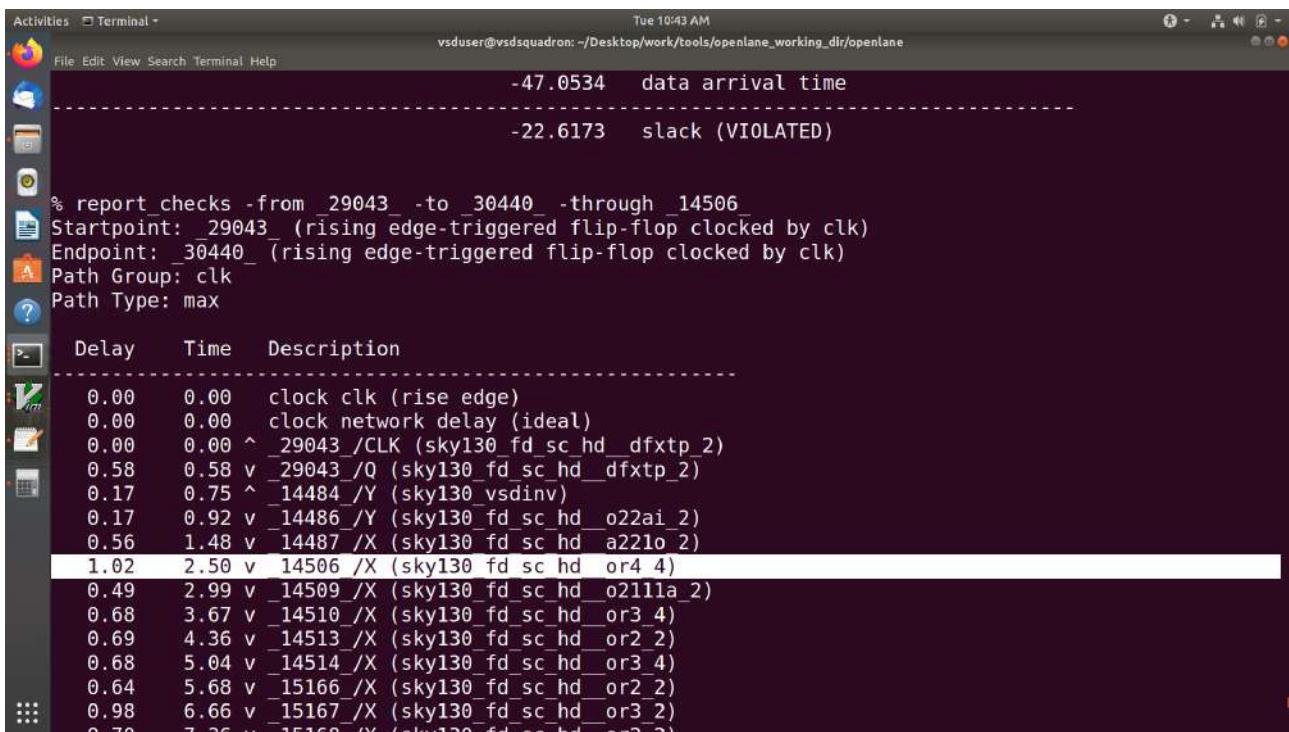
```

Commands to verify instance _14506_ is replaced with sky130_fd_sc_hd_or4_4

Generating custom timing report

report_checks -from _29043_ -to _30440_ -through _14506_

Screenshot of replaced instance



The screenshot shows a terminal window with the following output:

```
Tue 10:43 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
-47.0534  data arrival time
-----
-22.6173  slack (VIOLATED)

% report_checks -from 29043 -to 30440 -through 14506
Startpoint: 29043 (rising edge-triggered flip-flop clocked by clk)
Endpoint: 30440 (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Delay    Time    Description
-----
0.00    0.00    clock clk (rise edge)
0.00    0.00    clock network delay (ideal)
0.00    0.00 ^ 29043 /CLK (sky130_fd_sc_hd_dfxtpl_2)
0.58    0.58 v 29043 /Q (sky130_fd_sc_hd_dfxtpl_2)
0.17    0.75 ^ 14484 /Y (sky130_vsdinv)
0.17    0.92 v 14486 /Y (sky130_fd_sc_hd_o22ai_2)
0.56    1.48 v 14487 /X (sky130_fd_sc_hd_a22lo_2)
1.02    2.50 v 14506 /X (sky130_fd_sc_hd_or4_4)
0.49    2.99 v 14509 /X (sky130_fd_sc_hd_o2111a_2)
0.68    3.67 v 14510 /X (sky130_fd_sc_hd_or3_4)
0.69    4.36 v 14513 /X (sky130_fd_sc_hd_or2_2)
0.68    5.04 v 14514 /X (sky130_fd_sc_hd_or3_4)
0.64    5.68 v 15166 /X (sky130_fd_sc_hd_or2_2)
0.98    6.66 v 15167 /X (sky130_fd_sc_hd_or3_2)
0.70    7.26 v 15168 /X (sky130_fd_sc_hd_or2_2)
```

We started ECO fixes at wns -23.9000 and now we stand at wns -22.6173 we reduced around 1.2827 ns of violation

11. Replace the old netlist with the new netlist generated after timing ECO fix and implement the floorplan, placement and cts.

Now to insert this updated netlist to PnR flow and we can use write_verilog and overwrite the synthesis netlist but before that we are going to make a copy of the old old netlist

Commands to make copy of netlist

```
# Change from home directory to synthesis results directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
25-03_18-52/results/synthesis/
```

```
# List contents of the directory
```

```
ls
```

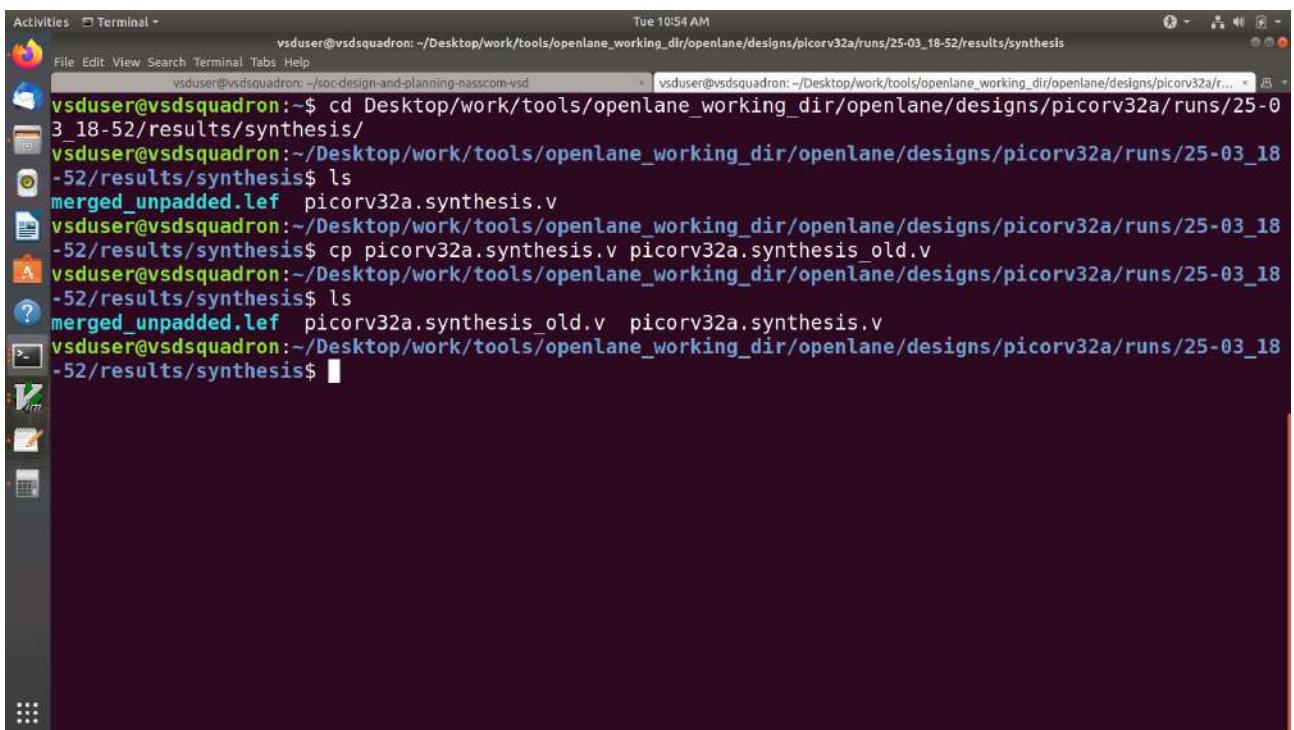
```
# Copy and rename the netlist
```

```
cp picorv32a.synthesis.v picorv32a.synthesis_old.v
```

```
# List contents of the directory
```

```
ls
```

Screenshot of commands run



The screenshot shows a terminal window titled "Terminal" running on a Linux desktop environment. The window title bar includes the text "Activities Terminal" and the date "Tue 10:54 AM". The terminal itself has two tabs open. The current tab displays a command-line session:

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$ ls
merged_unpadded.lef picorv32a.synthesis.v
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$ cp picorv32a.synthesis.v picorv32a.synthesis_old.v
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$ ls
merged_unpadded.lef picorv32a.synthesis_old.v picorv32a.synthesis.v
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$
```

Commands to write verilog

```
# Check syntax
```

```
help write_verilog
```

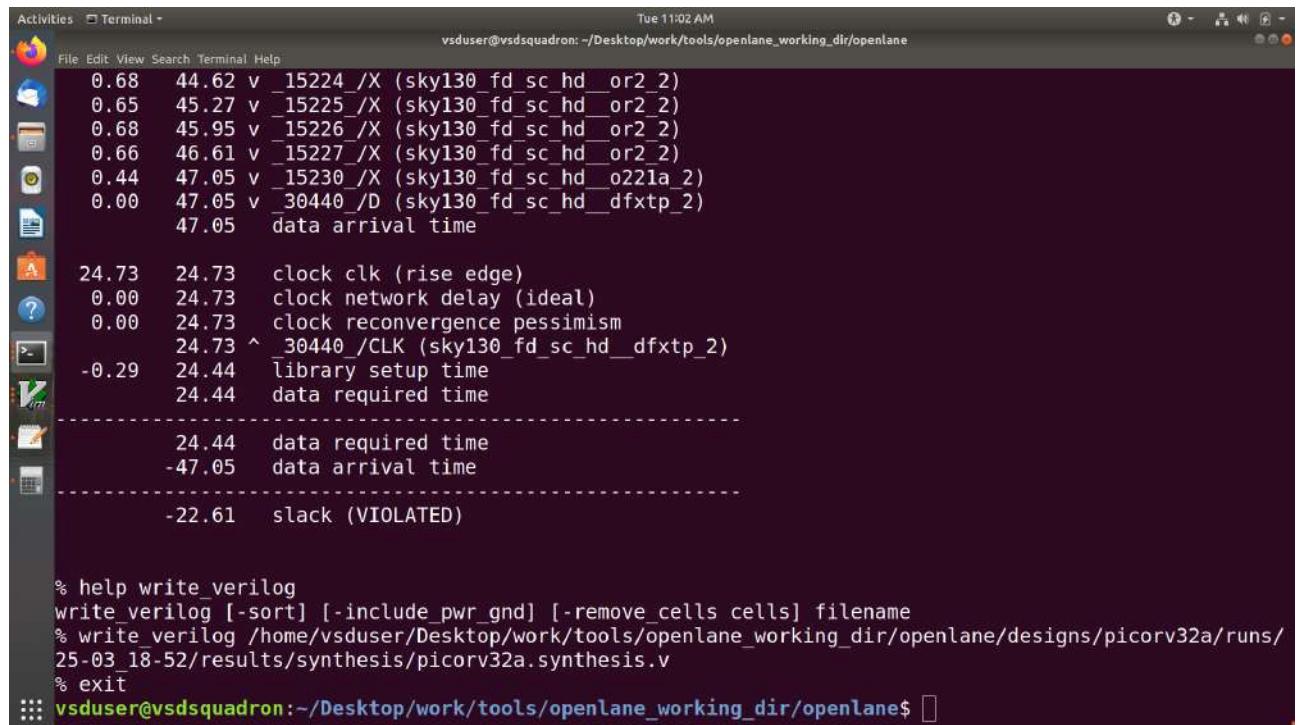
```
# Overwriting current synthesis netlist
```

```
write_verilog /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis/picorv32a.synthesis.v
```

```
# Exit from OpenSTA since timing analysis is done
```

```
exit
```

Screenshot of commands run



The screenshot shows a terminal window with the following content:

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
Tue 11:02 AM
File Edit View Search Terminal Help
0.68 44.62 v _15224_X (sky130_fd_sc_hd_or2_2)
0.65 45.27 v _15225_X (sky130_fd_sc_hd_or2_2)
0.68 45.95 v _15226_X (sky130_fd_sc_hd_or2_2)
0.66 46.61 v _15227_X (sky130_fd_sc_hd_or2_2)
0.44 47.05 v _15230_X (sky130_fd_sc_hd_o221a_2)
0.00 47.05 v _30440_D (sky130_fd_sc_hd_dfxtp_2)
47.05 data arrival time

24.73 24.73 clock clk (rise edge)
0.00 24.73 clock network delay (ideal)
0.00 24.73 clock reconvergence pessimism
24.73 ^ _30440_CLK (sky130_fd_sc_hd_dfxtp_2)
-0.29 24.44 library setup time
24.44 data required time
-----
24.44 data required time
-47.05 data arrival time
-----
-22.61 slack (VIOLATED)

% help write_verilog
write_verilog [-sort] [-include_pwr_gnd] [-remove_cells cells] filename
% write_verilog /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis/picorv32a.synthesis.v
% exit
::: vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$
```

Verified that the netlist is overwritten by checking that instance `_14506_` is replaced with `sky130_fd_sc_hd_or4_4`

```

Activities  M. GVim -
Tue 11:01 AM
picorv32a.synthesis.v (~-/Desktop/work/too...ns/25-03_18-52/results/synthesis) - GVIM2
File Edit Tools Syntax Buffers Window Help
16359     .Y(_11665_));
16360   sky130_fd_sc_hd_o22ai_2 _14504_ (.A1(\irq_mask[21]),
16361     .A2(_11664),
16362     .B1(\irq_mask[23]),
16363     .B2(_11665),
16364     .Y(_11666));
16365   sky130_fd_sc_hd_a221o_2 _14505_ (.A1(_11662),
16366     .A2(\irq_pending[20]),
16367     .B1(_11663),
16368     .B2(\irq_pending[22]),
16369     .C1(_11666),
16370     .X(_11667));
16371   sky130_fd_sc_hd_or4_4 _14506_ (.A(_11649),
16372     .B(_11655),
16373     .C(_11661),
16374     .D(_11667),
16375     .X(_11668));
16376   sky130_vsdinv _14507_ (.A(irq_active),
16377     .Y(_11669));
16378   sky130_vsdinv _14508_ (.A(irq_delay),
16379     .Y(_11670));
16380   sky130_fd_sc_hd_o2111a_2 _14509_ (.A1(_11643),
16381     .A2(_11668),
16382     .B1(_11669),
16383     .C1(_11670),
hlsearch
16371,25      21%

```

Since we confirmed that netlist is replaced and will be loaded in PnR but since we want to follow up on the earlier o violation design we are continuing with the clean design to further stages

Commands load the design and run necessary stages

```
# Now once again we have to prep design so as to update variables
```

```
prep -design picorv32a -tag 24-03_10-03 -overwrite
```

```
# Additional commands to include newly added lef to openlane flow merged.lef
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_STRATEGY
```

```
set ::env(SYNTH_STRATEGY) "DELAY 3"

# Command to set new value for SYNTH_SIZING

set ::env(SYNTH_SIZING) 1

# Now that the design is prepped and ready, we can run synthesis using following
# command

run_synthesis

# Following commands are altogether sourced in "run_floorplan" command

init_floorplan

place_io

tap_decap_or

# Now we are ready to run placement

run_placement

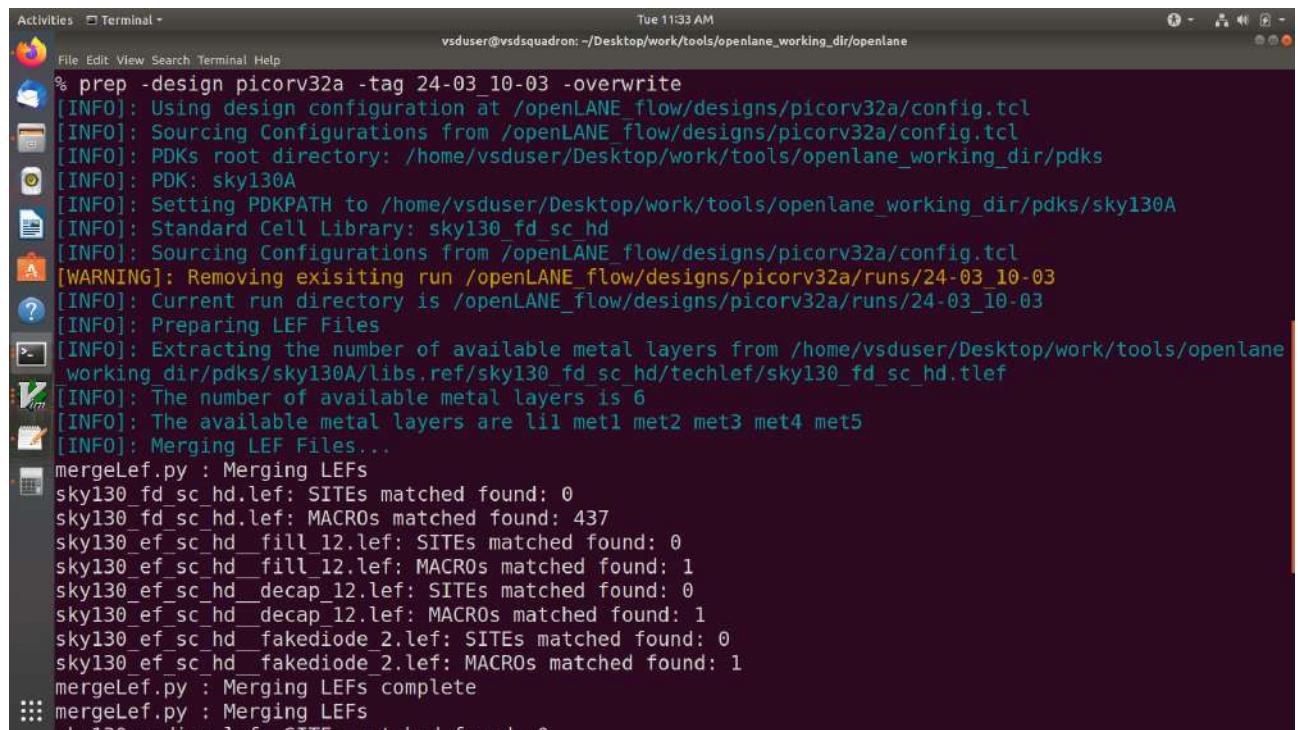
# Incase getting error

unset ::env(LIB_CTS)
```

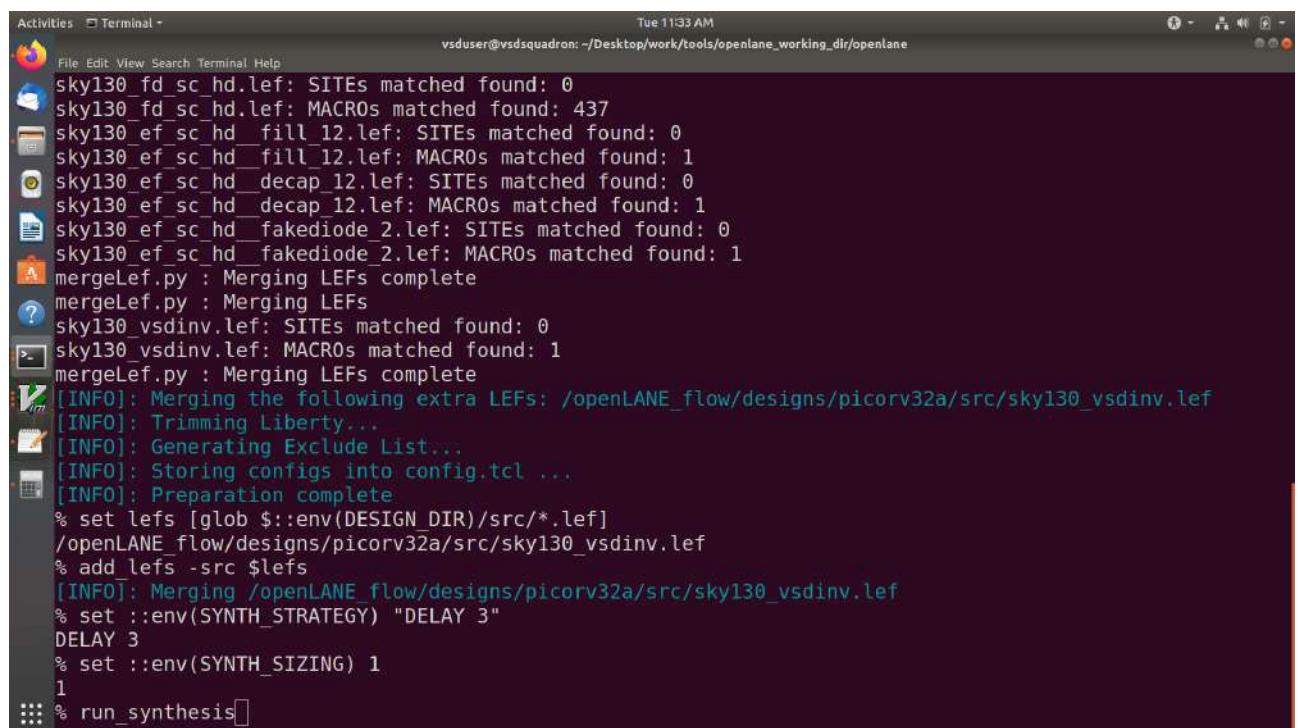
```
# With placement done we are now ready to run CTS
```

```
run_cts
```

Screenshots of commands run



```
Activities Terminal Tue 11:33 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% prep -design picorv32a -tag 24-03_10-03 -overwrite
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130 fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[WARNING]: Removing existing run /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.tlef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1l met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
::: mergeLef.py : Merging LEFs
    120 SITEs and 15 MACROs
```



```
Activities Terminal Tue 11:33 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% set ::env(SYNTH_STRATEGY) "DELAY 3"
DELAY 3
% set ::env(SYNTH_SIZING) 1
1
::: % run_synthesis
```

```
Activities Terminal - Tue 11:35 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
::: % init_floorplan
```

```
Activities Terminal - Tue 11:36 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
% init_floorplan
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 8
OpenROAD 0.9.0 1415572a73
A This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
[INFO IFP-0001] Added 264 rows of 1566 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 731.615 742.335 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/8-verilog2def.die_area.rpt.
[INFO] Floorplanned on a core area of 5.52 10.88 725.88 728.96 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/8-verilog2def.core_area.rpt.
[INFO]: Core area width: 720.36
[INFO]: Core area height: 718.08
[INFO]: Changing layout from 0 to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def
::: % place_io
```

```
Activities Terminal - Tue 11:37 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% place_io
[INFO]: Running IO Placement...
[INFO]: current step index: 9
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def
#Macro blocks found: 0
Using 5u default boundaries offset
Random pin placement
RandomMode Even
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def
::: % tap_decap_or
```

```
Activities Terminal - Tue 11:38 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% place_io
[INFO]: Running IO Placement...
[INFO]: current step index: 9
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def
Step 1: Cut rows...
[INFO TAP-0001] Macro blocks found: 0
[INFO TAP-0002] #Original rows: 264
[INFO TAP-0003] #Cut rows: 0
Step 2: Insert endcaps...
[INFO TAP-0004] #Endcaps inserted: 528
Step 3: Insert tapcells...
[INFO TAP-0005] #Tapcells inserted: 7180
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/floorplan/picorv32a.floorplan.def
::: % run_placement
```

```
Activities Terminal - Tue 11:39 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
legalized HPWL      910806.5 u
delta HPWL          2 %

[INFO DPL-0020] Mirrored 6650 instances
[INFO DPL-0021] HPWL before      910806.5 u
[INFO DPL-0022] HPWL after       895297.0 u
[INFO DPL-0023] HPWL delta      -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/11-resize.r.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 15
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
% run_cts
```

```
Activities Terminal - Tue 12:00 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 25690 components and 145610 component-terminals.
Notice 0:     Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
[INFO]: Changing netlist from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis_optimized.v to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis_cts.v
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 19
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def.png'
Done
[INFO]: Screenshot taken.
% 
```

12. Post-CTS OpenROAD timing analysis.

Commands to be run in OpenLANE flow to do OpenROAD timing analysis with integrated OpenSTA in OpenROAD

```
# Command to run OpenROAD tool
```

```
openroad
```

```
# Reading lef file
```

```
read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
```

```
# Reading def file
```

```
read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
```

```
# Creating an OpenROAD database to work with
```

```
write_db pico_cts.db
```

```
# Loading the created database in OpenROAD
```

```
read_db pico_cts.db
```

```
# Read netlist post CTS
```

```
read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/  
picorv32a.synthesis_cts.v
```

```
# Read library for design
```

```
read_liberty $::env(LIB_SYNTH_COMPLETE)
```

```
# Link design and library

link_design picorv32a

# Read in the custom sdc we created

read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc

# Setting all cloks as propagated clocks

set_propagated_clock [all_clocks]

# Check syntax of 'report_checks' command

help report_checks

# Generating custom timing report

report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format
full_clock_expanded -digits 4

# Exit to OpenLANE flow

exit
```

Screenshots of commands run and timing report generated

```
Activities Terminal - Tue 12:55 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% openroad
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
% read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
% read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 25690 components and 145610 component-terminals.
Notice 0:     Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
% write_db pico_cts.db
% read_db pico_cts.db
% read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis
_cts.v
% read_liberty $::env(LIB_SYNTH_COMPLETE)
1
% link_design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_tapvpwrvgnd_1 has no liberty cell.
```

```

Activities Terminal - Tue 12:58 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
11 0.0206
    0.0650  0.0000  1.6203 ^ _30955/_CLK (sky130_fd_sc_hd_dfxtp_2)
    0.0000  1.6203  clock reconvergence pessimism
   -0.0263  1.5941  library hold time
    1.5941  data required time
-----
    1.5941  data required time
   -1.8059  data arrival time
-----
    0.2119  slack (MET)

Startpoint: resetn (input port clocked by clk)
Endpoint: mem_la_read (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
----- 0.0000 0.0000 0.0000 0.0000 clock clk (rise edge)
          0.0000 0.0000 4.9460 4.9460 ^ input external delay
          0.0172 0.0055 4.9515 ^ resetn (in)
          0.0042 0.0172 0.0000 4.9515 ^ input101/A (sky130_fd_sc_hd_clkbuf_8)
          0.0582 0.1265 5.0780 ^ input101/X (sky130_fd_sc_hd_clkbuf_8)
          0.0234 0.0582 0.0000 5.0780 ^ net101 (net)

```

```

Activities Terminal - Tue 11:09 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
6 0.0270
    0.0947  0.0000  5.2526 ^ 12638_(net)
    0.1284  0.1277  5.3802 v 17093/_C (sky130_fd_sc_hd_nand3_4)
          0.1284  0.0000  5.3802 v 17093/_Y (sky130_fd_sc_hd_nand3_4)
          0.0799  0.1239  5.5041 ^ 13857_(net)
          0.0023 0.0799 0.0000 5.5041 ^ 18867/_B1 (sky130_fd_sc_hd_a21oi_4)
          0.0799  0.0000 5.5041 ^ 18867/_Y (sky130_fd_sc_hd_a21oi_4)
          0.0177 0.1052 0.1596 5.6637 ^ net199_(net)
          0.1052 0.0000 5.6637 ^ output199/A (sky130_fd_sc_hd_clkbuf_2)
          0.1052 0.0000 5.6637 ^ output199/X (sky130_fd_sc_hd_clkbuf_2)
          0.0000 0.0000 24.7300 24.7300 clock clk (rise edge)
          0.0000 0.0000 24.7300 24.7300 clock network delay (propagated)
          0.0000 0.0000 24.7300 24.7300 clock reconvergence pessimism
         -4.9460 19.7840 19.7840 output external delay
         19.7840 19.7840 data required time
         -5.6637 14.1203 14.1203 data arrival time
-----
         19.7840 14.1203 slack (MET)

% exit
%
```

**13. Explore post-CTS OpenROAD timing analysis by removing
'sky130_fd_sc_hd_clkbuf_1' cell from clock buffer list variable
'CTS_CLK_BUFFER_LIST'.**

**Commands to be run in OpenLANE flow to do OpenROAD timing analysis after
changing CTS_CLK_BUFFER_LIST**

```
# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)

# Removing 'sky130_fd_sc_hd_clkbuf_1' from the list

set ::env(CTS_CLK_BUFFER_LIST) [lreplace $::env(CTS_CLK_BUFFER_LIST) 0 0]

# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)

# Checking current value of 'CURRENT_DEF'

echo $::env(CURRENT_DEF)

# Setting def as placement def

set ::env(CURRENT_DEF) /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/
placement/picorv32a.placement.def

# Run CTS again

run_cts

# Checking current value of 'CTS_CLK_BUFFER_LIST'
```

```
echo $::env(CTS_CLK_BUFFER_LIST)

# Command to run OpenROAD tool

openroad

# Reading lef file

read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef

# Reading def file

read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def

# Creating an OpenROAD database to work with

write_db pico_cts1.db

# Loading the created database in OpenROAD

read_db pico_cts.db

# Read netlist post CTS

read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/
picorv32a.synthesis_cts.v
```

```
# Read library for design

read_liberty $::env(LIB_SYNTH_COMPLETE)

# Link design and library

link_design picorv32a

# Read in the custom sdc we created

read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc

# Setting all cloks as propagated clocks

set_propagated_clock [all_clocks]

# Generating custom timing report

report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format
full_clock_expanded -digits 4

# Report hold skew

report_clock_skew -hold
```

```
# Report setup skew

report_clock_skew -setup

# Exit to OpenLANE flow

exit

# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)

# Inserting 'sky130_fd_sc_hd__clkbuf_1' to first index of list

set ::env(CTS_CLK_BUFFER_LIST) [linsert $::env(CTS_CLK_BUFFER_LIST) 0
sky130_fd_sc_hd__clkbuf_1]

# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)
```

Screenshots of commands run and timing report generated

```
Activities Terminal - Tue 1:42 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_
8
% set ::env(CTS_CLK_BUFFER_LIST) [lreplace $::env(CTS_CLK_BUFFER_LIST) 0 0]
sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
% set ::env(CURRENT_DEF) /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
% run_cts
[INFO]: Running TritonCTS...
[INFO]: current step index: 20
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Done
```

```
Activities Terminal - Tue 1:45 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def.png'
Done
[INFO]: Screenshot taken.
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% openroad
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
% read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
% read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 25690 components and 145610 component-terminals.
Notice 0: Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
% write_db pico_cts1.db
% read_db pico_cts.db
```

```

Activities Terminal - Tue 1:48 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% write_db pico_cts1.db
% read_db pico_cts.db
% read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis
_cts.v
% read_liberty $::env(LIB_SYNTH_COMPLETE)
1
% link_design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_tapvpwrvgnd_1 has no liberty cell.
% read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
[INFO]: Setting output delay to: 4.946000000000001
[INFO]: Setting input delay to: 4.946000000000001
[INFO]: Setting load to: 0.017653
% set_propagated_clock [all_clocks]
% report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
Startpoint: _30990_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30955_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----  

1 0.0079 0.0225 0.0000 0.0100 ^ clkbuf_0_clk/A (sky130_fd_sc_hd_clkbuf_16)  

0.0225 0.0000 0.0100 ^ clkbuf_0_clk/X (sky130_fd_sc_hd_clkbuf_16)
0.0225 0.0000 0.0100 ^ clkbuf_0_clk/Y (sky130_fd_sc_hd_clkbuf_16)

```

```

Activities Terminal - Tue 1:48 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
0.0520 0.0000 1.2459 ^ _30955/_CLK (sky130_fd_sc_hd_dfxtpl_2)
0.0000 1.2459 clock reconvergence pessimism
-0.0280 1.2179 library hold time
1.2179 data required time
-----  

1.2179 data required time
-1.5305 data arrival time
-----  

0.3125 slack (MET)

Startpoint: resetn (input port clocked by clk)
Endpoint: mem_la_read (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
-----  

1 0.0042 0.0172 0.0000 4.9460 0.0000 ^ clock clk (rise edge)
0.0000 0.0000 ^ clock network delay (propagated)
4.9460 4.9460 ^ input external delay
0.0172 0.0055 4.9515 ^ resetn (in)
resetn (net)
7 0.0234 0.0172 0.0000 4.9515 ^ input101/A (sky130_fd_sc_hd_clkbuf_8)
0.0582 0.1265 5.0780 ^ input101/X (sky130_fd_sc_hd_clkbuf_8)
0.0582 0.0000 5.0780 ^ net101 (net)
0.0582 0.0000 5.0780 ^ 15304/A (sky130_fd_sc_hd_clkbuf_4)
0.0042 0.1746 5.2526 ^ 15304/X (sky130_fd_sc_hd_clkbuf_4)

```

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      Tue 1:50 PM
          -4.9460  19.7840  output external delay
          19.7840  data required time
          19.7840  data required time
          -5.6637  data arrival time
          14.1203  slack (MET)

% report_clock_skew -hold
Clock clk
Latency CRPR Skew
_31226 /CLK ^
    1.36
_32416 /CLK ^
    0.94    0.00    0.42

% report_clock_skew -setup
Clock clk
Latency CRPR Skew
_31226 /CLK ^
    1.36
_32416 /CLK ^
    0.94    0.00    0.42

% exit
%
```

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      Tue 1:53 PM
          % echo $::env(CTS_CLK_BUFFER_LIST)
          sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
          % set ::env(CTS_CLK_BUFFER_LIST) [linsert $::env(CTS_CLK_BUFFER_LIST) 0 sky130_fd_sc_hd_clkbuf_1]
          sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_
          8
          % echo $::env(CTS_CLK_BUFFER_LIST)
          sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_
          8
%
```

Section 5 - Final steps for RTL2GDS using tritonRoute and openSTA (25/03/2024 - 26/03/2024)

Theory

Implementation

- **Section 5 tasks:-**
25. Perform generation of Power Distribution Network (PDN) and explore the PDN layout.
 26. Perform detailed routing using TritonRoute.
 27. Post-Route parasitic extraction using SPEF extractor.
 28. Post-Route OpenSTA timing analysis with the extracted parasitics of the route.
- All section 5 logs, reports and results can be found in following run folder:

Section 5 Run - 26-03_08-45

1. Perform generation of Power Distribution Network (PDN) and explore the PDN layout.

Commands to perform all necessary stages up until now

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:vo.21'
```

```
# Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command
```

```
docker
```

```
# Now that we have entered the OpenLANE flow contained docker sub-system we can  
invoke the OpenLANE flow in the Interactive mode using the following command
```

```
./flow.tcl -interactive
```

```
# Now that OpenLANE flow is open we have to input the required packages for proper  
functionality of the OpenLANE flow
```

```
package require openlane 0.9
```

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the  
design creating some necessary files and directories for running a specific design which in  
our case is 'picorv32a'
```

```
prep -design picorv32a
```

```
# Additional commands to include newly added lef to openlane flow merged.lef
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_STRATEGY
```

```
set ::env(SYNTH_STRATEGY) "DELAY 3"
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

Now that the design is prepped and ready, we can run synthesis using following command

```
run_synthesis
```

Following commands are altogether sourced in "run_floorplan" command

```
init_floorplan
```

```
place_io
```

```
tap_decap_or
```

Now we are ready to run placement

```
run_placement
```

```
# Incase getting error
```

```
unset ::env(LIB_CTS)
```

With placement done we are now ready to run CTS

```
run_cts
```

Now that CTS is done we can do power distribution network

gen_pdn

Screenshots of power distribution network run

```
Activities Terminal Tue 2:22 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: Screenshot taken.
% gen pdn
[INFO]: Generating PDN...
[INFO]: current step index: 14
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 25690 components and 145610 component-terminals.
Notice 0:     Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/cts/picorv32a.cts.def
[INFO] [PDNG-0016] Power Delivery Network Generator: Generating PDN
[INFO] [PDNG-0016] config: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdkss/sky130A/libs.tech/openlane/common_pdn.tcl
[INFO] [PDNG-0008] Design Name is picorv32a
[INFO] [PDNG-0009] Reading technology data
[INFO] [PDNG-0011] ***** INFO *****
Tunne: stdcell -mid
```

```
Activities Terminal Tue 2:22 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[WARNING PSM-0030] Vsrc location at (705.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
[WARNING PSM-0030] Vsrc location at (425.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 563.420um).
[WARNING PSM-0030] Vsrc location at (705.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 710.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 716.600um).
[WARNING PSM-0030] Vsrc location at (705.520um, 710.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 716.600um).
[INFO PSM-0031] Number of nodes on net VGND = 24383.
[INFO PSM-0037] G matrix created successfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/cts/picorv32a.cts.def to /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
% 
```

Commands to load PDN def in magic in another terminal

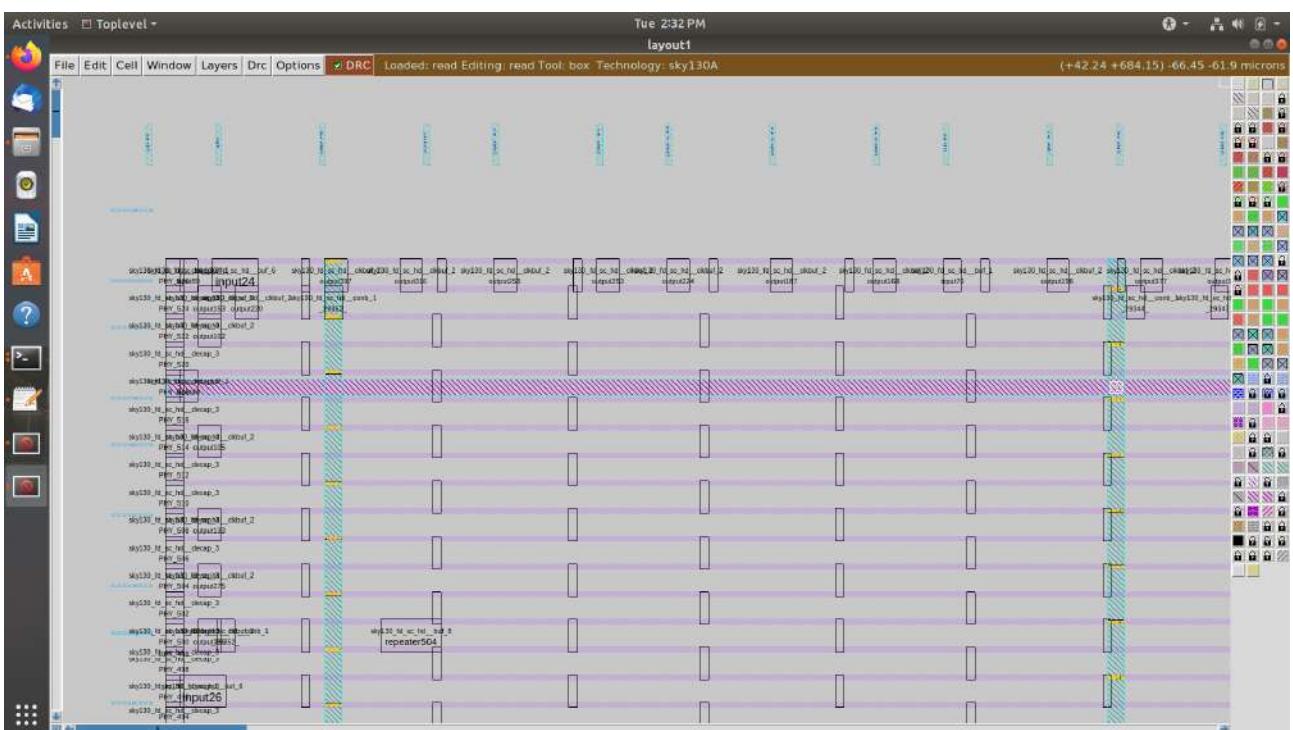
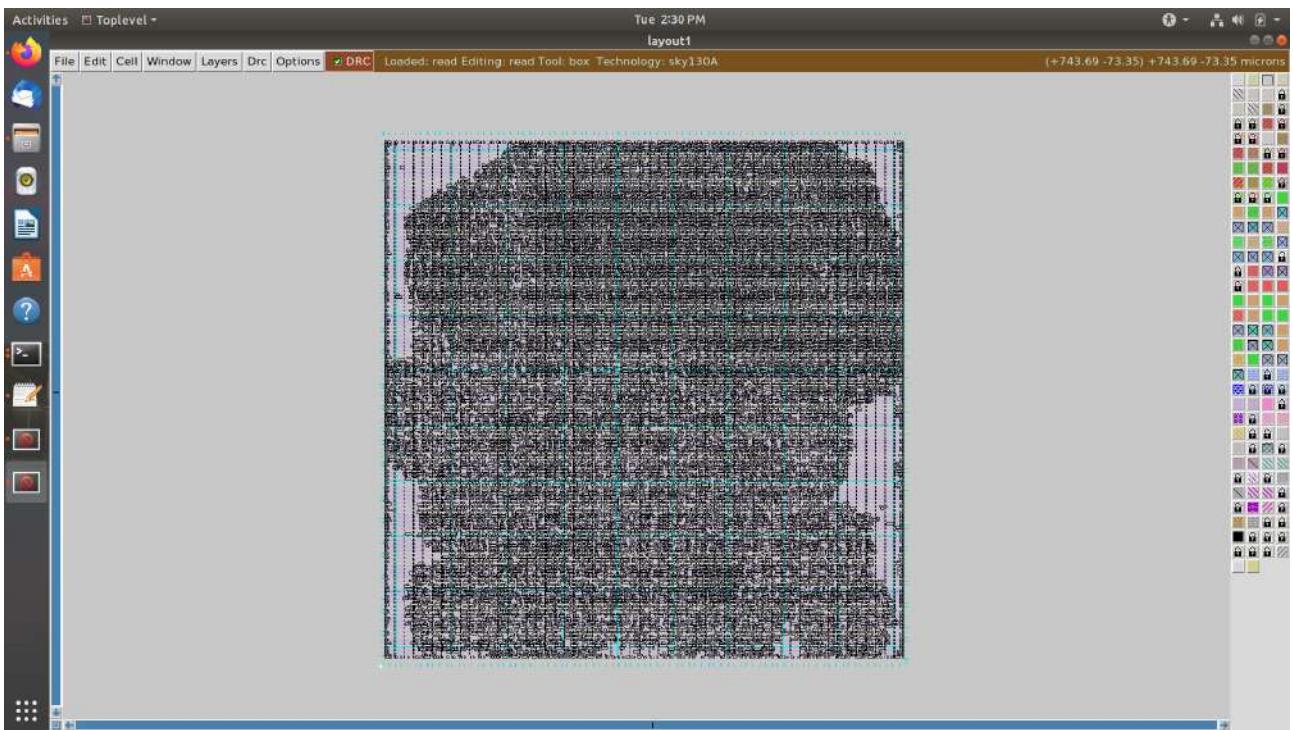
```
# Change directory to path containing generated PDN def
```

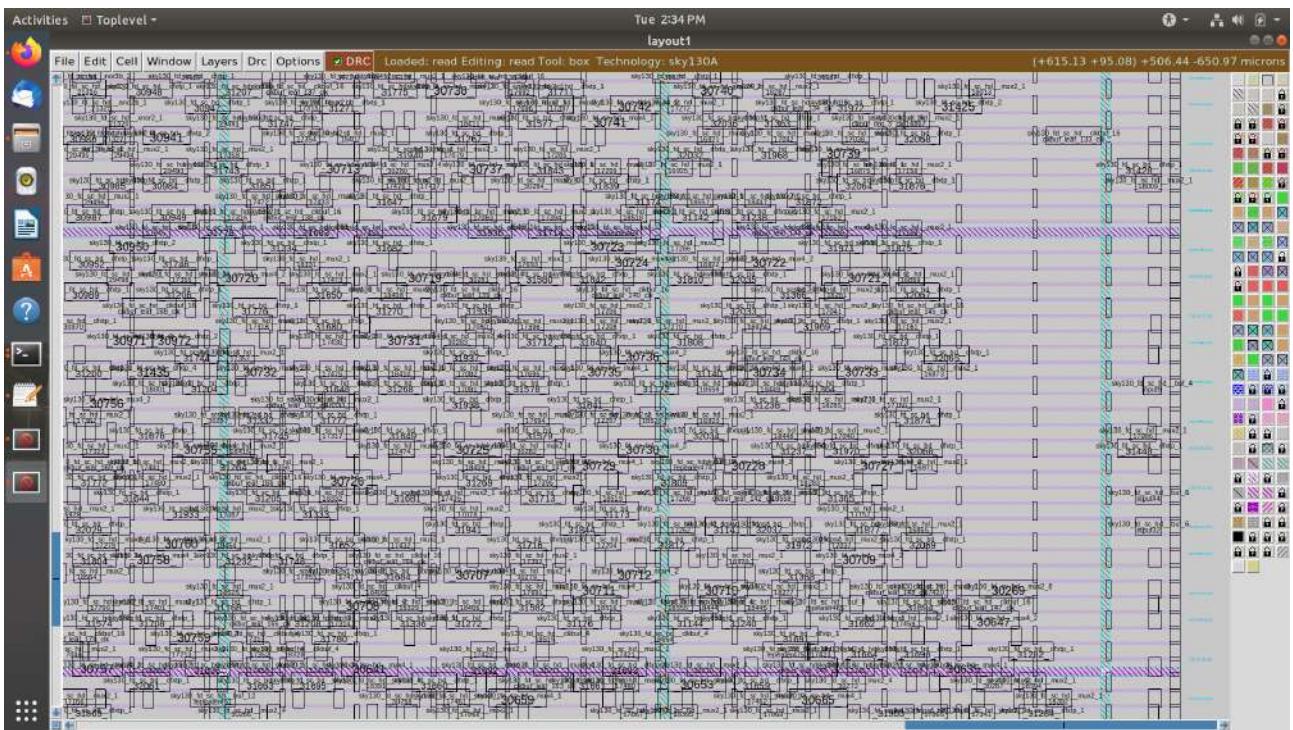
```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/  
26-03_08-45/tmp/floorplan/
```

```
# Command to load the PDN def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read 14-pdn.def &
```

Screenshots of PDN def





2. Perform detailed routing using TritonRoute and explore the routed layout.

Command to perform routing

```
# Check value of 'CURRENT_DEF'
```

```
echo $::env(CURRENT_DEF)
```

```
# Check value of 'ROUTING_STRATEGY'
```

```
echo $::env(ROUTING_STRATEGY)
```

```
# Command for detailed route using TritonRoute
```

```
run_routing
```

Screenshots of routing run

```
Activities Terminal - Tue 2:48 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
% echo $::env(ROUTING_STRATEGY)
can't read "::env(ROUTING_STRATEGY)": no such variable
% run_routing
[INFO]: Routing...
[INFO]: Running Global Routing...
[INFO]: current step index: 15
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
Notice 0: Design: picorv32a
Notice 0: Created 411 pins.
Notice 0: Created 25690 components and 145610 component-terminals.
Notice 0: Created 2 special nets and 0 connections.
Notice 0: Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
Min routing layer: 2
Max routing layer: 6
```

```
Activities Terminal - Tue 3:38 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
elapsed time = 00:00:08, memory = 782.73 (MB)
completing 60% with 0 violations
elapsed time = 00:00:10, memory = 782.73 (MB)
completing 70% with 0 violations
elapsed time = 00:00:12, memory = 782.73 (MB)
completing 80% with 0 violations
elapsed time = 00:00:14, memory = 782.73 (MB)
completing 90% with 0 violations
elapsed time = 00:00:15, memory = 782.73 (MB)
completing 100% with 0 violations
elapsed time = 00:00:17, memory = 782.73 (MB)
number of violations = 0
cpu time = 00:00:16, elapsed time = 00:00:17, memory = 782.73 (MB), peak = 854.19 (MB)
total wire length = 1103187 um
total wire length on LAYER l1l = 2639 um
total wire length on LAYER met1 = 483058 um
total wire length on LAYER met2 = 482317 um
total wire length on LAYER met3 = 122196 um
total wire length on LAYER met4 = 12976 um
total wire length on LAYER met5 = 0 um
total number of vias = 145509
up-via summary (total 145509):

-----
FR_MASTERSLICE      0
      l1l    60472
      met1   78129
      met2   6540
```

```
Tue 3:29 PM  
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane  
File Edit View Search Terminal Help  
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]  
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]  
puts "[INFO]: Setting output delay to: $output_delay_value"  
[INFO]: Setting output delay to: 4.946000000000001  
puts "[INFO]: Setting input delay to: $input_delay_value"  
[INFO]: Setting input delay to: 4.946000000000001  
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]  
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]  
#set rst_indx [lsearch [all_inputs] [get_port resetn]]  
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]  
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]  
set all_inputs_wo_clk_rst $all_inputs_wo_clk  
# correct resetn  
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst  
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}  
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]  
# TODO set this as parameter  
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]  
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]  
puts "[INFO]: Setting load to: $cap_load"  
[INFO]: Setting load to: 0.01765  
set_load $cap_load [all_outputs]  
tns 0.00  
wns 0.00  
[INFO]: Calculating Runtime From the Start...  
[INFO]: Routing completed for picorv32a/26-03_08-45 in 1h7m11s  
::: %
```

Commands to load routed def in magic in another terminal

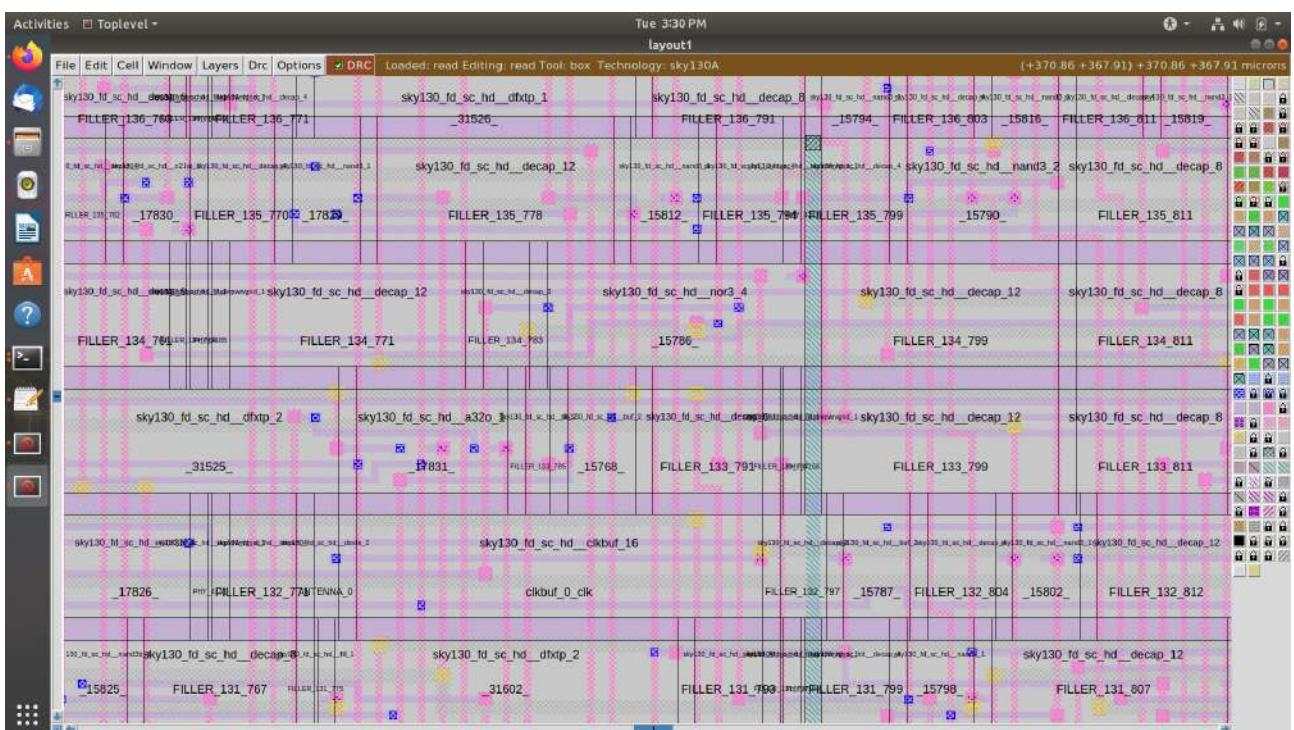
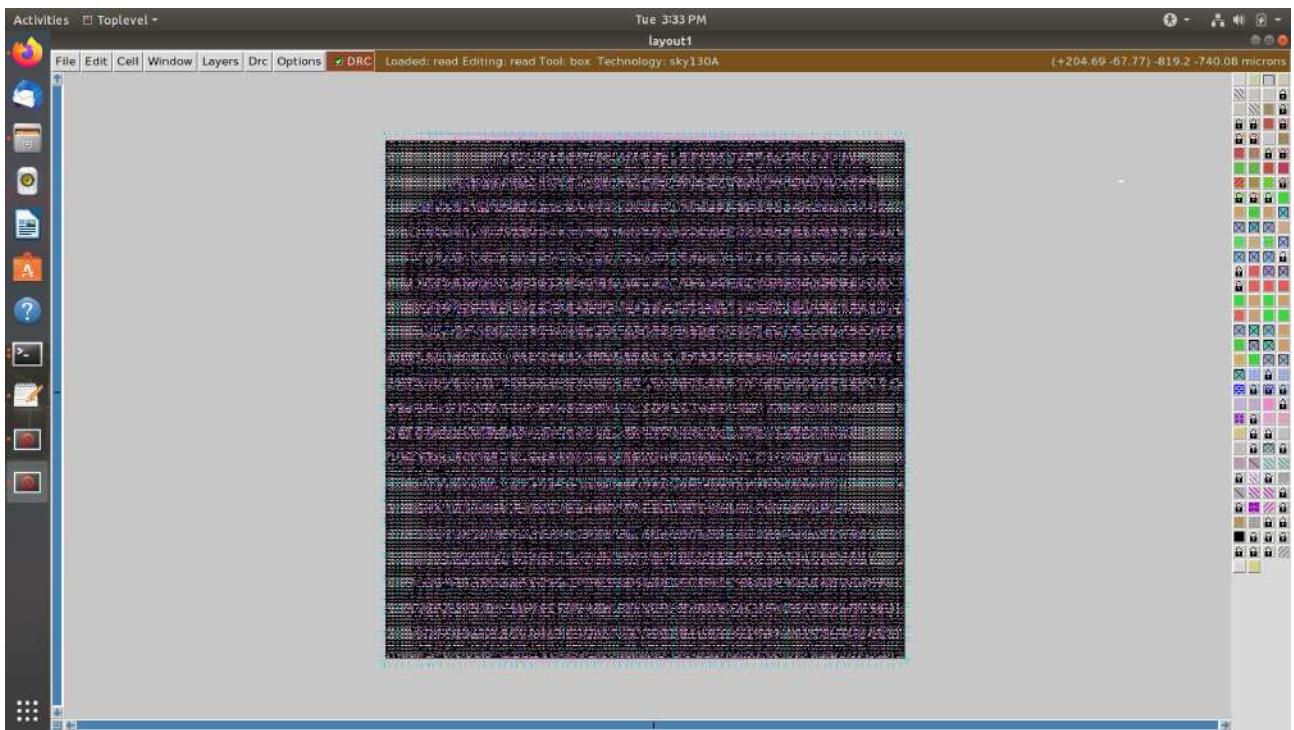
Change directory to path containing routed def

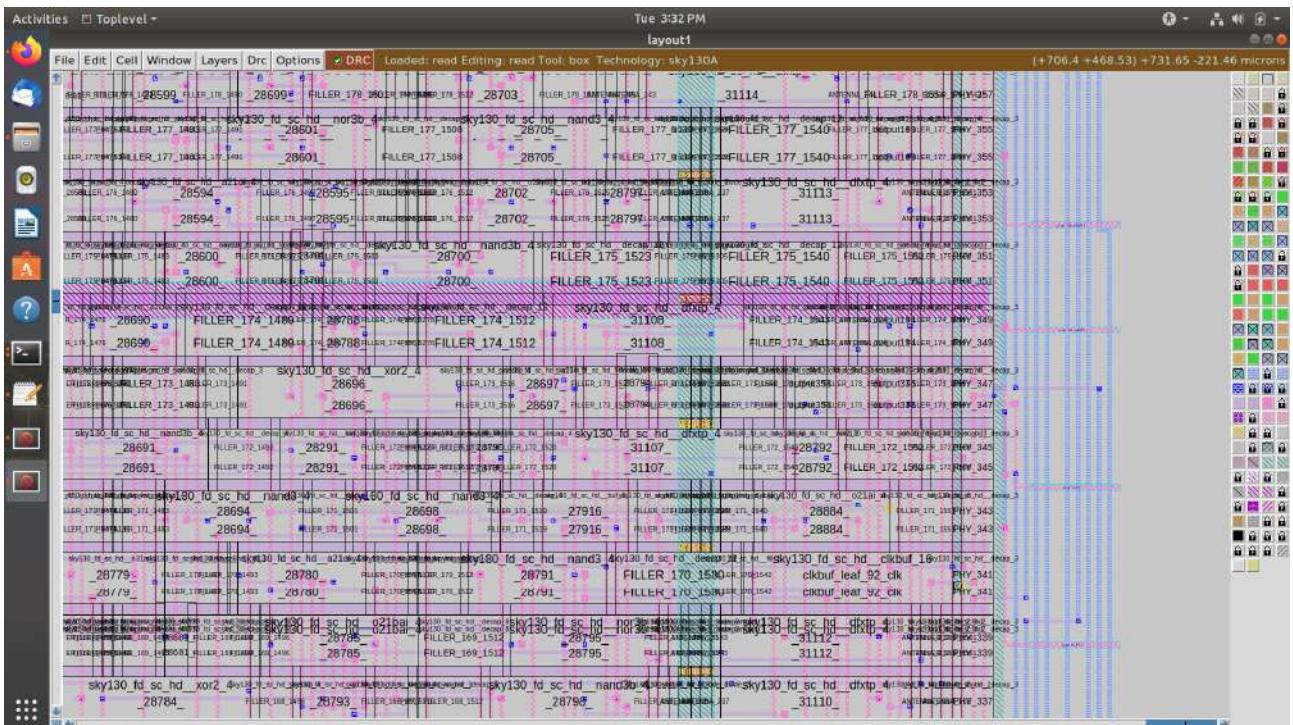
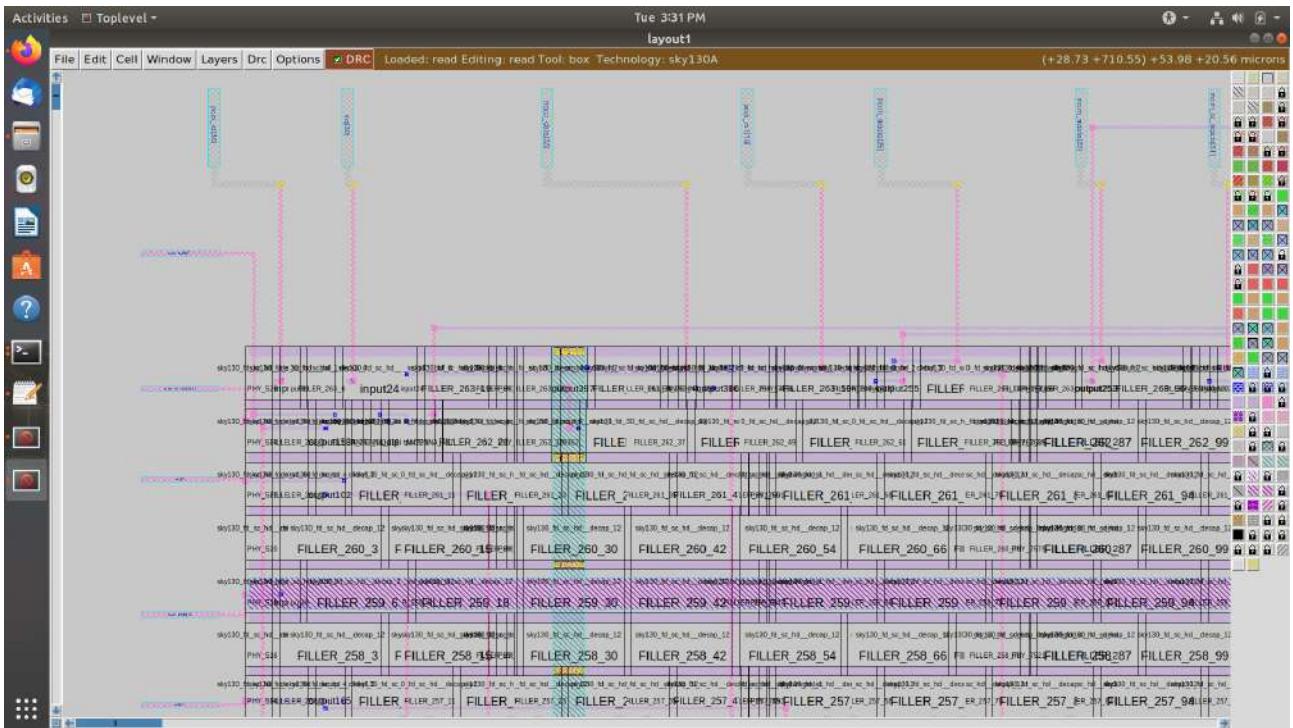
```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/  
26-03_08-45/results/routing/
```

Command to load the routed def in magic tool

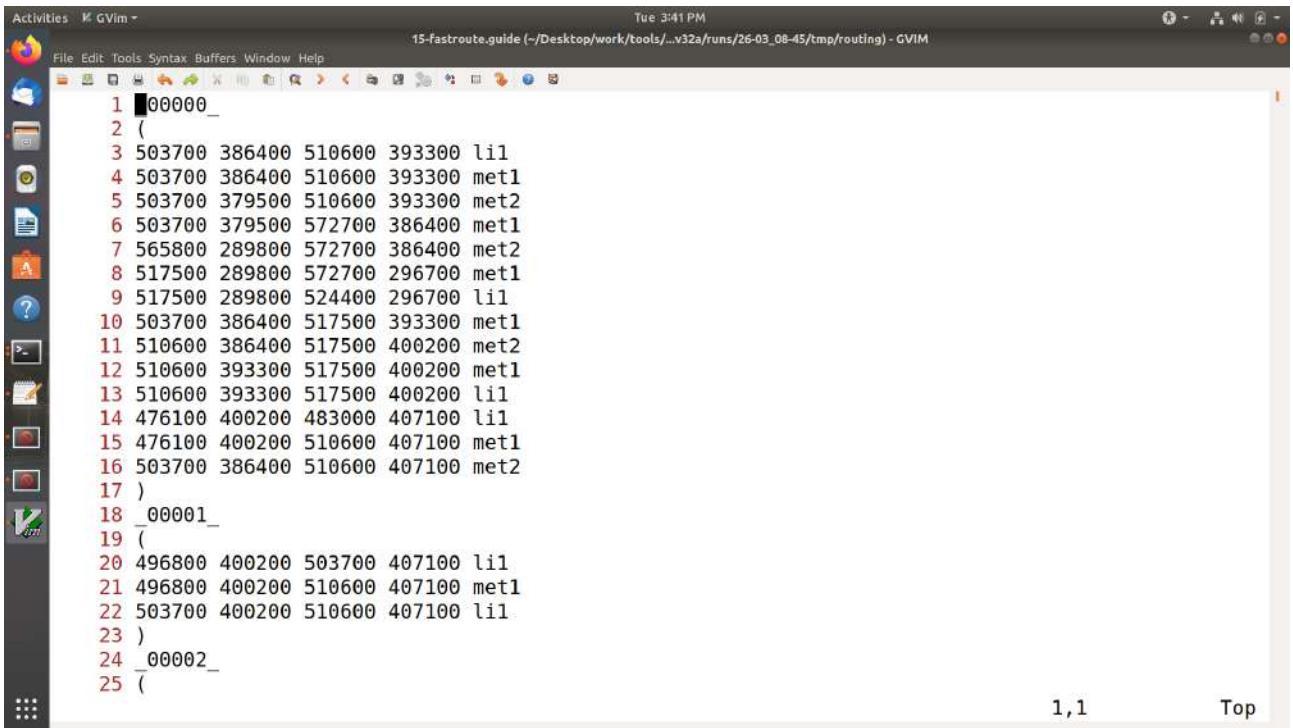
```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.def &
```

Screenshots of routed def





Screenshot of fast route guide present in openlane/designs/picorv32a/runs/26-03_08-45/tmp/routing directory



The screenshot shows a terminal window titled "Activities" with "GVim" selected. The title bar indicates the file is "15-fastroute.guide (~/Desktop/work/tools/...v32a/runs/26-03_08-45/tmp/routing) - GVIM" and the time is "Tue 3:41 PM". The GVim interface has a toolbar with icons for file operations like Open, Save, and Cut/Paste. The left sidebar contains a file tree and a search bar. The main editor area displays the following text:

```
1 _00000_
2 (
3 503700 386400 510600 393300 l1l
4 503700 386400 510600 393300 met1
5 503700 379500 510600 393300 met2
6 503700 379500 572700 386400 met1
7 565800 289800 572700 386400 met2
8 517500 289800 572700 296700 met1
9 517500 289800 524400 296700 l1l
10 503700 386400 517500 393300 met1
11 510600 386400 517500 400200 met2
12 510600 393300 517500 400200 met1
13 510600 393300 517500 400200 l1l
14 476100 400200 483000 407100 l1l
15 476100 400200 510600 407100 met1
16 503700 386400 510600 407100 met2
17 )
18 _00001_
19 (
20 496800 400200 503700 407100 l1l
21 496800 400200 510600 407100 met1
22 503700 400200 510600 407100 l1l
23 )
24 _00002_
25 )
```

The status bar at the bottom right shows "1,1" and "Top".

3. Post-Route parasitic extraction using SPEF extractor.

Commands for SPEF extraction using external tool

```
# Change directory
```

```
cd Desktop/work/tools/SPEF_EXTRACTOR
```

```
# Command extract spef
```

```
python3 main.py /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/
designs/picorv32a/runs/26-03_08-45/tmp/merged.lef /home/vsduser/Desktop/work/tools/
openlane_working_dir/openlane/designs/picorv32a/runs/26-03_08-45/results/routing/
picorv32a.def
```

4. Post-Route OpenSTA timing analysis with the extracted parasitics of the route.

Commands to be run in OpenLANE flow to do OpenROAD timing analysis with integrated OpenSTA in OpenROAD

```
# Command to run OpenROAD tool
```

```
openroad
```

```
# Reading lef file
```

```
read_lef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
```

```
# Reading def file
```

```
read_def /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/  
picorv32a.def
```

```
# Creating an OpenROAD database to work with
```

```
write_db pico_route.db
```

```
# Loading the created database in OpenROAD
```

```
read_db pico_route.db
```

```
# Read netlist post CTS
```

```
read_verilog /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/synthesis/  
picorv32a.synthesis_preroute.v
```

```
# Read library for design

read_liberty $::env(LIB_SYNTH_COMPLETE)

# Link design and library

link_design picorv32a

# Read in the custom sdc we created

read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc

# Setting all cloks as propagated clocks

set_propagated_clock [all_clocks]

# Read SPEF

read_spef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/
picorv32a.spef

# Generating custom timing report

report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format
full_clock_expanded -digits 4
```

```
# Exit to OpenLANE flow
```

```
exit
```

Screenshots of commands run and timing report generated

```

Activities Terminal - Tue 11:16 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% openroad
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
% read_lef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
% read_def /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.def
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.def
Notice 0: Design: picorv32a
Notice 0: Created 429 pins.
Notice 0: Created 65617 components and 305814 component-terminals.
Notice 0: Created 2 special nets and 0 connections.
Notice 0: Created 18084 nets and 60532 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.def
% write_db pico_route.db
% read_db pico_route.db
% read_verilog /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/synthesis/picorv32a.synthesis_preroute.v
% read_liberty /openLANE_flow/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib
1
::: % link design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_fill_1 has no liberty cell.

```

```

Activities Terminal - Tue 11:17 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% link_design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_fill_1 has no liberty cell.
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_fill_2 has no liberty cell.
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_tapvpwrvrnd_1 has no liberty cell.
% read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
[INFO]: Setting output delay to: 4.9460000000000001
[INFO]: Setting input delay to: 4.9460000000000001
[INFO]: Setting load to: 0.017653
% set_propagated_clock [all_clocks]
% read_spef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.spef
1
% report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
Startpoint: _30900_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30910_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----
                           0.0000  0.0000  clock clk (rise edge)
                           0.0000  0.0000  clock source latency
                           0.0897  0.0624  0.0624 ^ clk (in)
                           0.0563          clk (net)
                           0.0900  0.0000  0.0624 ^ clkbuf_0_clk/A (sky130_fd_sc_hd_clkbuff_16)
                           0.0371  0.1366  0.1990 ^ clkbuf_0_clk/X (sky130_fd_sc_hd_clkbuff_16)
                           2     0.0143          clknet_0_clk (net)

```

```

Activities Terminal - Tue 11:17 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      5  0.0099
      0.0596  0.0002  2.3273 ^ clknet_leaf_220_clk (net)
      0.0000  2.3273  clock reconvergence pessimism
      -0.0274  2.2998  library hold time
      2.2998  data required time
      2.2998  data required time
      -1.9092  data arrival time
      -0.3907  slack (VIOLATED)

Startpoint: resetn (input port clocked by clk)
Endpoint: mem_la_read (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout   Cap     Slew     Delay    Time   Description
-----+-----+-----+-----+-----+
          0.0000  0.0000  clock clk (rise edge)
          0.0000  0.0000  clock network delay (propagated)
          4.9460  4.9460 ^ input external delay
          0.0172  0.0055  4.9515 ^ resetn (in)
          1  0.0042   resetn (net)
          0.0172  0.0000  4.9515 ^ input101/A (sky130_fd_sc_hd_clkbuf_8)
          0.0662  0.1329  5.0843 ^ input101/X (sky130_fd_sc_hd_clkbuf_8)
          7  0.0299   net101 (net)

```

```

Activities Terminal - Tue 11:17 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      6  0.0211
      0.0760  0.0002  5.2498 ^ 12638_(net)
      0.0933  0.0927  5.3425 v 17093/_C (sky130_fd_sc_hd_nand3_4)
      4  0.0143
      0.0933  0.0001  5.3426 v 17093/_Y (sky130_fd_sc_hd_nand3_4)
      0.4344  0.3758  5.7184 ^ 13857_(net)
      2  0.0603
      0.4349  0.0115  5.7299 ^ 18867/_B1 (sky130_fd_sc_hd_a21oi_4)
      0.1189  0.2493  5.9793 ^ 18867/_Y (sky130_fd_sc_hd_a21oi_4)
      1  0.0177
      0.1189  0.0002  5.9795 ^ net199 (net)
      0.1189  0.0002  5.9795 ^ mem_la_read (net)
      24.7300  24.7300  clock clk (rise edge)
      0.0000  24.7300  clock network delay (propagated)
      0.0000  24.7300  clock reconvergence pessimism
      -4.9460  19.7840  output external delay
      19.7840  data required time
      -5.9795  data arrival time
      13.8045  slack (MET)

% exit
%
```

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2 Week digital VLSI SoC design and planning workshop with complete RTL2GDSII flow organised by VSD in collaboration with NASSCOM (Advanced Physical Design using OpenLANE/Sky130)

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History

Desktop/work/tools/ openlane working dir	Add files via upload	

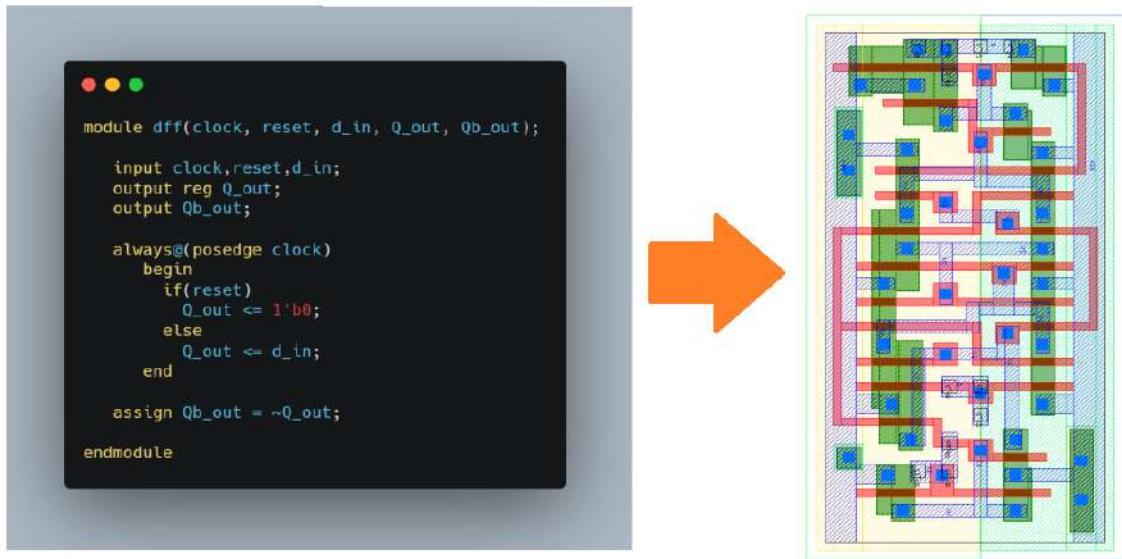
drc test	Add files via upload	

README.m d	Update README.md	

drc tests.tg z	Add files via upload	

Repository files navigation

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Digital VLSI SoC Design & Planning (RTL2GDSII Flow)

Digital VLSI SoC Design and Planning

OS linux

EDA Tools OpenLANE-Flow, Yosys, abc, OpenROAD, TritonRoute, OpenSTA, magic, netgen, GUNA

languages verilog, bash, TCL last commit last wednesday languages 12

verilog 96.2% repo size 179 MB code size 32.9 MB files 4

2 Week digital VLSI SoC design and planning workshop with complete RTL2GDSII flow organised by VSD in collaboration with NASSCOM

Section 1 - Inception of open-source EDA, OpenLANE and Sky130 PDK (14/03/2024 - 15/03/2024)

Theory

Expand or Collapse

Implementation

Section 1 tasks:-

1. Run 'picorv32a' design synthesis using OpenLANE flow and generate necessary outputs.
2. Calculate the flop ratio.

- All section 1 logs, reports and results can be found in following run folder:

Section 1 Run - 15-03_15-51

1. Run 'picorv32a' design synthesis using OpenLANE flow and generate necessary outputs.

Commands to invoke the OpenLANE flow and perform synthesis

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:vo.21'
```

```
# Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command
```

```
docker
```

```
# Now that we have entered the OpenLANE flow contained docker sub-system we can  
invoke the OpenLANE flow in the Interactive mode using the following command
```

```
./flow.tcl -interactive
```

```
# Now that OpenLANE flow is open we have to input the required packages for proper  
functionality of the OpenLANE flow
```

```
package require openlane 0.9
```

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the  
design creating some necessary files and directories for running a specific design which in  
our case is 'picorv32a'
```

```
prep -design picorv32a
```

```
# Now that the design is prepped and ready, we can run synthesis using following  
command
```

```
run_synthesis
```

```
# Exit from OpenLANE flow
```

```
exit
```

```
# Exit from OpenLANE flow docker sub-system
```

`exit`

Screenshots of running each commands

Activities Terminal Fri 9:23 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
vsduser@vsdsquadron:~$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ docker
bash-4.2$ ./flow.tcl -interactive
[INFO]:
[INFO]: Version: v0.21
[INFO]: Running interactively
% package require openlane 0.9
0.9
% prep -design picorv32a
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/15-03_15-51
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane
```

Activities Terminal Fri 9:24 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/15-03_15-51
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.tlef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1l met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
[INFO]: % run_synthesis[]
```

```
Activities Terminal Fri 9:29 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -759.46
wns -24.89
[INFO]: Synthesis was successful
::: %
```

2. Calculate the flop ratio.

Screenshots of synthesis statistics report file with required values highlighted

Activities M GVim Fri 10:02 PM

File Edit Tools Syntax Buffers Window Help

```

1 28. Printing statistics.
2
3 === picorv32a ===
4
5     Number of wires:          14596
6     Number of wire bits:      14978
7     Number of public wires:   1565
8     Number of public wire bits: 1947
9
10    Number of memories:       0
11    Number of memory bits:    0
12    Number of processes:      0
13    Number of cells:          14876
14        sky130_fd_sc_hd_a2111o_2      1
15        sky130_fd_sc_hd_a211o_2      35
16        sky130_fd_sc_hd_a211oi_2     60
17        sky130_fd_sc_hd_a21bo_2      149
18        sky130_fd_sc_hd_a21boi_2     8
19        sky130_fd_sc_hd_a21o_2       57
20        sky130_fd_sc_hd_a21oi_2      244
21        sky130_fd_sc_hd_a221o_2      86
22        sky130_fd_sc_hd_a22o_2       1013
23        sky130_fd_sc_hd_a2bb2o_2     1748
24        sky130_fd_sc_hd_a2bb2oi_2    81
25        sky130_fd_sc_hd_a311o_2      2

```

hlsearch 25, 38 Top

Activities M GVIM Fri 10:03 PM

File Edit Tools Syntax Buffers Window Help

```

25    sky130_fd_sc_hd_a311o_2      2
26    sky130_fd_sc_hd_a31o_2       49
27    sky130_fd_sc_hd_a31oi_2      7
28    sky130_fd_sc_hd_a32o_2       46
29    sky130_fd_sc_hd_a41o_2       1
30    sky130_fd_sc_hd_and2_2       157
31    sky130_fd_sc_hd_and3_2       58
32    sky130_fd_sc_hd_and4_2       345
33    sky130_fd_sc_hd_and4b_2      1
34    sky130_fd_sc_hd_buf_1        1656
35    sky130_fd_sc_hd_buf_2        8
36    sky130_fd_sc_hd_conb_1       42
37    sky130_fd_sc_hd_dfxtp_2      1613
38    sky130_fd_sc_hd_inv_2        1615
39    sky130_fd_sc_hd_mux2_1       1224
40    sky130_fd_sc_hd_mux2_2       2
41    sky130_fd_sc_hd_mux4_1       221
42    sky130_fd_sc_hd_nand2_2      78
43    sky130_fd_sc_hd_nor2_2       524
44    sky130_fd_sc_hd_nor2b_2      1
45    sky130_fd_sc_hd_nor3_2       42
46    sky130_fd_sc_hd_nor4_2       1
47    sky130_fd_sc_hd_o2111a_2     2
48    sky130_fd_sc_hd_o211a_2      69
49    sky130_fd_sc_hd_o211ai_2     6

```

search hit BOTTOM, continuing at TOP 49, 38 48%

Calculation of Flop Ratio and DFF % from synthesis statistics report file

Section 2 - Good floorplan vs bad floorplan and introduction to library cells (16/03/2024 - 17/03/2024)

Theory

Implementation

Section 2 tasks:-

1. Run 'picorv32a' design floorplan using OpenLANE flow and generate necessary outputs.
 2. Calculate the die area in microns from the values in floorplan def.
 3. Load generated floorplan def in magic tool and explore the floorplan.
 4. Run 'picorv32a' design congestion aware placement using OpenLANE flow and generate necessary outputs.
 5. Load generated placement def in magic tool and explore the placement.
-
- All section 2 logs, reports and results can be found in following run folder:

Section 2 Run - 17-03_12-06

1. Run 'picorv32a' design floorplan using OpenLANE flow and generate necessary outputs.

Commands to invoke the OpenLANE flow and perform floorplan

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:v0.21'
```

Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command

```
docker
```

Now that we have entered the OpenLANE flow contained docker sub-system we can invoke the OpenLANE flow in the interactive mode using the following command

```
./flow.tcl -interactive
```

Now that OpenLANE flow is open we have to input the required packages for proper functionality of the OpenLANE flow

```
package require openlane 0.9
```

Now the OpenLANE flow is ready to run any design and initially we have to prep the design creating some necessary files and directories for running a specific design which in our case is 'picorv32a'

```
prep -design picorv32a
```

Now that the design is prepped and ready, we can run synthesis using following command

```
run_synthesis
```

```
# Now we can run floorplan
```

```
run_floorplan
```

Screenshot of floorplan run

```
Activities Terminal - Sun 6:06 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: Synthesis was successful
% run_floorplan
[INFO]: Running Floorplanning...
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 3
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/l
ib/sky130_fd_sc_hd_tt_025C_lv80.lib line 31, default_operating_condition tt_025C_lv80 not found.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/merged_unpadded.le
f
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 440 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/merged_unpadded.le
f
[INFO IFP-0001] Added 238 rows of 1412 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 660.685 671.405 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/reports/floorplan/3-verilog2def.die_area.rpt.
[INFO] Floorplanned on a core area of 5.52 10.88 655.04 658.24 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/reports/floorplan/3-verilog2def.core_area.rpt.
[INFO]: Core area width: 649.52
[INFO]: Core area height: 647.36
[INFO]: Changing layout from 0 to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/floorplan/3-verilog2def_openroad.def
[INFO]: Running IO Placement...
[INFO]: success! step index: 3
```

```
Activities Terminal - Sun 6:06 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
er stripe. Moving to closest stripe at (567.000um, 103.880um).
[WARNING PSM-0030] Vsrc location at (565.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 257.060um).
[WARNING PSM-0030] Vsrc location at (5.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (145.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
[WARNING PSM-0030] Vsrc location at (425.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 563.420um).
[INFO PSM-0031] Number of nodes on net VGND = 19223.
[INFO PSM-0037] G matrix created sucessfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/floorplan/picorv32a.floorplan.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/floorplan/7-pdn.def
1
% [ ]
```

2. Calculate the die area in microns from the values in floorplan def.

Screenshot of contents of floorplan def

```

1 VERSION 5.8 ;
2 DIVIDERCHAR "/";
3 BUSBITCHARS "[]";
4 DESIGN picorv32a ;
5 UNITS DISTANCE MICRONS 1000 ;
6 DIEAREA ( 0 0 ) ( 660685 671405 ) ;
7 ROW ROW_0 unithd 5520 10880 FS DO 1412 BY 1 STEP 460 0 ;
8 ROW ROW_1 unithd 5520 13600 N DO 1412 BY 1 STEP 460 0 ;
9 ROW ROW_2 unithd 5520 16320 FS DO 1412 BY 1 STEP 460 0 ;
10 ROW ROW_3 unithd 5520 19040 N DO 1412 BY 1 STEP 460 0 ;
11 ROW ROW_4 unithd 5520 21760 FS DO 1412 BY 1 STEP 460 0 ;
12 ROW ROW_5 unithd 5520 24480 N DO 1412 BY 1 STEP 460 0 ;
13 ROW ROW_6 unithd 5520 27200 FS DO 1412 BY 1 STEP 460 0 ;
14 ROW ROW_7 unithd 5520 29920 N DO 1412 BY 1 STEP 460 0 ;
15 ROW ROW_8 unithd 5520 32640 FS DO 1412 BY 1 STEP 460 0 ;
16 ROW ROW_9 unithd 5520 35360 N DO 1412 BY 1 STEP 460 0 ;
17 ROW ROW_10 unithd 5520 38080 FS DO 1412 BY 1 STEP 460 0 ;
18 ROW ROW_11 unithd 5520 40800 N DO 1412 BY 1 STEP 460 0 ;
19 ROW ROW_12 unithd 5520 43520 FS DO 1412 BY 1 STEP 460 0 ;
20 ROW ROW_13 unithd 5520 46240 N DO 1412 BY 1 STEP 460 0 ;
21 ROW ROW_14 unithd 5520 48960 FS DO 1412 BY 1 STEP 460 0 ;
22 ROW ROW_15 unithd 5520 51680 N DO 1412 BY 1 STEP 460 0 ;
23 ROW ROW_16 unithd 5520 54400 FS DO 1412 BY 1 STEP 460 0 ;
24 ROW ROW_17 unithd 5520 57120 N DO 1412 BY 1 STEP 460 0 ;
25 ROW ROW_18 unithd 5520 59840 FS DO 1412 BY 1 STEP 460 0 ;

```

According to floorplan def

3. Load generated floorplan def in magic tool and explore the floorplan.

Commands to load floorplan def in magic in another terminal

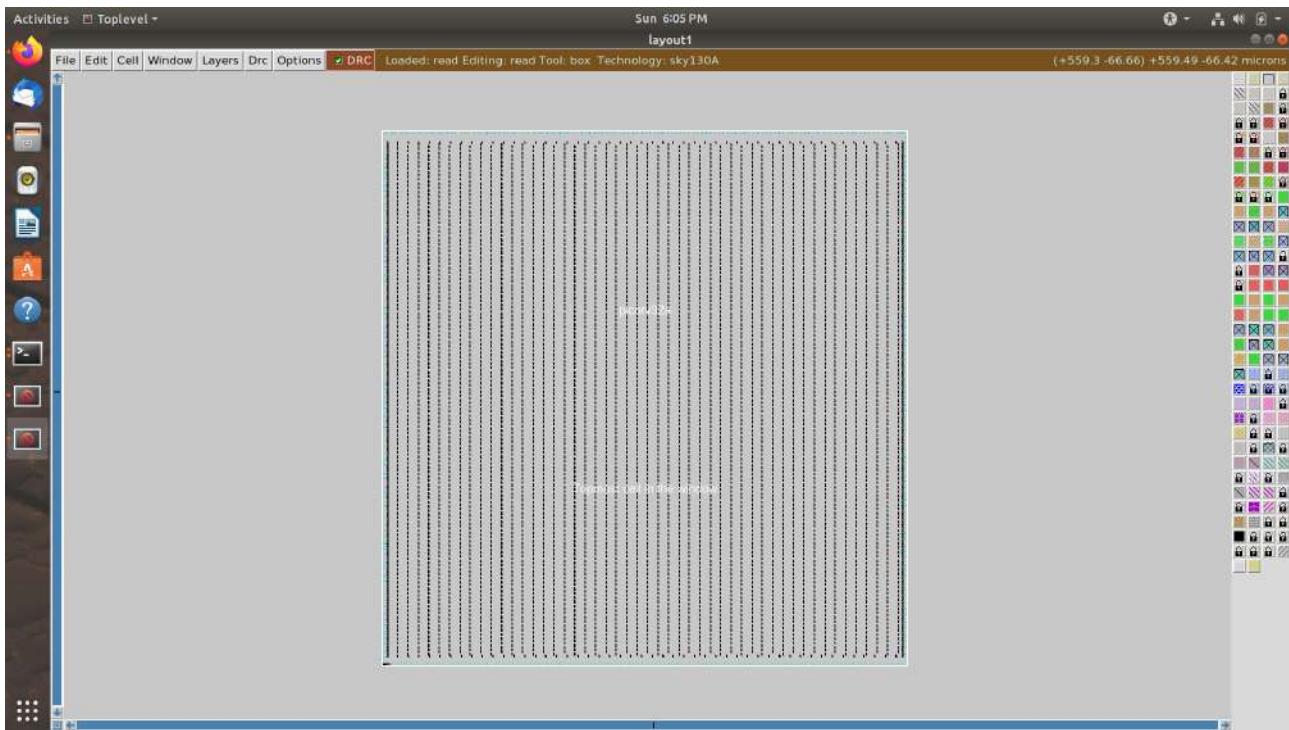
```
# Change directory to path containing generated floorplan def
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
17-03_12-06/results/floorplan/
```

```
# Command to load the floorplan def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.floorplan.def &
```

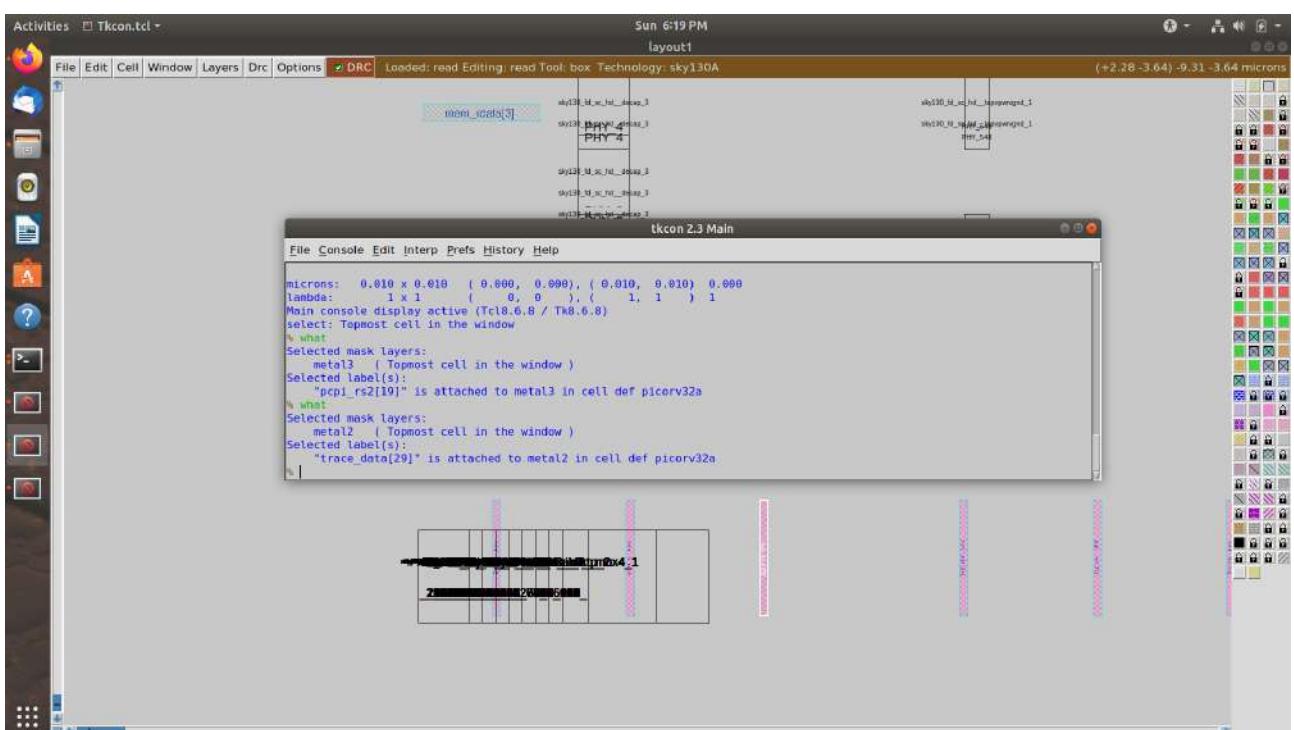
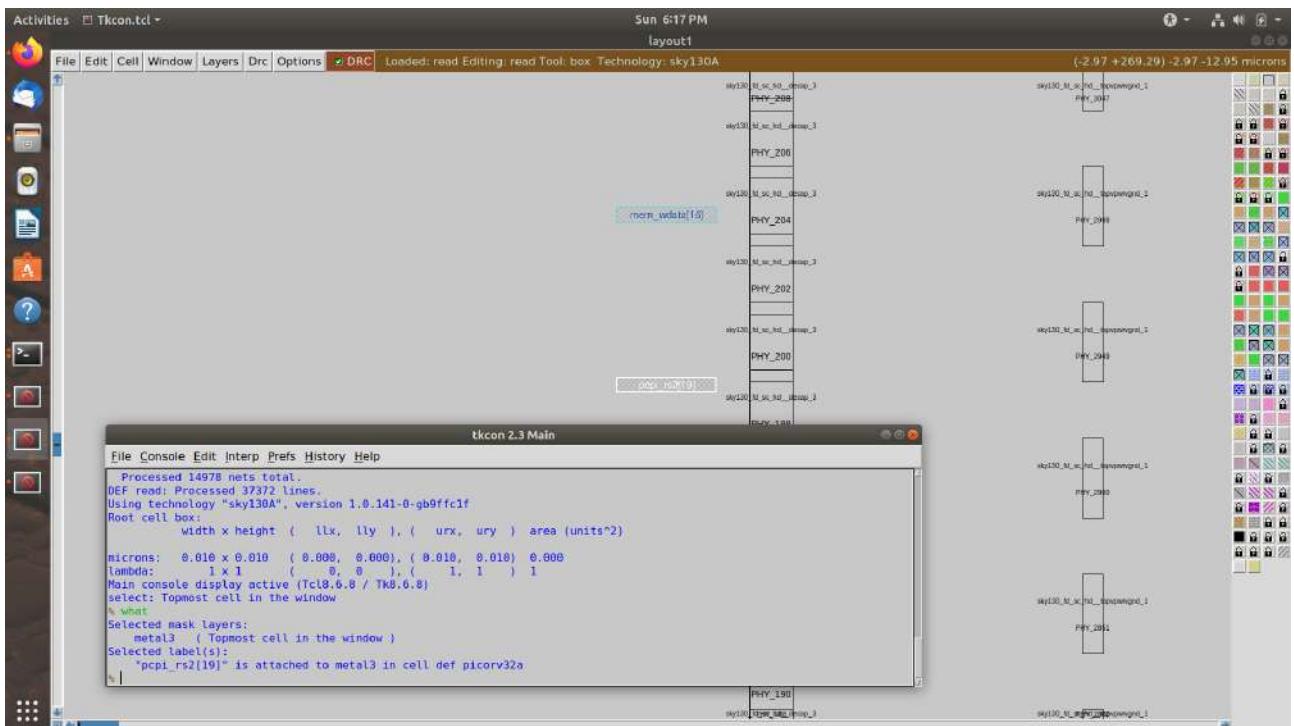
Screenshots of floorplan def in magic



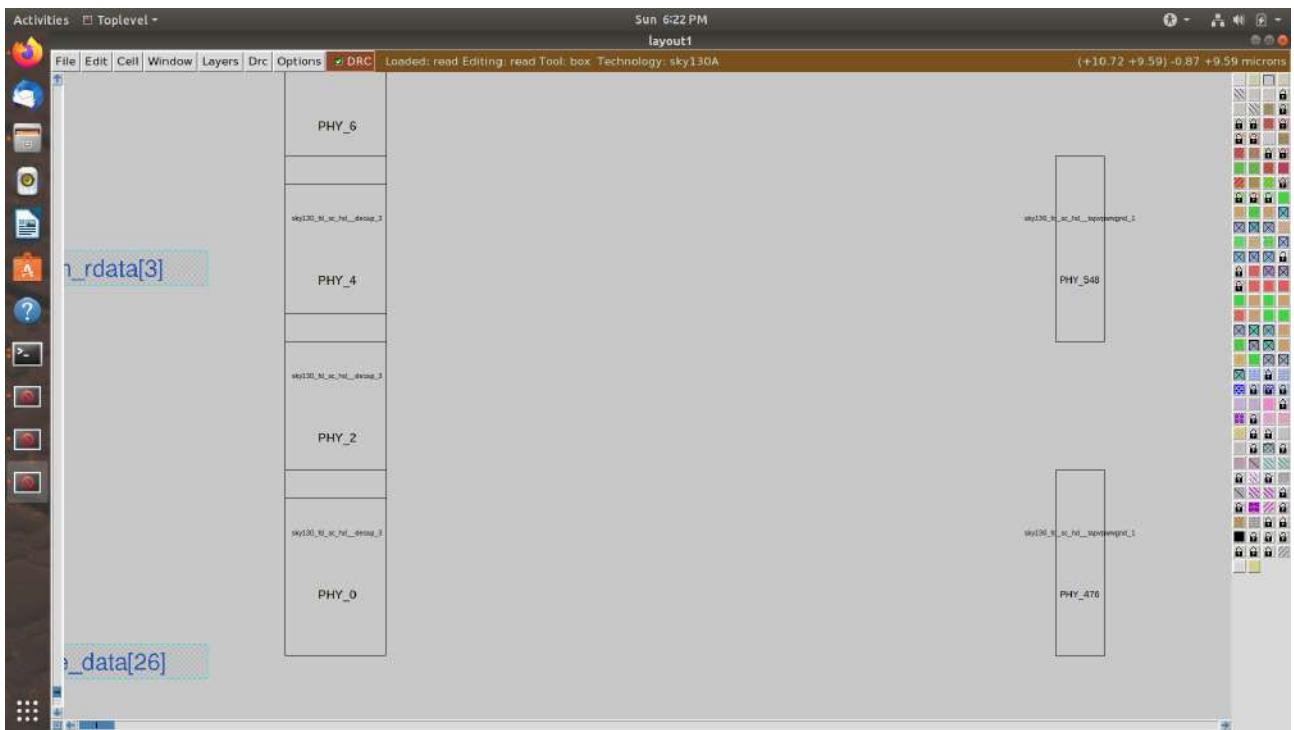
Equidistant placement of ports



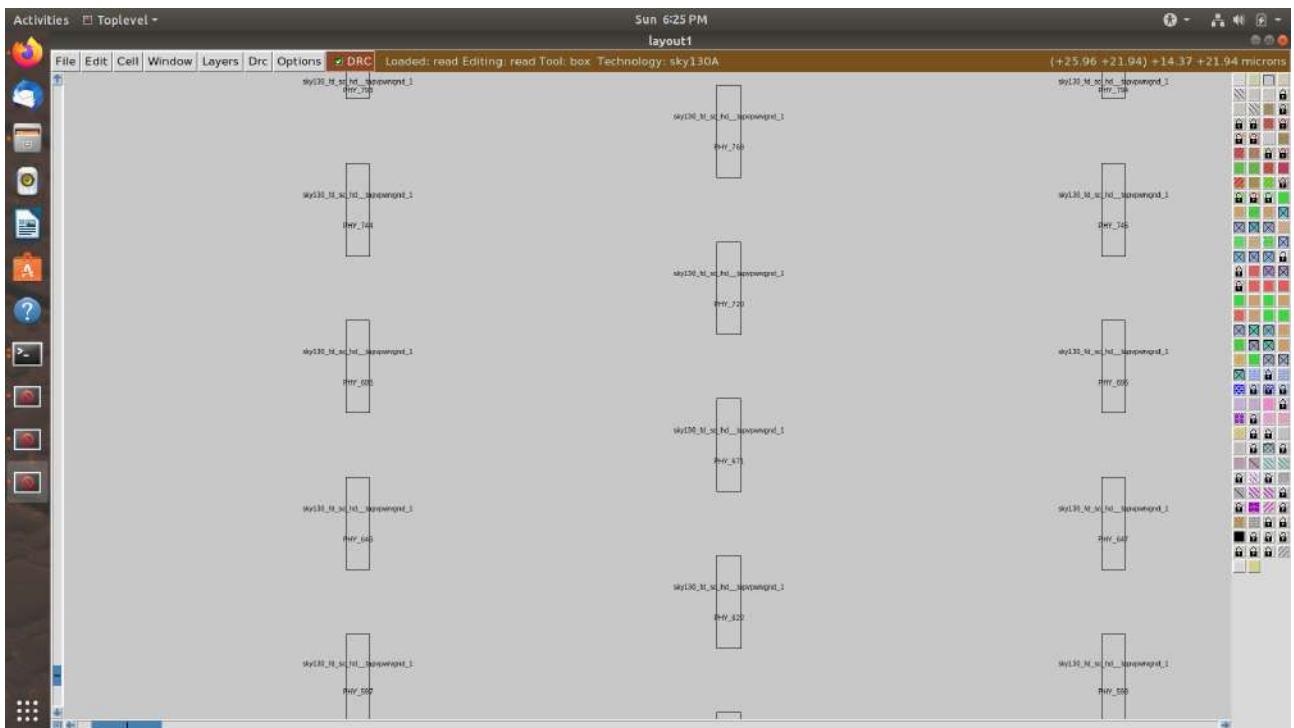
Port layer as set through config.tcl



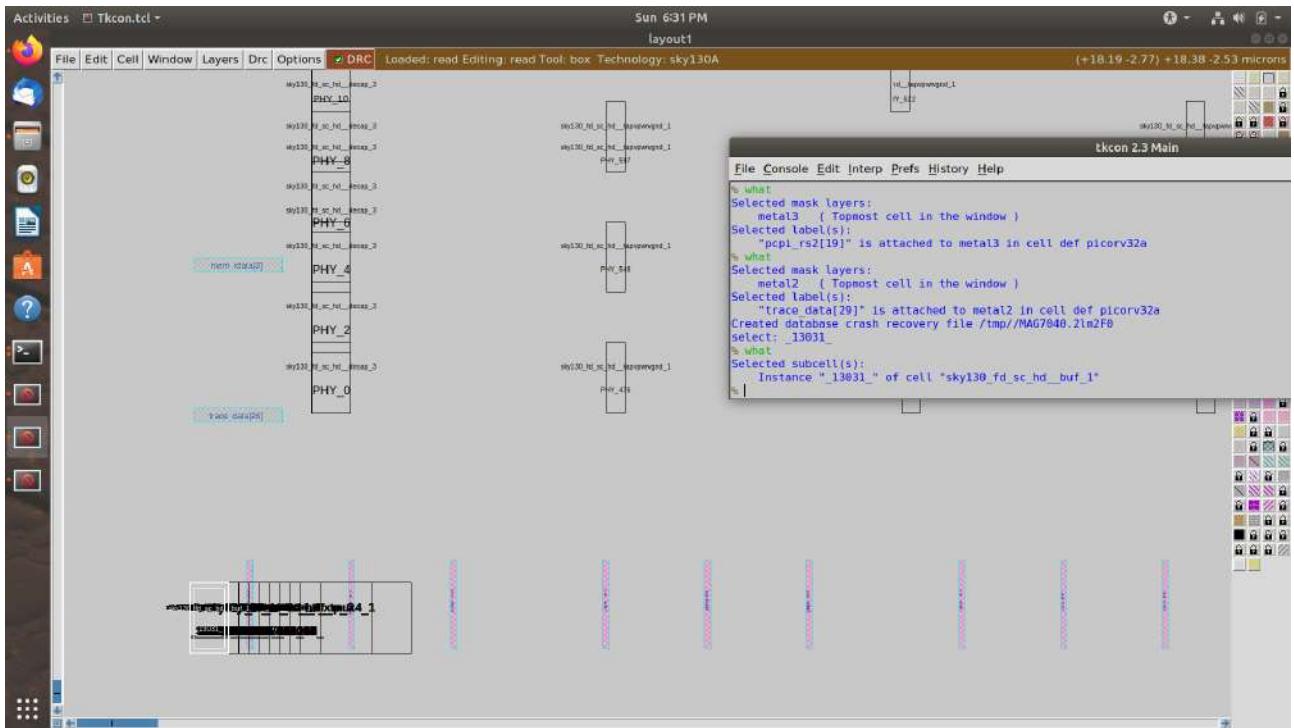
Decap Cells and Tap Cells



Diagonally equidistant Tap cells



Unplaced standard cells at the origin



4. Run 'picorv32a' design congestion aware placement using OpenLANE flow and generate necessary outputs.

Command to run placement

```
# Congestion aware placement by default
```

```
run_placement
```

Screenshots of placement run

```
Activities Terminal - Sun 10:44 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
er stripe. Moving to closest stripe at (567.000um, 103.880um).
[WARNING PSM-0030] Vsrc location at (565.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 257.060um).
[WARNING PSM-0030] Vsrc location at (5.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (145.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
[WARNING PSM-0030] Vsrc location at (425.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 563.420um).
[INFO PSM-0031] Number of nodes on net VGND = 19223.
[INFO PSM-0037] G matrix created sucessfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/floorplan/picorv32a.floorplan.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/floorplan/7-pdn.def
1
::: % run_placement
```

```
Activities Terminal - Sun 10:46 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
legalized HPWL      779196.5 u
delta HPWL          2 %

[INFO DPL-0020] Mirrored 6193 instances
[INFO DPL-0021] HPWL before      779196.5 u
[INFO DPL-0022] HPWL after       766080.0 u
[INFO DPL-0023] HPWL delta      -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/placement/8-resizer.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 12
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
::: %
```

5. Load generated placement def in magic tool and explore the placement.

Commands to load placement def in magic in another terminal

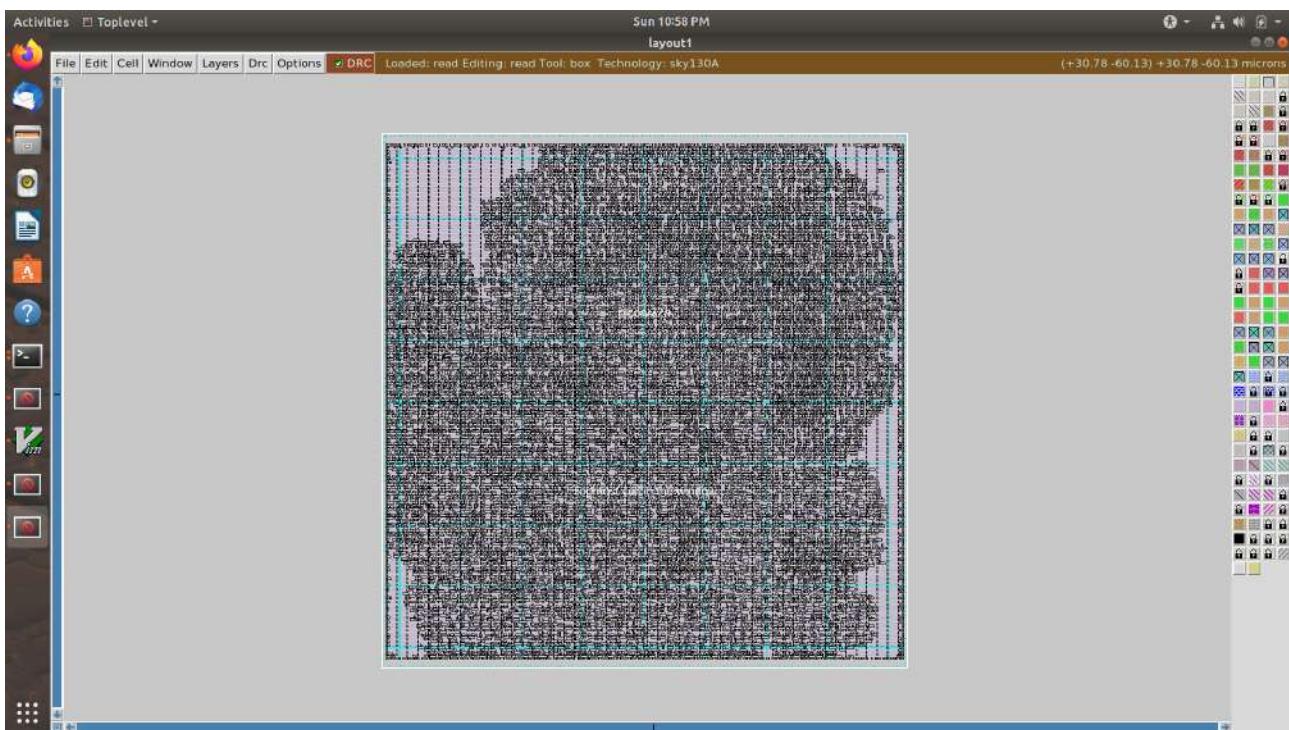
```
# Change directory to path containing generated placement def
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/  
17-03_12-06/results/placement/
```

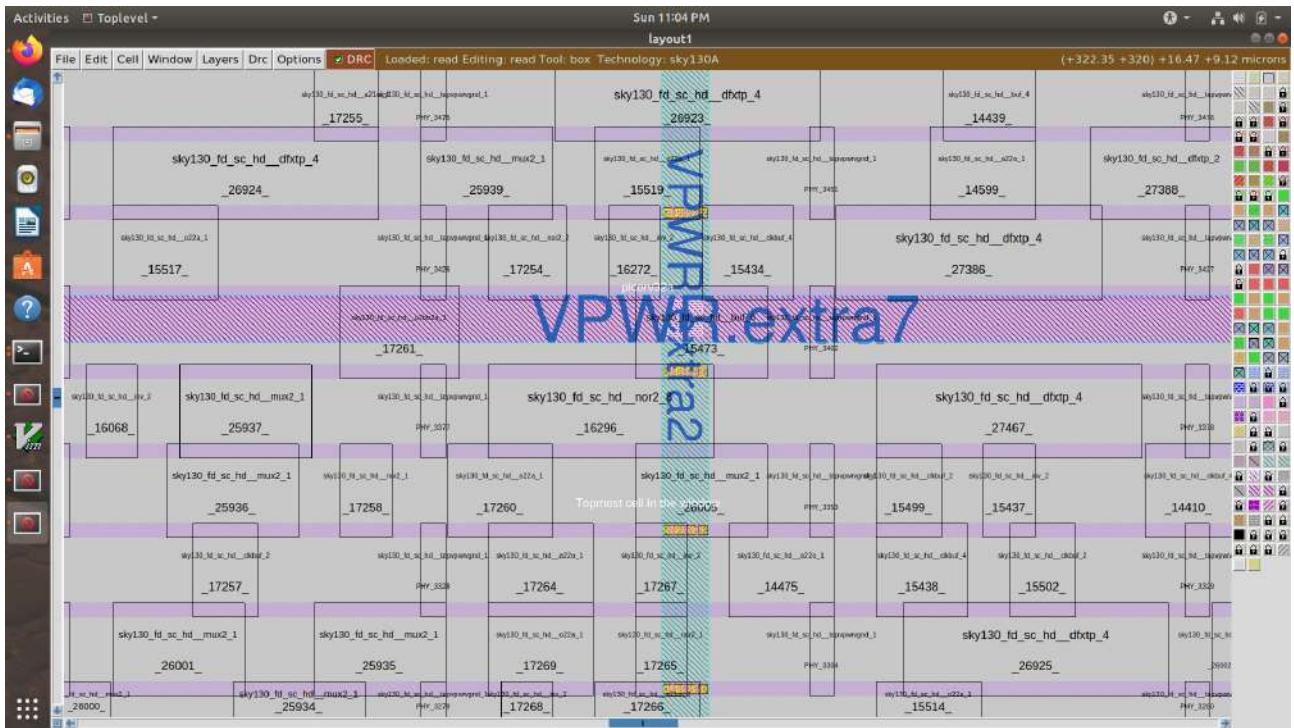
```
# Command to load the placement def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def  
&
```

Screenshots of floorplan def in magic



Standard cells legally placed



Commands to exit from current run

```
# Exit from OpenLANE flow
```

```
exit
```

```
# Exit from OpenLANE flow docker sub-system
```

```
exit
```

Section 3 - Design library cell using Magic Layout and ngspice characterization (18/03/2024 - 21/03/2024)

Theory

Implementation

- **Section 3 tasks:-**
- 6. Clone custom inverter standard cell design from github repository: [Standard cell design and characterization using OpenLANE flow.](#)
- 7. Load the custom inverter layout in magic and explore.
- 8. Spice extraction of inverter in magic.
- 9. Editing the spice model file for analysis through simulation.
- 10. Post-layout ngspice simulations.
- 11. Find problem in the DRC section of the old magic tech file for the skywater process and fix them.
- **Section 3 - Tasks 1 to 5 files, reports and logs can be found in the following folder:**

[Section 3 - Tasks 1 to 5 \(vsdstdcelldesign\)](#)

- **Section 3 - Task 6 files, reports and logs can be found in the following folder:**

[Section 3 - Task 6 \(drc_tests\)](#)

1. Clone custom inverter standard cell design from github repository

```
# Change directory to openlane
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# Clone the repository with custom inverter design
```

```
git clone https://github.com/nickson-jose/vsdstdcelldesign
```

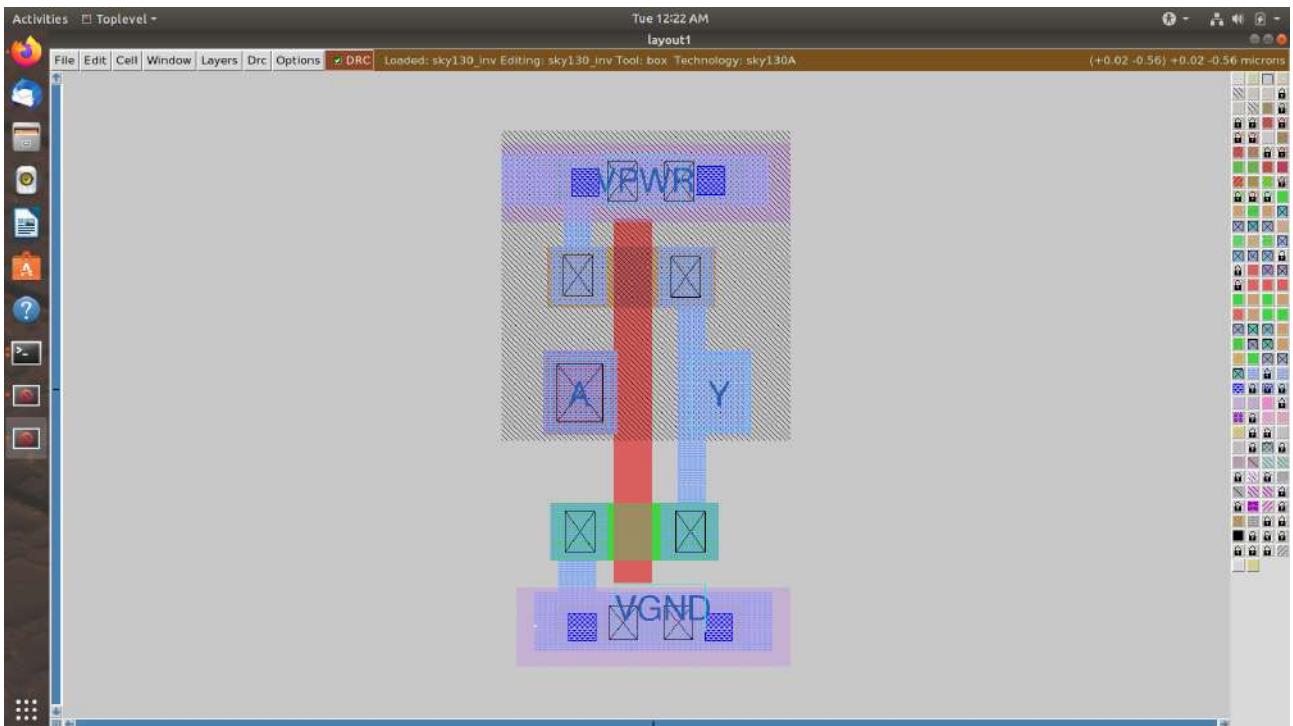
```
# Change into repository directory  
  
cd vsdstdcelldesign  
  
# Copy magic tech file to the repo directory for easy access  
  
cp /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/  
magic/sky130A.tech .  
  
# Check contents whether everything is present  
  
ls  
  
# Command to open custom inverter layout in magic  
  
magic -T sky130A.tech sky130_inv.mag &
```

Screenshot of commands run

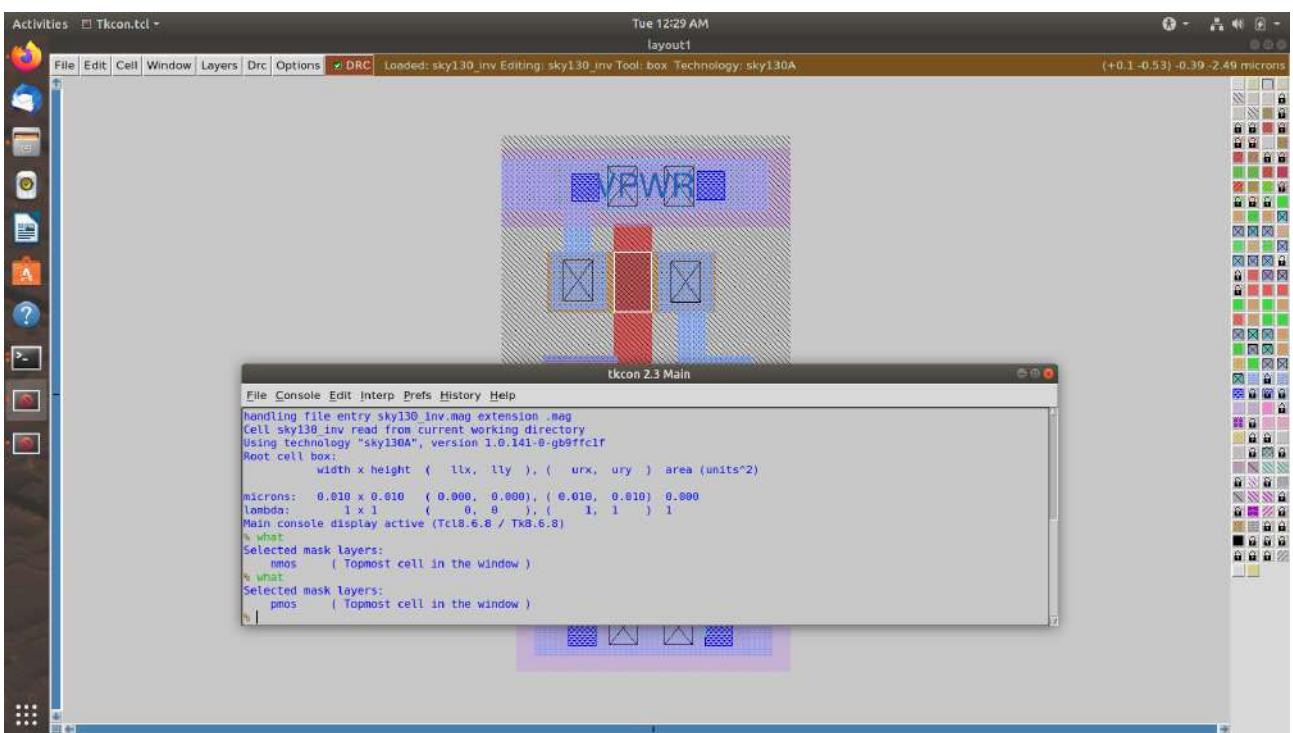
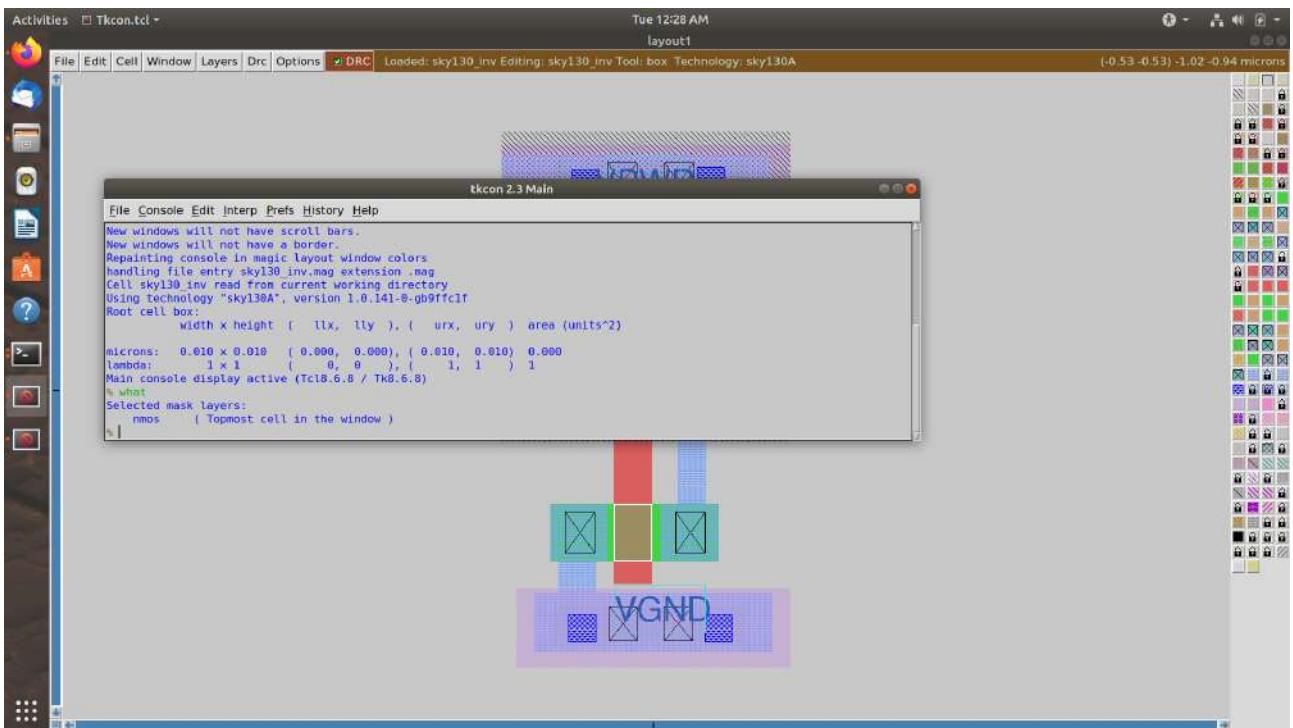
```
Activities Terminal Tue 12:22 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ git clone https://github.com/nickson-jose/vsdstdcelldesign
Cloning into 'vsdstdcelldesign'...
remote: Enumerating objects: 492, done.
remote: Counting objects: 100% (18/18), done.
remote: Compressing objects: 100% (18/18), done.
remote: Total 492 (delta 7), reused 0 (delta 0), pack-reused 474
Receiving objects: 100% (492/492), 24.08 MiB | 480.00 KiB/s, done.
Resolving deltas: 100% (210/210), done.
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd vsdstdcelldesign
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cp /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/magic/sky130A.tech .
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls
extras Images libs LICENSE README.md sky130A.tech sky130_inv.mag
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ magic -T sky130A.tech sky130_inv.mag &
[1] 4495
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```

2. Load the custom inverter layout in magic and explore.

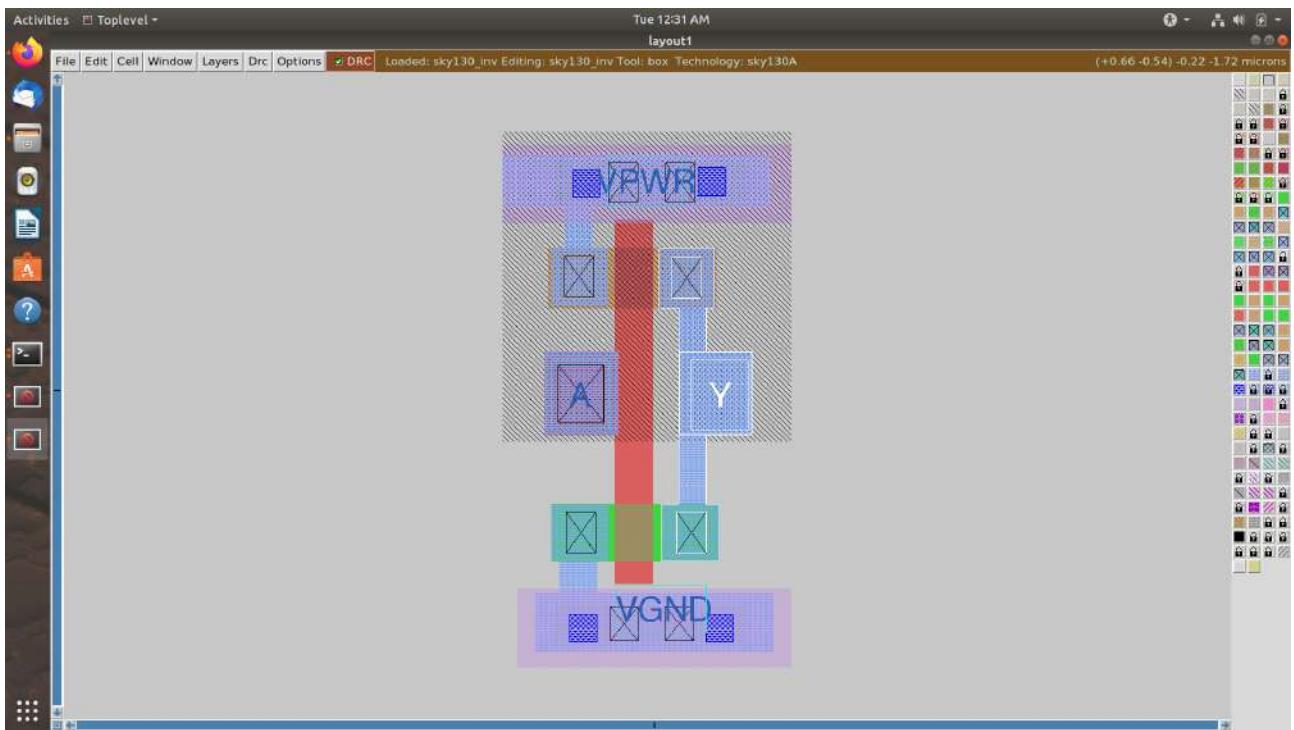
Screenshot of custom inverter layout in magic



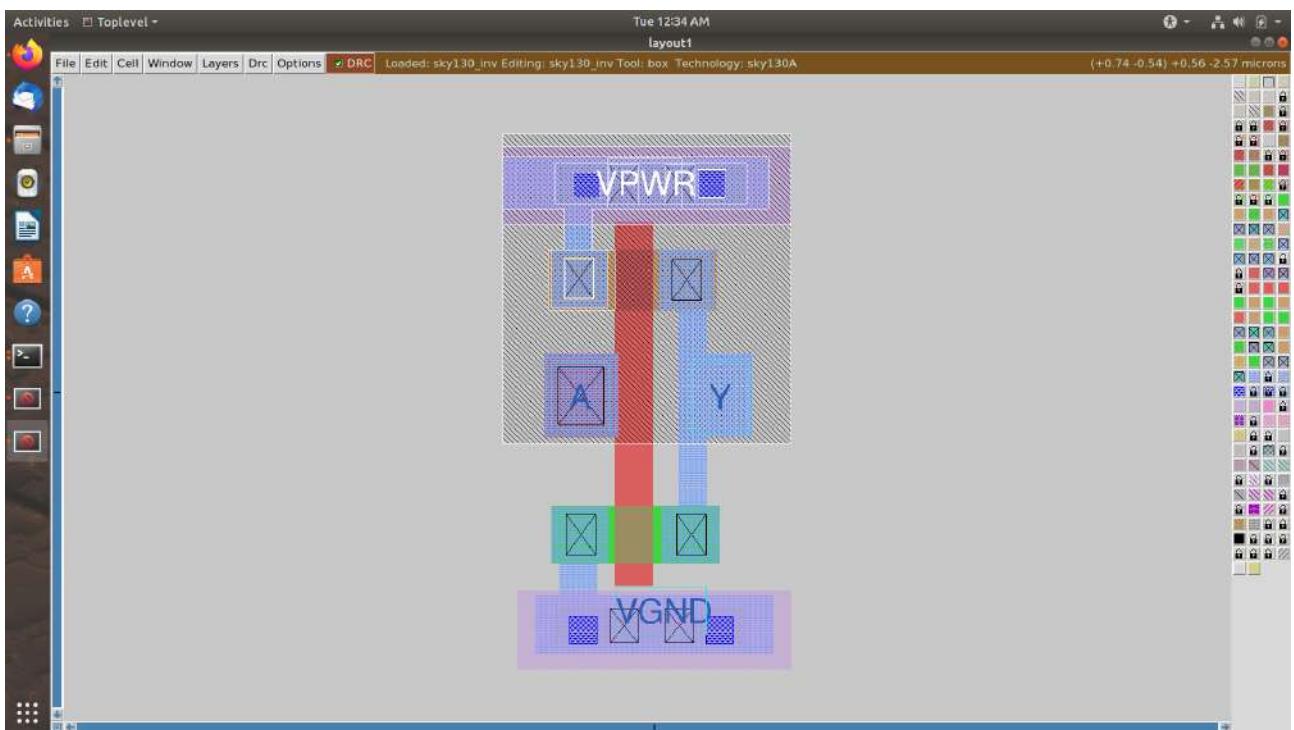
NMOS and PMOS identified



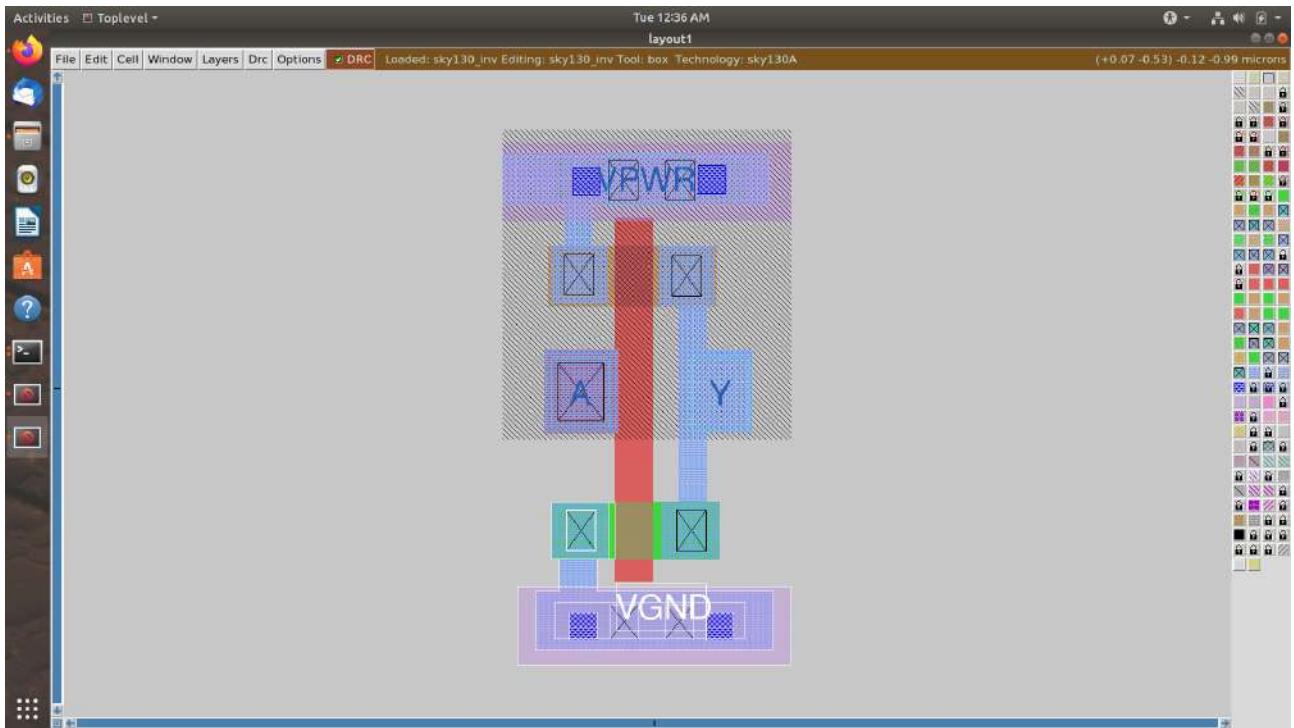
Output Y connectivity to PMOS and NMOS drain verified



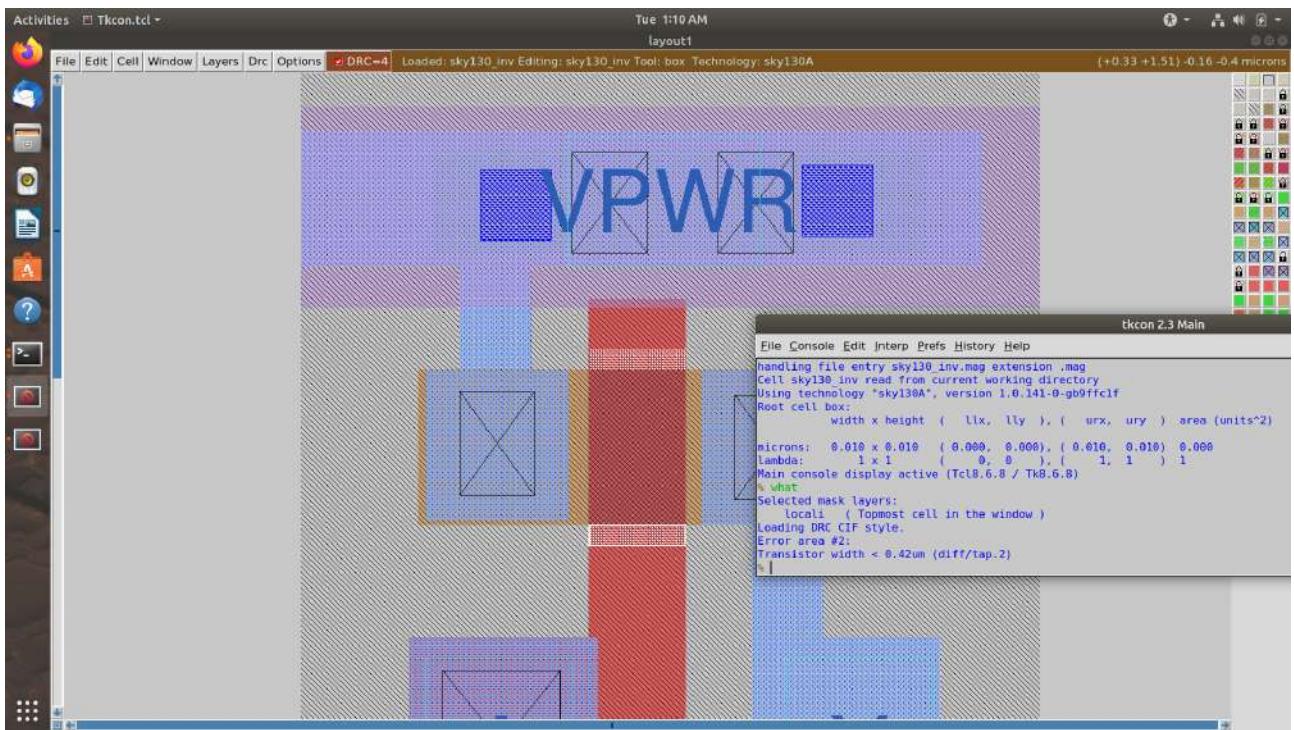
PMOS source connectivity to VDD (here VPWR) verified



NMOS source connectivity to VSS (here VGND) verified



Deleting necessary layout part to see DRC error



3. Spice extraction of inverter in magic.

Commands for spice extraction of the custom inverter layout to be used in tkcon window of magic

```
# Check current directory
```

pwd

```
# Extraction command to extract to .ext format
```

extract all

Before converting ext to spice this command enable the parasitic extraction also

`ext2splice cthresh 0 rthresh 0`

Converting to ext to spice

ext2spice

Screenshot of tkcon window after running above commands

```
Activities □ Tkcon.tcl - Tue 1:24 AM
tkcon 2.3 Main

File Console Edit Interp Prefs History Help
Loading history file ... 16 events added
Use openwrapper to create a new GUI-based layout window
Use closerwrapper to remove a new GUI-based layout window

Magic 8.3 revision 400 - Compiled on Mon May 22 20:58:24 IST 2023.
Starting magic under Tcl Interpreter
Using Tk console window
Using TrueColor, VisualID 0x21 depth 24
Input style sky130(): scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
    nmosc obsactive mvbsactive obsl11 obsm1 obsm2 obsm3 obsm4 obsm5 obsnrd1 ubm fillblock comment obscomment res0p35 res0p69 reslp41 res2p85 res5p73
Processing system .magicrc file
New windows will not have a title caption.
New windows will not have scroll bars.
New windows will not have a border.
Repainting console in magic layout window colors
handling file entry sky130_inv.mag extension .mag
Cell sky130_inv read from current working directory
Using technology "sky130A", version 1.0.141-0-gb9ffcf
Root cell box:
    width x height ( llx, lly ),( urx, ury ) area (units^2)
microns: 0.010 x 0.010 ( 0.000, 0.000 ),( 0.010, 0.010 ) 0.000
lambda: 1 x 1 ( 0, 0 ),( 1, 1 ) 1
Main console display active (Tcl8.6.8 / Tk8.6.8)
> .pmel
> /home/vsuser/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
> extract all
Extracting sky130_inv into sky130_inv.ext:
% ext2spice cthresh 0 rthresh 0
% ext2spice
ext2spice finished.
%
```

Screenshot of created spice file

Activities ▾ GVim ▾

Tue 1:27 AM

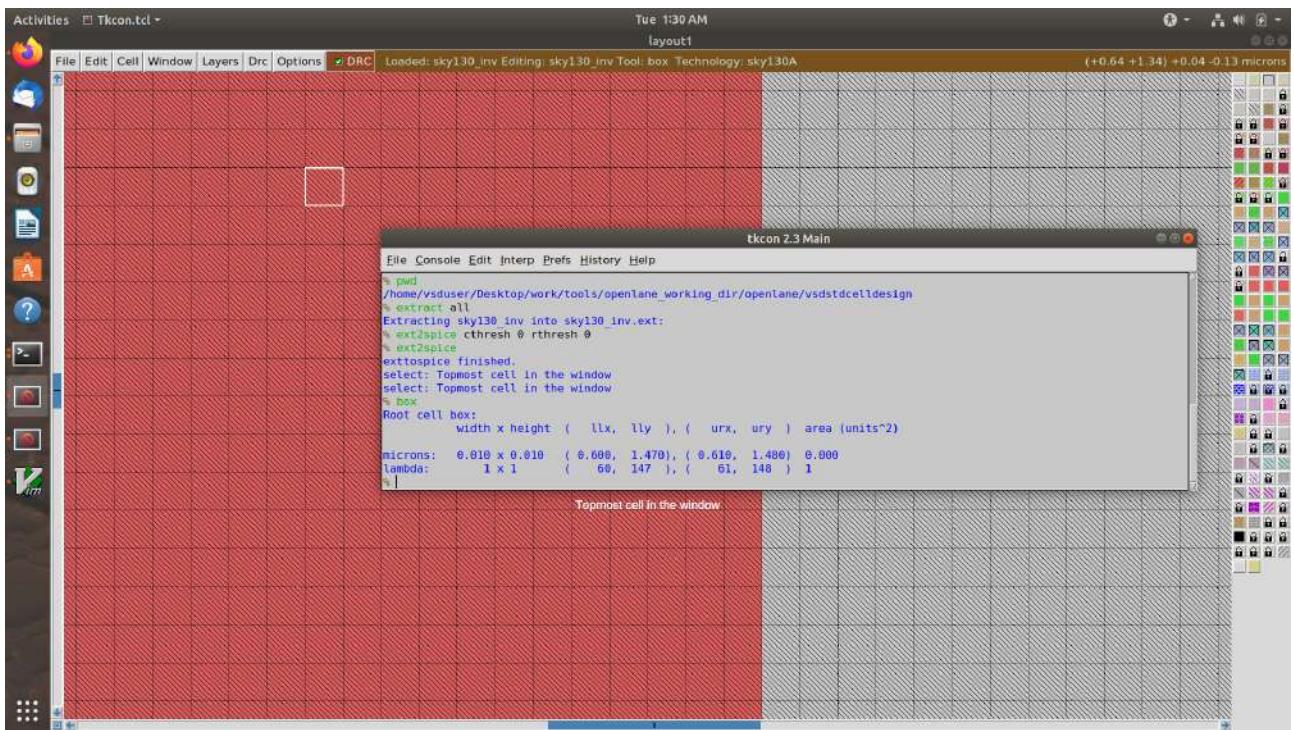
sky130_inv.spice (~/Desktop/work/tools/op...ng_dlr/openlane/vsdstdceldesign) - GVIM

File Edit Tools Syntax Buffers Window Help

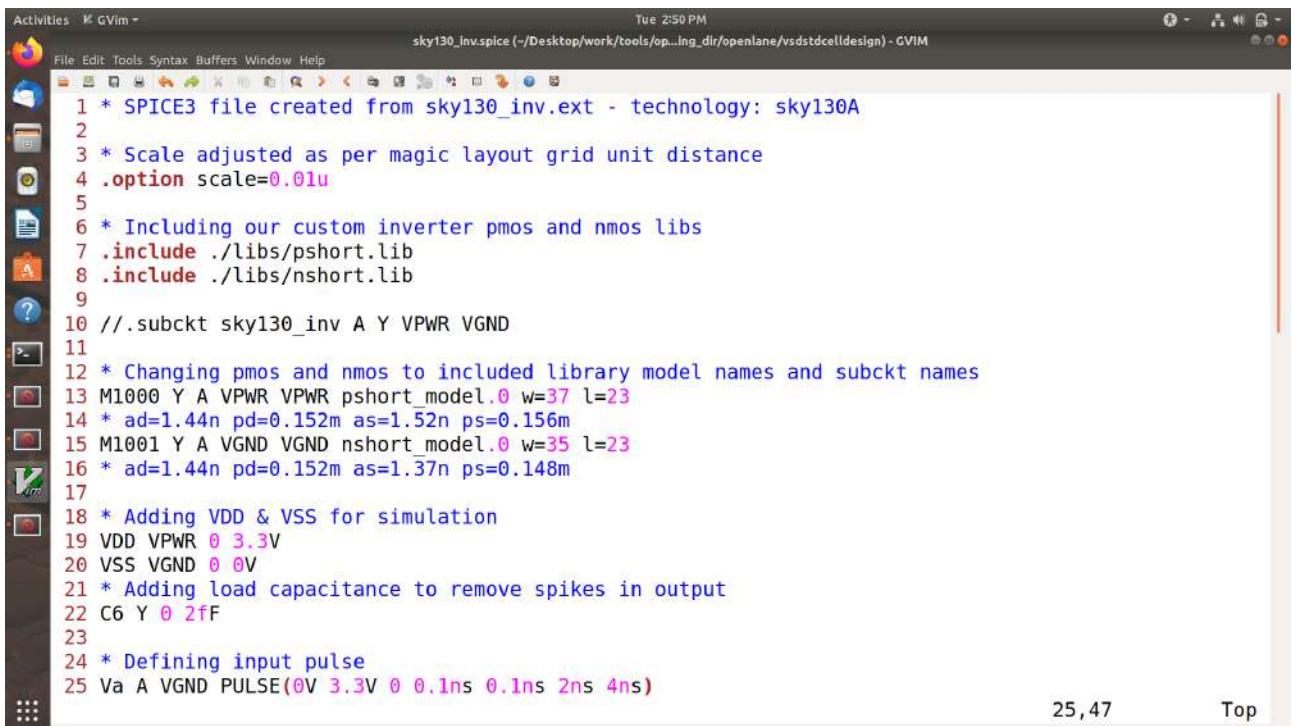
```
1 * SPICE3 file created from sky130_inv.ext - technology: sky130A
2
3 .option scale=10m
4
5 .subckt sky130_inv A Y VPWR VGND
6 X0 Y A VGND VGND sky130_fd_pr_nfet_01v8 ad=1.44n pd=0.152m as=1.37n ps=0.148m w=35 l=23
7 X1 Y A VPWR VPWR sky130_fd_pr_pfet_01v8 ad=1.44n pd=0.152m as=1.52n ps=0.156m w=37 l=23
8 C0 A VPWR 0.0774f
9 C1 Y VPWR 0.117f
10 C2 A Y 0.0754f
11 C3 Y VGND 0.279f
12 C4 A VGND 0.45f
13 C5 VPWR VGND 0.781f
14 .ends
```

4. Editing the spice model file for analysis through simulation.

Measuring unit distance in layout grid

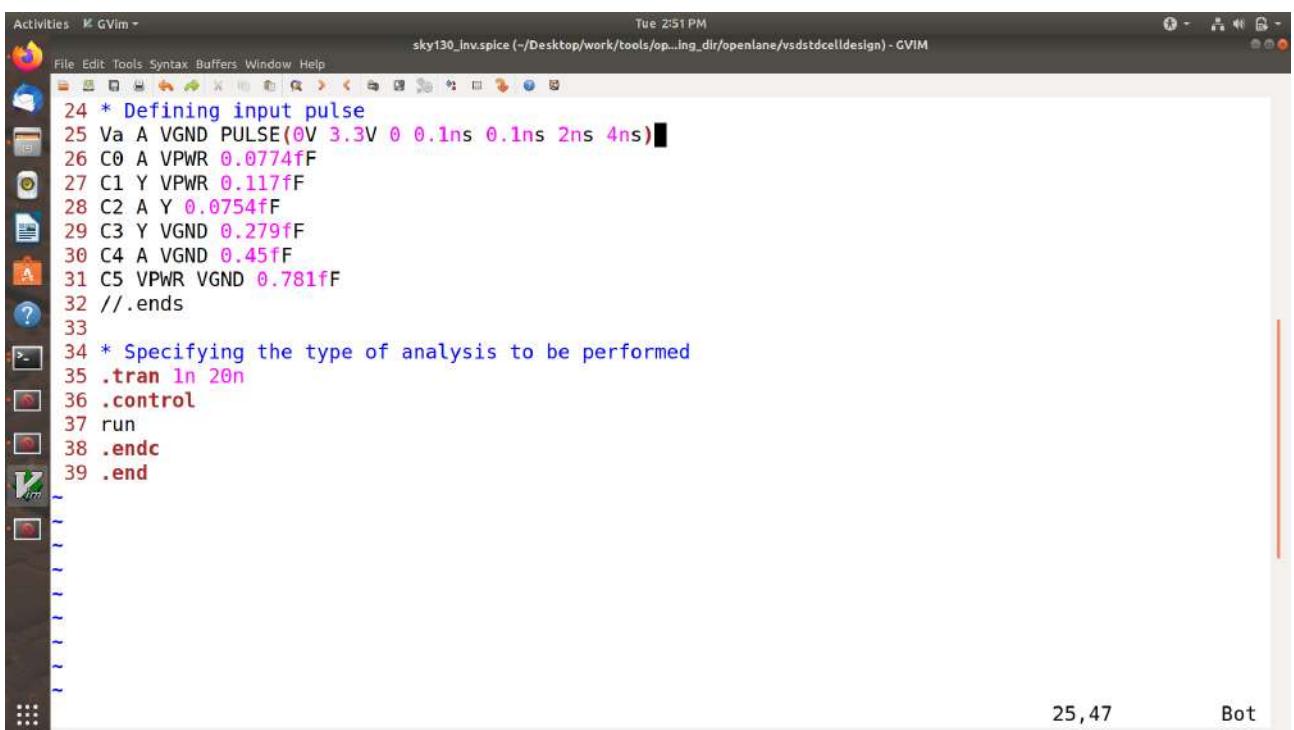


Final edited spice file ready for ngspice simulation



```
Activities  M GVim - Tue 2:50 PM
sky130_inv.spice (~/Desktop/work/tools/op...ing_dir/openlane/vsdstdcelldesign) - GVIM
File Edit Tools Syntax Buffers Window Help
1 * SPICE3 file created from sky130_inv.ext - technology: sky130A
2
3 * Scale adjusted as per magic layout grid unit distance
4 .option scale=0.01u
5
6 * Including our custom inverter pmos and nmos libs
7 .include ./libs/pshort.lib
8 .include ./libs/nshort.lib
9
10 // .subckt sky130_inv A Y VPWR VGND
11
12 * Changing pmos and nmos to included library model names and subckt names
13 M1000 Y A VPWR VPWR pshort_model.0 w=37 l=23
14 * ad=1.44n pd=0.152m as=1.52n ps=0.156m
15 M1001 Y A VGND VGND nshort_model.0 w=35 l=23
16 * ad=1.44n pd=0.152m as=1.37n ps=0.148m
17
18 * Adding VDD & VSS for simulation
19 VDD VPWR 0 3.3V
20 VSS VGND 0 0V
21 * Adding load capacitance to remove spikes in output
22 C6 Y 0 2fF
23
24 * Defining input pulse
25 Va A VGND PULSE(0V 3.3V 0 0.1ns 0.1ns 2ns 4ns)
26
27
28
29
30
31
32 // .ends
33
34 * Specifying the type of analysis to be performed
35 .tran 1n 20n
36 .control
37 run
38 .endc
39 .end
```

25,47 Top



```
Activities  M GVim - Tue 2:51 PM
sky130_inv.spice (~/Desktop/work/tools/op...ing_dir/openlane/vsdstdcelldesign) - GVIM
File Edit Tools Syntax Buffers Window Help
24 * Defining input pulse
25 Va A VGND PULSE(0V 3.3V 0 0.1ns 0.1ns 2ns 4ns)■
26 C0 A VPWR 0.0774fF
27 C1 Y VPWR 0.117fF
28 C2 A Y 0.0754fF
29 C3 Y VGND 0.279fF
30 C4 A VGND 0.45fF
31 C5 VPWR VGND 0.781fF
32 // .ends
33
34 * Specifying the type of analysis to be performed
35 .tran 1n 20n
36 .control
37 run
38 .endc
39 .end
```

25,47 Bot

5. Post-layout ngspice simulations.

Commands for ngspice simulation

Command to directly load spice file for simulation to ngspice

ngspice sky130_inv.spice

```
# Now that we have entered ngspice with the simulation spice file loaded we just have to  
load the plot
```

```
plot y vs time a
```

Screenshots of ngspice run

```

Activities Terminal - vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ngspice sky130_inv.spice
*****
** ngspice-27 : Circuit level simulation program
** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California.
** Please get your ngspice manual from http://ngspice.sourceforge.net/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Tue Dec 26 17:10:20 UTC 2017
*****
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node Voltage
-----
y 3.3
a 0
vpwr 3.3
vgnd 0
va#branch 0

```

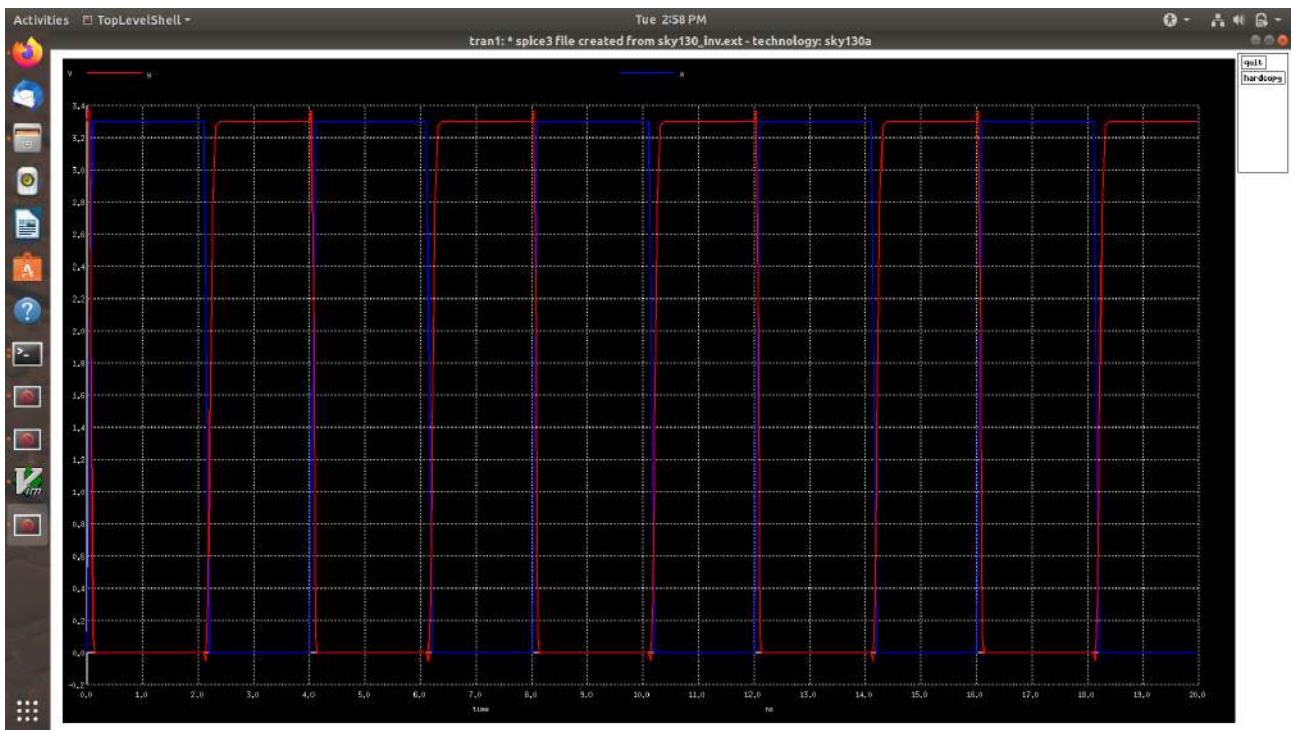
```

Activities TopLevelShell - vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ 
*****
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node Voltage
-----
y 3.3
a 0
vpwr 3.3
vgnd 0
va#branch 0
vss#branch 3.32351e-12
vdd#branch -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
::: ngspice 1 -> 

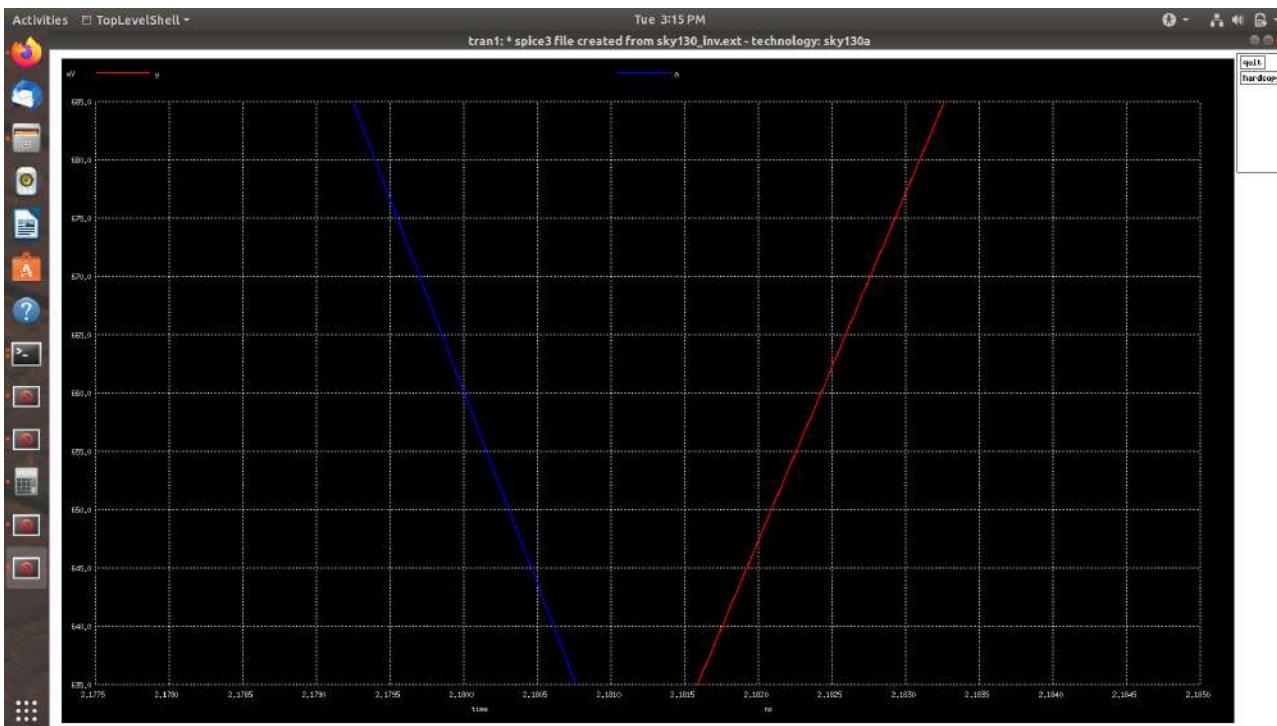
```

Screenshot of generated plot



Rise transition time calculation

20% Screenshots



Activities Terminal -

Tue 3:20 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign

```

File Edit View Search Terminal Help
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a

Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

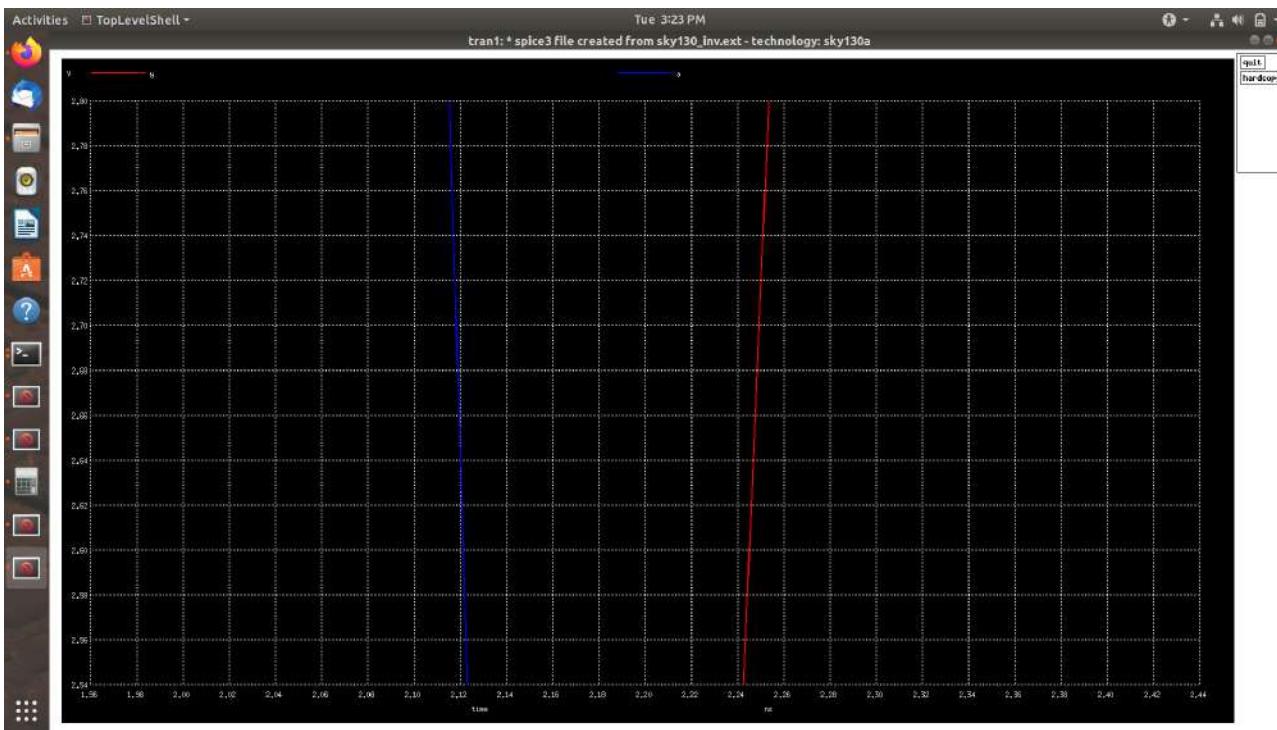
Warning: va: no DC value, transient time 0 value used

Initial Transient Solution
-----
Node          Voltage
---- 
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043

```

80% Screenshots



Activities Terminal -

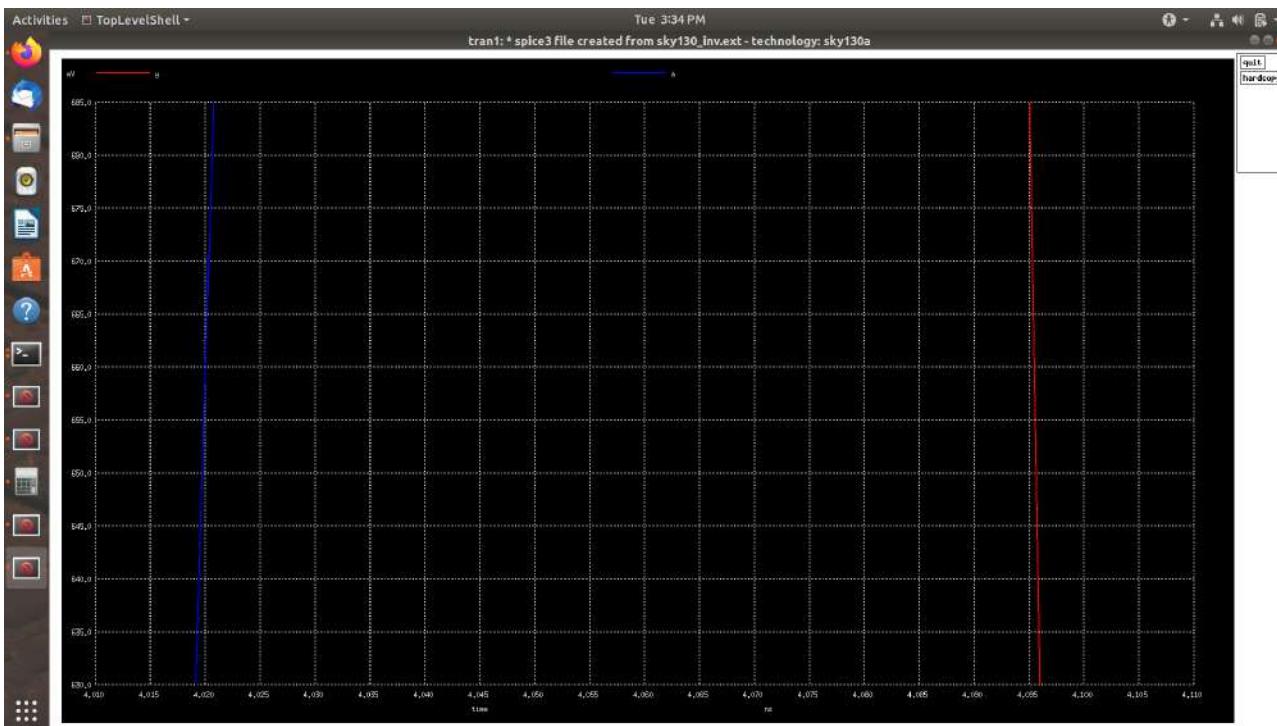
Tue 3:24 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```
File Edit View Search Terminal Help
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node          Voltage
-----
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
```

Fall transition time calculation

20% Screenshots



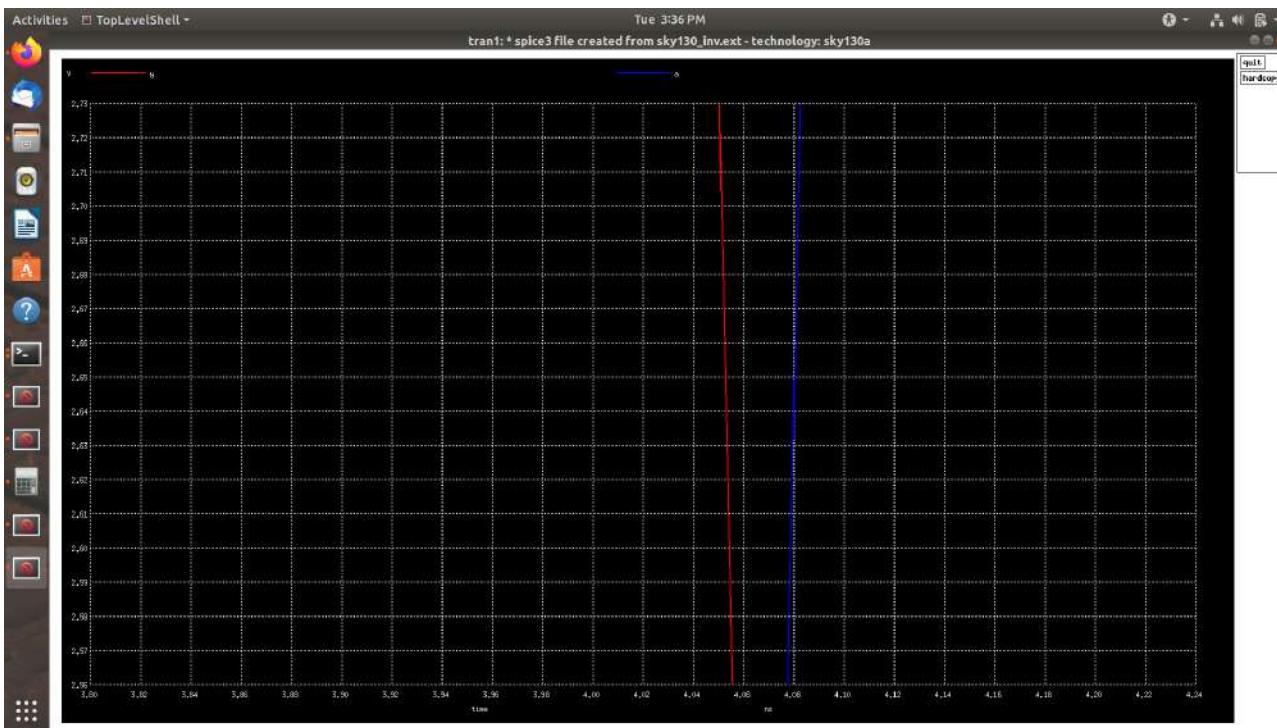
Activities Terminal

Tue 3:34 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node          Voltage
-----
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
x0 = 4.09555e-09, y0 = 0.660127
```

80% Screenshots



Activities Terminal -

Tue 3:36 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```

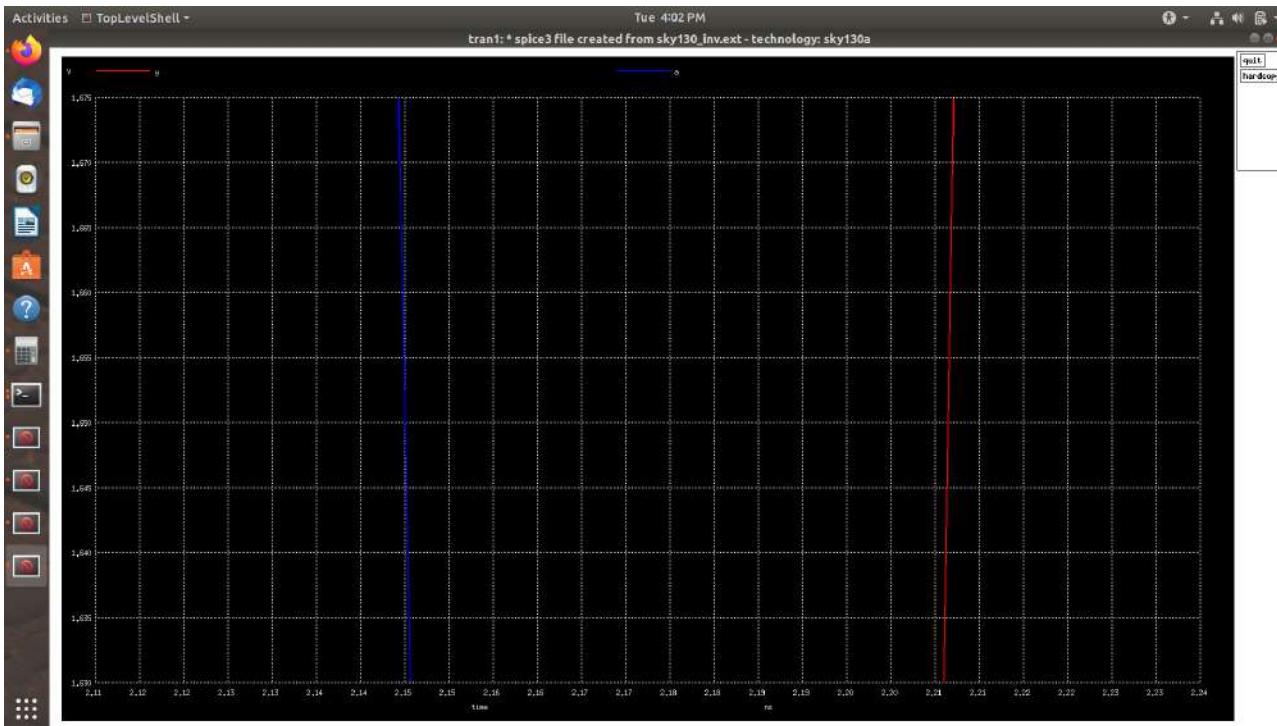
Initial Transient Solution
-----
Node          Voltage
-----
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
x0 = 4.09555e-09, y0 = 0.660127
x0 = 4.0536e-09, y0 = 2.64

```

Rise Cell Delay Calculation

50% Screenshots



Activities Terminal

Tue 4:03 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign

```

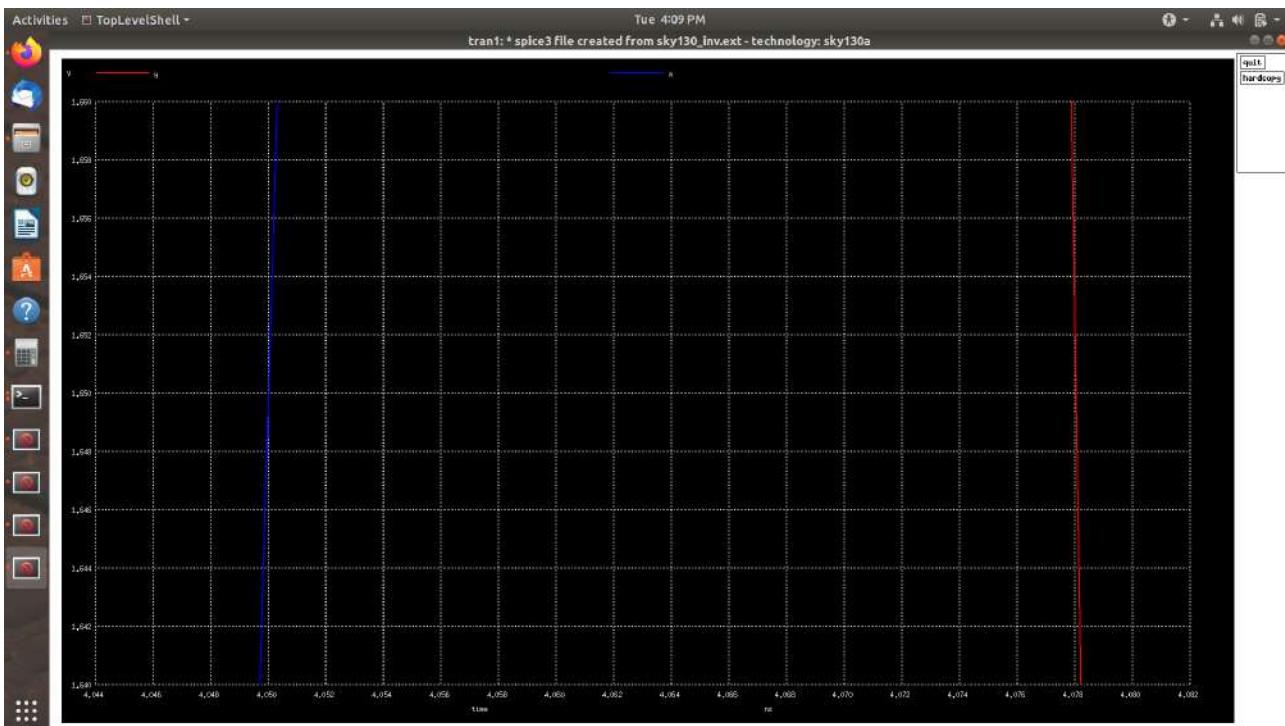
File Edit View Search Terminal Help
Node          Voltage
-----
y             3.3
a             0
vpwr          3.3
vgnd          0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
x0 = 4.09555e-09, y0 = 0.660127
x0 = 4.0536e-09, y0 = 2.64
x0 = 2.21144e-09, y0 = 1.65
x0 = 2.15008e-09, y0 = 1.6501

```

Fall Cell Delay Calculation

50% Screenshots



Activities Terminal Tue 4:10 PM

vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```

File Edit View Search Terminal Help
vpwr          3.3
vgnd          0
va#branch     0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
> x0 = 2.24638e-09, y0 = 2.6403
> x0 = 4.09555e-09, y0 = 0.660127
> x0 = 4.0536e-09, y0 = 2.64
> x0 = 2.21144e-09, y0 = 1.65
> x0 = 2.15008e-09, y0 = 1.6501
> x0 = 4.07807e-09, y0 = 1.65005
> x0 = 4.05e-09, y0 = 1.65002

```

6. Find problem in the DRC section of the old magic tech file for the skywater process and fix them.

Link to Sky130 Periphery rules: <https://skywater-pdk.readthedocs.io/en/main/rules/periphery.html>

Commands to download and view the corrupted skywater process magic tech file and associated files to perform drc corrections

```
# Change to home directory
```

```
cd
```

```
# Command to download the lab files
```

```
wget http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
```

```
# Since lab file is compressed command to extract it
```

```
tar xfz drc_tests.tgz
```

```
# Change directory into the lab folder
```

```
cd drc_tests
```

```
# List all files and directories present in the current directory
```

```
ls -al
```

```
# Command to view .magicrc file
```

```
gvim .magicrc
```

```
# Command to open magic tool in better graphics
```

```
magic -d XR &
```

Screenshots of commands run

Activities Terminal Thu 10:33 PM
vsduser@vsdsquadron:~/drc_tests

```
File Edit View Search Terminal Help
vsduser@vsdsquadron:~$ cd
vsduser@vsdsquadron:~$ wget http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
--2024-03-21 22:31:14-- http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
Resolving opencircuitdesign.com (opencircuitdesign.com)... 69.251.37.208
Connecting to opencircuitdesign.com (opencircuitdesign.com)|69.251.37.208|:80... connected.
HTTP request sent, awaiting response... 200 OK
Length: 41651 (41K) [application/x-gzip]
Saving to: 'drc_tests.tgz'

drc_tests.tgz          100%[=====] 40.67K 160KB/s in 0.3s

2024-03-21 22:31:15 (160 KB/s) - 'drc_tests.tgz' saved [41651/41651]

vsduser@vsdsquadron:~$ tar xfz drc_tests.tgz
vsduser@vsdsquadron:~$ cd drc_tests
vsduser@vsdsquadron:~/drc_tests$ ls -al
total 276
drwxrwxr-x 2 vsduser vsduser 4096 Sep 16 2020 .
drwxr-xr-x 22 vsduser vsduser 4096 Mar 21 22:31 ..
-rw-rw-r-- 1 vsduser vsduser 3178 Sep 15 2020 capm.mag
-rw-rw-r-- 1 vsduser vsduser 3610 Sep 16 2020 difftap.mag
-rw-rw-r-- 1 vsduser vsduser 1535 Sep 16 2020 dnwell.mag
-rw-rw-r-- 1 vsduser vsduser 1684 Sep 15 2020 hvtp.mag
-rw-rw-r-- 1 vsduser vsduser 897 Sep 15 2020 hvtr.mag
-rw-rw-r-- 1 vsduser vsduser 11586 Sep 15 2020 licon.mag
-rw-rw-r-- 1 vsduser vsduser 1480 Sep 15 2020 li.mag
-rw-rw-r-- 1 vsduser vsduser 4648 Sep 15 2020 lvtn.mag
-rw-rw-r-- 1 vsduser vsduser 2565 Sep 15 2020 .magicrc
```

Activities Terminal Thu 10:34 PM
vsduser@vsdsquadron:~/drc_tests

```
File Edit View Search Terminal Help
-rw-rw-r-- 1 vsduser vsduser 11586 Sep 15 2020 licon.mag
-rw-rw-r-- 1 vsduser vsduser 1480 Sep 15 2020 li.mag
-rw-rw-r-- 1 vsduser vsduser 4648 Sep 15 2020 lvtn.mag
-rw-rw-r-- 1 vsduser vsduser 2565 Sep 15 2020 .magicrc
-rw-rw-r-- 1 vsduser vsduser 1198 Sep 15 2020 mcon.mag
-rw-rw-r-- 1 vsduser vsduser 2103 Sep 15 2020 met1.mag
-rw-rw-r-- 1 vsduser vsduser 1799 Sep 15 2020 met2.mag
-rw-rw-r-- 1 vsduser vsduser 1500 Sep 16 2020 met3.mag
-rw-rw-r-- 1 vsduser vsduser 1114 Sep 16 2020 met4.mag
-rw-rw-r-- 1 vsduser vsduser 757 Sep 15 2020 met5.mag
-rw-rw-r-- 1 vsduser vsduser 1948 Sep 15 2020 npc.mag
-rw-rw-r-- 1 vsduser vsduser 2497 Sep 15 2020 nsd.mag
-rw-rw-r-- 1 vsduser vsduser 1351 Sep 16 2020 nwell.mag
-rw-rw-r-- 1 vsduser vsduser 536 Sep 15 2020 pad.mag
-rw-rw-r-- 1 vsduser vsduser 5588 Sep 16 2020 poly.mag
-rw-rw-r-- 1 vsduser vsduser 2565 Sep 15 2020 psd.mag
-rw-rw-r-- 1 vsduser vsduser 3025 Sep 15 2020 rpm.mag
-rw-rw-r-- 1 vsduser vsduser 135962 Sep 16 2020 sky130A.tech
-rw-rw-r-- 1 vsduser vsduser 2476 Sep 16 2020 tunm.mag
-rw-rw-r-- 1 vsduser vsduser 4114 Sep 16 2020 varac.mag
-rw-rw-r-- 1 vsduser vsduser 1271 Sep 15 2020 via2.mag
-rw-rw-r-- 1 vsduser vsduser 1267 Sep 15 2020 via3.mag
-rw-rw-r-- 1 vsduser vsduser 966 Sep 15 2020 via4.mag
-rw-rw-r-- 1 vsduser vsduser 955 Sep 15 2020 via.mag
vsduser@vsdsquadron:~/drc_tests$ gvim .magicrc
vsduser@vsdsquadron:~/drc_tests$ magic -d XR
```

Screenshot of .magicrc file

```

Thu 10:35 PM
.magicrc (~/.drc_tests) - GVIM

File Edit Tools Syntax Buffers Window Help
1 puts stdout "Sourcing design .magicrc for technology sky130A ..."
2
3 # Put grid on 0.005 pitch. This is important, as some commands don't
4 # rescale the grid automatically (such as lef read?).
5
6 set scalefac [tech lambda]
7 if {[lindex $scalefac 1] < 2} {
8     scalegrid 1 2
9 }
10
11 # drc off
12 drc euclidean on
13
14 # Allow override of PDK path from environment variable PDKPATH
15 if {[catch {set PDKPATH $env(PDKPATH)}]} {
16     set PDKPATH "~/cad/pdk/sky130A"
17 }
18
19 # loading technology
20 # tech load $PDKPATH/libs.tech/magic/sky130A.tech
21 tech load sky130A.tech
22
23 # load device generator
24 # source $PDKPATH/libs.tech/magic/sky130A.tcl
25

".magicrc" 74L, 2565C

```

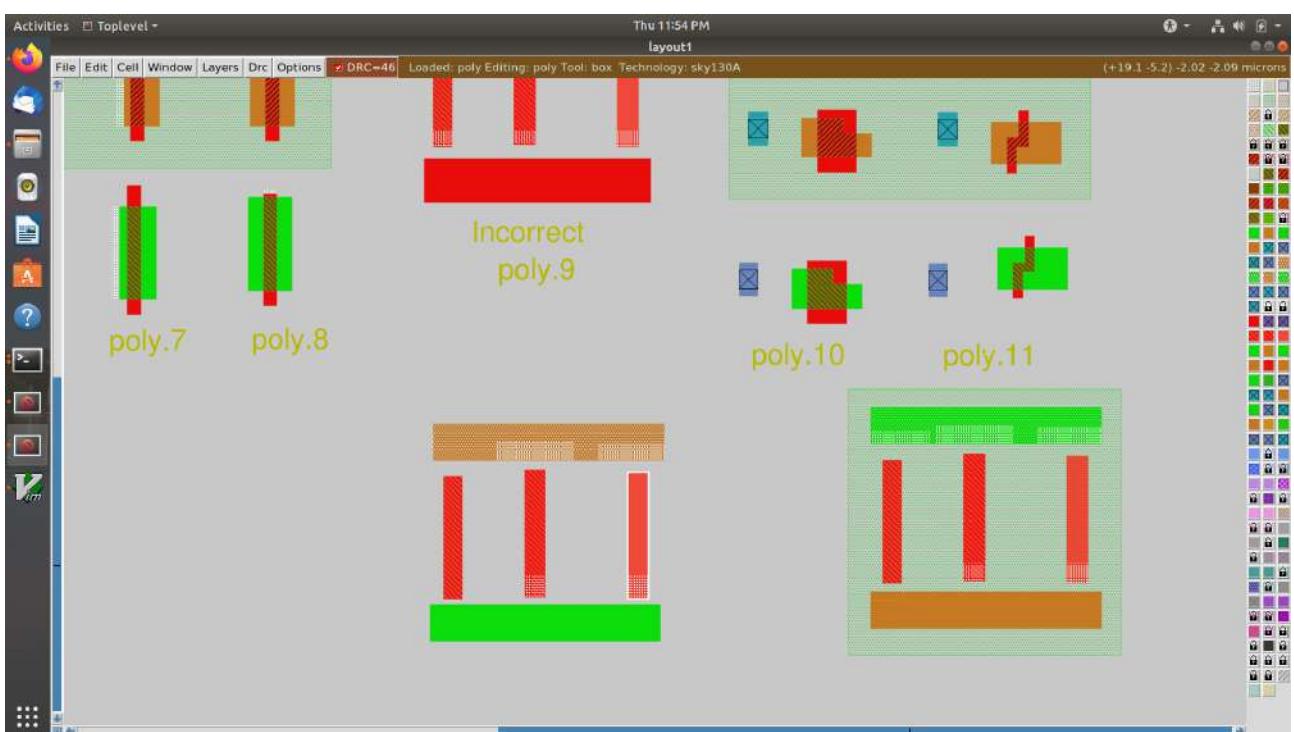
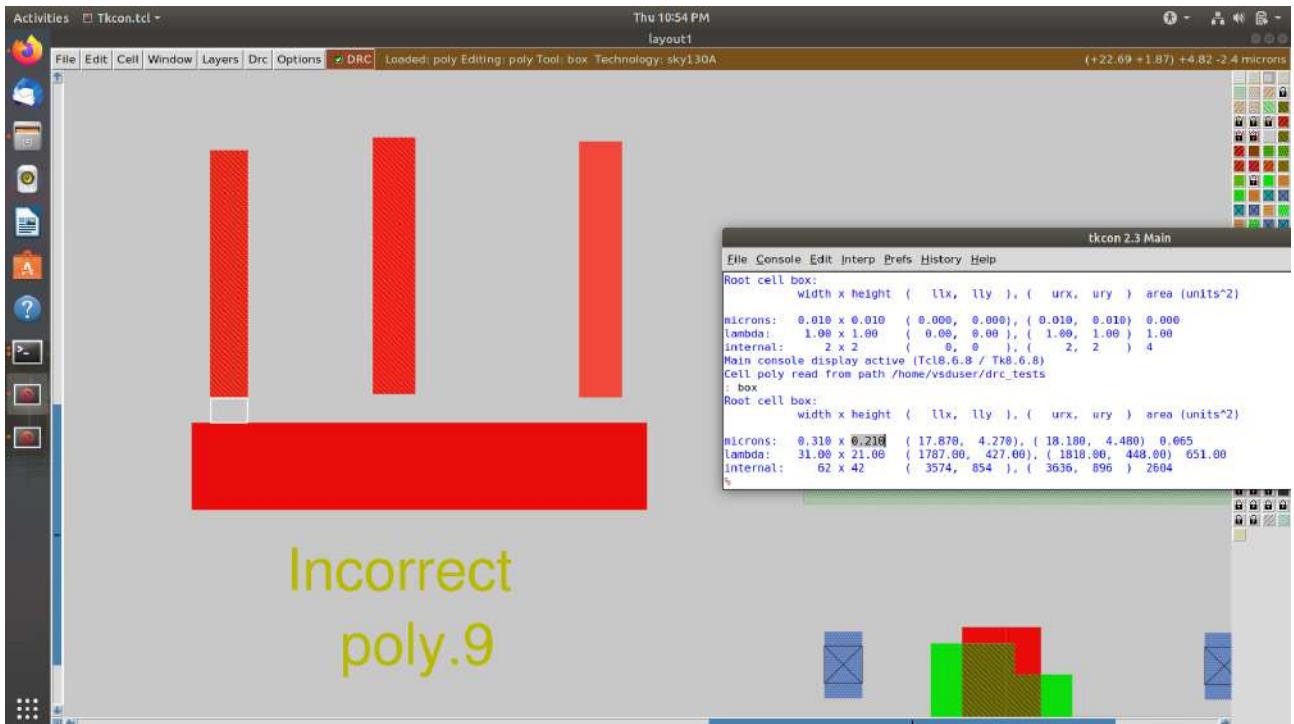
1,1 Top

Incorrectly implemented poly.9 simple rule correction

Screenshot of poly rules

Periphery Rules		Search	google/skywater-pdk
SkyWater SKY130 PDK	(poly.1a)	Width of poly	0.150 μm
Versioning Information	(poly.1b)	Min channel length (poly width) for peft overlapping lvtn (exempt rule for dummy_poly in cells listed on Table H3)	0.350 μm
Current Status	(poly.2)	Spacing of poly to poly except for poly.c2 and poly.c3. Exempt cell: sr_bld_eq where it is same as poly.c2	0.210 μm
Known Issues	(poly.3)	Min poly resistor width	0.330 μm
Design Rules	(poly.4)	Spacing of poly on field to diff (parallel edges only)	P 0.075 μm
PDK Contents	(poly.5)	Spacing of poly on field to tap	P 0.055 μm
Analog Design	(poly.6)	Spacing of poly on diff to abutting tap (min source)	P 0.300 μm
Digital Design	(poly.7)	Extension of diff beyond poly (min drain)	P 0.250
Simulation	(poly.8)	Extension of poly beyond diffusion (endcap)	P 0.130
Physical & Design Verification	(poly.9)	Poly resistor spacing to poly or spacing (no overlap) to diff/tap	0.480 μm
Python API	(poly.10)	Poly can't overlap inner corners of diff	
Previous Nomenclature	(poly.11)	No 90 deg turns of poly on diff	
Glossary	(poly.12)	(Poly NOT (inwell NOT hv)) may not overlap tap: Rule exempted for cell name "g8tge_n_fq2" and gated_rgn and inside UHVL.	P
How to Contribute	(poly.13)	Poly must not overlap diff/rs	
Partners	(poly.14)		
References	(poly.15)		

Incorrectly implemented poly.9 rule no drc violation even though spacing < 0.48μ



New commands inserted in sky130A.tech file to update drc

Activities M GVim Thu 11:58 PM
sky130A.tech (~/.drc_tests) - GVIM

```

4803
4804 variants *
4805
4806 #-----
4807 # POLY
4808 #-----
4809
4810 width allpoly 150 "poly.width < %d (poly.1a)"
4811 spacing allpoly allpoly 210 touching_ok "poly.spacing < %d (poly.2)"
4812 spacing allpolynonfet alldiffvnonfet 75 corner_ok allfets \
    "poly.spacing to Diffusion < %d (poly.4a)"
4813 spacing npres alldiff 480 touching_illegal \
    "poly.resistor spacing to alldiff < %d (poly.9)"
4814 spacing npres allpolynonres 480 touching_illegal \
    "poly.resistor spacing to allpolynonres < %d (poly.9)"
4815 overhang *ndiff,rndiff nfet,scnfet,npd,npass 250 "N-Diffusion overhang of nmos < %d (poly.7)"
4816 overhang *mvndiff,mvrndiff mvnfet,mvnnfet 250 \
    "N-Diffusion overhang of nmos < %d (poly.7)"
4817 overhang *pdifff,rdifff pfet,scpfet,ppu 250 "P-Diffusion overhang of pmos < %d (poly.7)"
4818 overhang *mvpdiff,mvrpdifff mvpfet 250 "P-Diffusion overhang of pmos < %d (poly.7)"
4819 overhang *poly allfets 130 "poly.overhang of transistor < %d (poly.8)"
4820 rect_only allfets "No bends in transistors (poly.11)"
4821 rect_only xhrpoly,uhrpoly "No bends in poly resistors (poly.11)"
4822 extend xpc/a xhrpoly,uhrpoly 2160 \
    "poly.contact extends poly resistor by < %d (lcon.1c + li.5)"
4823
4824 -- VISUAL --
4817,56-63 81%

```

Activities M GVim Thu 11:09 PM
sky130A.tech (~/.drc_tests) - GVIM

```

5168 # xhrpoly (P+ poly resistor)
5169 #-----
5170
5171 width xhrpoly 350 "xhrpoly resistor width < %d (P+ poly.1a)"
5172 # NOTE: xhrpoly resistor requires choice of discrete widths 0.35, 0.69, ... up to 1.27.
5173
5174 #-----
5175 # uhrpoly (P+ poly resistor, 2kOhm/sq)
5176 #-----
5177
5178 width uhrpoly 350 "uhrpoly resistor width < %d"
5179 spacing xhrpoly,uhrpoly,xpc alldiff 480 touching_illegal \
    "xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
5180 spacing xhrpoly,uhrpoly,xpc allpolynonres 480 touching_illegal \
    "xhrpoly/uhrpoly resistor spacing to allpolynonres < %d (poly.9)"
5181
5182
5183
5184
5185 #-----
5186 # MOS Varactor device rules
5187 #-----
5188
5189 overhang *nsd var,varhvt 250 \
    "N-Tap overhang of Varactor < %d (var.4)"
5190
5191
5192 overhang *mvnsd mvvar 250 \
-- VISUAL --
5182,67-74 87%

```

Commands to run in tkcon window

```
# Loading updated tech file
```

```
tech load sky130A.tech
```

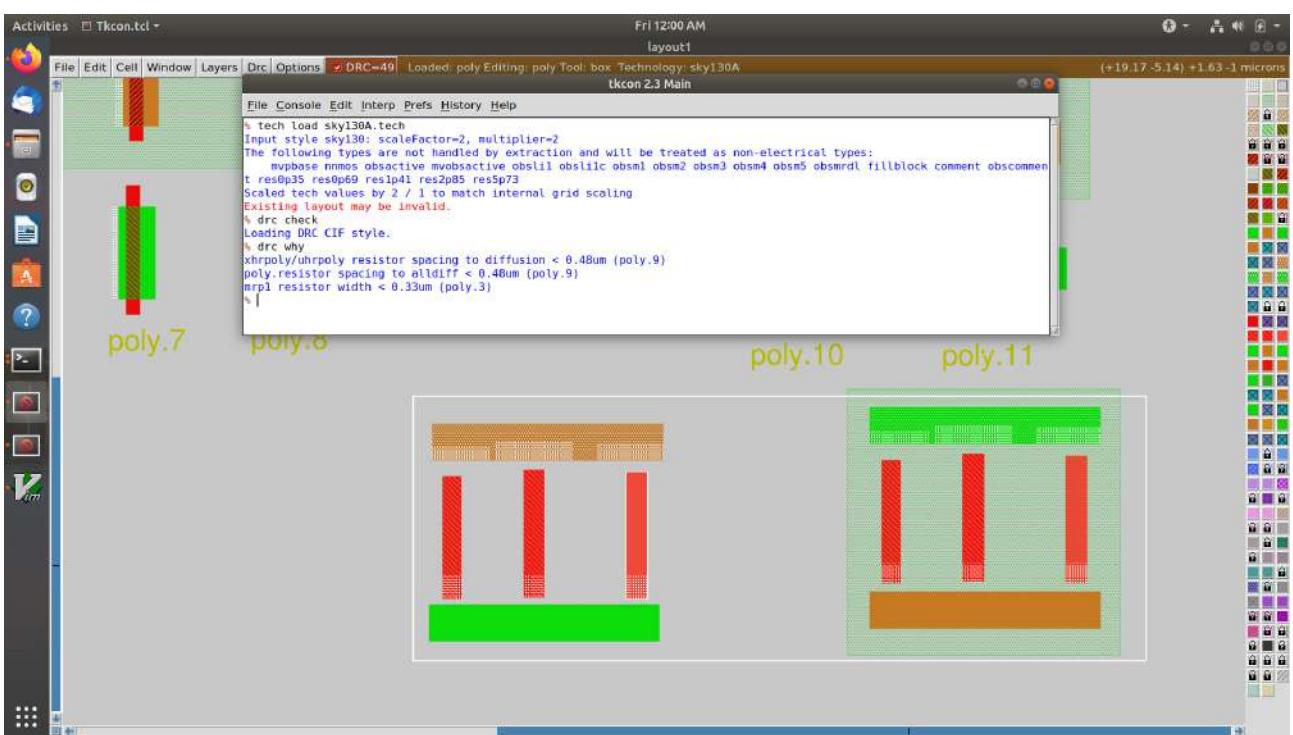
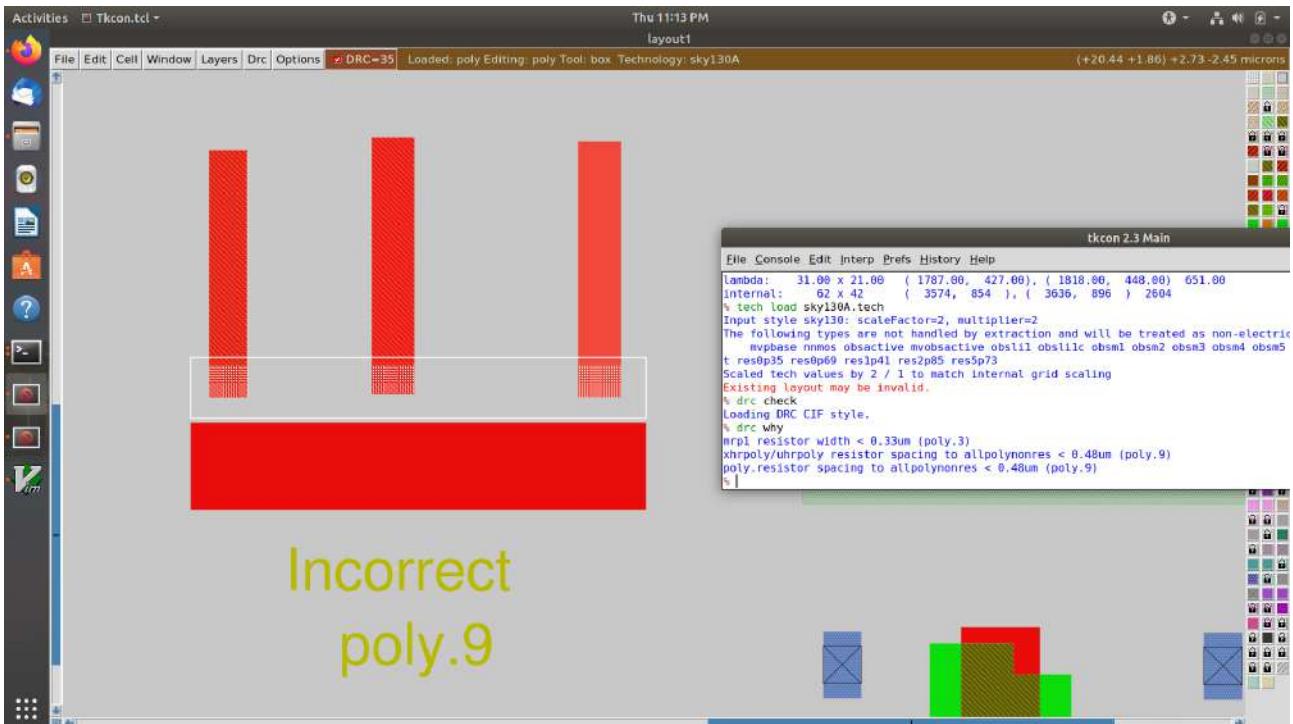
```
# Must re-run drc check to see updated drc errors
```

```
drc check
```

```
# Selecting region displaying the new errors and getting the error messages
```

```
drc why
```

Screenshot of magic window with rule implemented



Incorrectly implemented difftap.2 simple rule correction

Screenshot of difftap rules

Activities Firefox Web Browser Fri 12:14 AM

Editing soc-design-and... yosys-tcl-ui-report/RE... nickson-jose/vsdstdce... Online Clipboard Periphery Rules — Sky... Magic VLSI

<https://skywater-pdk.readthedocs.io/en/main/rules/periphery.html#difftap>

Periphery Rules Search google@skywater-pdk

SkyWater SKY130 PDK

Versioning Information Current Status Known Issues Design Rules PDK Contents Analog Design Digital Design Simulation Physical & Design Verification Python API Previous Nomenclature Glossary How to Contribute Partners References

Name Description Flags Value Unit

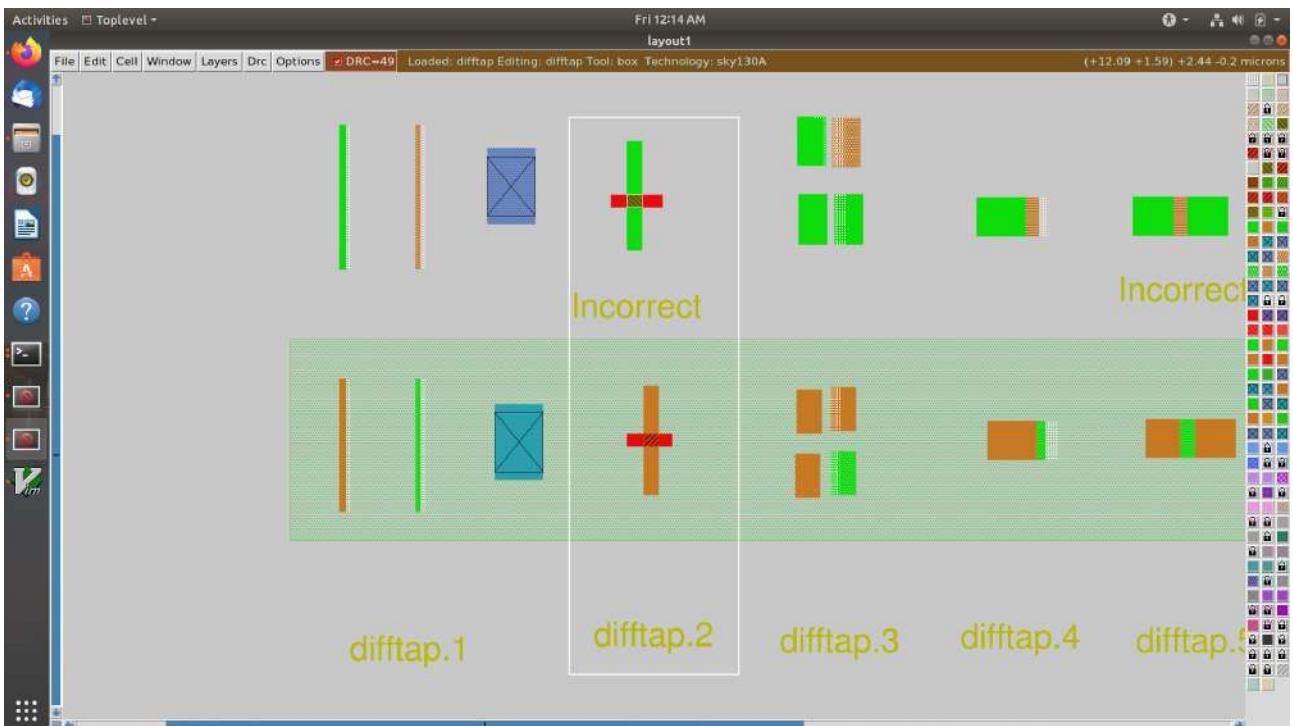
Table 38 Function: Defines active regions and contacts to substrate

Name	Description	Flags	Value	Unit
(difftap.1)	Width of diff or tap	P	0.150	μm
(difftap.2)	Minimum channel width (Diff And Poly) except for FETs inside areaid.sc: Rule exempted in the SP8* flows only, for the cells listed in rule difftap.2a	P	0.420	μm
(difftap.2a)	Minimum channel width (Diff And Poly) for cell names "s8cell_ee_plus_ssein_a", "s8cell_ee_plus_ssein_b", "s8cell_ee_plus_sseip_a", "s8cell_ee_plus_sseip_b", "s8lpls_pl8", "s8lpls_rdrv4", "s8lpls_rdrv4f" and "s8lpls_rdrv8"	P, NA	NA	μm
(difftap.2b)	Minimum channel width (Diff And Poly) for FETs inside areaid.sc	P	0.360	μm
(difftap.3)	Spacing of diff to diff, tap to tap, or non-abutting diff to tap		0.270	μm
(difftap.4)	Min tap bound by one diffusion		0.290	
(difftap.5)	Min tap bound by two diffusions	P	0.400	
(difftap.6)	Diff and tap are not allowed to extend beyond their abutting edge			
(difftap.7)	Spacing of difftap abutting edge to a non-conciding diff or tap edge	NE	0.130	μm
(difftap.8)	Enclosure of (p+) diffusion by N-well. Rule exempted inside UHVI.	DE NE P	0.180	μm
(difftap.9)	Spacing of (n+) diffusion to N-well outside UHVI	DE NE P	0.340	μm
(difftap.10)	Enclosure of (n+) tap by N-well. Rule exempted inside UHVI.	NE P	0.180	μm
Creation of resistors in N-well. Only recommended inside UHVI				
Δ 196 nm				

Contents

- Periphery Rules (x,-) (dnwell,-) (nwell,-) (pwell,-) (pudem,-) (hvtp,-) (hvtr,-) (lvtn,-) (ncm,-) (difftap,-) (tunn,-) (poly,-) (rpm,-) (varac,-) (photo,-) (npc,-) (n/ psd,-) (licon,-) (li,-) (ct,-) (capm,-) (vpp,-) /m1 -

Incorrectly implemented difftap.2 rule no drc violation even though spacing < 0.42μ



New commands inserted in sky130A.tech file to update drc

```
5178 width uhrpoly 350 "uhrpoly resistor width < %d"
5179 spacing xhrpoly,uhrpoly,xpc alldiff 480 touching_illegal \
      "xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
5180 spacing xhrpoly,uhrpoly,xpc allpolynonres 480 touching_illegal \
      "xhrpoly/uhrpoly resistor spacing to allpolynonres < %d (poly.9)"
5181
5182
5183
5184
5185 #-----
5186 # MOS Varactor device rules
5187 #-----
5188
5189 width pmos 420 \
      "mos transistor formed should have minimum width of < %d (difftap.2)"
5190 width nmos 420 \
      "mos transistor formed should have minimum width of < %d (difftap.2)"
5191
5192
5193 overhang *nsd var,varhvt 250 \
      "N-Tap overhang of Varactor < %d (var.4)"
5194
5195 overhang *mvnsd mvvar 250 \
      "N-Tap overhang of Varactor < %d (var.4)"
5196
5197 width var,varhvt,mvvar 180 "Varactor length < %d (var.1)"
5198 extend var,varhvt,mvvar *poly 1000 "Varactor width < %d (var.2)"
5199
5200
5201
5202
```

-- VISUAL --

5192, 71 88%

Commands to run in tkcon window

```
# Loading updated tech file
```

```
tech load sky130A.tech
```

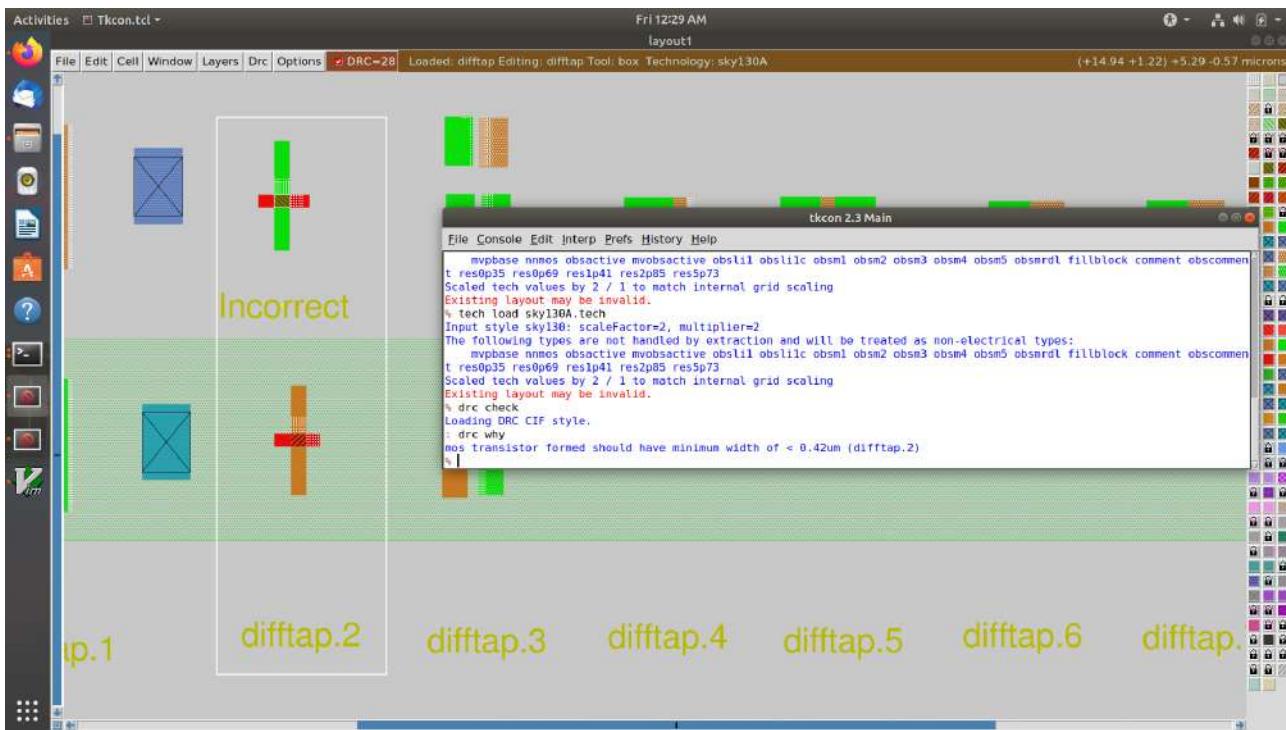
```
# Must re-run drc check to see updated drc errors
```

```
drc check
```

```
# Selecting region displaying the new errors and getting the error messages
```

```
drc why
```

Screenshot of magic window with rule implemented



Incorrectly implemented nwell.4 complex rule correction

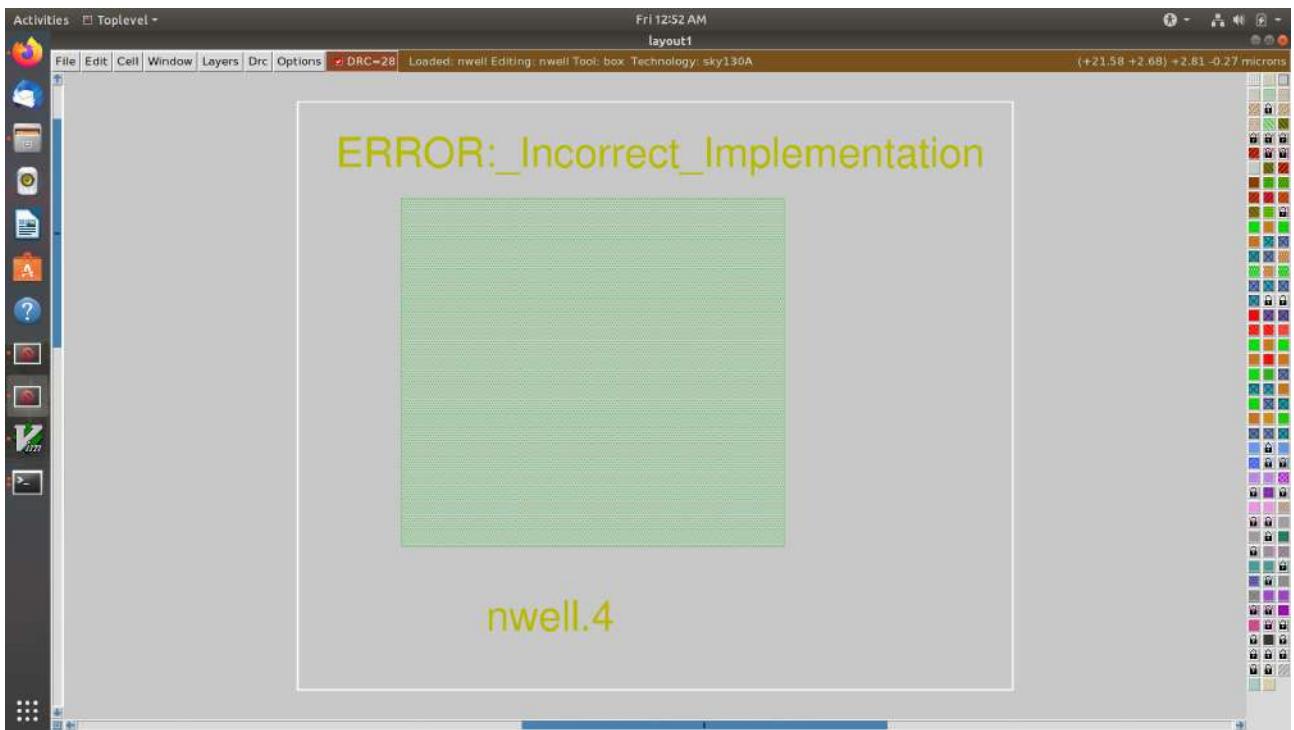
Screenshot of nwell rules

Table 31 Function: Define nwell implant regions.					
Name	Description	Flags	Value	Unit	
(nwell.1)	Width of nwell		0.840	μm	
(nwell.2a)	Spacing between two n-wells		1.270	μm	
(nwell.2b)	Manual merge wells if less than minimum				
(nwell.4)	All n-wells will contain metal-contacted tap (rule checks only for icon on top). Rule exempted from high voltage cells inside UHVI				
(nwell.5)	Deep nwell must be enclosed by nwell by atleast... Exempted inside UHVI or areaid.	TC	0.400	μm	
(nwell.5a)	min enclosure of nwell by dnwell inside UHVI		N/A	N/A	
(nwell.5b)	nwell inside UHVI must not be on the same net as nwell outside UHVI		N/A	N/A	
(nwell.6)	Min enclosure of nwell hole by deep nwell outside UHVI	TC	1.030	μm	
(nwell.7)	Min spacing between nwell and deep nwell on separate nets. Spacing between nwell and deep nwell on the same net is set by the sum of the rules nwell.2 and nwell.5. By default, DRC run on a cell checks for the separate-net spacing, when nwell and deep nwell nets are separate within the cell hierarchy and are joined in the upper hierarchy. To allow net names to be joined and make the same-net rule applicable in this case, the 'joinNets' switch should be turned on. waffle_chip	TC	4.500	μm	

Contents

- Periphery Rules
 - (x,-)
 - (dnwell,-)
 - (nwell,-)
 - (pwbn,-)
 - (pwdem,-)
 - (hvtc,-)
 - (hvtr,-)
 - (lvtn,-)
 - (ncm,-)
 - (difftap,-)
 - (tunn,-)
 - (poly,-)
 - (rpm,-)
 - (varac,-)
 - (photo,-)
 - (npc,-)
 - (n/ psd,-)
 - (licon,-)
 - (li,-,-)
 - (ct,-)
 - (capc,-)
 - (vpp,-)
 - (v_main)

Incorrectly implemented nwell.4 rule no drc violation even though no tap present in nwell



New commands inserted in sky130A.tech file to update drc

Activities M GVim

Fri 1:03 AM
sky130A.tech (~/.drc_tests) - GVIM

```

1230 options calma-permissive-labels
1231
1232 # Ensure nwell overlaps dnwell at least 0.4um outside and 1.03um inside
1233 templayer dnwell_shrink dnwell
1234 shrink 1030
1235
1236 templayer nwell_missing dnwell
1237 grow 400
1238 and-not dnwell_shrink
1239 and-not nwell
1240
1241 templayer nwell_tapped
1242 bloat-all nsc nwell
1243
1244 templayer nwell_untapped nwell
1245 and-not nwell_tapped
1246
1247 # SONOS nFET devices must be in deep nwell
1248 templayer dnwell_missing nsonos
1249 and-not dnwell
1250
1251 # Define MiM cap bottom plate for spacing rule
1252 templayer mim_bottom
1253 bloat-all *mimcap *metal3
1254
-- VISUAL --

```

1245, 22 20%

Activities M GVim

Fri 1:04 AM
sky130A.tech (~/.drc_tests) - GVIM

```

4721 spacing dnwell dnwell 6300 touching_ok "Deep N-well spacing < %d (dnwell.3)"
4722 spacing dnwell allnwell 4500 surround_ok \
4723 "Deep N-well spacing to N-well < %d (nwell.7)"
4724 cifmaxwidth nwell_missing 0 bend_illegal \
4725 "N-well overlap of Deep N-well < 0.4um outside, 1.03um inside (nwell.5a, 7)"
4726 cifmaxwidth dnwell_missing 0 bend_illegal \
4727 "SONOS nFET must be in Deep N-well (tunm.6a)"
4728
4729 #-----
4730 # NWELL
4731 #-----
4732
4733 width allnwell 840 "N-well width < %d (nwell.1)"
4734 spacing allnwell allnwell 1270 touching_ok "N-well spacing < %d (nwell.2a)"
4735
4736 variants (full)
4737 cifmaxwidth nwell_untapped 0 bend_illegal \
4738 "Nwell missing tap (nwell.4)"
4739 variants *
4740
4741 #-----
4742 # DIFF
4743 #-----
@ -- VISUAL --

```

4739, 11 80%

Commands to run in tkcon window

```
# Loading updated tech file
```

```
tech load sky130A.tech
```

Change drc style to drc full

drc style drc(full)

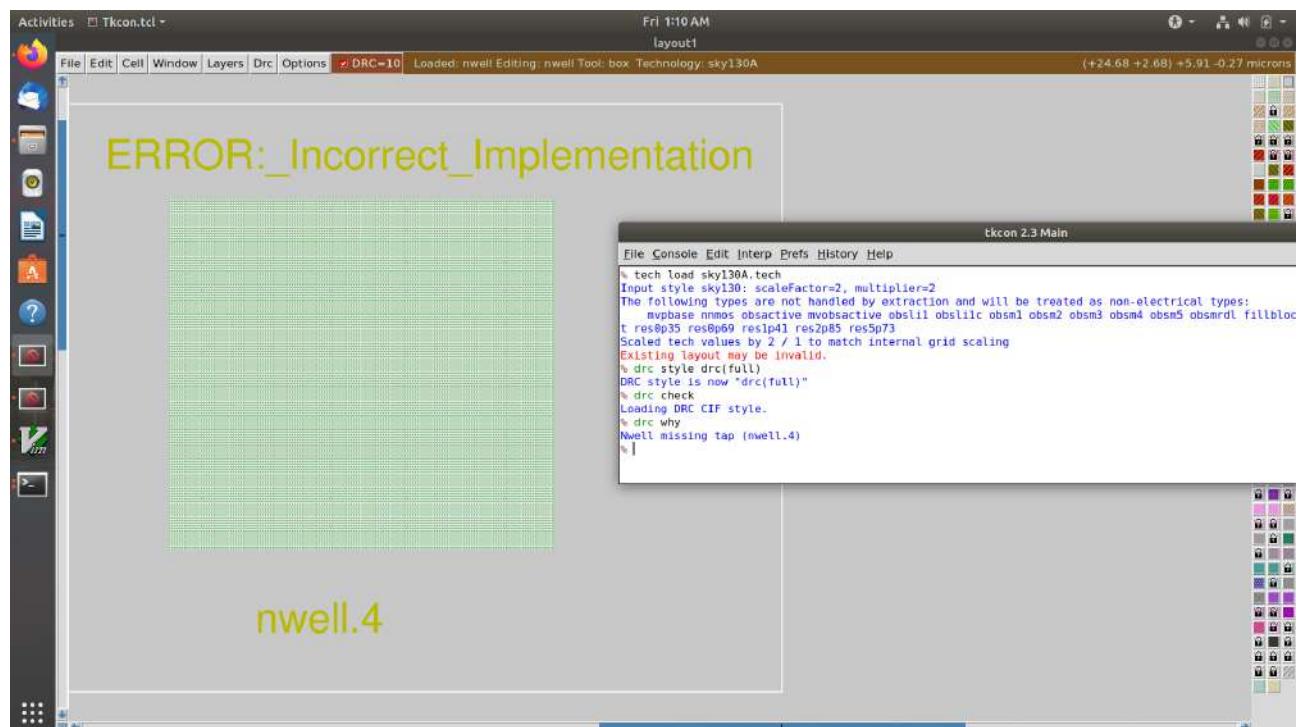
```
# Must re-run drc check to see updated drc errors
```

drc check

Selecting region displaying the new errors and getting the error messages

drc why

Screenshot of magic window with rule implemented



Section 4 - Pre-layout timing analysis and importance of good clock tree (22/03/2024 - 24/03/2024)

Theory

Implementation

- Section 4 tasks:-
 12. Fix up small DRC errors and verify the design is ready to be inserted into our flow.
 13. Save the finalized layout with custom name and open it.
 14. Generate lef from the layout.
 15. Copy the newly generated lef and associated required lib files to 'picorv32a' design 'src' directory.
 16. Edit 'config.tcl' to change lib file and add the new extra lef into the openlane flow.
 17. Run openlane flow synthesis with newly inserted custom inverter cell.
 18. Remove/reduce the newly introduced violations with the introduction of custom inverter cell by modifying design parameters.
 19. Once synthesis has accepted our custom inverter we can now run floorplan and placement and verify the cell is accepted in PnR flow.
 20. Do Post-Synthesis timing analysis with OpenSTA tool.
 21. Make timing ECO fixes to remove all violations.

22. Replace the old netlist with the new netlist generated after timing ECO fix and implement the floorplan, placement and cts.
23. Post-CTS OpenROAD timing analysis.
24. Explore post-CTS OpenROAD timing analysis by removing 'sky130_fd_sc_hd_clkbuf_1' cell from clock buffer list variable 'CTS_CLK_BUFFER_LIST'.
 - Section 4 - Tasks 1 to 4 files, reports and logs can be found in the following folder:

Section 4 - Tasks 1 to 4 (vsdstdcelldesign)

- Section 4 - Task 4 files, reports and logs can be found in the following folder:

Section 4 - Task 4 (src)

- Section 4 - Task 5 files, reports and logs can be found in the following folder:

Section 4 - Task 5 (picorv32a)

- Section 4 - Tasks 6 to 8 & 11 to 13 logs, reports and results can be found in following run folder:

Section 4 - Tasks 6 to 8 & 11 to 13 Run (24-03_10-03)

- Section 4 - Tasks 9 to 11 logs, reports and results can be found in following run folder:

Section 4 - Tasks 9 to 11 Run (25-03_18-52)

1. Fix up small DRC errors and verify the design is ready to be inserted into our flow.

Conditions to be verified before moving forward with custom designed cell layout:

- Condition 1: The input and output ports of the standard cell should lie on the intersection of the vertical and horizontal tracks.
- Condition 2: Width of the standard cell should be odd multiples of the horizontal track pitch.
- Condition 3: Height of the standard cell should be even multiples of the vertical track pitch.

Commands to open the custom inverter layout

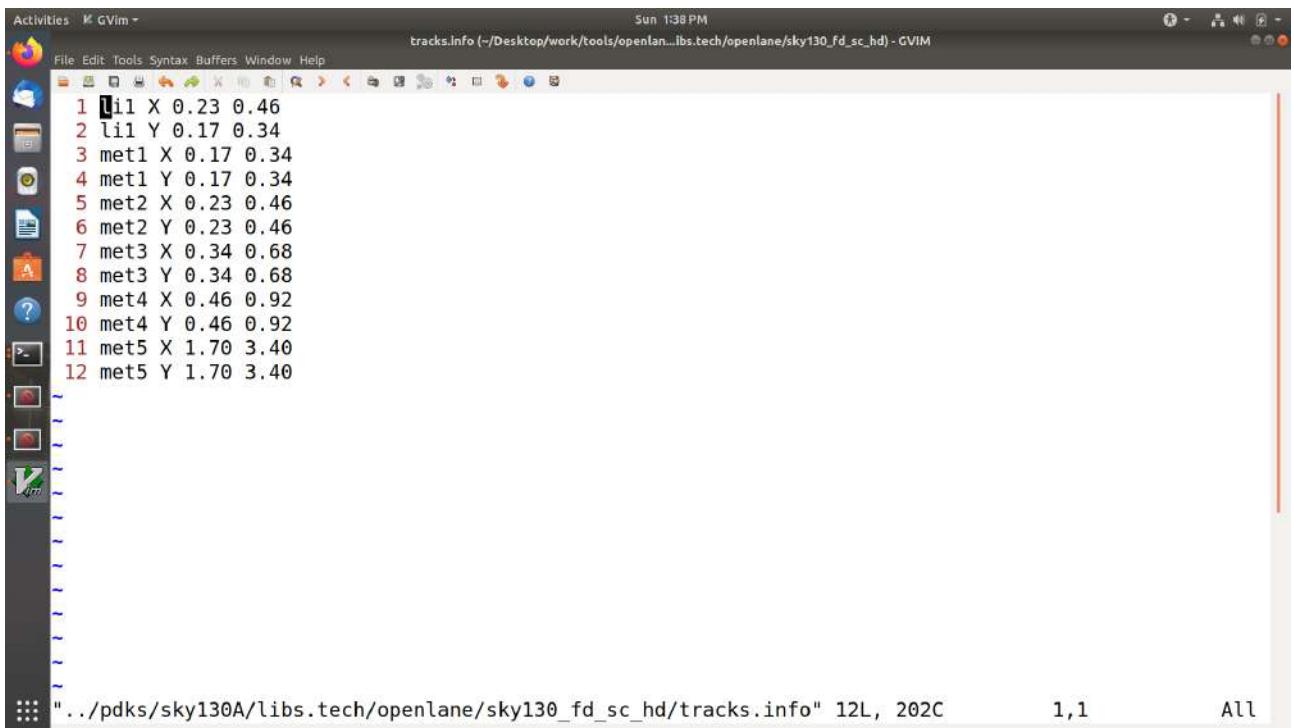
```
# Change directory to vsdstdcelldesign
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
```

```
# Command to open custom inverter layout in magic
```

```
magic -T sky130A.tech sky130_inv.mag &
```

Screenshot of tracks.info of sky130_fd_sc_hd



A screenshot of the GVIM text editor window. The title bar reads "activities K. GVIM" and "tracks.info (~/Desktop/work/tools/openlane/libs.tech/openlane/sky130_fd_sc_hd) - GVIM". The status bar shows "Sun 1:38 PM" and "1,1 All". The main pane displays a list of track coordinates:

```
1 l1l X 0.23 0.46
2 l1l Y 0.17 0.34
3 met1 X 0.17 0.34
4 met1 Y 0.17 0.34
5 met2 X 0.23 0.46
6 met2 Y 0.23 0.46
7 met3 X 0.34 0.68
8 met3 Y 0.34 0.68
9 met4 X 0.46 0.92
10 met4 Y 0.46 0.92
11 met5 X 1.70 3.40
12 met5 Y 1.70 3.40
```

Commands for tkcon window to set grid as tracks of locali layer

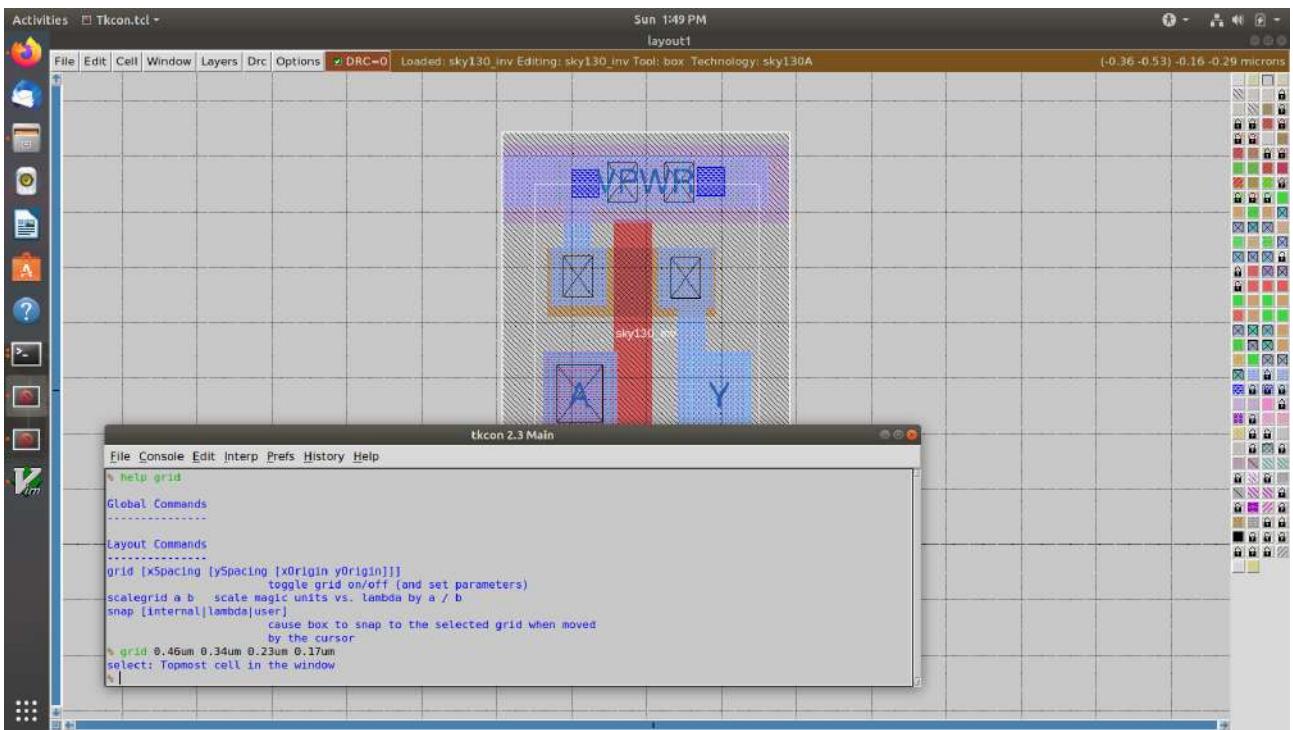
```
# Get syntax for grid command
```

```
help grid
```

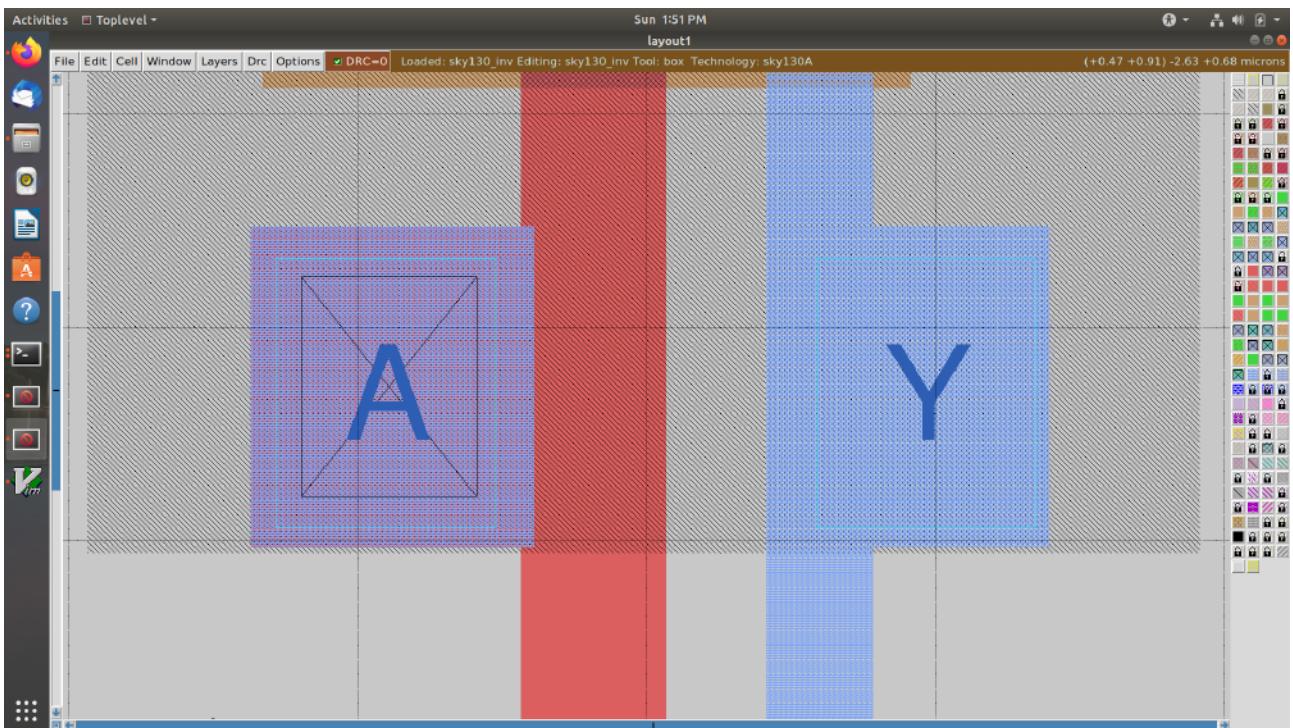
```
# Set grid values accordingly
```

```
grid 0.46um 0.34um 0.23um 0.17um
```

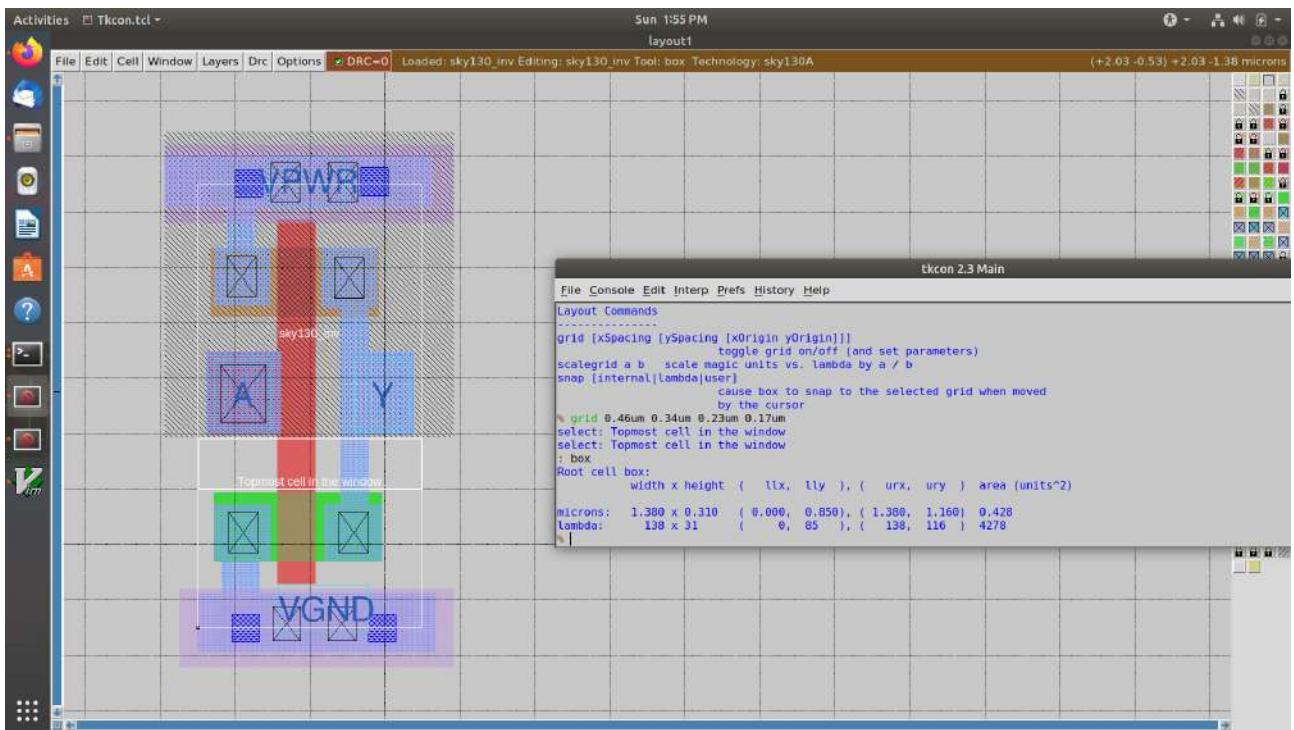
Screenshot of commands run



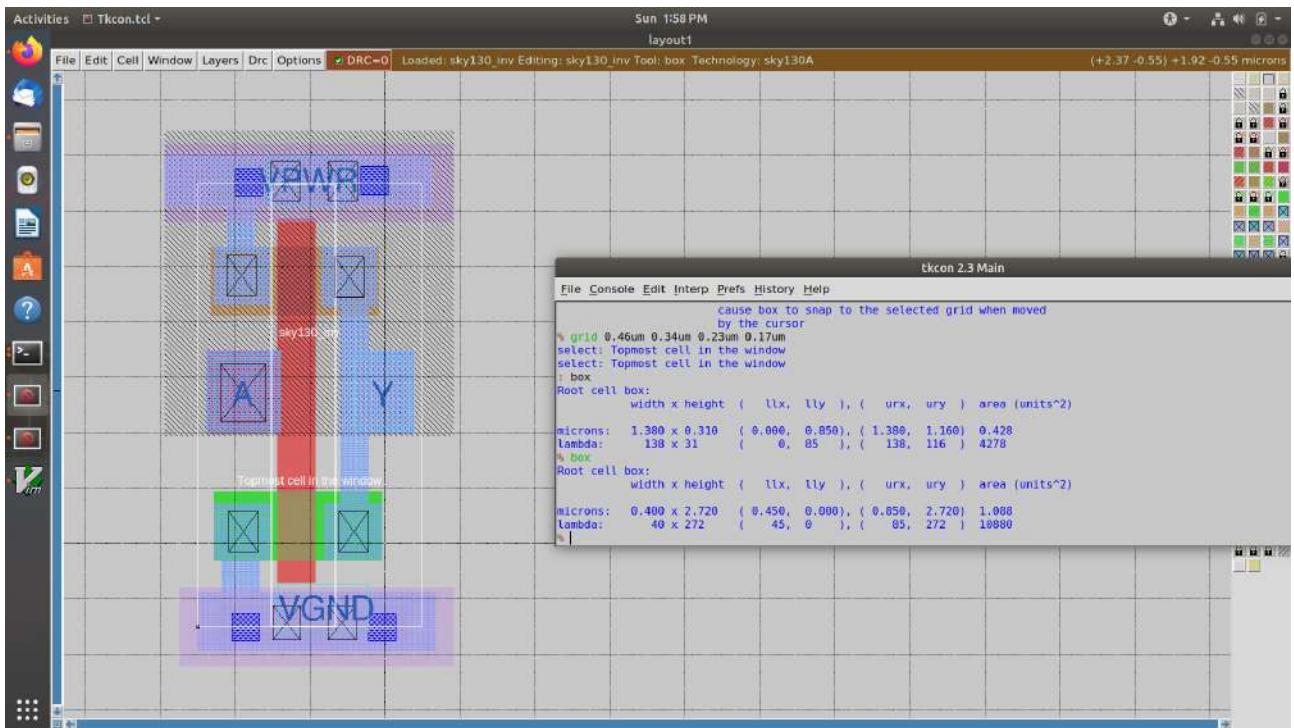
Condition 1 verified



Condition 2 verified



Condition 3 verified



2. Save the finalized layout with custom name and open it.

Command for tkcon window to save the layout with custom name

```
# Command to save as
```

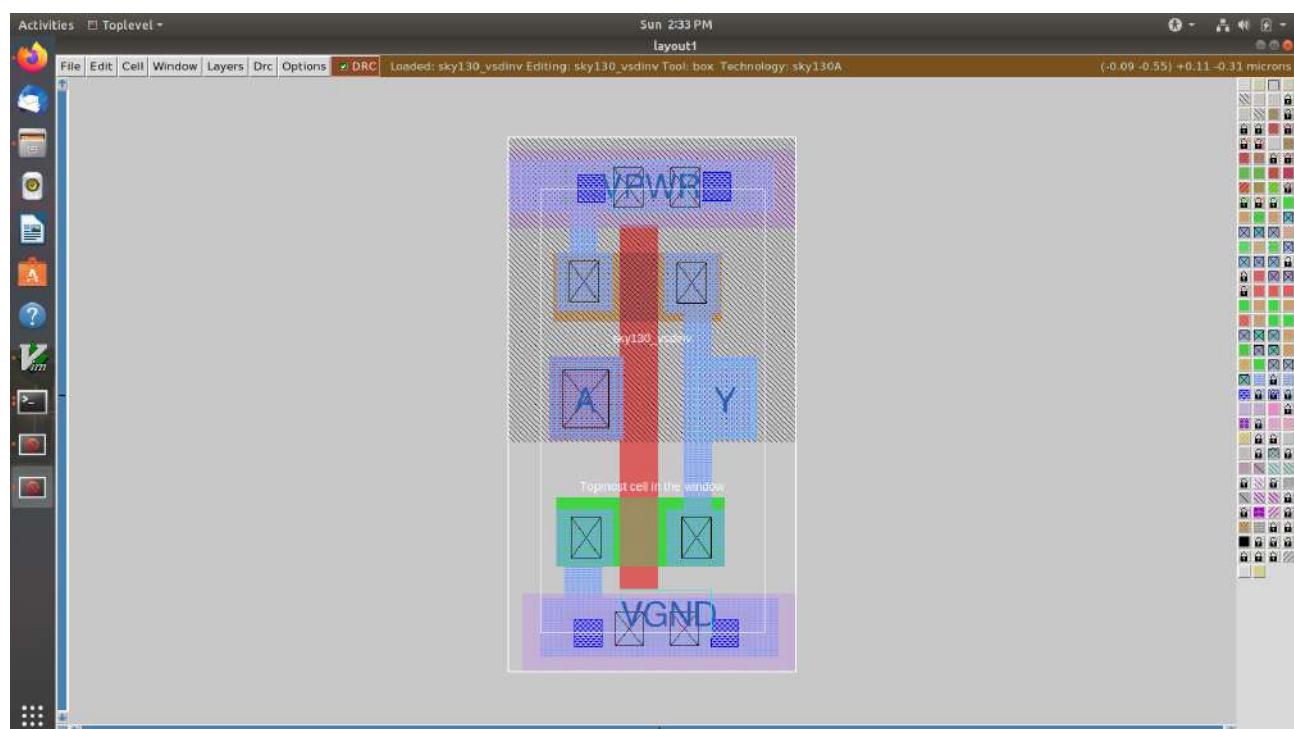
```
save sky130_vsdinv.mag
```

Command to open the newly saved layout

```
# Command to open custom inverter layout in magic
```

```
magic -T sky130A.tech sky130_vsdinv.mag &
```

Screenshot of newly saved layout



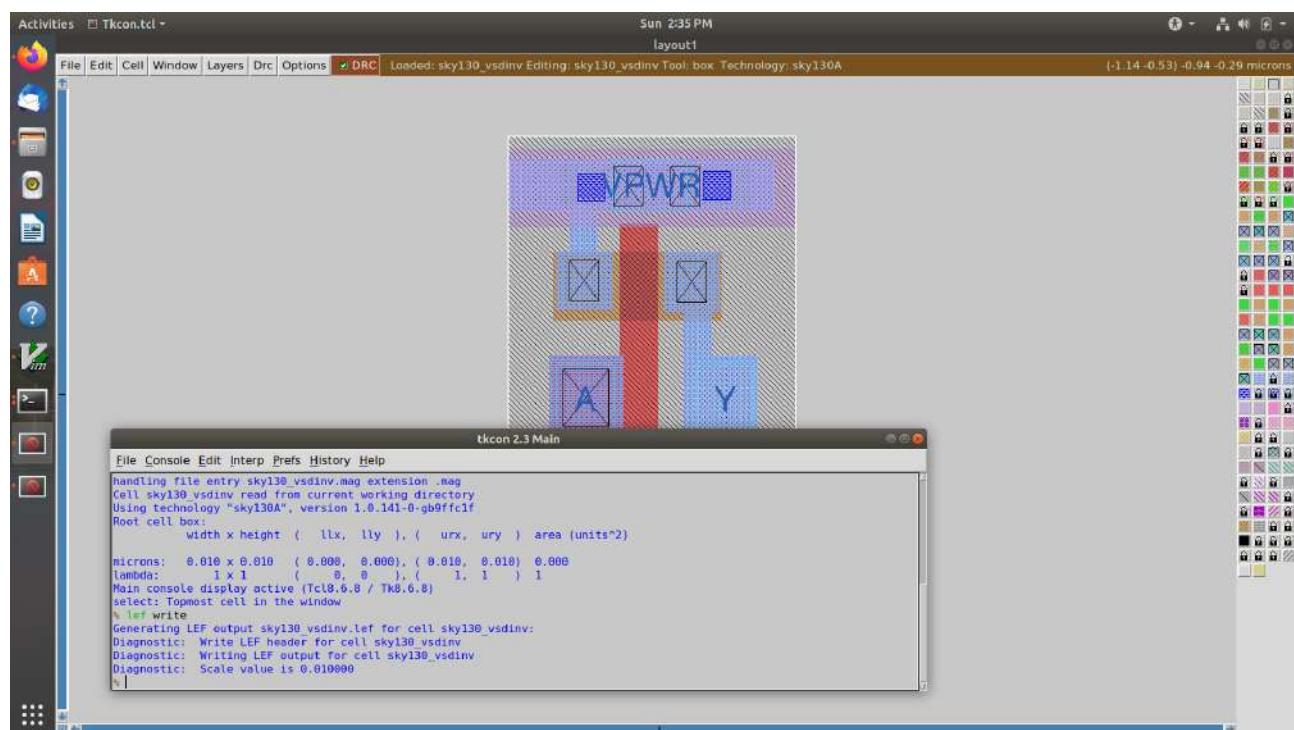
3. Generate lef from the layout.

Command for tkcon window to write lef

```
# lef command
```

```
lef write
```

Screenshot of command run



Screenshot of newly created lef file

The screenshot shows a GVIM window with the title 'sky130_vsdinv.lef (~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a) - GVIM'. The file contains a LEF (Liberty Cell Format) script with the following content:

```
1 VERSION 5.7 ;
2 NOWIREEXTENSIONATPIN ON ;
3 DIVIDERCHAR "/" ;
4 BUSBITCHARS "[]" ;
5 MACRO sky130_vsdinv
6 CLASS CORE ;
7 FOREIGN sky130_vsdinv ;
8 ORIGIN 0.000 0.000 ;
9 SIZE 1.380 BY 2.720 ;
10 SITE unithd ;
11 PIN A
12     DIRECTION INPUT ;
13     USE SIGNAL ;
14     ANTENNAGATEAREA 0.193200 ;
15     PORT
16         LAYER li1 ;
17         RECT 0.060 1.180 0.510 1.690 ;
18     END
19 END A
20 PIN Y
21     DIRECTION OUTPUT ;
22     USE SIGNAL ;
23     ANTENNADIFFAREA 0.336000 ;
24     PORT
25         LAYER li1 ;
```

4. Copy the newly generated lef and associated required lib files to 'picorv32a' design 'src' directory.

Commands to copy necessary files to 'picorv32a' design 'src' directory

```
# Copy lef file
```

```
cp sky130_vsdinv.lef ~/Desktop/work/tools/openlane_working_dir/openlane/designs/
picorv32a/src/
```

```
# List and check whether it's copied
```

```
ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
```

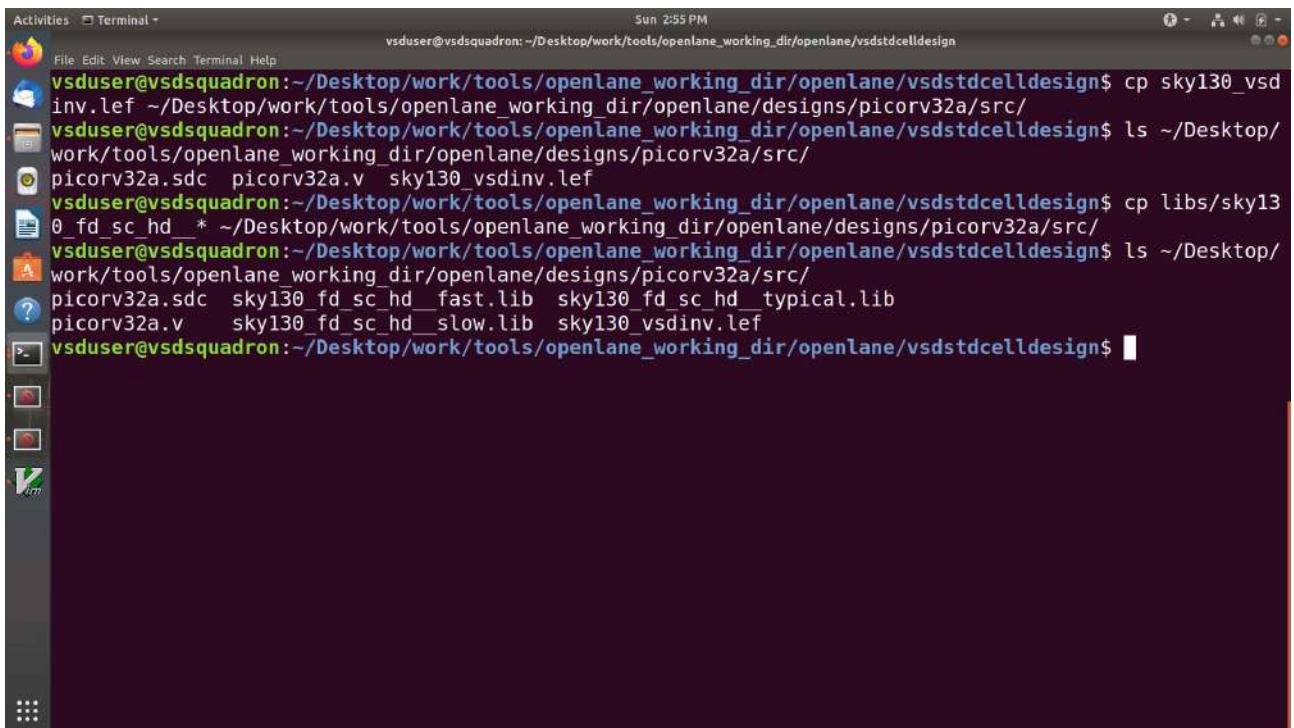
```
# Copy lib files
```

```
cp libs/sky130_fd_sc_hd_* ~/Desktop/work/tools/openlane_working_dir/openlane/designs/
picorv32a/src/
```

```
# List and check whether it's copied
```

```
ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
```

Screenshot of commands run



```
Activities Terminal Sun 2:55 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cp sky130_vsdinv.lef ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
picorv32a.sdc picorv32a.v sky130_vsdinv.lef
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cp libs/sky130_fd_sc_hd_* ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
picorv32a.sdc sky130_fd_sc_hd_fast.lib sky130_fd_sc_hd_typical.lib
picorv32a.v sky130_fd_sc_hd_slow.lib sky130_vsdinv.lef
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```

5. Edit 'config.tcl' to change lib file and add the new extra lef into the openlane flow.

Commands to be added to config.tcl to include our custom cell in the openlane flow

```
set ::env(LIB_SYNTH) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib"

set ::env(LIB_FASTEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib"

set ::env(LIB_SLOWEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib"
```

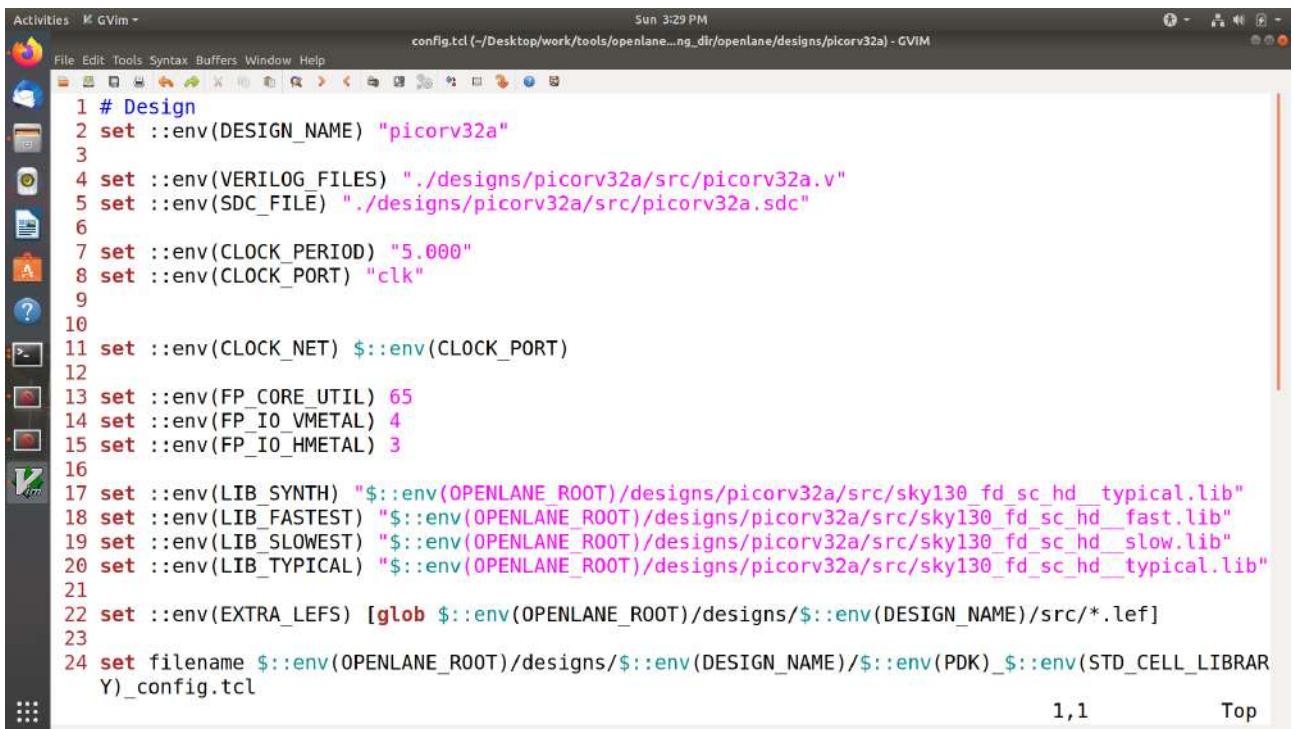
```

set ::env(LIB_TYPICAL) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/
sky130_fd_sc_hd_typical.lib"

set ::env(EXTRA_LEFS) [glob $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/
src/*.lef]

```

Edited config.tcl to include the added lef and change library to ones we added in src directory



```

Activities  M GVIM - Sun 3:29 PM config.tcl (-/Desktop/work/tools/openlane...ng_dir/openlane/designs/picorv32a) - GVIM
File Edit Tools Syntax Buffers Window Help
1 # Design
2 set ::env(DESIGN_NAME) "picorv32a"
3
4 set ::env(VERILOG_FILES) "./designs/picorv32a/src/picorv32a.v"
5 set ::env(SDC_FILE) "./designs/picorv32a/src/picorv32a.sdc"
6
7 set ::env(CLOCK_PERIOD) "5.000"
8 set ::env(CLOCK_PORT) "clk"
9
10
11 set ::env(CLOCK_NET) $::env(CLOCK_PORT)
12
13 set ::env(FP_CORE_UTIL) 65
14 set ::env(FP_IO_VMETAL) 4
15 set ::env(FP_IO_HMETAL) 3
16
17 set ::env(LIB_SYNTH) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib"
18 set ::env(LIB_FASTEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib"
19 set ::env(LIB_SLOWEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib"
20 set ::env(LIB_TYPICAL) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib"
21
22 set ::env(EXTRA_LEFS) [glob $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/src/*.lef]
23
24 set filename $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/$::env(PDK)_$::env(STD_CELL_LIBRARY)_config.tcl
1,1 Top

```

6. Run openlane flow synthesis with newly inserted custom inverter cell.

Commands to invoke the OpenLANE flow include new lef and perform synthesis

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:v0.21'
```

```
# Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command
```

```
docker
```

```
# Now that we have entered the OpenLANE flow contained docker sub-system we can invoke the OpenLANE flow in the Interactive mode using the following command
```

```
./flow.tcl -interactive
```

```
# Now that OpenLANE flow is open we have to input the required packages for proper functionality of the OpenLANE flow
```

```
package require openlane 0.9
```

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the design creating some necessary files and directories for running a specific design which in our case is 'picorv32a'
```

```
prep -design picorv32a
```

```
# Additional commands to include newly added lef to openlane flow
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

Now that the design is prepped and ready, we can run synthesis using following command

`run_synthesis`

Screenshots of commands run

Activities Terminal Sun 3:36 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
vsduser@vsdsquadron:~$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ docker
bash-4.2$ ./flow.tcl -interactive
[INFO]:

[INFO]: Version: v0.21
[INFO]: Running interactively
% package require openlane 0.9
% prep -design picorv32a
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
```

Activities Terminal Sun 3:37 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
? sky130_fd_sc_hd.lef: SITEs matched found: 0
? sky130_fd_sc_hd.lef: MACROs matched found: 437
? sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
? sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
? sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
? sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
? sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
? sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
```

```

Activities Terminal - Sun 3:37 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
::: % run_synthesis

```

```

Activities Terminal - Sun 3:45 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
::: %

```

7. Remove/reduce the newly introduced violations with the introduction of custom inverter cell by modifying design parameters.

Noting down current design values generated before modifying parameters to improve timing

```

Activities Terminal - Sun 4:00 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
sky130_fd_sc_hd_o31la_2 8
sky130_fd_sc_hd_o31a_2 19
sky130_fd_sc_hd_o31ai_2 1
sky130_fd_sc_hd_o32a_2 109
sky130_fd_sc_hd_o41a_2 2
sky130_fd_sc_hd_or2_2 1088
sky130_fd_sc_hd_or2b_2 25
sky130_fd_sc_hd_or3_2 68
sky130_fd_sc_hd_or3b_2 5
sky130_fd_sc_hd_or4_2 93
sky130_fd_sc_hd_or4b_2 6
sky130_fd_sc_hd_or4bb_2 2
sky130_vsdinv 1554

Chip area for module '\picorv32a': 147712.918400

29. Executing Verilog backend.
Dumping module '\picorv32a'.

Warnings: 307 unique messages, 307 total
End of script. Logfile hash: ea6f91c309, CPU: user 11.69s system 3.17s, MEM: 95.95 MB peak
Yosys 0.9+3621 (git sha1 84e9fa7, gcc 8.3.1 -fPIC -Os)
Time spent: 57% 2x abc (18 sec), 12% 33x opt_expr (4 sec), ...
[INFO]: Changing netlist from 0 to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis
/picorv32a.synthesis.v
[INFO]: Running Static Timing Analysis...
[INFO]: current step index: 2
OpenSTA 2.2.0-28b40207a8 Copyright (c) 2019, Parallever Software, Inc.

```

```

Activities Terminal - Sun 4:13 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.9460000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.9460000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
[INFO]: % 

```

Commands to view and change parameters to improve timing and run synthesis

Now once again we have to prep design so as to update variables

prep -design picorv32a -tag 24-03_10-03 -overwrite

```
# Addiitional commands to include newly added lef to openlane flow merged.lef
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to display current value of variable SYNTH_STRATEGY
```

```
echo $::env(SYNTH_STRATEGY)
```

```
# Command to set new value for SYNTH_STRATEGY
```

```
set ::env(SYNTH_STRATEGY) "DELAY 3"
```

```
# Command to display current value of variable SYNTH_BUFFERING to check whether it's  
enabled
```

```
echo $::env(SYNTH_BUFFERING)
```

```
# Command to display current value of variable SYNTH_SIZING
```

```
echo $::env(SYNTH_SIZING)
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

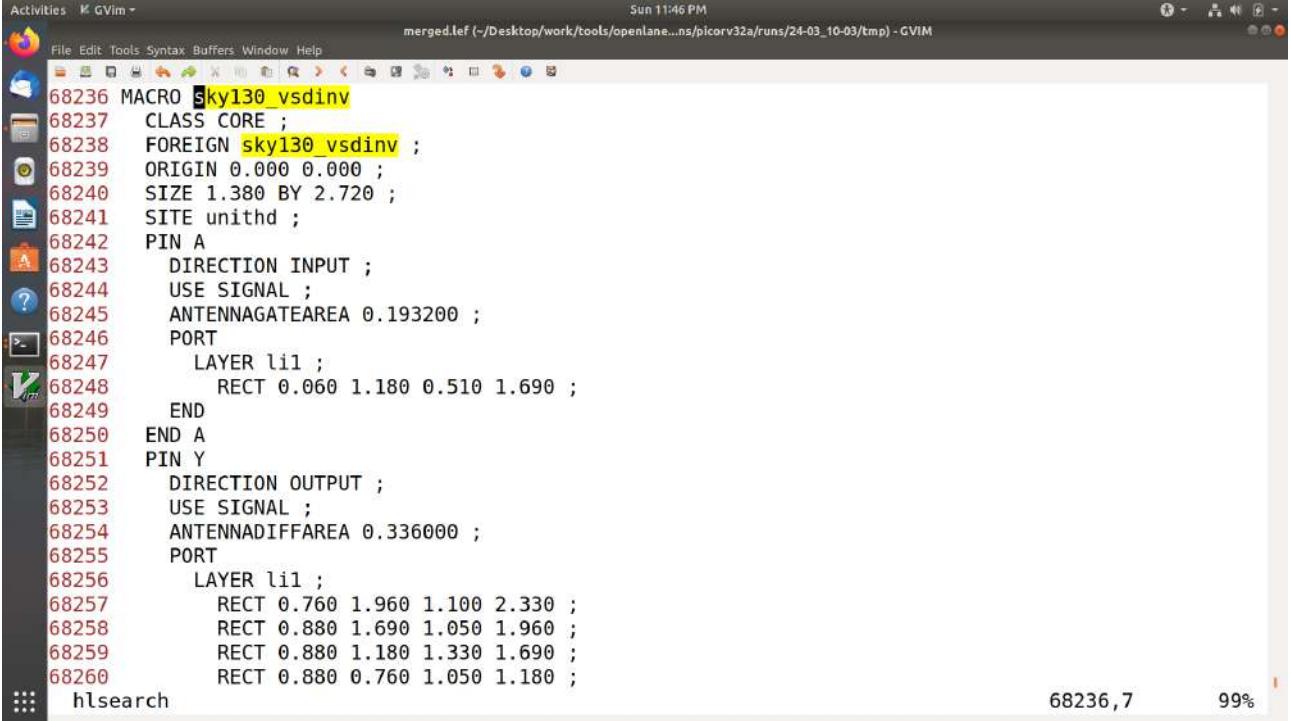
```
# Command to display current value of variable SYNTH_DRIVING_CELL to check whether it's the proper cell or not
```

```
echo $::env(SYNTH_DRIVING_CELL)
```

```
# Now that the design is prepped and ready, we can run synthesis using following command
```

```
run_synthesis
```

Screenshot of merged.lef in tmp directory with our custom inverter as macro



The screenshot shows a GVim window displaying the contents of a LEF (Library Exchange Format) file named "merged.lef". The file is located at `~/Desktop/work/tools/openlane...ns/picorv32a/runs/24-03_10-03/tmp`. The code in the file defines a macro for a custom inverter cell, "sky130_vsdinv". The macro includes details such as class, origin, size, site, and two pins (A and Y) with their respective directions, signals, and bounding boxes. The GVim interface shows standard menu bars (File, Edit, Tools, Syntax, Buffers, Window, Help), toolbars, and status bars indicating the file name, line number (68236,7), and character percentage (99%).

```
68236 MACRO Sky130_vsdinv
68237   CLASS CORE ;
68238   FOREIGN sky130_vsdinv ;
68239   ORIGIN 0.000 0.000 ;
68240   SIZE 1.380 BY 2.720 ;
68241   SITE unithd ;
68242   PIN A
68243     DIRECTION INPUT ;
68244     USE SIGNAL ;
68245     ANTENNAGATEAREA 0.193200 ;
68246     PORT
68247       LAYER l1l ;
68248       RECT 0.060 1.180 0.510 1.690 ;
68249     END
68250   END A
68251   PIN Y
68252     DIRECTION OUTPUT ;
68253     USE SIGNAL ;
68254     ANTENNADIFFAREA 0.336000 ;
68255     PORT
68256       LAYER l1l ;
68257       RECT 0.760 1.960 1.100 2.330 ;
68258       RECT 0.880 1.690 1.050 1.960 ;
68259       RECT 0.880 1.180 1.330 1.690 ;
68260       RECT 0.880 0.760 1.050 1.180 ;
```

Screenshots of commands run

```
Activities Terminal Sun 5:09 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% prep -design picorv32a -tag 24-03_10-03 -overwrite
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[WARNING]: Removing existing run /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
::: mergeLef.py : Merging LEFs
::: mergeLef.py : Merging LEFs
```

```
Activities Terminal Sun 5:09 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add lefs -src $lefs
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% echo $::env(SYNTH_STRATEGY)
AREA 0
% set ::env(SYNTH_STRATEGY) "DELAY 3"
DELAY 3
% echo $::env(SYNTH_BUFFERING)
1
% echo $::env(SYNTH_SIZING)
0
% set ::env(SYNTH_SIZING) 1
1
% echo $::env(SYNTH_DRIVING_CELL)
sky130_fd_sc_hd_inv_8
::: % run_synthesis
```

```
Activities Terminal - Sun 5:10 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
::: %
```

Comparing to previously noted run values area has increased and worst negative slack has become 0

```

Activities Terminal - Sun 5:11 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
sky130_fd_sc_hd_o32a_2 9
sky130_fd_sc_hd_o32ai_2 3
sky130_fd_sc_hd_o41ai_2 18
sky130_fd_sc_hd_or2_2 80
sky130_fd_sc_hd_or2b_2 264
sky130_fd_sc_hd_or3_2 6
sky130_fd_sc_hd_or3b_2 5
sky130_fd_sc_hd_or4_2 68
sky130_fd_sc_hd_or4b_2 4
sky130_fd_sc_hd_xnor2_2 700
sky130_fd_sc_hd_xor2_2 1164
sky130_vsdinv 1434

Chip area for module '\picorv32a': 181730.544000

29. Executing Verilog backend.
Dumping module '\picorv32a'.

Warnings: 307 unique messages, 307 total
End of script. Logfile hash: befd735e75, CPU: user 12.56s system 2.87s, MEM: 97.45 MB peak
Yosys 0.9+3621 (git sha1 84e9fa7, gcc 8.3.1 -fPIC -Os)
Time spent: 64% 2x abc (26 sec), 10% 33x opt_expr (4 sec), ...
[INFO]: Changing netlist from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis.v to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis.v
[INFO]: Running Static Timing Analysis...
[INFO]: current step index: 11
OpenSTA 2.2.0-28b10207a8 Copyright (c) 2019, Parallever Software, Inc.

```

```

Activities Terminal - Sun 5:11 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk $all_inputs_wo_clk

# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
[INFO]: % 

```

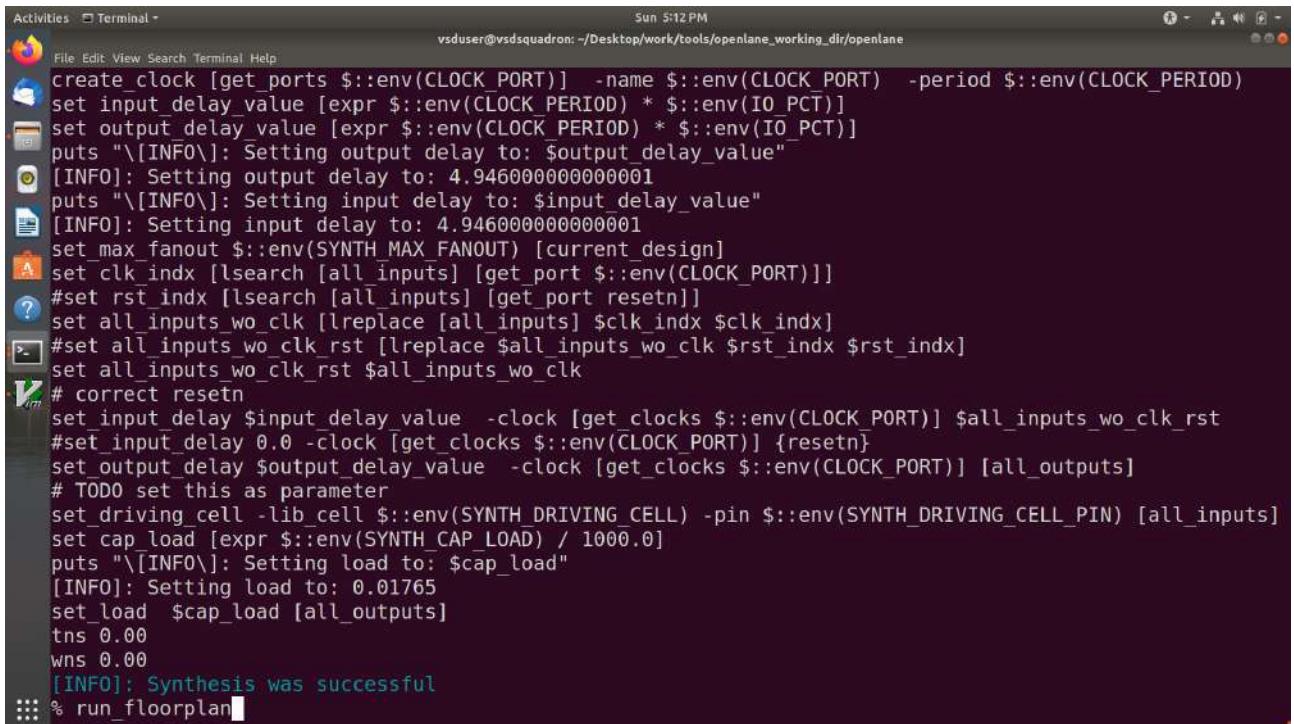
8. Once synthesis has accepted our custom inverter we can now run floorplan and placement and verify the cell is accepted in PnR flow.

Now that our custom inverter is properly accepted in synthesis we can now run floorplan using following command

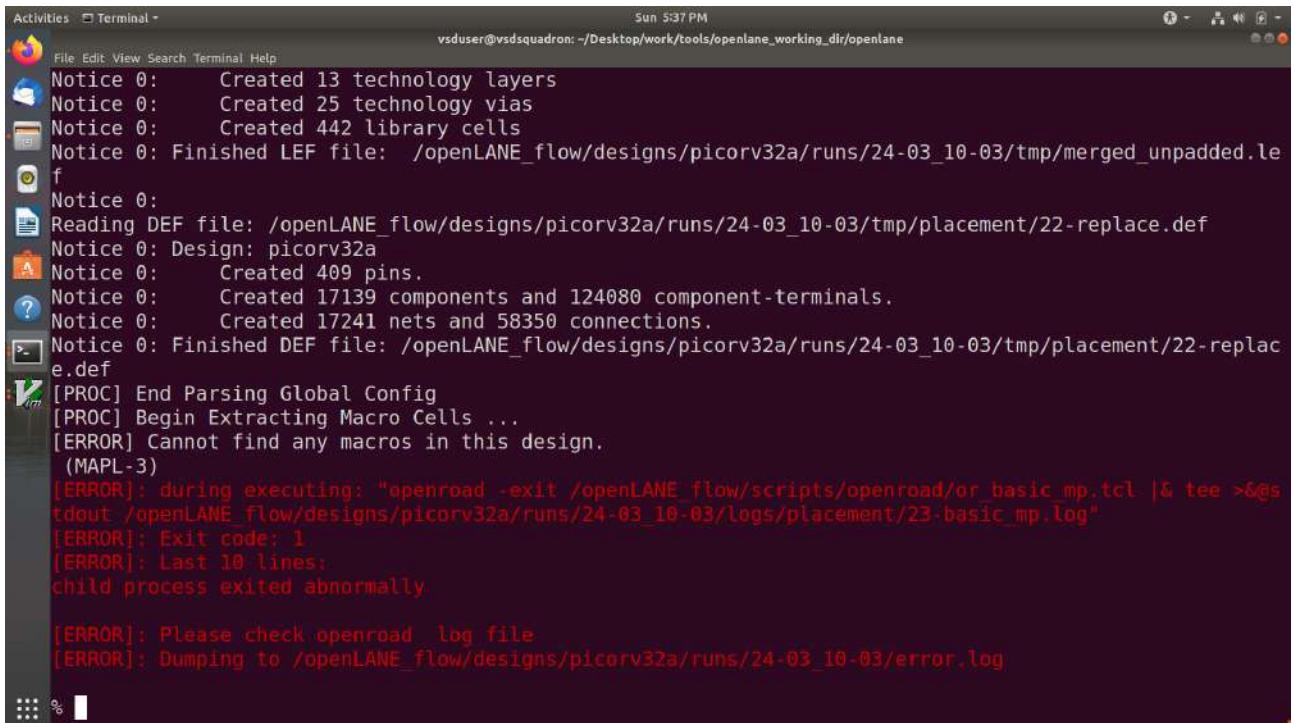
Now we can run floorplan

run_floorplan

Screenshots of command run



```
Activities Terminal Sun 5:12 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
:: % run_floorplan
```



```
Activities Terminal Sun 5:37 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/22-replace.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/22-replace.def
[PROC] End Parsing Global Config
[PROC] Begin Extracting Macro Cells ...
[ERROR] Cannot find any macros in this design.
(MAPL-3)
[ERROR]: during executing: "openroad -exit /openLANE_flow/scripts/openroad/or_basic_mp.tcl |& tee >& stdout /openLANE_flow/designs/picorv32a/runs/24-03_10-03/logs/placement/23-basic_mp.log"
[ERROR]: Exit code: 1
[ERROR]: Last 10 lines:
child process exited abnormally

[ERROR]: Please check openroad log file
[ERROR]: Dumping to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/error.log
:: %
```

Since we are facing unexpected un-explainable error while using run_floorplan command, we can instead use the following set of commands available based on information from Desktop/work/tools/openlane_working_dir/openlane/scripts/tcl_commands/floorplan.tcl and also based on Floorplan Commands section in Desktop/work/tools/openlane_working_dir/openlane/docs/source/OpenLANE_commands.md

Following commands are altogether sourced in "run_floorplan" command

init_floorplan

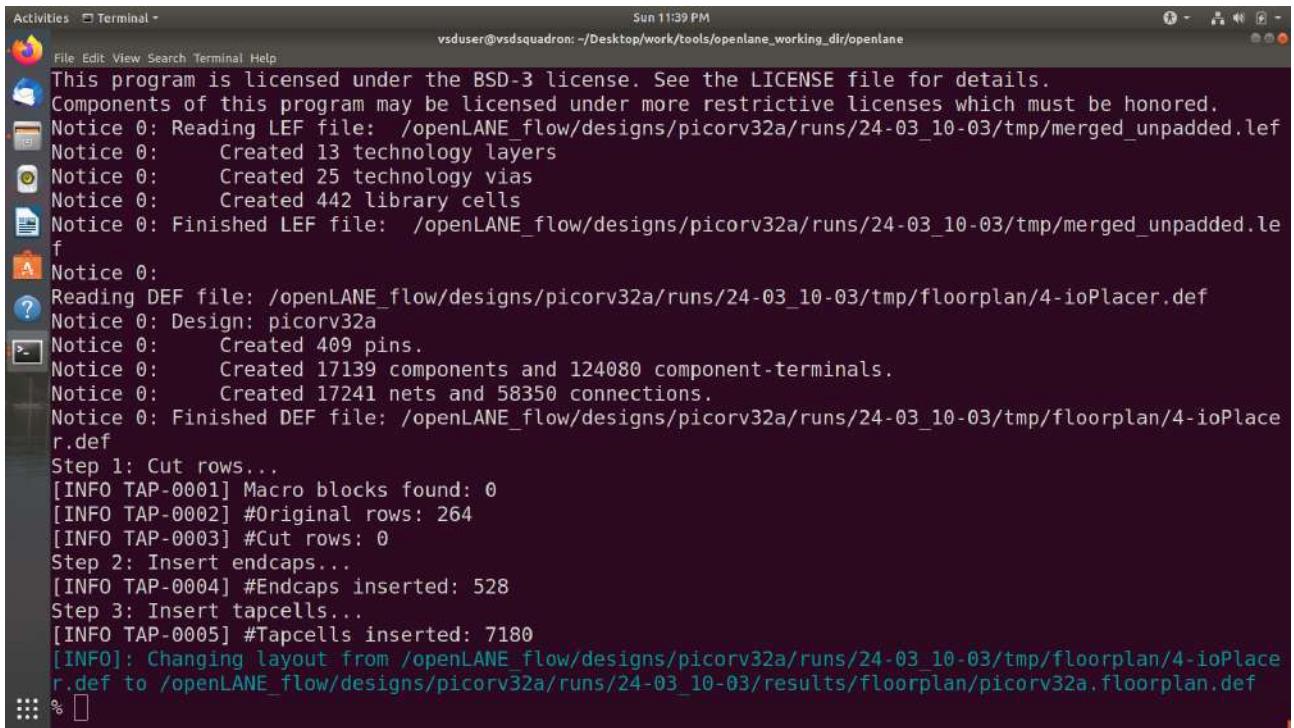
place_io

tap_decap_or

Screenshots of commands run

```
Activities Terminal Sun 11:38 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
% init_floorplan
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 3
OpenROAD 0.9.0 1415572a73
A This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
[INFO IFP-0001] Added 264 rows of 1566 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 731.615 742.335 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/3-verilog2def.die_area.rpt.
[INFO] Floorplanned on a core area of 5.52 10.88 725.88 728.96 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/3-verilog2def.core_area.rpt.
[INFO]: Core area width: 720.36
[INFO]: Core area height: 718.08
[INFO]: Changing layout from 0 to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def
::: % place_io
```

```
Activities Terminal Sun 11:38 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% place_io
[INFO]: Running IO Placement...
[INFO]: current step index: 4
OpenROAD 0.9.0 1415572a73
A This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def
#Macro blocks found: 0
Using 5u default boundaries offset
Random pin placement
RandomMode Even
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
::: % tap_decap_or
```



```
Sun 11:39 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 17139 components and 124080 component-terminals.
Notice 0:     Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Step 1: Cut rows...
[INFO TAP-0001] Macro blocks found: 0
[INFO TAP-0002] #Original rows: 264
[INFO TAP-0003] #Cut rows: 0
Step 2: Insert endcaps...
[INFO TAP-0004] #Endcaps inserted: 528
Step 3: Insert tapcells...
[INFO TAP-0005] #Tapcells inserted: 7180
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/floorplan/picorv32a.floorplan.def
```

Now that floorplan is done we can do placement using following command

Now we are ready to run placement

run_placement

Screenshots of command run

```
Activities Terminal Sun 11:49 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 17139 components and 124080 component-terminals.
Notice 0:     Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Step 1: Cut rows...
[INFO TAP-0001] Macro blocks found: 0
[INFO TAP-0002] #Original rows: 264
[INFO TAP-0003] #Cut rows: 0
Step 2: Insert endcaps...
[INFO TAP-0004] #Endcaps inserted: 528
Step 3: Insert tapcells...
[INFO TAP-0005] #Tapcells inserted: 7180
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/floorplan/picorv32a.floorplan.def
::: % run_placement
```

```
Activities Terminal Sun 11:51 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
legalized HPWL      910806.5 u
delta HPWL          2 %

[INFO DPL-0020] Mirrored 6650 instances
[INFO DPL-0021] HPWL before      910806.5 u
[INFO DPL-0022] HPWL after       895297.0 u
[INFO DPL-0023] HPWL delta       -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/6-resizer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 10
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
::: %
```

Commands to load placement def in magic in another terminal

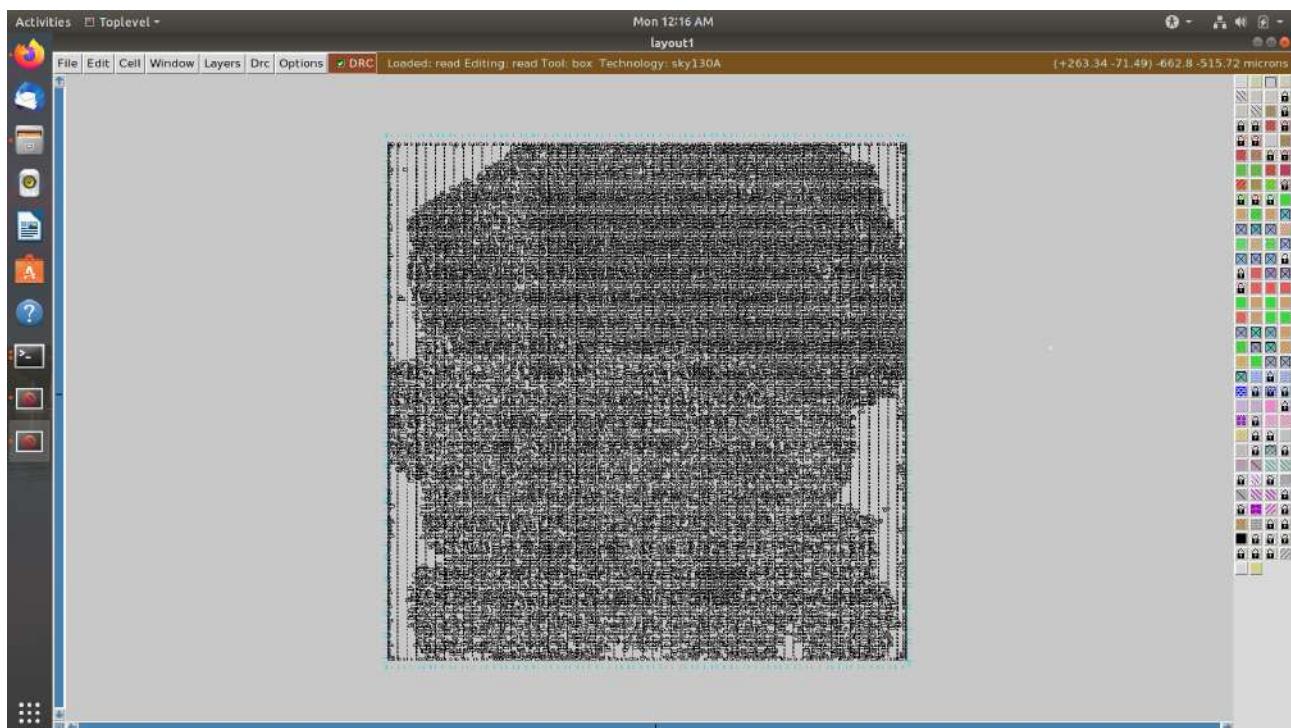
```
# Change directory to path containing generated placement def
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
24-03_10-03/results/placement/
```

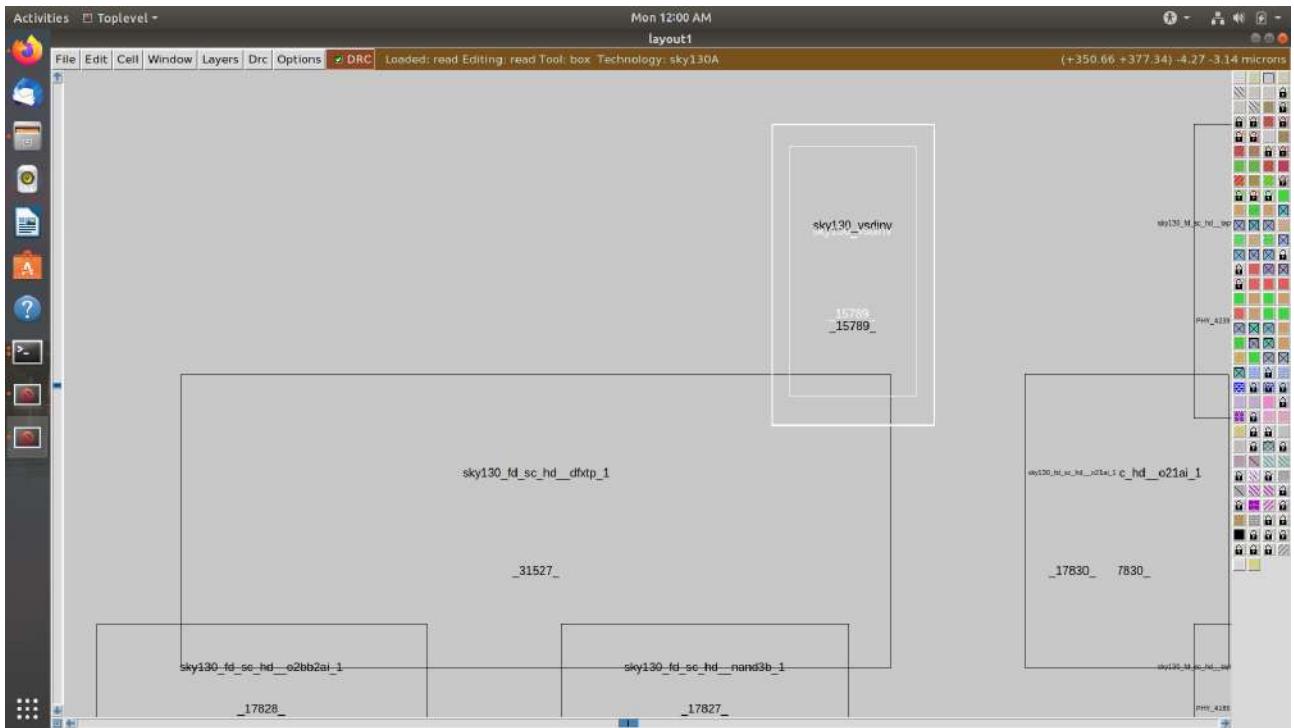
```
# Command to load the placement def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def  
&
```

Screenshot of placement def in magic



Screenshot of custom inverter inserted in placement def with proper abutment

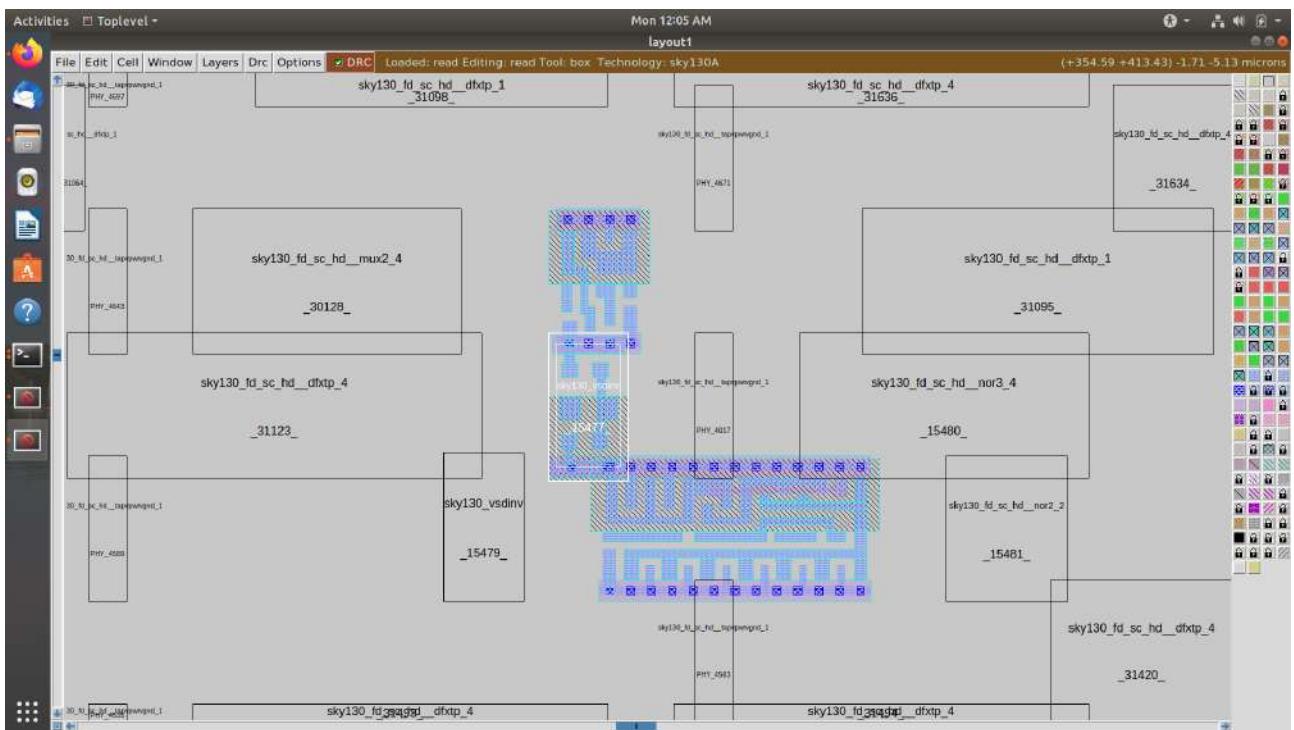
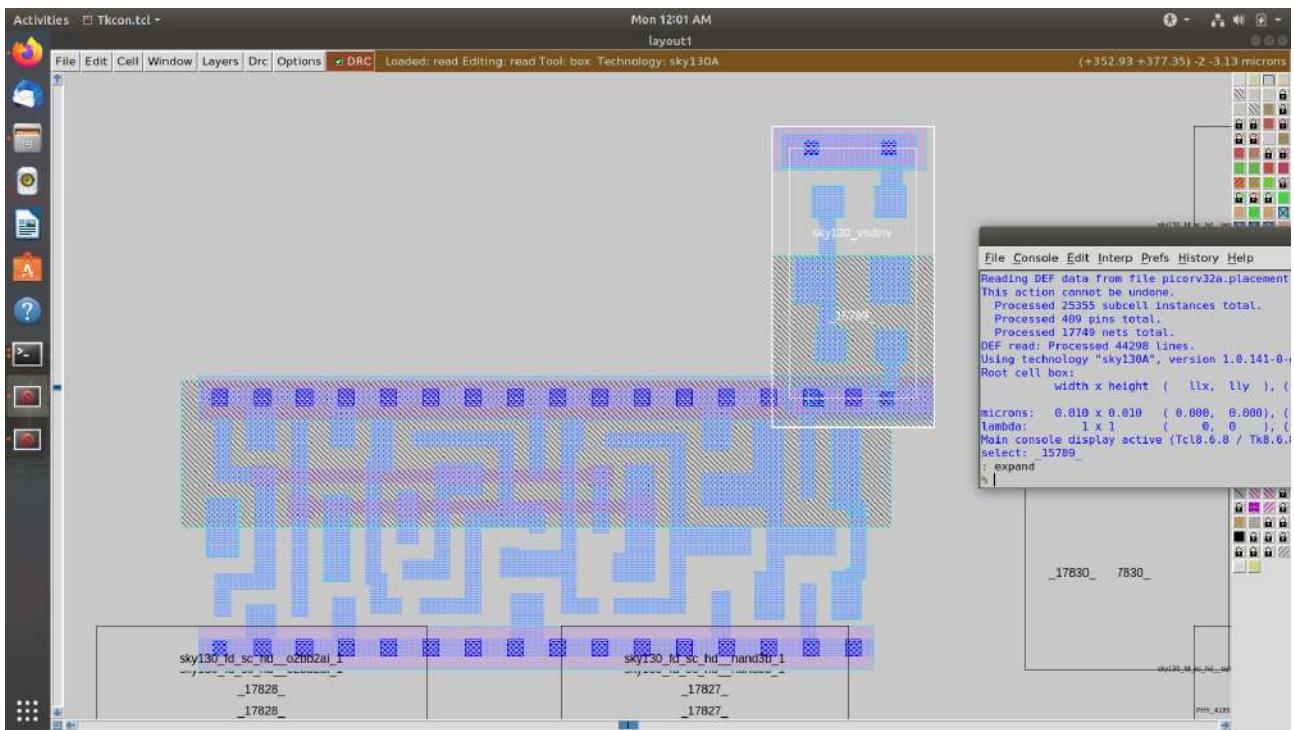


Command for tkcon window to view internal layers of cells

```
# Command to view internal connectivity layers
```

```
expand
```

Abutment of power pins with other cell from library clearly visible



9. Do Post-Synthesis timing analysis with OpenSTA tool.

Since we are having own after improved timing run we are going to do timing analysis on initial run of synthesis which has lots of violations and no parameters were added to improve timing

Commands to invoke the OpenLANE flow include new lef and perform synthesis

Change directory to openlane flow directory

cd Desktop/work/tools/openlane_working_dir/openlane

alias docker='docker run -it -v \$(pwd):/openLANE_flow -v \$PDK_ROOT:\$PDK_ROOT -e PDK_ROOT=\$PDK_ROOT -u \$(id -u \$USER):\$(id -g \$USER) efabless/openlane:vo.21'

Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command

docker

Now that we have entered the OpenLANE flow contained docker sub-system we can invoke the OpenLANE flow in the Interactive mode using the following command

./flow.tcl -interactive

Now that OpenLANE flow is open we have to input the required packages for proper functionality of the OpenLANE flow

package require openlane 0.9

Now the OpenLANE flow is ready to run any design and initially we have to prep the design creating some necessary files and directories for running a specific design which in our case is 'picorv32a'

prep -design picorv32a

```
# Additional commands to include newly added lef to openlane flow
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Now that the design is prepped and ready, we can run synthesis using following command
```

```
run_synthesis
```

Commands run final screenshot

Activities Terminal Tue 5:52 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
```

Newly created pre_sta.conf for STA analysis in openlane directory

Newly created `my_base.sdc` for STA analysis in `openlane/designs/picorv32a/src` directory based on the file `openlane/scripts/base.sdc`

```
Activities  M GVim - Tue 5:55 AM my_base.sdc (~Desktop/work/tools/openlane/r/openlane/designs/picorv32a/src) - GVIM1
File Edit Tools Syntax Buffers Window Help
1 set ::env(CLOCK_PORT) cLK
2 set ::env(CLOCK_PERIOD) 24.73
3 #set ::env(SYNTH_DRIVING_CELL) sky130_vsdinv
4 set ::env(SYNTH_DRIVING_CELL) sky130_fd_sc_hd_inv_8
5 set ::env(SYNTH_DRIVING_CELL_PIN) Y
6 set ::env(SYNTH_CAP_LOAD) 17.653
7 set ::env(IO_PCT) 0.2
8 set ::env(SYNTH_MAX_FANOUT) 6
9
10 create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
11 set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
12 set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
13 puts "\[INFO\]: Setting output delay to: $output_delay_value"
14 puts "\[INFO\]: Setting input delay to: $input_delay_value"
15
16 set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
17
18 set clk_idx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
19 #set rst_idx [lsearch [all_inputs] [get_port resetn]]
20 set all_inputs_wo_clk [lreplace [all_inputs] $clk_idx $clk_idx]
21 #set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_idx $rst_idx]
22 set all_inputs_wo_clk_rst $all_inputs_wo_clk
23
24 # correct resetn
```

24,16

Top

```
Activities  M GVim - Tue 5:55 AM my_base.sdc (~Desktop/work/tools/openlane/r/openlane/designs/picorv32a/src) - GVIM1
File Edit Tools Syntax Buffers Window Help
24 # correct resetn
25 set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
26 #set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
27 set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
28
29 # TODO set this as parameter
30 set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
31 set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
32 puts "\[INFO\]: Setting load to: $cap_load"
33 set_load $cap_load [all_outputs]
```

25,16

Bot

Commands to run STA in another terminal

```
# Change directory to openlane
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# Command to invoke OpenSTA tool with script
```

```
sta pre_sta.conf
```

Screenshots of commands run

```
Activities Terminal Tue 6:04 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
vsduser@vsdsquadron:~$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ sta pre_sta.conf
OpenSTA 2.4.0 ac3479bc24 Copyright (c) 2021, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type `show copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type `show warranty'.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib line 24, default_fanout_load is 0.0.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib line 23, default_fanout_load is 0.0.
[INFO]: Setting output delay to: 4.946000000000001
[INFO]: Setting input delay to: 4.946000000000001
[INFO]: Setting load to: 0.017653
Startpoint: _26669_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _26669_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _26669/_0 (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.00  0.00  cpuregs[0][0] (net)
          0.03  0.00  0.00 ^ _15938/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _15938/_X (sky130_fd_sc_hd_buf_1)
          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _26669/_D (sky130_fd_sc_hd_dfxtp_2)
          0.02  0.00  0.23  data arrival time
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data arrival time
          -0.02 -0.02  0.00  slack (MET)
```

```
Activities Terminal Tue 6:05 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _26669/_0 (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.00  0.00  cpuregs[0][0] (net)
          0.03  0.00  0.00 ^ _15938/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _15938/_X (sky130_fd_sc_hd_buf_1)
          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _26669/_D (sky130_fd_sc_hd_dfxtp_2)
          0.02  0.00  0.23  data arrival time
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data arrival time
          -0.02 -0.02  0.00  slack (MET)
```

```

Activities Terminal - Tue 6:05 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
Startpoint: _27860_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _27762_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
-----
          0.00 0.00 0.00 clock clk (rise edge)
          0.00 0.00 0.00 clock network delay (ideal)
          0.00 0.00 0.00 ^ _27860/_CLK (sky130_fd_sc_hd_dfxtp_2)
          0.10 0.64 0.64 ^ _27860/_Q (sky130_fd_sc_hd_dfxtp_2)
          4   0.01      irq_mask[1] (net)
          0.10 0.00 0.64 ^ _13108/_A (sky130_vsdinv)
          0.13 0.15 0.79 v _13108/_Y (sky130_vsdinv)
          6   0.01      _10510_ (net)
          0.13 0.00 0.79 v _13113/_A1 (sky130_fd_sc_hd_a221o_2)
          0.08 0.65 1.44 v _13113/_X (sky130_fd_sc_hd_a221o_2)
          1   0.00      _10515_ (net)
          0.08 0.00 1.44 v _13132/_A (sky130_fd_sc_hd_or4_2)
          0.21 1.53 2.98 v _13132/_X (sky130_fd_sc_hd_or4_2)
          1   0.00      _10534_ (net)
          0.21 0.00 2.98 v _13160/_A1 (sky130_fd_sc_hd_o2111a_2)
          0.07 0.54 3.52 v _13160/_X (sky130_fd_sc_hd_o2111a_2)
          2   0.00      _10562_ (net)
          0.07 0.00 3.52 v _13161/_C (sky130_fd_sc_hd_or3_2)
          0.17 0.97 4.48 v _13161/_X (sky130_fd_sc_hd_or3_2)
          2   0.00      _10563_ (net)
          0.17 0.00 4.48 v _13164/_A (sky130_fd_sc_hd_or2_2)

```

```

Activities Terminal - Tue 6:08 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
          0.14 0.68 47.22 v _13750/_X (sky130_fd_sc_hd_or2_2)
          3   0.01      10970_ (net)
          0.14 0.00 47.22 v _13751/_B (sky130_fd_sc_hd_or2_2)
          0.12 0.66 47.88 v _13751/_X (sky130_fd_sc_hd_or2_2)
          2   0.00      10971_ (net)
          0.12 0.00 47.88 v _13754/_B2 (sky130_fd_sc_hd_o221a_2)
          0.07 0.44 48.32 v _13754/_X (sky130_fd_sc_hd_o221a_2)
          1   0.00      03928_ (net)
          0.07 0.00 48.32 v _27762/_D (sky130_fd_sc_hd_dfxtp_2)
          48.32 data arrival time
          0.00 24.73 24.73 clock clk (rise edge)
          0.00 24.73 24.73 clock network delay (ideal)
          0.00 24.73 24.73 clock reconvergence pessimism
          24.73 ^ _27762/_CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.29 24.44 library setup time
          24.44 data required time
          24.44 data required time
          -48.32 data arrival time
          -23.89 slack (VIOLATED)

tns -711.59
wns -23.89
%
```

Since more fanout is causing more delay we can add parameter to reduce fanout and do synthesis again

Commands to include new lef and perform synthesis

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the  
design creating some necessary files and directories for running a specific design which in  
our case is 'picorv32a'
```

```
prep -design picorv32a -tag 25-03_18-52 -overwrite
```

```
# Additional commands to include newly added lef to openlane flow
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Command to set new value for SYNTH_MAX_FANOUT
```

```
set ::env(SYNTH_MAX_FANOUT) 4
```

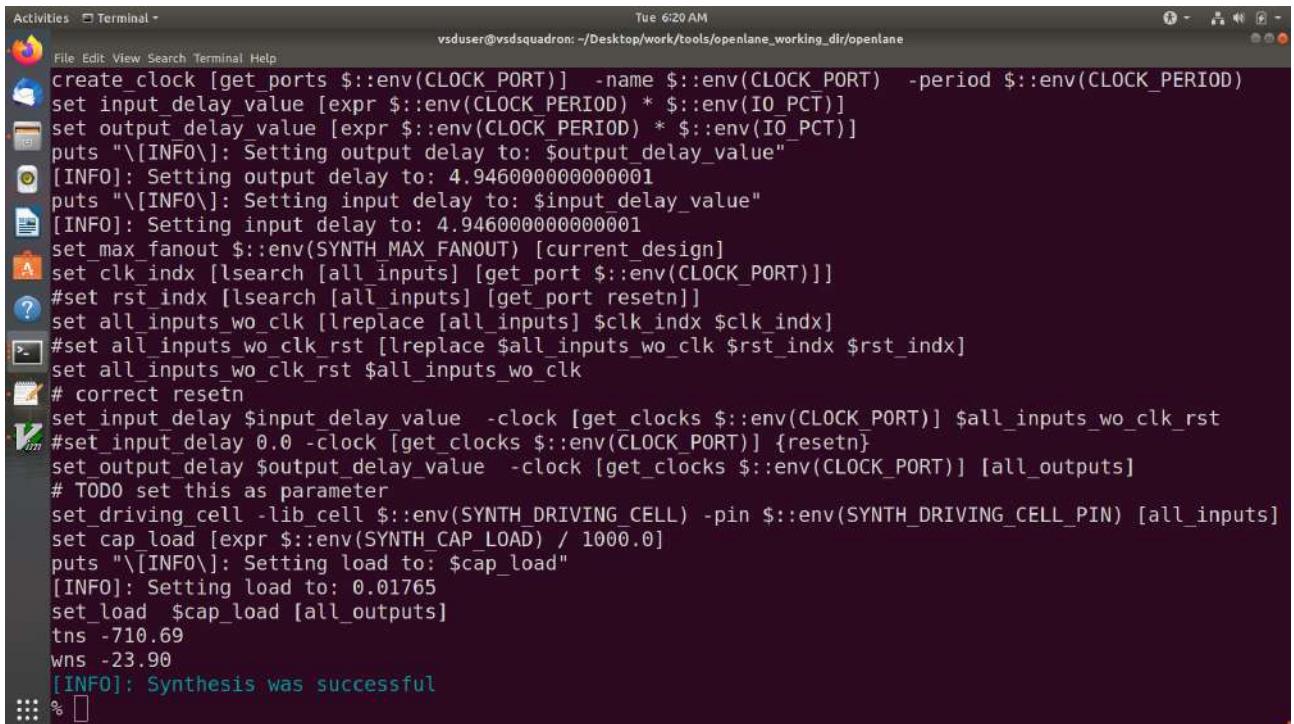
```
# Command to display current value of variable SYNTH_DRIVING_CELL to check whether  
it's the proper cell or not
```

```
echo $::env(SYNTH_DRIVING_CELL)
```

```
# Now that the design is prepped and ready, we can run synthesis using following  
command
```

run_synthesis

Commands run final screenshot



A screenshot of a terminal window titled "Terminal". The window shows a series of commands being run and their corresponding output. The commands relate to setting clock ports, input and output delays, and driving cell parameters. The output includes several "[INFO]" messages indicating the progress of the synthesis process. The terminal window has a dark background with light-colored text.

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -710.69
wns -23.90
[INFO]: Synthesis was successful
```

Commands to run STA in another terminal

```
# Change directory to openlane
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# Command to invoke OpenSTA tool with script
```

```
sta pre_sta.conf
```

Screenshots of commands run

```

Activities Terminal - Tue 6:22 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ sta pre_sta.conf
OpenSTA 2.4.0 ac3479bc24 Copyright (c) 2021, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type `show copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type `show warranty'.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib line 24, default_fanout_load is 0.0.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib line 23, default_fanout_load is 0.0.
[INFO]: Setting output delay to: 4.9460000000000001
[INFO]: Setting input delay to: 4.9460000000000001
[INFO]: Setting load to: 0.017653
Startpoint: _29347_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _29347_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _29347_/Q (sky130_fd_sc_hd_dfxtp_2)
          2   0.00          cpuregs[0][0] (net)
          0.02  0.00  0.10 ^ _17885/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _17885/_X (sky130_fd_sc_hd_buf_1)
          1   0.00          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _29347/_D (sky130_fd_sc_hd_dfxtp_2)
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data required time
          -0.23 -0.23  0.00  data arrival time
          0.24  slack (MET)

```

```

Activities Terminal - Tue 6:22 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _29347_/Q (sky130_fd_sc_hd_dfxtp_2)
          2   0.00          cpuregs[0][0] (net)
          0.03  0.00  0.18 ^ _17885/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _17885/_X (sky130_fd_sc_hd_buf_1)
          1   0.00          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _29347/_D (sky130_fd_sc_hd_dfxtp_2)
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data required time
          -0.23 -0.23  0.00  data arrival time
          0.24  slack (MET)

```

Activities Terminal - Tue 6:22 AM
 vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```

Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00 ^ _29052_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.06  0.58  0.58 v _29052/_Q (sky130_fd_sc_hd_dfxtp_2)
          4   0.01           irq_pending[3] (net)
          0.06  0.00  0.58 v _14460/_A (sky130_vsdinv)
          0.19  0.17  0.75 ^ _14460/_Y (sky130_vsdinv)
          3   0.01           _11622_ (net)
          0.19  0.00  0.75 ^ _14461/_B2 (sky130_fd_sc_hd_o22ai_2)
          0.09  0.14  0.89 v _14461/_Y (sky130_fd_sc_hd_o22ai_2)
          1   0.00           _11623_ (net)
          0.09  0.00  0.89 v _14462/_C1 (sky130_fd_sc_hd_a221o_2)
          0.08  0.55  1.44 v _14462/_X (sky130_fd_sc_hd_a221o_2)
          1   0.00           _11624_ (net)
          0.08  0.00  1.44 v _14481/_A (sky130_fd_sc_hd_or4_2)
          0.21  1.53  2.97 v _14481/_X (sky130_fd_sc_hd_or4_2)
          1   0.00           _11643_ (net)
          0.21  0.00  2.97 v _14509/_A1 (sky130_fd_sc_hd_o2111a_2)
          0.07  0.54  3.51 v _14509/_X (sky130_fd_sc_hd_o2111a_2)
          2   0.00
  
```

Activities Terminal - Tue 6:23 AM
 vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```

          0.14  0.68  47.23 v _15226/_X (sky130_fd_sc_hd_or2_2)
          3   0.01           _12208_ (net)
          0.14  0.00  47.23 v _15227/_B (sky130_fd_sc_hd_or2_2)
          0.12  0.66  47.89 v _15227/_X (sky130_fd_sc_hd_or2_2)
          2   0.00           _12209_ (net)
          0.12  0.00  47.89 v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
          0.07  0.44  48.33 v _15230/_X (sky130_fd_sc_hd_o221a_2)
          1   0.00           _03928_ (net)
          0.07  0.00  48.33 v _30440/_D (sky130_fd_sc_hd_dfxtp_2)
          48.33 data arrival time
          0.00  24.73  24.73  clock clk (rise edge)
          0.00  24.73  24.73  clock network delay (ideal)
          0.00  24.73  24.73  clock reconvergence pessimism
          24.73 ^ _30440_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.29 24.44  24.44  library setup time
          24.44 24.44  24.44  data required time
          24.44 data required time
          -48.33 data arrival time
  ----- -23.90 slack (VIOLATED)

tns -710.69
wns -23.90
  
```

10. Make timing ECO fixes to remove all violations.

OR gate of drive strength 2 is driving 4 fanouts

Activities Terminal Tue 6:55 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

		0.19	0.00	0.75	^ _14461 /B2 (sky130_fd_sc_hd_o22ai_2)
1	0.00	0.09	0.14	0.89 v	_14461 /Y (sky130_fd_sc_hd_o22ai_2)
					11623 (net)
		0.09	0.00	0.89 v	_14462 /C1 (sky130_fd_sc_hd_a22lo_2)
1	0.00	0.08	0.55	1.44 v	_14462 /X (sky130_fd_sc_hd_a22lo_2)
					11624 (net)
		0.08	0.00	1.44 v	_14481 /A (sky130_fd_sc_hd_or4_2)
1	0.00	0.21	1.53	2.97 v	_14481 /X (sky130_fd_sc_hd_or4_2)
					11643 (net)
		0.21	0.00	2.97 v	_14509 /A1 (sky130_fd_sc_hd_o2111a_2)
2	0.00	0.07	0.54	3.51 v	_14509 /X (sky130_fd_sc_hd_o2111a_2)
					11671 (net)
		0.07	0.00	3.51 v	_14510 /C (sky130_fd_sc_hd_or3_2)
4	0.01	0.21	1.04	4.55 v	_14510 /X (sky130_fd_sc_hd_or3_2)
					11672 (net)
		0.21	0.00	4.55 v	_14513 /A (sky130_fd_sc_hd_or2_2)
2	0.00	0.11	0.71	5.26 v	_14513 /X (sky130_fd_sc_hd_or2_2)
					11674 (net)
		0.11	0.00	5.26 v	_14514 /C (sky130_fd_sc_hd_or3_2)
4	0.01	0.20	1.03	6.29 v	_14514 /X (sky130_fd_sc_hd_or3_2)
					11675 (net)
		0.20	0.00	6.29 v	_15166 /B (sky130_fd_sc_hd_or2_2)
2	0.00	0.11	0.67	6.96 v	_15166 /X (sky130_fd_sc_hd_or2_2)
					12148 (net)
		0.11	0.00	6.96 v	_15167 /C (sky130_fd_sc_hd_or3_2)
2	0.00	0.17	0.98	7.94 v	_15167 /X (sky130_fd_sc_hd_or3_2)
					12149 (net)
		0.17	0.00	7.94 v	_15168 /B (sky130_fd_sc_hd_or2_2)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

report_net -connections _11672_

Checking command syntax

help replace_cell

Replacing cell

replace_cell _14510_ sky130_fd_sc_hd_or3_4

Generating custom timing report

```
report_checks -fields {net cap slew input_pins} -digits 4
```

Result - slack reduced

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
----- [-23.90 slack (VIOLATED)]
tns -710.69
wns -23.90
% report_net -connections _11672_
Net _11672_
Driver pins
_14510 /X output (sky130_fd_sc_hd_or3_2)
Load pins
_14513 /A input (sky130_fd_sc_hd_or2_2)
_15505 /B input (sky130_fd_sc_hd_or2_2)
_18231 /A input (sky130_fd_sc_hd_buf_1)
_18326 /B input (sky130_fd_sc_hd_nand2_2)

% help replace_cell
replace_cell instance lib_cell
% replace_cell _14510_ sky130_fd_sc_hd_or3_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Fanout Cap Slew Delay Time Description
```

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Fanout Cap Slew Delay Time Description
-----
```

Fanout	Cap	Slew	Delay	Time	Description
		0.0000	0.0000	0.0000	clock clk (rise edge)
		0.0000	0.0000	0.0000	clock network delay (ideal)
		0.0000	0.0000	0.0000 ^	_29052_ /CLK (sky130_fd_sc_hd_dfxtp_2)
		0.0572	0.5830	0.5830 v	_29052_ /Q (sky130_fd_sc_hd_dfxtp_2)
					irq_pending[3] (net)
4	0.0067	0.0572	0.0000	0.5830 v	_14460_ /A (sky130_vsdinv)
		0.1856	0.1667	0.7497 ^	_14460_ /Y (sky130_vsdinv)
					11622 (net)
3	0.0138	0.1856	0.0000	0.7497 ^	_14461_ /B2 (sky130_fd_sc_hd_o22ai_2)
		0.0878	0.1436	0.8933 v	_14461_ /Y (sky130_fd_sc_hd_o22ai_2)
1	0.0021	0.0878	0.0000	0.8933 v	_14462_ /C1 (sky130_fd_sc_hd_a221o_2)
		0.0784	0.5469	1.4402 v	_14462_ /X (sky130_fd_sc_hd_a221o_2)
1	0.0013	0.0784	0.0000	1.4402 v	
		0.2106	1.5344	2.9746 v	_14481_ /A (sky130_fd_sc_hd_or4_2)
1	0.0024	0.2106	0.0000	2.9746 v	_14481_ /X (sky130_fd_sc_hd_or4_2)
		0.0792	0.5466	3.5212 v	_11643_ (net)
2	0.0044				_14509_ /A1 (sky130_fd_sc_hd_o2111a_2)
					14509 /X (sky130_fd_sc_hd_o2111a_2)
					11671 (net)

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

Tue 9:42 AM

3	0.0138	0.1856	0.0000	0.7497	^ _11622_ (net)
		0.0878	0.1436	0.8933	v _14461/_B2 (sky130_fd_sc_hd_o22ai_2)
1	0.0021	0.0878	0.0000	0.8933	v _14461/_Y (sky130_fd_sc_hd_o22ai_2)
		0.0784	0.5469	1.4402	v _11623_ (net)
1	0.0013	0.0784	0.0000	1.4402	v _14462/_C1 (sky130_fd_sc_hd_a221o_2)
		0.2106	1.5344	2.9746	v _14462/_X (sky130_fd_sc_hd_a221o_2)
1	0.0024	0.2106	0.0000	2.9746	v _11624_ (net)
		0.0792	0.5466	3.5212	v _14481/_A (sky130_fd_sc_hd_or4_2)
2	0.0044	0.0792	0.0000	3.5212	v _14481/_X (sky130_fd_sc_hd_or4_2)
		0.1349	0.6755	4.1967	v _11643_ (net)
4	0.0089	0.1349	0.0000	4.1967	v _14509/_A1 (sky130_fd_sc_hd_o2111a_2)
		0.1121	0.6770	4.8737	v _14509/_X (sky130_fd_sc_hd_o2111a_2)
2	0.0025	0.1121	0.0000	4.8737	v _11671_ (net)
		0.1967	1.0321	5.9057	v _14514/_C (sky130_fd_sc_hd_or3_2)
4	0.0070	0.1967	0.0000	5.9057	v _14514/_X (sky130_fd_sc_hd_or3_2)
		0.1148	0.6684	6.5742	v _11675_ (net)
2	0.0032	0.1148	0.0000	6.5742	v _15166/_B (sky130_fd_sc_hd_or2_2)
		0.1692	0.9831	7.5573	v _15166/_X (sky130_fd_sc_hd_or2_2)
2	0.0025	0.0000	0.0000	7.5573	v _12148_ (net)
		0.0000	0.0000	7.5573	v _15167/_C (sky130_fd_sc_hd_or3_2)
		0.0000	0.0000	7.5573	v _15167/_X (sky130_fd_sc_hd_or3_2)
		0.0000	0.0000	7.5573	v _12149_ (net)

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

Tue 7:07 AM

2	0.0035	0.1162	0.0000	46.1648	v _12207_ (net)
		0.1421	0.6813	46.8462	v _15226/_B (sky130_fd_sc_hd_or2_2)
3	0.0079	0.1421	0.0000	46.8462	v _15226/_X (sky130_fd_sc_hd_or2_2)
		0.1228	0.6610	47.5072	v _12208_ (net)
2	0.0044	0.1228	0.0000	47.5072	v _15227/_B (sky130_fd_sc_hd_or2_2)
		0.0713	0.4381	47.9453	v _15227/_X (sky130_fd_sc_hd_or2_2)
1	0.0016	0.0713	0.0000	47.9453	v _12209_ (net)
		0.0000	24.7300	24.7300	v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
		0.0000	24.7300	24.7300	v _15230/_X (sky130_fd_sc_hd_o221a_2)
		0.0000	24.7300	24.7300	v _03928_ (net)
		0.0000	24.7300	24.7300	v _30440/_D (sky130_fd_sc_hd_dfxtip_2)
		0.0000	24.7300	24.7300	v data arrival time
		0.0000	24.7300	24.7300	v clock clk (rise edge)
		0.0000	24.7300	24.7300	v clock network delay (ideal)
		0.0000	24.7300	24.7300	v clock reconvergence pessimism
		24.7300	24.7300	24.7300	v ^ _30440/_CLK (sky130_fd_sc_hd_dfxtip_2)
		-0.2939	24.4361	24.4361	v library setup time
		-0.2939	24.4361	24.4361	v data required time
		24.4361	24.4361	24.4361	v data required time
		-47.9453	-47.9453	-47.9453	v data arrival time
		-23.5092	-23.5092	-23.5092	v slack (VIOLATED)

OR gate of drive strength 2 is driving 4 fanouts

Activities Terminal Tue 9:46 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

1	0.0024	0.2106	1.5344	2.9746 v	_14481/_X (sky130_fd_sc_hd_or4_2) 11643_ (net)
		0.2106	0.0000	2.9746 v	14509/_A1 (sky130_fd_sc_hd_o2111a_2)
		0.0792	0.5466	3.5212 v	14509/_X (sky130_fd_sc_hd_o2111a_2)
2	0.0044	0.0792	0.0000	3.5212 v	11671_ (net)
		0.1349	0.6755	4.1967 v	14510/_C (sky130_fd_sc_hd_or3_4) 14510/_X (sky130_fd_sc_hd_or3_4)
4	0.0089	0.1349	0.0000	4.1967 v	11672_ (net)
		0.1121	0.6770	4.8737 v	14513/_A (sky130_fd_sc_hd_or2_2) 14513/_X (sky130_fd_sc_hd_or2_2)
2	0.0025	0.1121	0.0000	4.8737 v	11674_ (net)
		0.1967	1.0321	5.9057 v	14514/_C (sky130_fd_sc_hd_or3_2) 14514/_X (sky130_fd_sc_hd_or3_2)
4	0.0070	0.1967	0.0000	5.9057 v	11675_ (net)
		0.1148	0.6684	6.5742 v	15166/_B (sky130_fd_sc_hd_or2_2) 15166/_X (sky130_fd_sc_hd_or2_2)
2	0.0032	0.1148	0.0000	6.5742 v	12148_ (net)
		0.1692	0.9831	7.5573 v	15167/_C (sky130_fd_sc_hd_or3_2) 15167/_X (sky130_fd_sc_hd_or3_2)
2	0.0035	0.1692	0.0000	7.5573 v	12149_ (net)
		0.1422	0.7026	8.2599 v	15168/_B (sky130_fd_sc_hd_or2_2) 15168/_X (sky130_fd_sc_hd_or2_2)
3	0.0079	0.1422	0.0000	8.2599 v	12150_ (net)
		0.1162	0.6492	8.9091 v	15169/_B (sky130_fd_sc_hd_or2_2) 15169/_X (sky130_fd_sc_hd_or2_2)
2	0.0035	0.1162	0.0000	8.9091 v	12151_ (net)
		0.1422	0.6817	9.5904 v	15170/_B (sky130_fd_sc_hd_or2_2) 15170/_X (sky130_fd_sc_hd_or2_2)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

report_net -connections _11675_

Replacing cell

replace_cell _14514_ sky130_fd_sc_hd_or3_4

Generating custom timing report

report_checks -fields {net cap slew input_pins} -digits 4

Result - slack reduced

```

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Tue 9:49 AM
-47.9453  data arrival time
-----
-23.5092  slack (VIOLATED)

% report_net -connections _11675_
Net _11675_
Driver pins
_14514/_X output (sky130_fd_sc_hd_or3_2)
Load pins
_14515/_A input (sky130_vsdinv)
_14521/_B2 input (sky130_fd_sc_hd_o221a_2)
_14662/_B input (sky130_fd_sc_hd_or2_2)
_15166/_B input (sky130_fd_sc_hd_or2_2)

% replace_cell _14514_ sky130_fd_sc_hd_or3_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout      Cap      Slew      Delay      Time      Description
-----      -----      -----      -----      -----      -----
          0.0000  0.0000  0.0000  clock clk (rise edge)
          0.0000  0.0000  slack network delay (ideal)

```

Tue 9:50 AM						
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane						
Fanout	Cap	Slew	Delay	Time	Description	
1	0.0013				11624_ (net)	
		0.0784	0.0000	1.4402	v 14481/_A (sky130_fd_sc_hd_or4_2)	
		0.2106	1.5344	2.9746	v 14481/_X (sky130_fd_sc_hd_or4_2)	
1	0.0024				11643_ (net)	
		0.2106	0.0000	2.9746	v 14509/_A1 (sky130_fd_sc_hd_o2111a_2)	
		0.0792	0.5466	3.5212	v 14509/_X (sky130_fd_sc_hd_o2111a_2)	
2	0.0044				11671_ (net)	
		0.0792	0.0000	3.5212	v 14510/_C (sky130_fd_sc_hd_or3_4)	
		0.1349	0.6755	4.1967	v 14510/_X (sky130_fd_sc_hd_or3_4)	
4	0.0089				11672_ (net)	
		0.1349	0.0000	4.1967	v 14513/_A (sky130_fd_sc_hd_or2_2)	
		0.1182	0.6880	4.8847	v 14513/_X (sky130_fd_sc_hd_or2_2)	
2	0.0034				11674_ (net)	
		0.1182	0.0000	4.8847	v 14514/_C (sky130_fd_sc_hd_or3_4)	
		0.1290	0.6794	5.5641	v 14514/_X (sky130_fd_sc_hd_or3_4)	
4	0.0070				11675_ (net)	
		0.1290	0.0000	5.5641	v 15166/_B (sky130_fd_sc_hd_or2_2)	
		0.1148	0.6414	6.2055	v 15166/_X (sky130_fd_sc_hd_or2_2)	
2	0.0032				12148_ (net)	
		0.1148	0.0000	6.2055	v 15167/_C (sky130_fd_sc_hd_or3_2)	
		0.1692	0.9831	7.1886	v 15167/_X (sky130_fd_sc_hd_or3_2)	
2	0.0035				12149_ (net)	
		0.1692	0.0000	7.1886	v 15168/_B (sky130_fd_sc_hd_or2_2)	
		0.1422	0.7026	7.8912	v 15168/_X (sky130_fd_sc_hd_or2_2)	
3	0.0079				12150_ (net)	
		0.1422	0.0000	7.8912	v 15169/_B (sky130_fd_sc_hd_or2_2)	
		0.1162	0.6492	8.5404	v 15169/_X (sky130_fd_sc_hd_or2_2)	
2	0.0025				12151_ (net)	

```
Activities Terminal Tue 9:50 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
2 0.0035
          0.1162  0.0000  45.7962 v _12207_(net)
          0.1421  0.6813  46.4775 v _15226/_B (sky130_fd_sc_hd_or2_2)
          0.1421  0.0000  46.4775 v _15226/_X (sky130_fd_sc_hd_or2_2)
3 0.0079
          0.1228  0.6610  47.1385 v _15227/_B (sky130_fd_sc_hd_or2_2)
          0.1228  0.0000  47.1385 v _15227/_X (sky130_fd_sc_hd_or2_2)
2 0.0044
          0.1228  0.0000  47.1385 v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
          0.0713  0.4381  47.5766 v _15230/_X (sky130_fd_sc_hd_o221a_2)
1 0.0016
          0.0713  0.0000  47.5766 v _30440/_D (sky130_fd_sc_hd_dfxtp_2)
          0.0713  0.0000  47.5766 v data arrival time

          0.0000  24.7300  24.7300  clock clk (rise edge)
          0.0000  24.7300  24.7300  clock network delay (ideal)
          0.0000  24.7300  24.7300  clock reconvergence pessimism
          -0.2939 24.4361  ^ _30440/_CLK (sky130_fd_sc_hd_dfxtp_2)
          24.4361  library setup time
          24.4361  data required time
          24.4361  data required time
          -47.5766  data arrival time
          -23.1405  slack (VIOLATED)
```

OR gate of drive strength 2 driving OA gate has more delay

vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane					
Fanout	Cap	Slew	Delay	Time	Description
			0.0000	0.0000	clock clk (rise edge)
			0.0000	0.0000	clock network delay (ideal)
			0.0000	0.0000	^ _29052_/_CLK (sky130_fd_sc_hd_dfxtp_2)
			0.0572	0.5830	v _29052_/_Q (sky130_fd_sc_hd_dfxtp_2)
4	0.0067				irq_pending[3] (net)
			0.0572	0.0000	0.5830 v _14460_/_A (sky130_vsdinv)
			0.1856	0.1667	0.7497 ^ _14460_/_Y (sky130_vsdinv)
					11622 (net)
3	0.0138				
			0.1856	0.0000	0.7497 ^ _14461_/_B2 (sky130_fd_sc_hd_o22ai_2)
			0.0878	0.1436	0.8933 v _14461_/_Y (sky130_fd_sc_hd_o22ai_2)
					11623 (net)
1	0.0021				
			0.0878	0.0000	0.8933 v _14462_/_C1 (sky130_fd_sc_hd_a221o_2)
			0.0784	0.5469	1.4402 v _14462_/_X (sky130_fd_sc_hd_a221o_2)
1	0.0013				_11624_ (net)
			0.0784	0.0000	1.4402 v _14481_/_A (sky130_fd_sc_hd_or4_2)
			0.2106	1.5344	2.9746 v _14481_/_X (sky130_fd_sc_hd_or4_2)
1	0.0024				_11643_ (net)
			0.2106	0.0000	2.9746 v _14509_/_A1 (sky130_fd_sc_hd_o2111a_2)
			0.0792	0.5466	3.5212 v _14509_/_X (sky130_fd_sc_hd_o2111a_2)
2	0.0044				_11671_ (net)
			0.0792	0.0000	3.5212 v _14510_/_C (sky130_fd_sc_hd_or3_4)
			0.1349	0.6755	4.1967 v _14510_/_X (sky130_fd_sc_hd_or3_4)
4	0.0089				_11672_ (net)
			0.1349	0.0000	4.1967 v _14513_/_A (sky130_fd_sc_hd_or2_2)
			0.1182	0.6880	4.8847 v _14513_/_X (sky130_fd_sc_hd_or2_2)
3	0.0034				_11674_ (net)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

```
report_net -connections _11643_
```

```
# Replacing cell
```

```
replace_cell _14481_ sky130_fd_sc_hd__or4_4
```

```
# Generating custom timing report
```

```
report_checks -fields {net cap slew input_pins} -digits 4
```

Result - slack reduced

```
Activities Terminal - Tue 10:29 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
-47.5766  data arrival time
-----  
-23.1405  slack (VIOLATED)

% report net -connections _11643_
Net _11643_
Driver pins
_14481/_X output (sky130_fd_sc_hd_or4_2)
Load pins
_14509/_A1 input (sky130_fd_sc_hd_o2111a_2)

% replace_cell _14481_ sky130_fd_sc_hd_hd_or4_4
1

% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29043_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout      Cap      Slew      Delay      Time      Description
-----  
0.0000      0.0000      0.0000      0.0000  clock clk (rise edge)
0.0000      0.0000      0.0000      0.0000  clock network delay (ideal)
0.0000      0.0000      0.0000 ^ _29043_/CLK (sky130_fd_sc_hd_dfxtp_2)
0.0581      0.5838      0.5838 v _29043/_Q (sky130_fd_sc_hd_dfxtp_2)
```

```
Activities Terminal + Tue 10:29 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
2 0.0035
          0.1162  0.0000  45.7918 v _12207_(net)
          0.1421  0.6813  46.4731 v _15226/_B (sky130_fd_sc_hd_or2_2)
          0.1421  0.0000  46.4731 v _15226/_X (sky130_fd_sc_hd_or2_2)
3 0.0079
          0.1228  0.6610  47.1341 v _15227/_B (sky130_fd_sc_hd_or2_2)
          0.1228  0.0000  47.1341 v _15227/_X (sky130_fd_sc_hd_or2_2)
2 0.0044
          0.0713  0.4381  47.5723 v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
          0.0713  0.0000  47.5723 v _15230/_X (sky130_fd_sc_hd_o221a_2)
          0.0016
          0.0713  0.0000  47.5723 v _30440/_D (sky130_fd_sc_hd_dfxtp_2)
          0.0713  0.0000  47.5723 data arrival time
          0.0000  24.7300  24.7300  clock clk (rise edge)
          0.0000  24.7300  24.7300  clock network delay (ideal)
          0.0000  24.7300  24.7300  clock reconvergence pessimism
          -0.2939  24.4361 ^ _30440/_CLK (sky130_fd_sc_hd_dfxtp_2)
          24.4361  library setup time
          24.4361  data required time
          24.4361  data required time
          -47.5723  data arrival time
-----
          -23.1362  slack (VIOLATED)
```

OR gate of drive strength 2 driving OA gate has more delay

Activities Terminal Tue 10:32 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

				irq_pending[12] (net)
4	0.0069	0.0581	0.0000	0.5838 v _14484 /A (sky130_vsdinv)
		0.1864	0.1676	0.7515 ^ _14484 /Y (sky130_vsdinv)
3	0.0139	0.1864	0.0000	11646 (net)
		0.0878	0.1674	0.7515 ^ _14486 /A2 (sky130_fd_sc_hd_o22ai_2)
1	0.0021	0.0878	0.0000	0.9189 v _14486 /Y (sky130_fd_sc_hd_o22ai_2)
		0.0784	0.5469	11648 (net)
1	0.0013	0.0784	0.0000	1.4658 v _14487 /C1 (sky130_fd_sc_hd_a22lo_2)
		0.2092	1.5317	11649 (net)
1	0.0023	0.2092	0.0000	2.9975 v _14506 /A (sky130_fd_sc_hd_or4_2)
		0.0792	0.5193	11668 (net)
2	0.0044	0.0792	0.0000	3.5168 v _14509 /A2 (sky130_fd_sc_hd_o2111a_2)
		0.1349	0.6755	11671 (net)
4	0.0089	0.1349	0.0000	3.5168 v _14510 /C (sky130_fd_sc_hd_or3_4)
		0.1182	0.6880	4.1923 v _14510 /X (sky130_fd_sc_hd_or3_4)
2	0.0034	0.1182	0.0000	11672 (net)
		0.1290	0.6794	4.8803 v _14513 /A (sky130_fd_sc_hd_or2_2)
4	0.0070	0.1290	0.0000	4.8803 v _14513 /X (sky130_fd_sc_hd_or2_2)
		0.1148	0.6414	11674 (net)
2	0.0022	0.1148	0.0000	5.5597 v _14514 /C (sky130_fd_sc_hd_or3_4)
		0.1290	0.6414	5.5597 v _14514 /X (sky130_fd_sc_hd_or3_4)
4	0.0070	0.1290	0.0000	11675 (net)
		0.1148	0.6414	6.2011 v _15166 /B (sky130_fd_sc_hd_or2_2)
2	0.0022	0.1148	0.0000	6.2011 v _15166 /X (sky130_fd_sc_hd_or2_2)
		0.1290	0.6414	11676 (net)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

report_net -connections _11668_

Replacing cell

replace_cell _14506_ sky130_fd_sc_hd_or4_4

Generating custom timing report

report_checks -fields {net cap slew input_pins} -digits 4

Result - slack reduced

```

Activities Terminal - Tue 10:36 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
-47.5723  data arrival time
-----  

-23.1362  slack (VIOLATED)

% report_net -connections _11668_
Net _11668
Driver pins
_14506 /X output (sky130_fd_sc_hd_or4_2)
Load pins
_14509 /A2 input (sky130_fd_sc_hd_o2111a_2)

% replace_cell _14506_ sky130_fd_sc_hd_or4_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout      Cap      Slew      Delay      Time      Description
-----  

          0.0000  0.0000  0.0000  clock clk (rise edge)
          0.0000  0.0000  0.0000  clock network delay (ideal)
          0.0000  0.0000  0.0000 ^ _29052 /CLK (sky130_fd_sc_hd_dfxtp_2)
          0.0572  0.5830  0.5830 v _29052 /Q (sky130_fd_sc_hd_dfxtp_2)
           0.0067  


```

```

Activities Terminal - Tue 10:37 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
2  0.0035
          0.1162  0.0000  45.2729 v _12207_(net)
          0.1421  0.6813  45.9542 v _15226 /B (sky130_fd_sc_hd_or2_2)
          0.1421  0.0000  45.9542 v _15226 /X (sky130_fd_sc_hd_or2_2)
          0.1228  0.6610  46.6153 v _12208_(net)
          0.1228  0.0000  46.6153 v _15227 /B (sky130_fd_sc_hd_or2_2)
          0.1228  0.0000  46.6153 v _15227 /X (sky130_fd_sc_hd_or2_2)
          0.0713  0.4381  47.0534 v _12209_(net)
          0.0713  0.0000  47.0534 v _15230 /B2 (sky130_fd_sc_hd_o221a_2)
          0.0713  0.0000  47.0534 v _15230 /X (sky130_fd_sc_hd_o221a_2)
          0.0713  0.0000  47.0534 v _03928_(net)
          0.0713  0.0000  47.0534 v _30440 /D (sky130_fd_sc_hd_dfxtp_2)
          0.0713  0.0000  47.0534 v data arrival time
          0.0000  24.7300  24.7300  clock clk (rise edge)
          0.0000  24.7300  24.7300  clock network delay (ideal)
          0.0000  24.7300  24.7300  clock reconvergence pessimism
          0.0000  24.7300  24.7300 ^ _30440 /CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.2939  24.4361  library setup time
          24.4361  data required time
          24.4361  data arrival time
-----  

-22.6173  slack (VIOLATED)

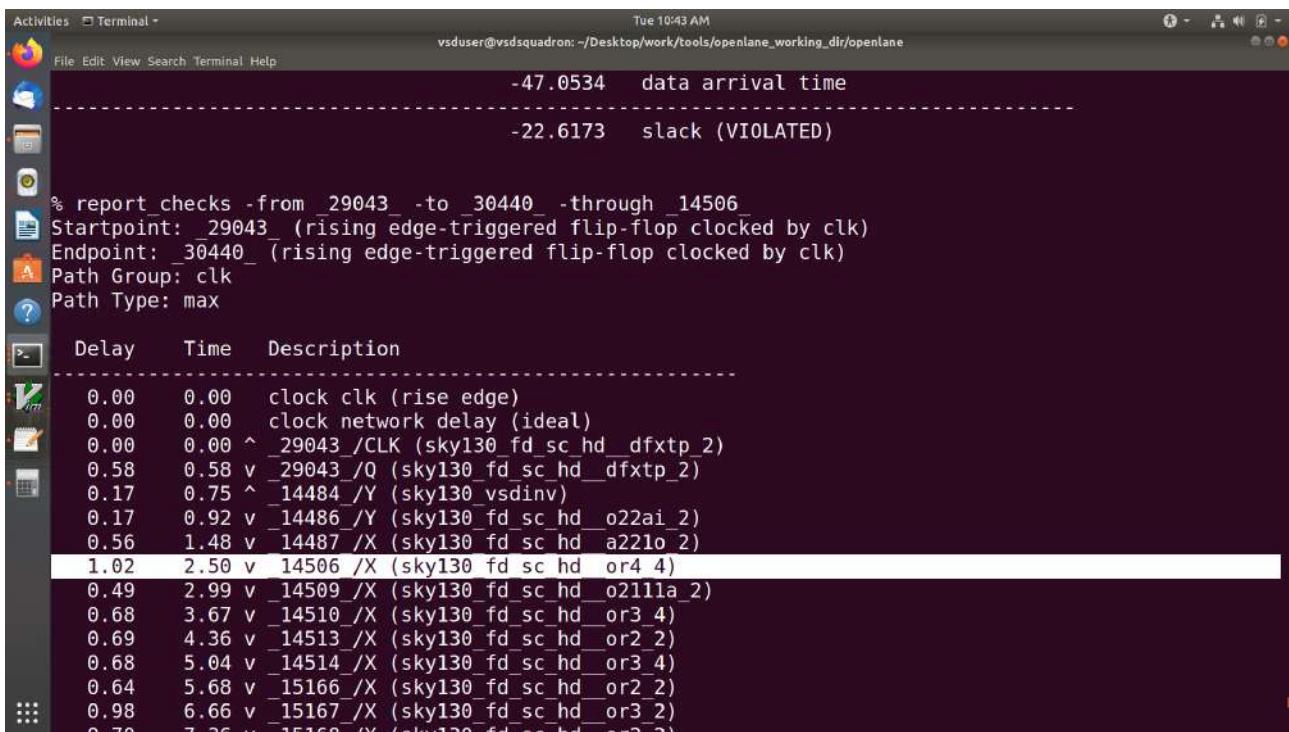
```

Commands to verify instance _14506_ is replaced with sky130_fd_sc_hd_or4_4

Generating custom timing report

report_checks -from _29043_ -to _30440_ -through _14506_

Screenshot of replaced instance



The screenshot shows a terminal window with the following output:

```
Tue 10:43 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
-47.0534  data arrival time
-----
-22.6173  slack (VIOLATED)

% report_checks -from 29043 -to 30440 -through 14506
Startpoint: 29043 (rising edge-triggered flip-flop clocked by clk)
Endpoint: 30440 (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Delay      Time      Description
-----
0.00      0.00      clock clk (rise edge)
0.00      0.00      clock network delay (ideal)
0.00      0.00 ^ 29043 /CLK (sky130_fd_sc_hd_dfxtpl_2)
0.58      0.58 v 29043 /Q (sky130_fd_sc_hd_dfxtpl_2)
0.17      0.75 ^ 14484 /Y (sky130_vsdinv)
0.17      0.92 v 14486 /Y (sky130_fd_sc_hd_o22ai_2)
0.56      1.48 v 14487 /X (sky130_fd_sc_hd_a22lo_2)
1.02      2.50 v 14506 /X (sky130_fd_sc_hd_or4_4)
0.49      2.99 v 14509 /X (sky130_fd_sc_hd_o2111a_2)
0.68      3.67 v 14510 /X (sky130_fd_sc_hd_or3_4)
0.69      4.36 v 14513 /X (sky130_fd_sc_hd_or2_2)
0.68      5.04 v 14514 /X (sky130_fd_sc_hd_or3_4)
0.64      5.68 v 15166 /X (sky130_fd_sc_hd_or2_2)
0.98      6.66 v 15167 /X (sky130_fd_sc_hd_or3_2)
0.70      7.26 v 15168 /X (sky130_fd_sc_hd_or2_2)
```

We started ECO fixes at wns -23.9000 and now we stand at wns -22.6173 we reduced around 1.2827 ns of violation

11. Replace the old netlist with the new netlist generated after timing ECO fix and implement the floorplan, placement and cts.

Now to insert this updated netlist to PnR flow and we can use write_verilog and overwrite the synthesis netlist but before that we are going to make a copy of the old old netlist

Commands to make copy of netlist

```
# Change from home directory to synthesis results directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
25-03_18-52/results/synthesis/
```

```
# List contents of the directory
```

```
ls
```

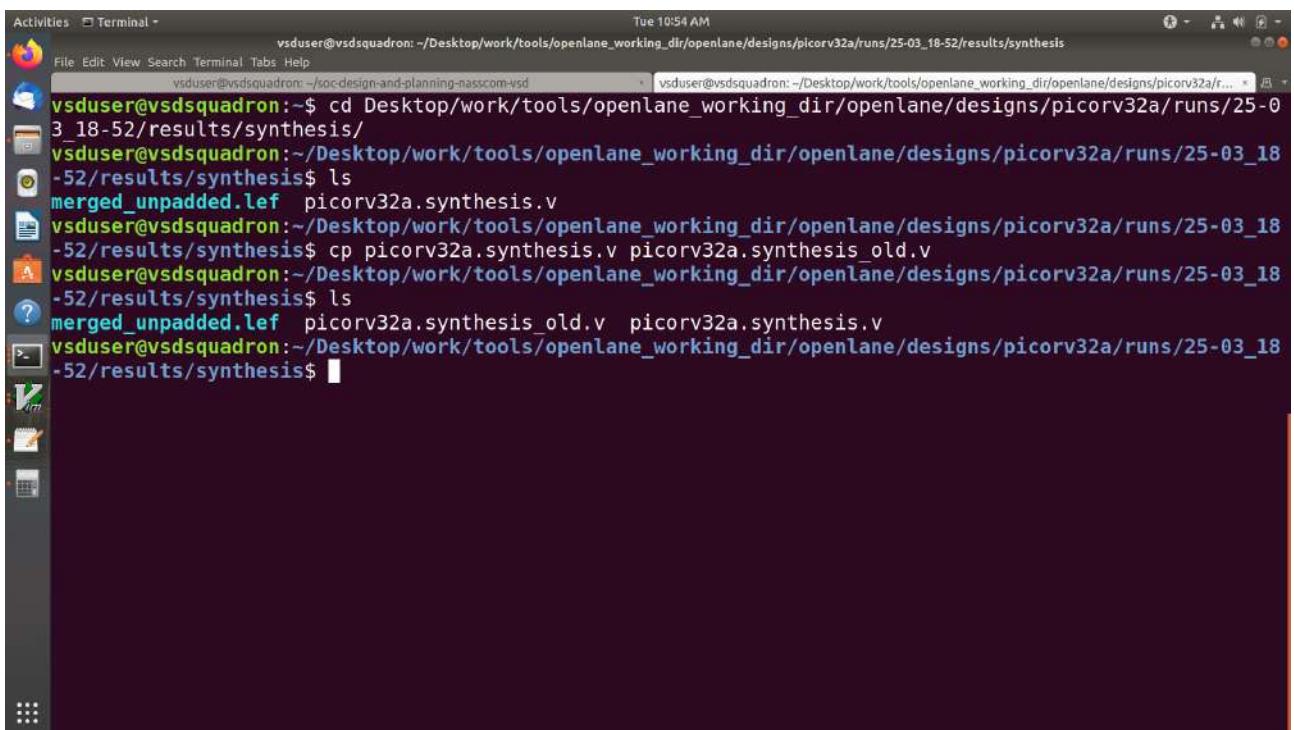
```
# Copy and rename the netlist
```

```
cp picorv32a.synthesis.v picorv32a.synthesis_old.v
```

```
# List contents of the directory
```

```
ls
```

Screenshot of commands run



The screenshot shows a terminal window titled "Terminal" with a dark theme. The window contains the following command history:

```
Tue 10:54 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$ ls
merged_unpadded.lef picorv32a.synthesis.v
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$ cp picorv32a.synthesis.v picorv32a.synthesis_old.v
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$ ls
merged_unpadded.lef picorv32a.synthesis_old.v picorv32a.synthesis.v
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$
```

Commands to write verilog

```
# Check syntax
```

```
help write_verilog
```

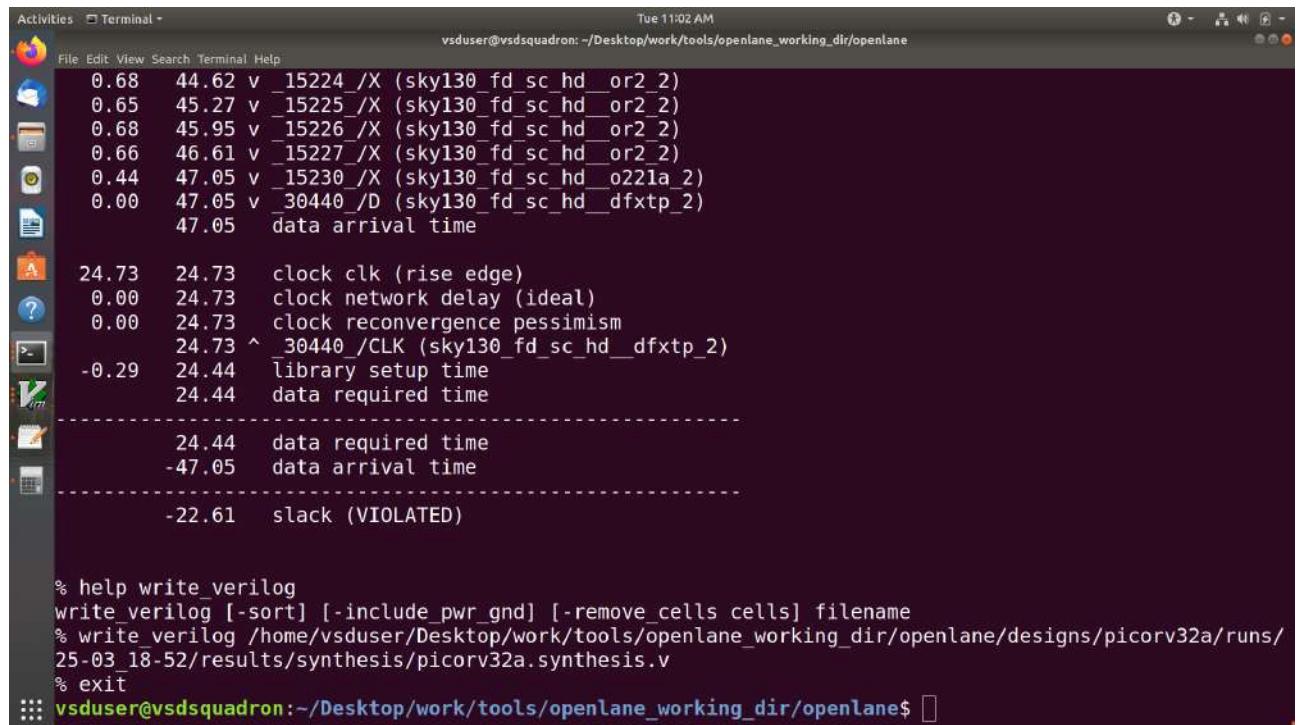
```
# Overwriting current synthesis netlist
```

```
write_verilog /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis/picorv32a.synthesis.v
```

```
# Exit from OpenSTA since timing analysis is done
```

```
exit
```

Screenshot of commands run



The screenshot shows a terminal window with the following content:

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
Tue 11:02 AM
File Edit View Search Terminal Help
0.68 44.62 v _15224_X (sky130_fd_sc_hd_or2_2)
0.65 45.27 v _15225_X (sky130_fd_sc_hd_or2_2)
0.68 45.95 v _15226_X (sky130_fd_sc_hd_or2_2)
0.66 46.61 v _15227_X (sky130_fd_sc_hd_or2_2)
0.44 47.05 v _15230_X (sky130_fd_sc_hd_o221a_2)
0.00 47.05 v _30440_D (sky130_fd_sc_hd_dfxtp_2)
47.05 data arrival time

24.73 24.73 clock clk (rise edge)
0.00 24.73 clock network delay (ideal)
0.00 24.73 clock reconvergence pessimism
24.73 ^ _30440_CLK (sky130_fd_sc_hd_dfxtp_2)
-0.29 24.44 library setup time
24.44 data required time
-----
24.44 data required time
-47.05 data arrival time
-----
-22.61 slack (VIOLATED)

% help write_verilog
write_verilog [-sort] [-include_pwr_gnd] [-remove_cells cells] filename
% write_verilog /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis/picorv32a.synthesis.v
% exit
::: vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$
```

Verified that the netlist is overwritten by checking that instance `_14506_` is replaced with `sky130_fd_sc_hd_or4_4`

```

Activities  M. GVim -
Tue 11:01 AM
picorv32a.synthesis.v (~-/Desktop/work/too...ns/25-03_18-52/results/synthesis) - GVIM2
File Edit Tools Syntax Buffers Window Help
16359     .Y(_11665_));
16360   sky130_fd_sc_hd_o22ai_2 _14504_ (.A1(\irq_mask[21]),
16361     .A2(_11664),
16362     .B1(\irq_mask[23]),
16363     .B2(_11665),
16364     .Y(_11666));
16365   sky130_fd_sc_hd_a221o_2 _14505_ (.A1(_11662),
16366     .A2(\irq_pending[20]),
16367     .B1(_11663),
16368     .B2(\irq_pending[22]),
16369     .C1(_11666),
16370     .X(_11667));
16371   sky130_fd_sc_hd_or4_4 _14506_ (.A(_11649),
16372     .B(_11655),
16373     .C(_11661),
16374     .D(_11667),
16375     .X(_11668));
16376   sky130_vsdinv _14507_ (.A(irq_active),
16377     .Y(_11669));
16378   sky130_vsdinv _14508_ (.A(irq_delay),
16379     .Y(_11670));
16380   sky130_fd_sc_hd_o2111a_2 _14509_ (.A1(_11643),
16381     .A2(_11668),
16382     .B1(_11669),
16383     .C1(_11670),
hlsearch
16371,25      21%

```

Since we confirmed that netlist is replaced and will be loaded in PnR but since we want to follow up on the earlier o violation design we are continuing with the clean design to further stages

Commands load the design and run necessary stages

```
# Now once again we have to prep design so as to update variables
```

```
prep -design picorv32a -tag 24-03_10-03 -overwrite
```

```
# Additional commands to include newly added lef to openlane flow merged.lef
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_STRATEGY
```

```
set ::env(SYNTH_STRATEGY) "DELAY 3"

# Command to set new value for SYNTH_SIZING

set ::env(SYNTH_SIZING) 1

# Now that the design is prepped and ready, we can run synthesis using following
# command

run_synthesis

# Following commands are altogether sourced in "run_floorplan" command

init_floorplan

place_io

tap_decap_or

# Now we are ready to run placement

run_placement

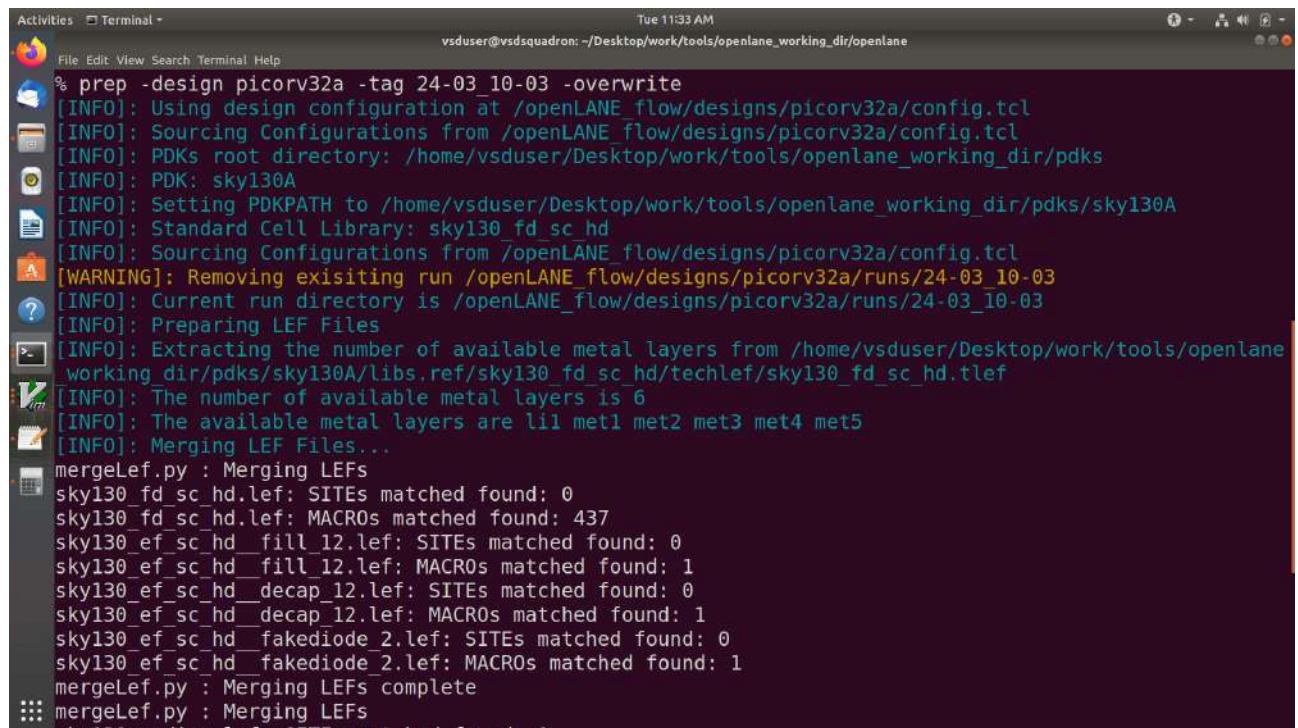
# Incase getting error

unset ::env(LIB_CTS)
```

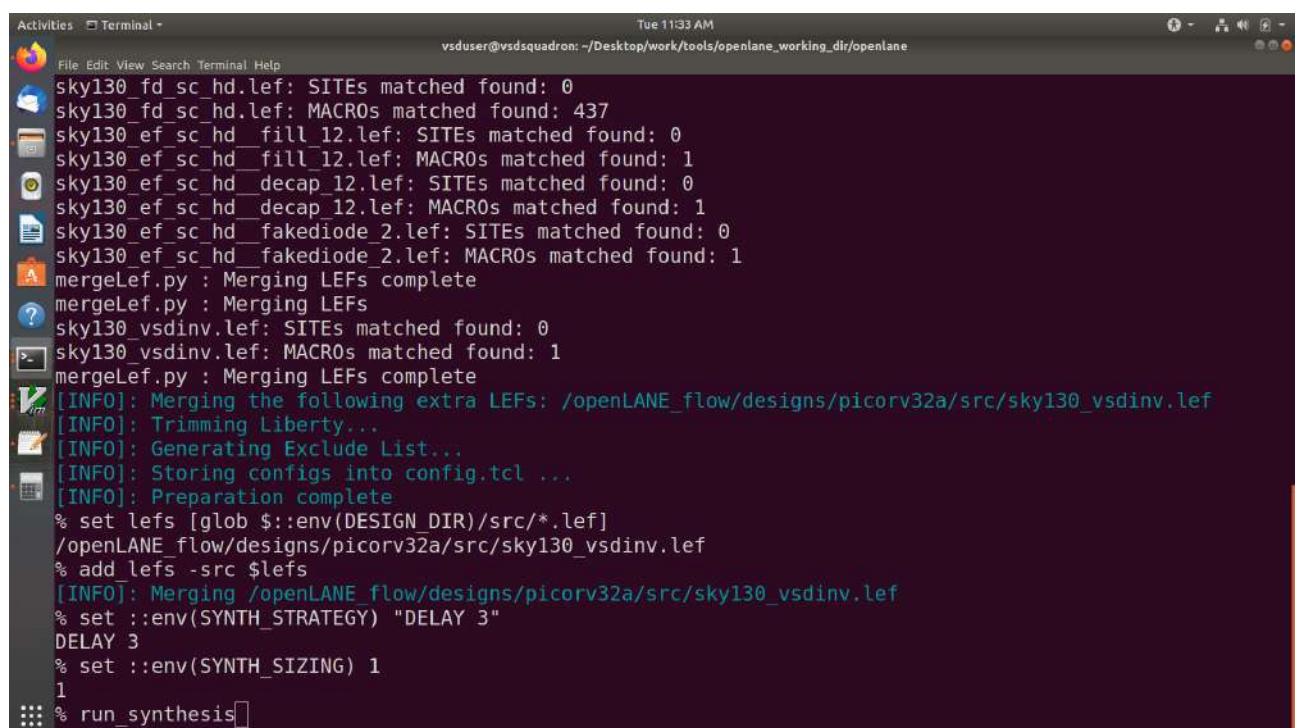
```
# With placement done we are now ready to run CTS
```

```
run_cts
```

Screenshots of commands run



```
Activities Terminal Tue 11:33 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% prep -design picorv32a -tag 24-03_10-03 -overwrite
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130 fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[WARNING]: Removing existing run /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.tlef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1l met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
::: mergeLef.py : Merging LEFs
    120 SITEs and 15 MACROs
```



```
Activities Terminal Tue 11:33 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% set ::env(SYNTH_STRATEGY) "DELAY 3"
DELAY 3
% set ::env(SYNTH_SIZING) 1
1
::: % run_synthesis
```

```
Activities Terminal - Tue 11:35 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
::: % init_floorplan
```

```
Activities Terminal - Tue 11:36 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
% init_floorplan
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 8
OpenROAD 0.9.0 1415572a73
A This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
[INFO IFP-0001] Added 264 rows of 1566 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 731.615 742.335 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/8-verilog2def.die_area.rpt.
[INFO] Floorplanned on a core area of 5.52 10.88 725.88 728.96 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/8-verilog2def.core_area.rpt.
[INFO]: Core area width: 720.36
[INFO]: Core area height: 718.08
[INFO]: Changing layout from 0 to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def
::: % place_io
```

```
Activities Terminal - Tue 11:37 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% place_io
[INFO]: Running IO Placement...
[INFO]: current step index: 9
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def
#Macro blocks found: 0
Using 5u default boundaries offset
Random pin placement
RandomMode Even
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def
::: % tap_decap_or
```

```
Activities Terminal - Tue 11:38 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% place_io
[INFO]: Running IO Placement...
[INFO]: current step index: 9
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def
Step 1: Cut rows...
[INFO TAP-0001] Macro blocks found: 0
[INFO TAP-0002] #Original rows: 264
[INFO TAP-0003] #Cut rows: 0
Step 2: Insert endcaps...
[INFO TAP-0004] #Endcaps inserted: 528
Step 3: Insert tapcells...
[INFO TAP-0005] #Tapcells inserted: 7180
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/floorplan/picorv32a.floorplan.def
::: % run_placement
```

```
Activities Terminal - Tue 11:39 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
legalized HPWL      910806.5 u
delta HPWL          2 %

[INFO DPL-0020] Mirrored 6650 instances
[INFO DPL-0021] HPWL before      910806.5 u
[INFO DPL-0022] HPWL after       895297.0 u
[INFO DPL-0023] HPWL delta      -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/11-resize.r.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 15
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
% run_cts
```

```
Activities Terminal - Tue 12:00 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 25690 components and 145610 component-terminals.
Notice 0:     Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
[INFO]: Changing netlist from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis_optimized.v to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis_cts.v
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 19
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def.png'
Done
[INFO]: Screenshot taken.
% 
```

12. Post-CTS OpenROAD timing analysis.

Commands to be run in OpenLANE flow to do OpenROAD timing analysis with integrated OpenSTA in OpenROAD

```
# Command to run OpenROAD tool
```

```
openroad
```

```
# Reading lef file
```

```
read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
```

```
# Reading def file
```

```
read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
```

```
# Creating an OpenROAD database to work with
```

```
write_db pico_cts.db
```

```
# Loading the created database in OpenROAD
```

```
read_db pico_cts.db
```

```
# Read netlist post CTS
```

```
read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/  
picorv32a.synthesis_cts.v
```

```
# Read library for design
```

```
read_liberty $::env(LIB_SYNTH_COMPLETE)
```

```
# Link design and library

link_design picorv32a

# Read in the custom sdc we created

read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc

# Setting all cloks as propagated clocks

set_propagated_clock [all_clocks]

# Check syntax of 'report_checks' command

help report_checks

# Generating custom timing report

report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format
full_clock_expanded -digits 4

# Exit to OpenLANE flow

exit
```

Screenshots of commands run and timing report generated

```
Activities Terminal - Tue 12:55 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% openroad
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
% read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
% read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 25690 components and 145610 component-terminals.
Notice 0:     Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
% write_db pico_cts.db
% read_db pico_cts.db
% read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis
_cts.v
% read_liberty $::env(LIB_SYNTH_COMPLETE)
1
% link_design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_tapvpwrvgnd_1 has no liberty cell.
```

```
Activities Terminal Tue 12:57 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
[INFO]: Setting output delay to: 4.9460000000000001
[INFO]: Setting input delay to: 4.9460000000000001
[INFO]: Setting load to: 0.017653
[INFO]: Setting propagated_clock [all_clocks]
% help report_checks
report_checks
report_checks [-from from_list|-rise_from from_list|-fall_from from_list] [-through through_list|-rise_through through_list|-fall_through through_list] [-to to_list|-rise_to to_list|-fall_to to_list] [-unconstrained] [-path_delay min|min_rise|min_fall|max|max_rise|max_fall|min_max] [-corner corner_name] [-group_count path_count] [-endpoint_count path_count] [-unique_paths_to_endpoint] [-slack_max slack_max] [-slack_min slack_min] [-sort_by slack] [-path_group group_name] [-format full|full_clock|full_clock_expanded|short|end|summary] [-fields [capacitance|slew|input_pin|net]] [-digits digits] [-no_line_splits] [> filename] [>> filename]
% report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
Startpoint: _30990_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30955_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----.
                               0.0000  0.0000  clock clk (rise edge)
                               0.0000  0.0000  clock source latency
                               0.0225  0.0100  0.0100 ^ clk (in)
                               0.0079  0.0000  0.0100 ^ clk (net)
1  0.0079  0.0000  0.0100 ^ clk (net)
```

```

Activities Terminal - Tue 12:58 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
11 0.0206
    0.0650  0.0000  1.6203 ^ _30955/_CLK (sky130_fd_sc_hd_dfxtp_2)
    0.0000  1.6203  clock reconvergence pessimism
   -0.0263  1.5941  library hold time
    1.5941  data required time
-----
    1.5941  data required time
   -1.8059  data arrival time
-----
    0.2119  slack (MET)

Startpoint: resetn (input port clocked by clk)
Endpoint: mem_la_read (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
----- 0.0000 0.0000 0.0000 0.0000 clock clk (rise edge)
          0.0000 0.0000 4.9460 4.9460 ^ input external delay
          0.0172 0.0055 4.9515 ^ resetn (in)
          0.0042 0.0172 0.0000 4.9515 ^ input101/A (sky130_fd_sc_hd_clkbuf_8)
          0.0582 0.1265 5.0780 ^ input101/X (sky130_fd_sc_hd_clkbuf_8)
          0.0234 0.0582 0.0000 5.0780 ^ net101 (net)

```

```

Activities Terminal - Tue 11:09 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
6 0.0270
    0.0947  0.0000  5.2526 ^ 12638_(net)
    0.1284  0.1277  5.3802 v 17093/_C (sky130_fd_sc_hd_nand3_4)
          0.1284  0.0000  5.3802 v 17093/_Y (sky130_fd_sc_hd_nand3_4)
          0.0799  0.1239  5.5041 ^ 13857_(net)
          0.0023 0.0799 0.0000 5.5041 ^ 18867/_B1 (sky130_fd_sc_hd_a21oi_4)
          0.0799  0.0000 5.5041 ^ 18867/_Y (sky130_fd_sc_hd_a21oi_4)
          0.0177 0.1052 0.1596 5.6637 ^ net199_(net)
          0.1052 0.0000 5.6637 ^ output199/A (sky130_fd_sc_hd_clkbuf_2)
          0.1052 0.0000 5.6637 ^ output199/X (sky130_fd_sc_hd_clkbuf_2)
          0.0000 0.0000 24.7300 24.7300 clock clk (rise edge)
          0.0000 0.0000 24.7300 24.7300 clock network delay (propagated)
          0.0000 0.0000 24.7300 24.7300 clock reconvergence pessimism
         -4.9460 19.7840 19.7840 output external delay
         19.7840 19.7840 data required time
         -5.6637 14.1203 14.1203 data arrival time
-----
         19.7840 14.1203 slack (MET)

% exit
%
```

13. Explore post-CTS OpenROAD timing analysis by removing

'sky130_fd_sc_hd_clkbuf_1' cell from clock buffer list variable

'CTS_CLK_BUFFER_LIST'.

Commands to be run in OpenLANE flow to do OpenROAD timing analysis after changing CTS_CLK_BUFFER_LIST

```
# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)

# Removing 'sky130_fd_sc_hd_clkbuf_1' from the list

set ::env(CTS_CLK_BUFFER_LIST) [lreplace $::env(CTS_CLK_BUFFER_LIST) 0 0]

# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)

# Checking current value of 'CURRENT_DEF'

echo $::env(CURRENT_DEF)

# Setting def as placement def

set ::env(CURRENT_DEF) /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/
placement/picorv32a.placement.def

# Run CTS again

run_cts

# Checking current value of 'CTS_CLK_BUFFER_LIST'
```

```
echo $::env(CTS_CLK_BUFFER_LIST)

# Command to run OpenROAD tool

openroad

# Reading lef file

read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef

# Reading def file

read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def

# Creating an OpenROAD database to work with

write_db pico_cts1.db

# Loading the created database in OpenROAD

read_db pico_cts.db

# Read netlist post CTS

read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/
picorv32a.synthesis_cts.v
```

```
# Read library for design

read_liberty $::env(LIB_SYNTH_COMPLETE)

# Link design and library

link_design picorv32a

# Read in the custom sdc we created

read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc

# Setting all cloks as propagated clocks

set_propagated_clock [all_clocks]

# Generating custom timing report

report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format
full_clock_expanded -digits 4

# Report hold skew

report_clock_skew -hold
```

```
# Report setup skew

report_clock_skew -setup

# Exit to OpenLANE flow

exit

# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)

# Inserting 'sky130_fd_sc_hd__clkbuf_1' to first index of list

set ::env(CTS_CLK_BUFFER_LIST) [linsert $::env(CTS_CLK_BUFFER_LIST) 0
sky130_fd_sc_hd__clkbuf_1]

# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)
```

Screenshots of commands run and timing report generated

```
Activities Terminal - Tue 1:42 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_
8
% set ::env(CTS_CLK_BUFFER_LIST) [lreplace $::env(CTS_CLK_BUFFER_LIST) 0 0]
sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
% set ::env(CURRENT_DEF) /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
% run_cts
[INFO]: Running TritonCTS...
[INFO]: current step index: 20
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Done
```

```
Activities Terminal - Tue 1:45 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def.png'
Done
[INFO]: Screenshot taken.
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% openroad
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
% read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
% read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 25690 components and 145610 component-terminals.
Notice 0: Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
% write_db pico_cts1.db
% read_db pico_cts.db
```

```

Activities Terminal - Tue 1:48 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% write_db pico_cts1.db
% read_db pico_cts.db
% read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis
_cts.v
% read_liberty $::env(LIB_SYNTH_COMPLETE)
1
% link_design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_tapvpwrvgnd_1 has no liberty cell.
% read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
[INFO]: Setting output delay to: 4.946000000000001
[INFO]: Setting input delay to: 4.946000000000001
[INFO]: Setting load to: 0.017653
% set_propagated_clock [all_clocks]
% report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
Startpoint: _30990_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30955_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----  

1 0.0079 0.0225 0.0000 0.0100 ^ clkbuf_0_clk/A (sky130_fd_sc_hd_clkbuf_16)  

0.0225 0.0000 0.0100 ^ clkbuf_0_clk/X (sky130_fd_sc_hd_clkbuf_16)
0.0225 0.0000 0.0100 ^ clkbuf_0_clk/Y (sky130_fd_sc_hd_clkbuf_16)

```

```

Activities Terminal - Tue 1:48 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
0.0520 0.0000 1.2459 ^ _30955/_CLK (sky130_fd_sc_hd_dfxtpl_2)
0.0000 1.2459 clock reconvergence pessimism
-0.0280 1.2179 library hold time
1.2179 data required time
-----  

1.2179 data required time
-1.5305 data arrival time
-----  

0.3125 slack (MET)

Startpoint: resetn (input port clocked by clk)
Endpoint: mem_la_read (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
-----  

1 0.0042 0.0172 0.0000 4.9460 0.0000 ^ clock clk (rise edge)
0.0000 0.0000 ^ clock network delay (propagated)
4.9460 4.9460 ^ input external delay
0.0172 0.0055 4.9515 ^ resetn (in)
resetn (net)
7 0.0234 0.0172 0.0000 4.9515 ^ input101/A (sky130_fd_sc_hd_clkbuf_8)
0.0582 0.1265 5.0780 ^ input101/X (sky130_fd_sc_hd_clkbuf_8)
0.0582 0.0000 5.0780 ^ net101 (net)
0.0582 0.0000 5.0780 ^ 15304/A (sky130_fd_sc_hd_clkbuf_4)
0.0042 0.1746 5.2526 ^ 15304/X (sky130_fd_sc_hd_clkbuf_4)

```

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      Tue 1:50 PM
          -4.9460  19.7840  output external delay
          19.7840  data required time
          19.7840  data required time
          -5.6637  data arrival time
          14.1203  slack (MET)

% report_clock_skew -hold
Clock clk
Latency CRPR Skew
_31226 /CLK ^
    1.36
_32416 /CLK ^
    0.94    0.00    0.42

% report_clock_skew -setup
Clock clk
Latency CRPR Skew
_31226 /CLK ^
    1.36
_32416 /CLK ^
    0.94    0.00    0.42

% exit
%
```

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      Tue 1:53 PM
          % echo $::env(CTS_CLK_BUFFER_LIST)
          sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
          % set ::env(CTS_CLK_BUFFER_LIST) [linsert $::env(CTS_CLK_BUFFER_LIST) 0 sky130_fd_sc_hd_clkbuf_1]
          sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_
          8
          % echo $::env(CTS_CLK_BUFFER_LIST)
          sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_
          8
%
```

Section 5 - Final steps for RTL2GDS using tritonRoute and openSTA (25/03/2024 - 26/03/2024)

Theory

Implementation

- **Section 5 tasks:-**
25. Perform generation of Power Distribution Network (PDN) and explore the PDN layout.
 26. Perform detailed routing using TritonRoute.
 27. Post-Route parasitic extraction using SPEF extractor.
 28. Post-Route OpenSTA timing analysis with the extracted parasitics of the route.
- All section 5 logs, reports and results can be found in following run folder:

Section 5 Run - 26-03_08-45

1. Perform generation of Power Distribution Network (PDN) and explore the PDN layout.

Commands to perform all necessary stages up until now

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:vo.21'
```

```
# Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command
```

```
docker
```

```
# Now that we have entered the OpenLANE flow contained docker sub-system we can  
invoke the OpenLANE flow in the Interactive mode using the following command
```

```
./flow.tcl -interactive
```

```
# Now that OpenLANE flow is open we have to input the required packages for proper  
functionality of the OpenLANE flow
```

```
package require openlane 0.9
```

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the  
design creating some necessary files and directories for running a specific design which in  
our case is 'picorv32a'
```

```
prep -design picorv32a
```

```
# Additional commands to include newly added lef to openlane flow merged.lef
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_STRATEGY
```

```
set ::env(SYNTH_STRATEGY) "DELAY 3"
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Now that the design is prepped and ready, we can run synthesis using following command
```

```
run_synthesis
```

```
# Following commands are altogether sourced in "run_floorplan" command
```

```
init_floorplan
```

```
place_io
```

```
tap_decap_or
```

```
# Now we are ready to run placement
```

```
run_placement
```

```
# Incase getting error
```

```
unset ::env(LIB_CTS)
```

```
# With placement done we are now ready to run CTS
```

```
run_cts
```

Now that CTS is done we can do power distribution network

gen_pdn

Screenshots of power distribution network run

```
Activities Terminal Tue 2:22 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: Screenshot taken.
% gen pdn
[INFO]: Generating PDN...
[INFO]: current step index: 14
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 25690 components and 145610 component-terminals.
Notice 0:     Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/cts/picorv32a.cts.def
[INFO] [PDNG-0016] Power Delivery Network Generator: Generating PDN
[INFO] [PDNG-0016] config: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdkss/sky130A/libs.tech/openlane/common_pdn.tcl
[INFO] [PDNG-0008] Design Name is picorv32a
[INFO] [PDNG-0009] Reading technology data
[INFO] [PDNG-0011] ***** INFO *****
Tunne: stdcell -mid
```

```
Activities Terminal Tue 2:22 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[WARNING PSM-0030] Vsrc location at (705.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
[WARNING PSM-0030] Vsrc location at (425.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 563.420um).
[WARNING PSM-0030] Vsrc location at (705.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 710.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 716.600um).
[WARNING PSM-0030] Vsrc location at (705.520um, 710.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 716.600um).
[INFO PSM-0031] Number of nodes on net VGND = 24383.
[INFO PSM-0037] G matrix created successfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/cts/picorv32a.cts.def to /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
% 
```

Commands to load PDN def in magic in another terminal

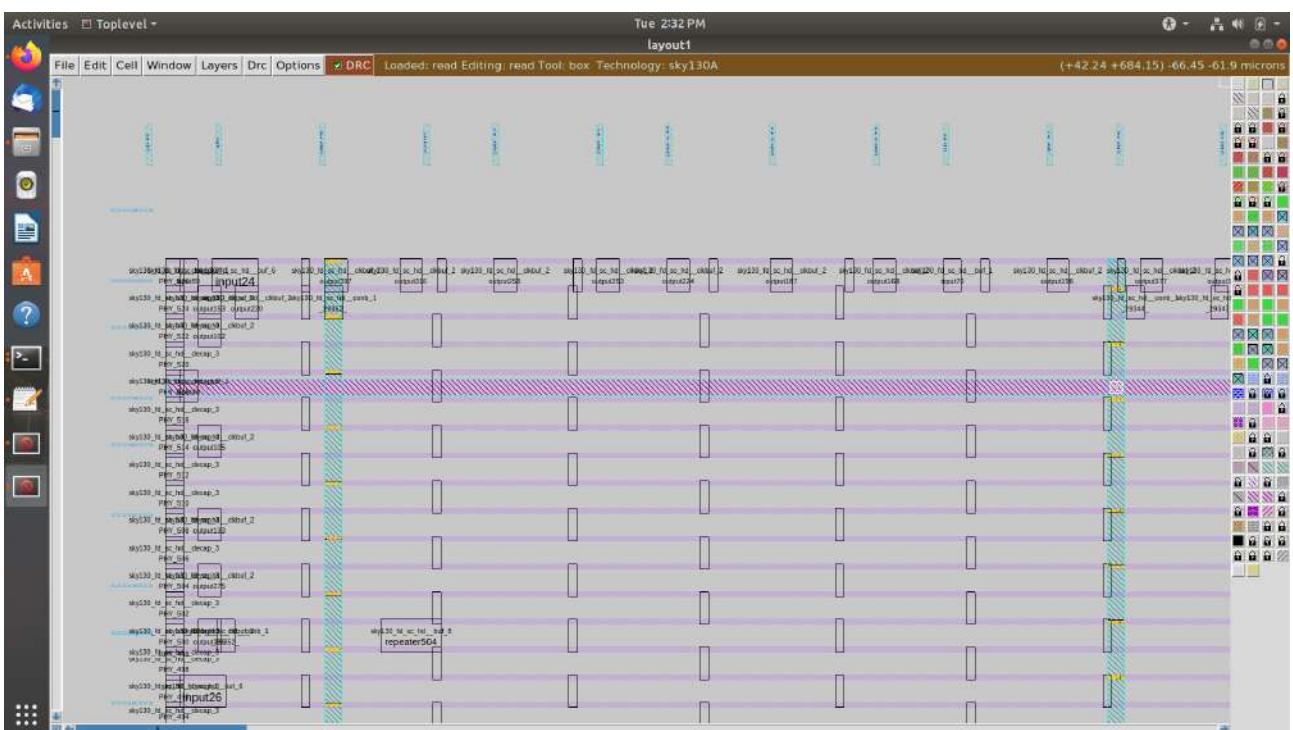
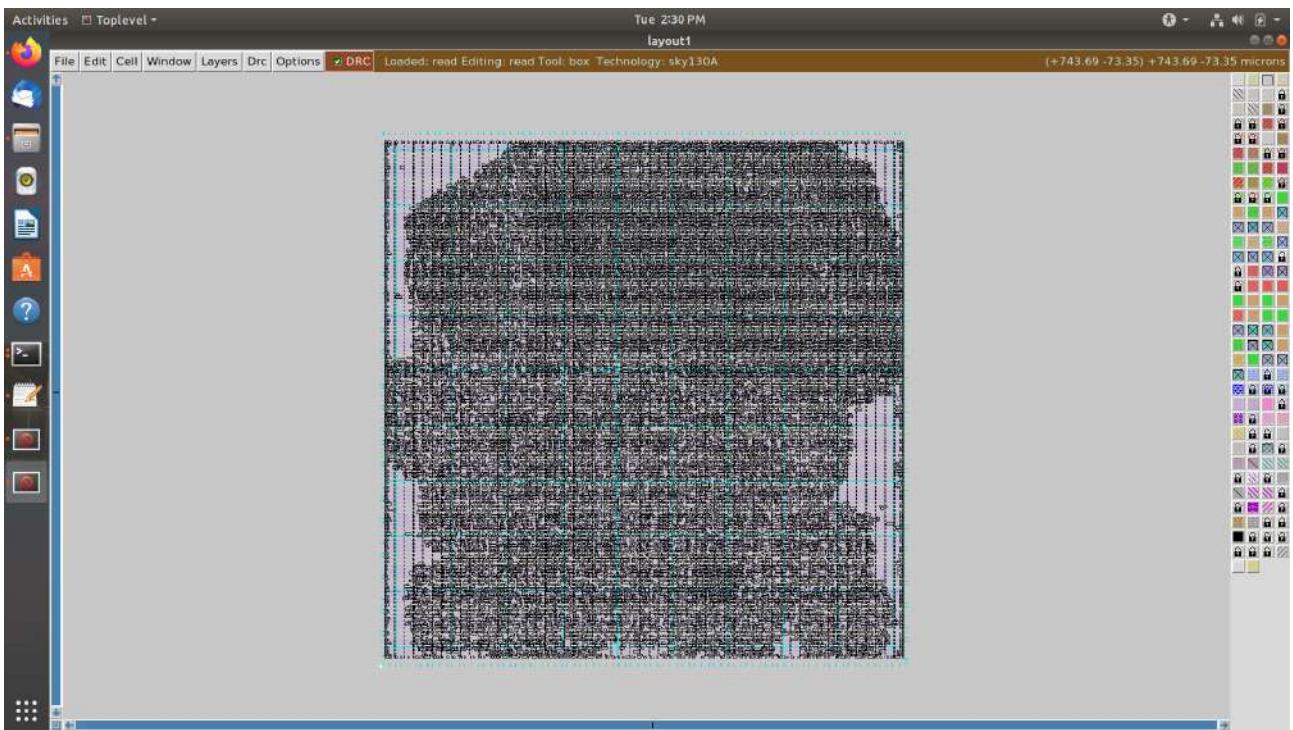
```
# Change directory to path containing generated PDN def
```

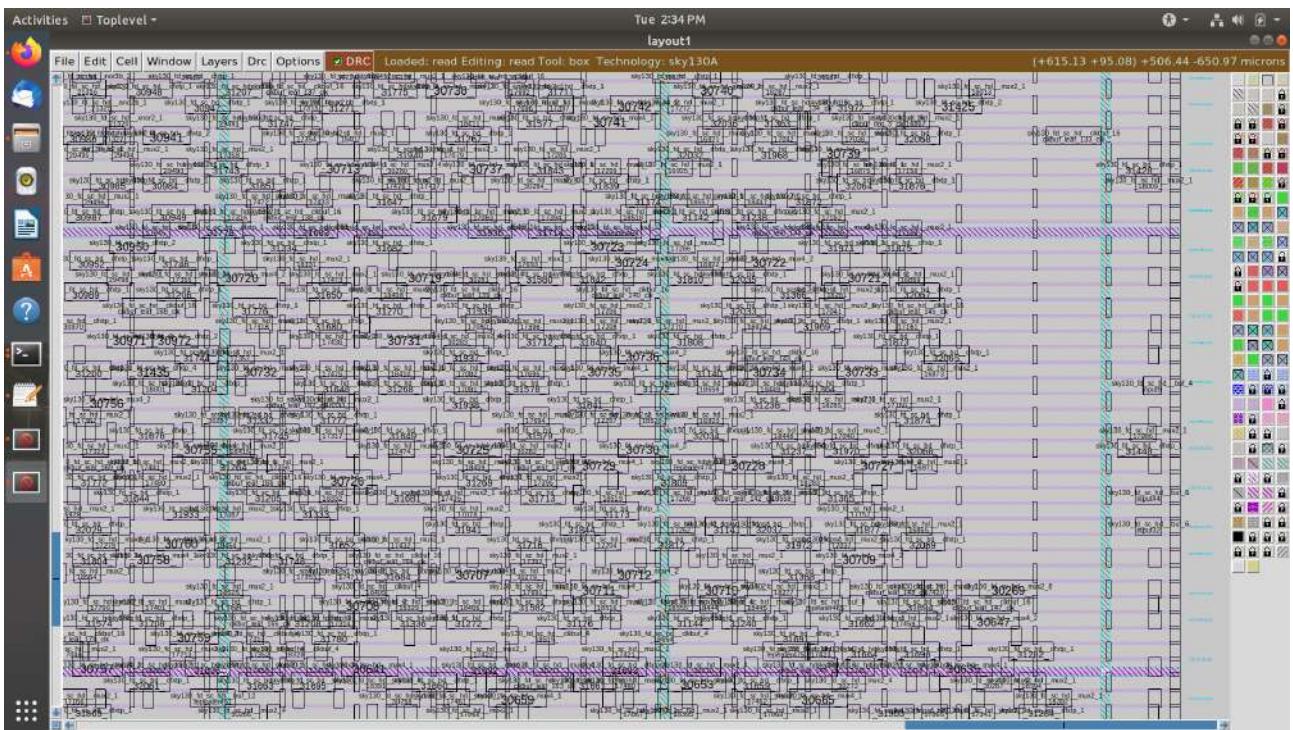
```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/  
26-03_08-45/tmp/floorplan/
```

```
# Command to load the PDN def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read 14-pdn.def &
```

Screenshots of PDN def





2. Perform detailed routing using TritonRoute and explore the routed layout.

Command to perform routing

```
# Check value of 'CURRENT_DEF'
```

```
echo $::env(CURRENT_DEF)
```

```
# Check value of 'ROUTING_STRATEGY'
```

```
echo $::env(ROUTING_STRATEGY)
```

```
# Command for detailed route using TritonRoute
```

```
run_routing
```

Screenshots of routing run

```
Activities Terminal - Tue 2:48 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
% echo $::env(ROUTING_STRATEGY)
can't read "::env(ROUTING_STRATEGY)": no such variable
% run_routing
[INFO]: Routing...
[INFO]: Running Global Routing...
[INFO]: current step index: 15
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
Notice 0: Design: picorv32a
Notice 0: Created 411 pins.
Notice 0: Created 25690 components and 145610 component-terminals.
Notice 0: Created 2 special nets and 0 connections.
Notice 0: Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
Min routing layer: 2
Max routing layer: 6
```

```
Activities Terminal - Tue 3:38 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
elapsed time = 00:00:08, memory = 782.73 (MB)
completing 60% with 0 violations
elapsed time = 00:00:10, memory = 782.73 (MB)
completing 70% with 0 violations
elapsed time = 00:00:12, memory = 782.73 (MB)
completing 80% with 0 violations
elapsed time = 00:00:14, memory = 782.73 (MB)
completing 90% with 0 violations
elapsed time = 00:00:15, memory = 782.73 (MB)
completing 100% with 0 violations
elapsed time = 00:00:17, memory = 782.73 (MB)
number of violations = 0
cpu time = 00:00:16, elapsed time = 00:00:17, memory = 782.73 (MB), peak = 854.19 (MB)
total wire length = 1103187 um
total wire length on LAYER l1l = 2639 um
total wire length on LAYER met1 = 483058 um
total wire length on LAYER met2 = 482317 um
total wire length on LAYER met3 = 122196 um
total wire length on LAYER met4 = 12976 um
total wire length on LAYER met5 = 0 um
total number of vias = 145509
up-via summary (total 145509):

-----
FR_MASTERSLICE      0
      l1l    60472
      met1   78129
      met2   6540
```

```

Activities Terminal - Tue 3:29 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Calculating Runtime From the Start...
[INFO]: Routing completed for picorv32a/26-03_08-45 in 1h7m11s
::: %

```

Commands to load routed def in magic in another terminal

Change directory to path containing routed def

```

cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
26-03_08-45/results/routing/

```

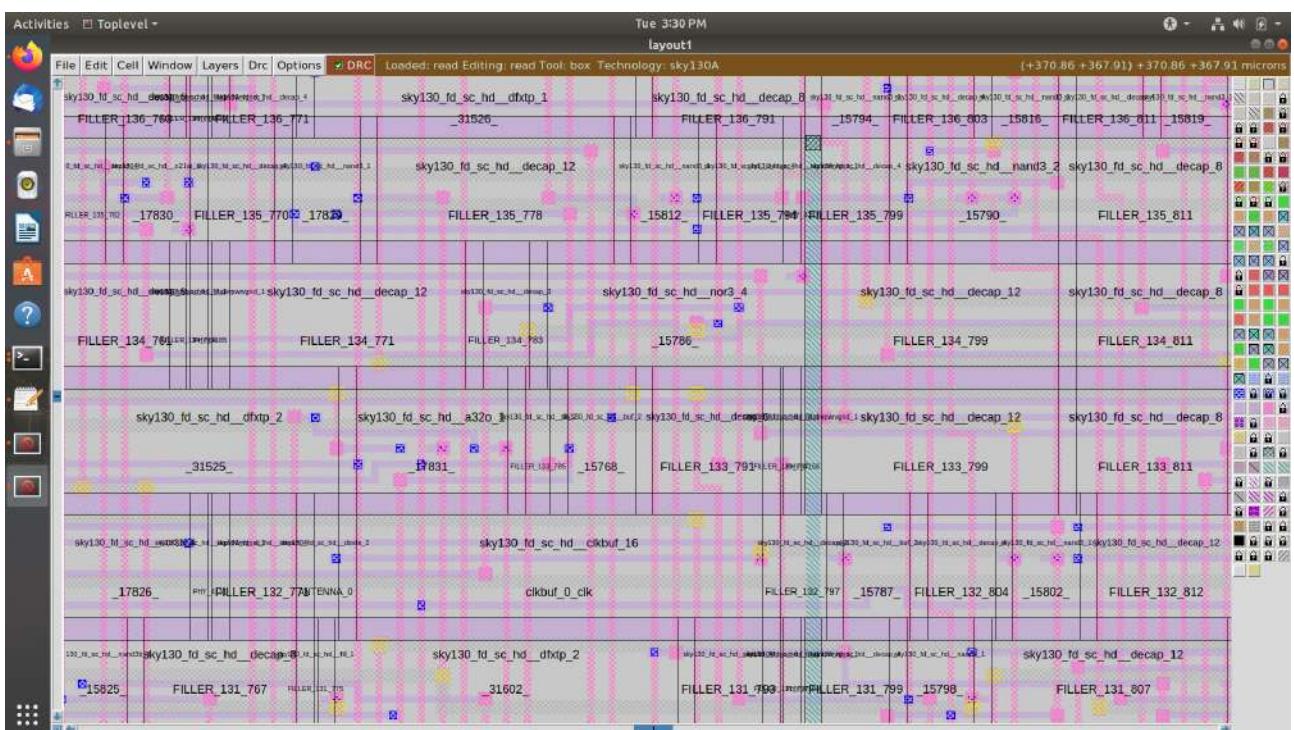
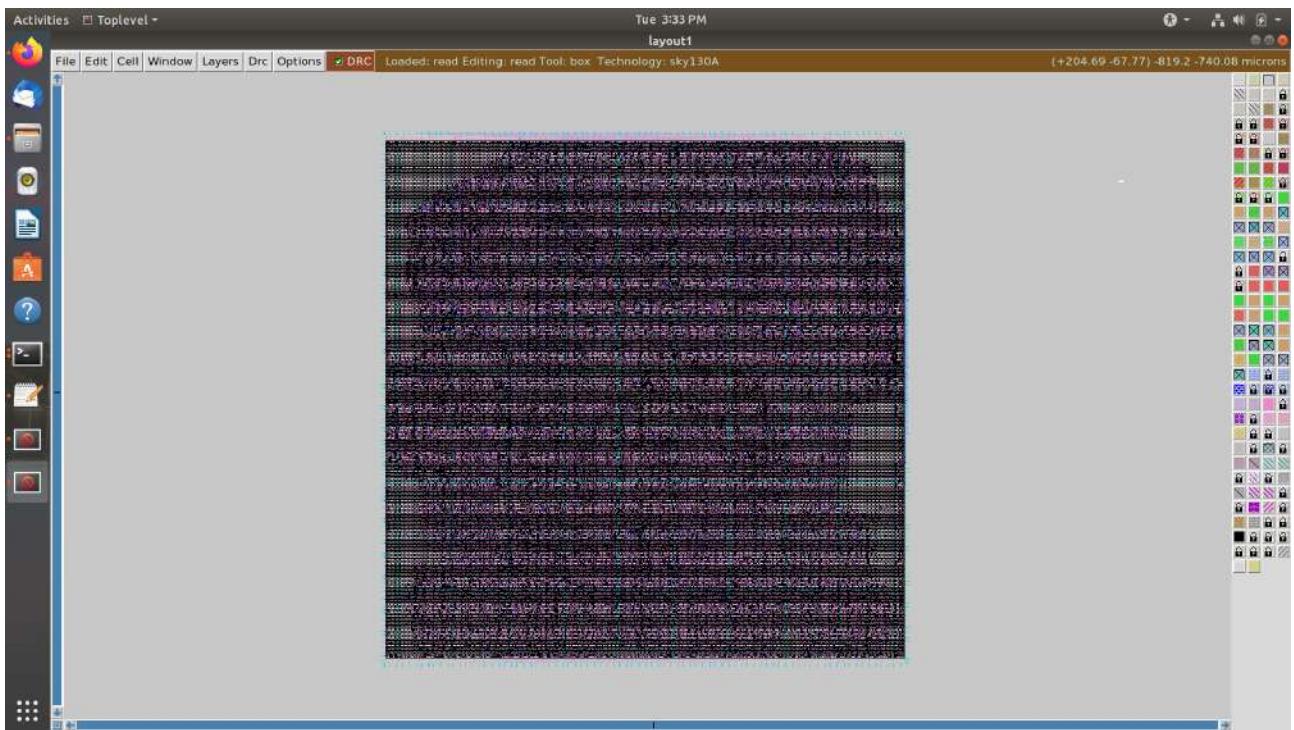
Command to load the routed def in magic tool

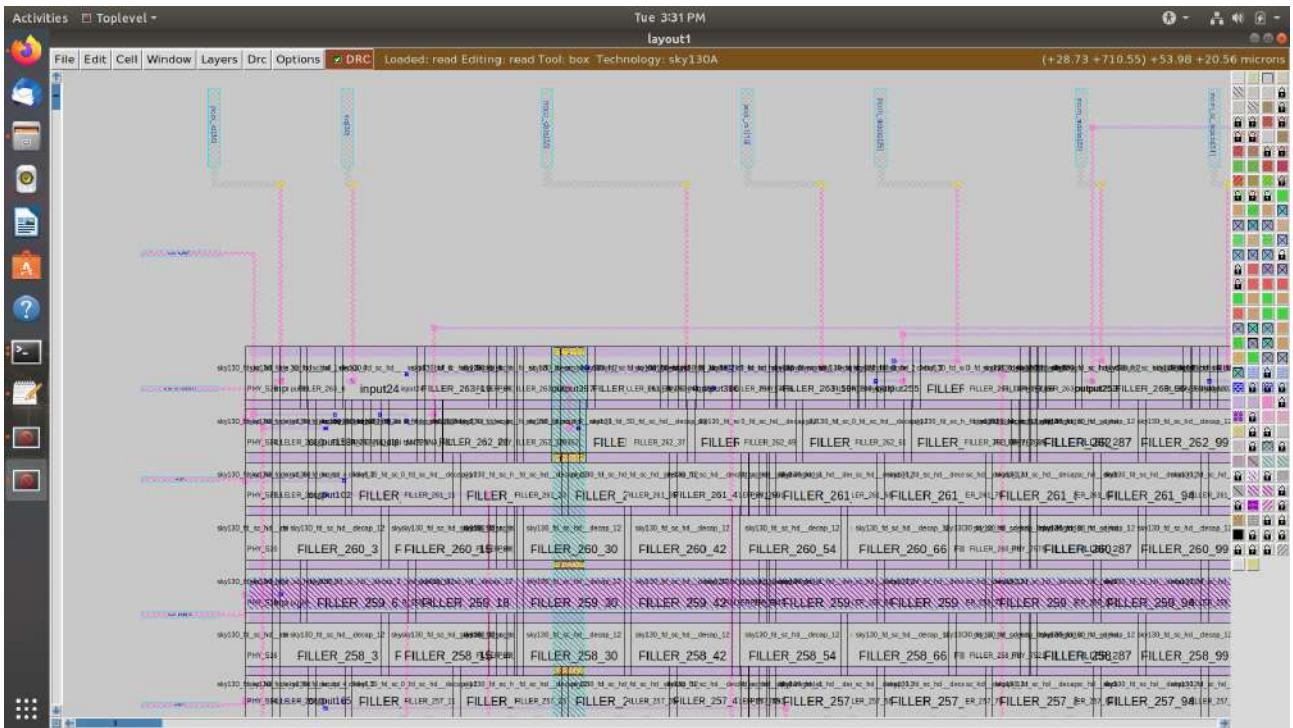
```

magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.def &

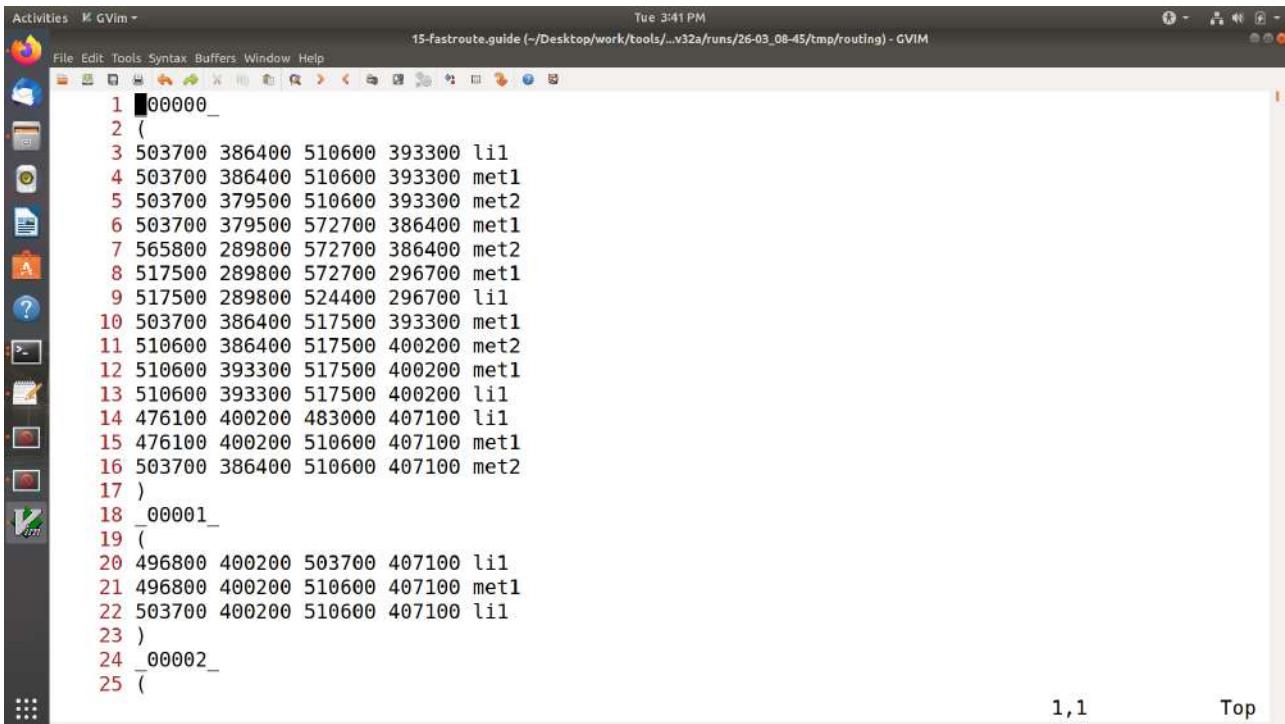
```

Screenshots of routed def





Screenshot of fast route guide present in openlane/designs/picorv32a/runs/26-03_08-45/tmp/routing directory



The screenshot shows a terminal window titled "Activities" with "GVim" selected. The title bar indicates the file is "15-fastroute.guide (~/Desktop/work/tools/...v32a/runs/26-03_08-45/tmp/routing) - GVIM" and the time is "Tue 3:41 PM". The GVim interface has a toolbar with icons for file operations like Open, Save, and Cut/Paste. The left sidebar contains a vertical list of icons for navigating between buffers and windows. The main editor area displays a text file with numbered lines from 1 to 25. The content consists of coordinate pairs and labels such as "lil", "met1", and "met2", which are likely parasitic components or contacts. The file ends with a closing brace on line 25.

```
1 _00000_
2 (
3 503700 386400 510600 393300 lil
4 503700 386400 510600 393300 met1
5 503700 379500 510600 393300 met2
6 503700 379500 572700 386400 met1
7 565800 289800 572700 386400 met2
8 517500 289800 572700 296700 met1
9 517500 289800 524400 296700 lil
10 503700 386400 517500 393300 met1
11 510600 386400 517500 400200 met2
12 510600 393300 517500 400200 met1
13 510600 393300 517500 400200 lil
14 476100 400200 483000 407100 lil
15 476100 400200 510600 407100 met1
16 503700 386400 510600 407100 met2
17 )
18 _00001_
19 (
20 496800 400200 503700 407100 lil
21 496800 400200 510600 407100 met1
22 503700 400200 510600 407100 lil
23 )
24 _00002_
25 (
```

3. Post-Route parasitic extraction using SPEF extractor.

Commands for SPEF extraction using external tool

```
# Change directory
```

```
cd Desktop/work/tools/SPEF_EXTRACTOR
```

```
# Command extract spef
```

```
python3 main.py /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/
designs/picorv32a/runs/26-03_08-45/tmp/merged.lef /home/vsduser/Desktop/work/tools/
openlane_working_dir/openlane/designs/picorv32a/runs/26-03_08-45/results/routing/
picorv32a.def
```

4. Post-Route OpenSTA timing analysis with the extracted parasitics of the route.

Commands to be run in OpenLANE flow to do OpenROAD timing analysis with integrated OpenSTA in OpenROAD

```
# Command to run OpenROAD tool
```

```
openroad
```

```
# Reading lef file
```

```
read_lef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
```

```
# Reading def file
```

```
read_def /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/  
picorv32a.def
```

```
# Creating an OpenROAD database to work with
```

```
write_db pico_route.db
```

```
# Loading the created database in OpenROAD
```

```
read_db pico_route.db
```

```
# Read netlist post CTS
```

```
read_verilog /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/synthesis/  
picorv32a.synthesis_preroute.v
```

```
# Read library for design

read_liberty $::env(LIB_SYNTH_COMPLETE)

# Link design and library

link_design picorv32a

# Read in the custom sdc we created

read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc

# Setting all cloks as propagated clocks

set_propagated_clock [all_clocks]

# Read SPEF

read_spef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/
picorv32a.spef

# Generating custom timing report

report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format
full_clock_expanded -digits 4
```

```
# Exit to OpenLANE flow
```

```
exit
```

Screenshots of commands run and timing report generated

```

Activities Terminal - Tue 11:16 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% openroad
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
% read_lef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
% read_def /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.def
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.def
Notice 0: Design: picorv32a
Notice 0: Created 429 pins.
Notice 0: Created 65617 components and 305814 component-terminals.
Notice 0: Created 2 special nets and 0 connections.
Notice 0: Created 18084 nets and 60532 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.def
% write_db pico_route.db
% read_db pico_route.db
% read_verilog /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/synthesis/picorv32a.synthesis_preroute.v
% read_liberty /openLANE_flow/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib
1
::: % link design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_fill_1 has no liberty cell.

```

```

Activities Terminal - Tue 11:17 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% link_design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_fill_1 has no liberty cell.
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_fill_2 has no liberty cell.
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_tapuvwrgnd_1 has no liberty cell.
% read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
[INFO]: Setting output delay to: 4.9460000000000001
[INFO]: Setting input delay to: 4.9460000000000001
[INFO]: Setting load to: 0.017653
% set_propagated_clock [all_clocks]
% read_spef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.spef
1
% report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
Startpoint: _30900_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30910_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----
                           0.0000  0.0000  clock clk (rise edge)
                           0.0000  0.0000  clock source latency
                           0.0897  0.0624  0.0624 ^ clk (in)
                           0.0563          clk (net)
                           0.0900  0.0000  0.0624 ^ clkbuf_0_clk/A (sky130_fd_sc_hd_clkbuff_16)
                           0.0371  0.1366  0.1990 ^ clkbuf_0_clk/X (sky130_fd_sc_hd_clkbuff_16)
                           2     0.0143          clknet_0_clk (net)

```

```

Activities Terminal - Tue 11:17 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      5  0.0099
          0.0596  0.0002  2.3273 ^ clknet_leaf_220_clk (net)
          0.0000  2.3273  clock reconvergence pessimism
          -0.0274  2.2998  library hold time
          2.2998  data required time
          2.2998  data required time
          -1.9092  data arrival time
          -0.3907  slack (VIOLATED)

Startpoint: resetn (input port clocked by clk)
Endpoint: mem_la_read (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout   Cap     Slew     Delay    Time   Description
-----+-----+-----+-----+-----+
           0.0000  0.0000  clock clk (rise edge)
           0.0000  0.0000  clock network delay (propagated)
           4.9460  4.9460 ^ input external delay
           0.0172  0.0055  4.9515 ^ resetn (in)
           1  0.0042   resetn (net)
           0.0172  0.0000  4.9515 ^ input101/A (sky130_fd_sc_hd_clkbuf_8)
           0.0662  0.1329  5.0843 ^ input101/X (sky130_fd_sc_hd_clkbuf_8)
           7  0.0299   net101 (net)

```

```

Activities Terminal - Tue 11:17 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      6  0.0211
          0.0760  0.0002  5.2498 ^ 12638_(net)
          0.0933  0.0927  5.3425 v 17093/_C (sky130_fd_sc_hd_nand3_4)
          4  0.0143   17093/_Y (sky130_fd_sc_hd_nand3_4)
          0.0933  0.0001  5.3426 v 13857_(net)
          0.4344  0.3758  5.7184 ^ 18867/_B1 (sky130_fd_sc_hd_a21oi_4)
          2  0.0603   18867/_Y (sky130_fd_sc_hd_a21oi_4)
          net199 (net)
          0.4349  0.0115  5.7299 ^ output199/A (sky130_fd_sc_hd_clkbuf_2)
          0.1189  0.2493  5.9793 ^ output199/X (sky130_fd_sc_hd_clkbuf_2)
          1  0.0177   mem_la_read (net)
          0.1189  0.0002  5.9795 ^ mem_la_read (out)
          24.7300  24.7300  data arrival time
          0.0000  24.7300  clock clk (rise edge)
          0.0000  24.7300  clock network delay (propagated)
          -4.9460  19.7840  clock reconvergence pessimism
          19.7840  19.7840  output external delay
          19.7840  19.7840  data required time
          -5.9795  13.8045  data arrival time
          -5.9795  13.8045  slack (MET)

% exit
%
```

About

2 Week digital VLSI SoC design and planning workshop with complete RTL2GDSII flow organised by VSD in collaboration with NASSCOM (Advanced Physical Design using OpenLANE/Sky130)

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History

--	--	--

Desktop/work/tools/ openlane working dir	Add files via upload	
--	--	--

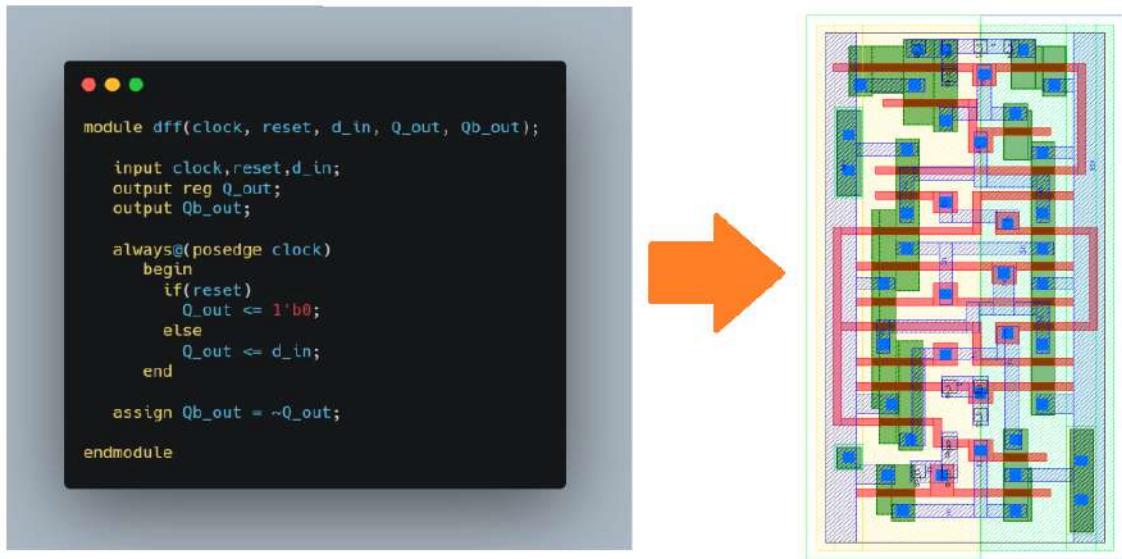
drc test	Add files via upload	
--------------------------	--	--

README.m d	Update README.md	
--------------------------------	--------------------------------------	--

drc tests.tg z	Add files via upload	
------------------------------------	--	--

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Digital VLSI SoC Design & Planning (RTL2GDSII Flow)

Digital VLSI SoC Design and Planning

OS linux

EDA Tools OpenLANE-Flow, Yosys, abc, OpenROAD, TritonRoute, OpenSTA, magic, netgen, GUNA

languages verilog, bash, TCL last commit last wednesday languages 12

verilog 96.2% repo size 179 MB code size 32.9 MB files 4

2 Week digital VLSI SoC design and planning workshop with complete RTL2GDSII flow organised by VSD in collaboration with NASSCOM

Section 1 - Inception of open-source EDA, OpenLANE and Sky130 PDK (14/03/2024 - 15/03/2024)

Theory

Expand or Collapse

Implementation

Section 1 tasks:-

1. Run 'picorv32a' design synthesis using OpenLANE flow and generate necessary outputs.
2. Calculate the flop ratio.

- All section 1 logs, reports and results can be found in following run folder:

Section 1 Run - 15-03_15-51

1. Run 'picorv32a' design synthesis using OpenLANE flow and generate necessary outputs.

Commands to invoke the OpenLANE flow and perform synthesis

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:vo.21'
```

```
# Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command
```

```
docker
```

```
# Now that we have entered the OpenLANE flow contained docker sub-system we can  
invoke the OpenLANE flow in the Interactive mode using the following command
```

```
./flow.tcl -interactive
```

```
# Now that OpenLANE flow is open we have to input the required packages for proper  
functionality of the OpenLANE flow
```

```
package require openlane 0.9
```

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the  
design creating some necessary files and directories for running a specific design which in  
our case is 'picorv32a'
```

```
prep -design picorv32a
```

```
# Now that the design is prepped and ready, we can run synthesis using following  
command
```

```
run_synthesis
```

```
# Exit from OpenLANE flow
```

```
exit
```

```
# Exit from OpenLANE flow docker sub-system
```

`exit`

Screenshots of running each commands

Activities Terminal Fri 9:23 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
vsduser@vsdsquadron:~$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ docker
bash-4.2$ ./flow.tcl -interactive
[INFO]:
[INFO]: Version: v0.21
[INFO]: Running interactively
% package require openlane 0.9
0.9
% prep -design picorv32a
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/15-03_15-51
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane
```

Activities Terminal Fri 9:24 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/15-03_15-51
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.tlef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1l met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
[INFO]: % run_synthesis[]
```

```
Activities Terminal Fri 9:29 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -759.46
wns -24.89
[INFO]: Synthesis was successful
::: %
```

2. Calculate the flop ratio.

Screenshots of synthesis statistics report file with required values highlighted

Activities M GVim Fri 10:02 PM

File Edit Tools Syntax Buffers Window Help

1-yosys_4.stat.rpt (~/Desktop/work/tools/...uns/15-03_15-51/reports/synthesis) - GVIM

```
1
2 28. Printing statistics.
3
4 === picorv32a ===
5
6 Number of wires: 14596
7 Number of wire bits: 14978
8 Number of public wires: 1565
9 Number of public wire bits: 1947
10 Number of memories: 0
11 Number of memory bits: 0
12 Number of processes: 0
13 Number of cells: 14876
14 sky130_fd_sc_hd_a2111o_2 1
15 sky130_fd_sc_hd_a211o_2 35
16 sky130_fd_sc_hd_a211oi_2 60
17 sky130_fd_sc_hd_a21bo_2 149
18 sky130_fd_sc_hd_a21boi_2 8
19 sky130_fd_sc_hd_a21o_2 57
20 sky130_fd_sc_hd_a21oi_2 244
21 sky130_fd_sc_hd_a221o_2 86
22 sky130_fd_sc_hd_a22o_2 1013
23 sky130_fd_sc_hd_a2bb2o_2 1748
24 sky130_fd_sc_hd_a2bb2oi_2 81
25 sky130_fd_sc_hd_a311o_2 2
```

hlsearch 25, 38 Top

Activities M GVim Fri 10:03 PM

File Edit Tools Syntax Buffers Window Help

1-yosys_4.stat.rpt (~/Desktop/work/tools/...uns/15-03_15-51/reports/synthesis) - GVIM

```
25 sky130_fd_sc_hd_a311o_2 2
26 sky130_fd_sc_hd_a31o_2 49
27 sky130_fd_sc_hd_a31oi_2 7
28 sky130_fd_sc_hd_a32o_2 46
29 sky130_fd_sc_hd_a41o_2 1
30 sky130_fd_sc_hd_and2_2 157
31 sky130_fd_sc_hd_and3_2 58
32 sky130_fd_sc_hd_and4_2 345
33 sky130_fd_sc_hd_and4b_2 1
34 sky130_fd_sc_hd_buf_1 1656
35 sky130_fd_sc_hd_buf_2 8
36 sky130_fd_sc_hd_conb_1 42
37 sky130_fd_sc_hd_dfxtp_2 1613
38 sky130_fd_sc_hd_inv_2 1615
39 sky130_fd_sc_hd_mux2_1 1224
40 sky130_fd_sc_hd_mux2_2 2
41 sky130_fd_sc_hd_mux4_1 221
42 sky130_fd_sc_hd_nand2_2 78
43 sky130_fd_sc_hd_nor2_2 524
44 sky130_fd_sc_hd_nor2b_2 1
45 sky130_fd_sc_hd_nor3_2 42
46 sky130_fd_sc_hd_nor4_2 1
47 sky130_fd_sc_hd_o2111a_2 2
48 sky130_fd_sc_hd_o211a_2 69
49 sky130_fd_sc_hd_o211ai_2 6
```

search hit BOTTOM, continuing at TOP 49, 38 48%

Calculation of Flop Ratio and DFF % from synthesis statistics report file

Section 2 - Good floorplan vs bad floorplan and introduction to library cells (16/03/2024 - 17/03/2024)

Theory

Implementation

Section 2 tasks:-

1. Run 'picorv32a' design floorplan using OpenLANE flow and generate necessary outputs.
 2. Calculate the die area in microns from the values in floorplan def.
 3. Load generated floorplan def in magic tool and explore the floorplan.
 4. Run 'picorv32a' design congestion aware placement using OpenLANE flow and generate necessary outputs.
 5. Load generated placement def in magic tool and explore the placement.
-
- All section 2 logs, reports and results can be found in following run folder:

Section 2 Run - 17-03_12-06

1. Run 'picorv32a' design floorplan using OpenLANE flow and generate necessary outputs.

Commands to invoke the OpenLANE flow and perform floorplan

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:v0.21'
```

Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command

```
docker
```

Now that we have entered the OpenLANE flow contained docker sub-system we can invoke the OpenLANE flow in the interactive mode using the following command

```
./flow.tcl -interactive
```

Now that OpenLANE flow is open we have to input the required packages for proper functionality of the OpenLANE flow

```
package require openlane 0.9
```

Now the OpenLANE flow is ready to run any design and initially we have to prep the design creating some necessary files and directories for running a specific design which in our case is 'picorv32a'

```
prep -design picorv32a
```

Now that the design is prepped and ready, we can run synthesis using following command

```
run_synthesis
```

```
# Now we can run floorplan
```

```
run_floorplan
```

Screenshot of floorplan run

```
Activities Terminal - Sun 6:06 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: Synthesis was successful
% run_floorplan
[INFO]: Running Floorplanning...
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 3
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/l
ib/sky130_fd_sc_hd_tt_025C_lv80.lib line 31, default_operating_condition tt_025C_lv80 not found.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/merged_unpadded.le
f
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 440 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/merged_unpadded.le
f
[INFO IFP-0001] Added 238 rows of 1412 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 660.685 671.405 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/reports/floorplan/3-verilog2def.die_area.rpt.
[INFO] Floorplanned on a core area of 5.52 10.88 655.04 658.24 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/reports/floorplan/3-verilog2def.core_area.rpt.
[INFO]: Core area width: 649.52
[INFO]: Core area height: 647.36
[INFO]: Changing layout from 0 to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/floorplan/3-verilog2def_openroad.def
[INFO]: Running IO Placement...
[INFO]: success! step index: 3
```

```
Activities Terminal - Sun 6:06 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
er stripe. Moving to closest stripe at (567.000um, 103.880um).
[WARNING PSM-0030] Vsrc location at (565.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 257.060um).
[WARNING PSM-0030] Vsrc location at (5.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (145.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
[WARNING PSM-0030] Vsrc location at (425.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 563.420um).
[INFO PSM-0031] Number of nodes on net VGND = 19223.
[INFO PSM-0037] G matrix created sucessfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/floorplan/picorv32a.floorplan.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/floorplan/7-pdn.def
1
% [ ]
```

2. Calculate the die area in microns from the values in floorplan def.

Screenshot of contents of floorplan def

```

1 VERSION 5.8 ;
2 DIVIDERCHAR "/";
3 BUSBITCHARS "[]";
4 DESIGN picorv32a ;
5 UNITS DISTANCE MICRONS 1000 ;
6 DIEAREA ( 0 0 ) ( 660685 671405 ) ;
7 ROW ROW_0 unithd 5520 10880 FS DO 1412 BY 1 STEP 460 0 ;
8 ROW ROW_1 unithd 5520 13600 N DO 1412 BY 1 STEP 460 0 ;
9 ROW ROW_2 unithd 5520 16320 FS DO 1412 BY 1 STEP 460 0 ;
10 ROW ROW_3 unithd 5520 19040 N DO 1412 BY 1 STEP 460 0 ;
11 ROW ROW_4 unithd 5520 21760 FS DO 1412 BY 1 STEP 460 0 ;
12 ROW ROW_5 unithd 5520 24480 N DO 1412 BY 1 STEP 460 0 ;
13 ROW ROW_6 unithd 5520 27200 FS DO 1412 BY 1 STEP 460 0 ;
14 ROW ROW_7 unithd 5520 29920 N DO 1412 BY 1 STEP 460 0 ;
15 ROW ROW_8 unithd 5520 32640 FS DO 1412 BY 1 STEP 460 0 ;
16 ROW ROW_9 unithd 5520 35360 N DO 1412 BY 1 STEP 460 0 ;
17 ROW ROW_10 unithd 5520 38080 FS DO 1412 BY 1 STEP 460 0 ;
18 ROW ROW_11 unithd 5520 40800 N DO 1412 BY 1 STEP 460 0 ;
19 ROW ROW_12 unithd 5520 43520 FS DO 1412 BY 1 STEP 460 0 ;
20 ROW ROW_13 unithd 5520 46240 N DO 1412 BY 1 STEP 460 0 ;
21 ROW ROW_14 unithd 5520 48960 FS DO 1412 BY 1 STEP 460 0 ;
22 ROW ROW_15 unithd 5520 51680 N DO 1412 BY 1 STEP 460 0 ;
23 ROW ROW_16 unithd 5520 54400 FS DO 1412 BY 1 STEP 460 0 ;
24 ROW ROW_17 unithd 5520 57120 N DO 1412 BY 1 STEP 460 0 ;
25 ROW ROW_18 unithd 5520 59840 FS DO 1412 BY 1 STEP 460 0 ;

```

According to floorplan def

3. Load generated floorplan def in magic tool and explore the floorplan.

Commands to load floorplan def in magic in another terminal

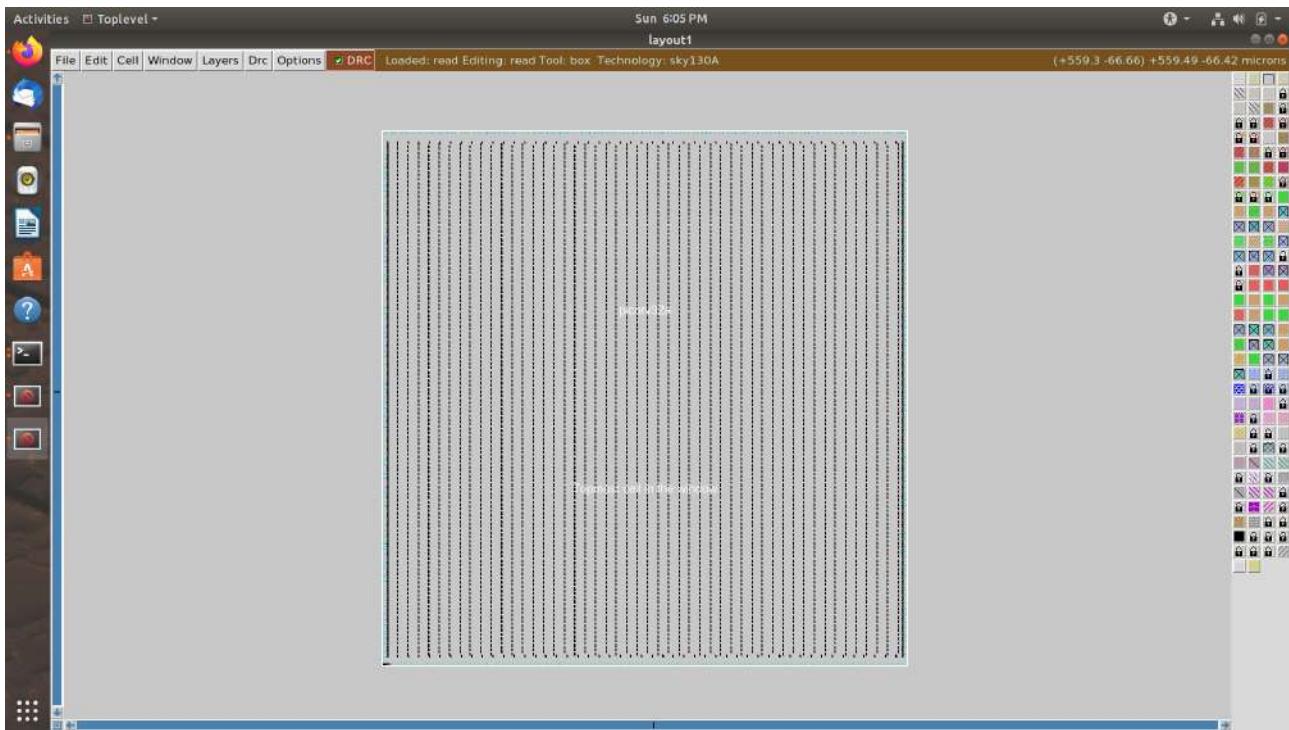
```
# Change directory to path containing generated floorplan def
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
17-03_12-06/results/floorplan/
```

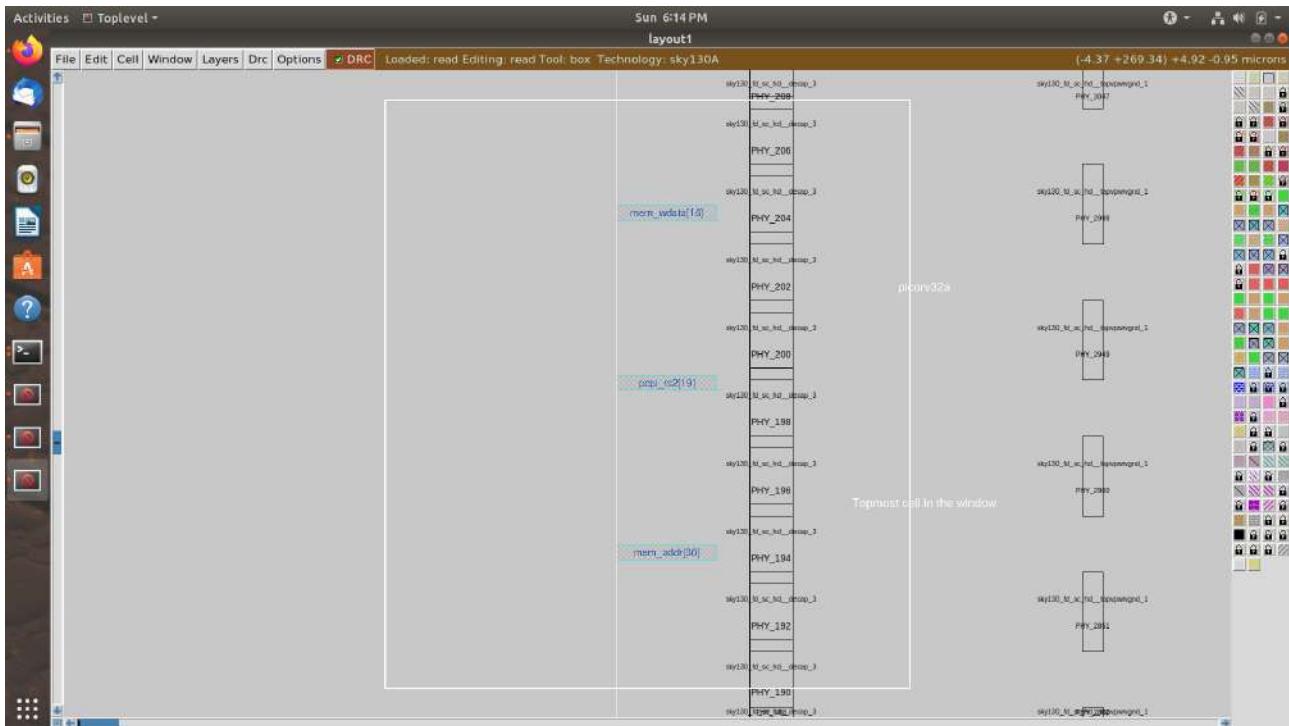
```
# Command to load the floorplan def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.floorplan.def &
```

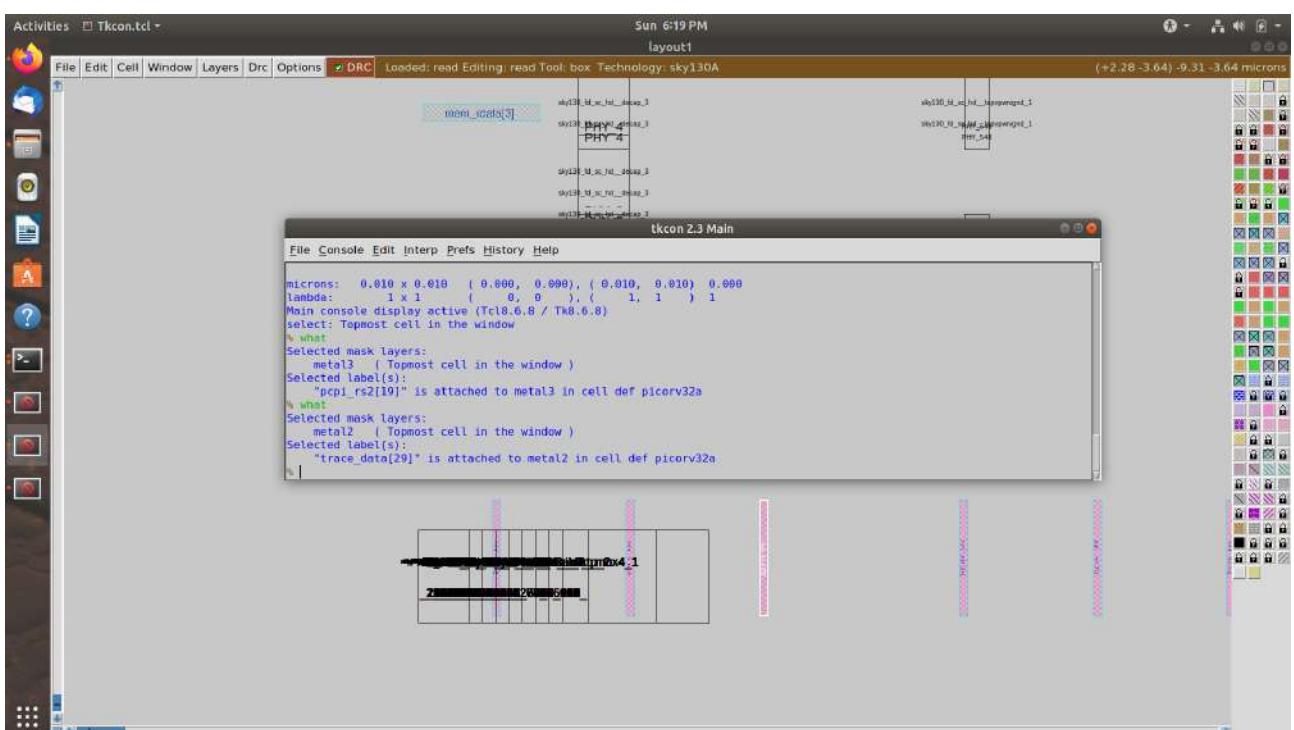
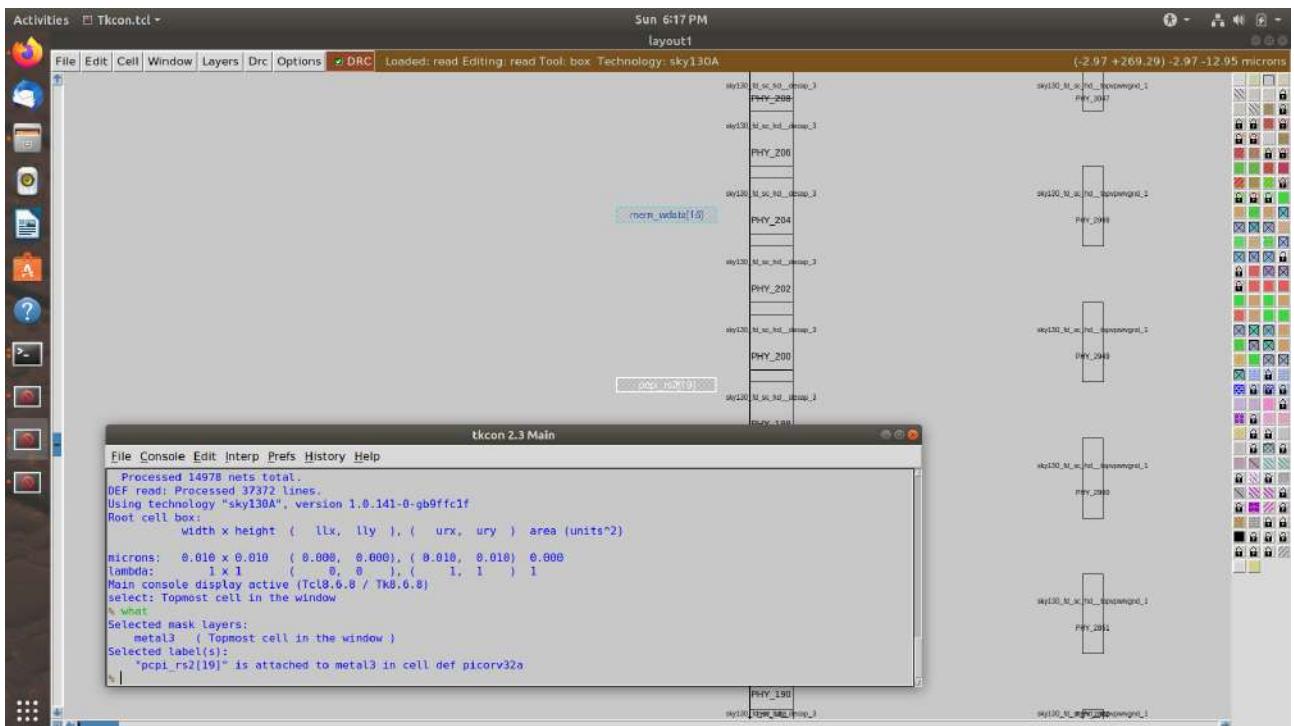
Screenshots of floorplan def in magic



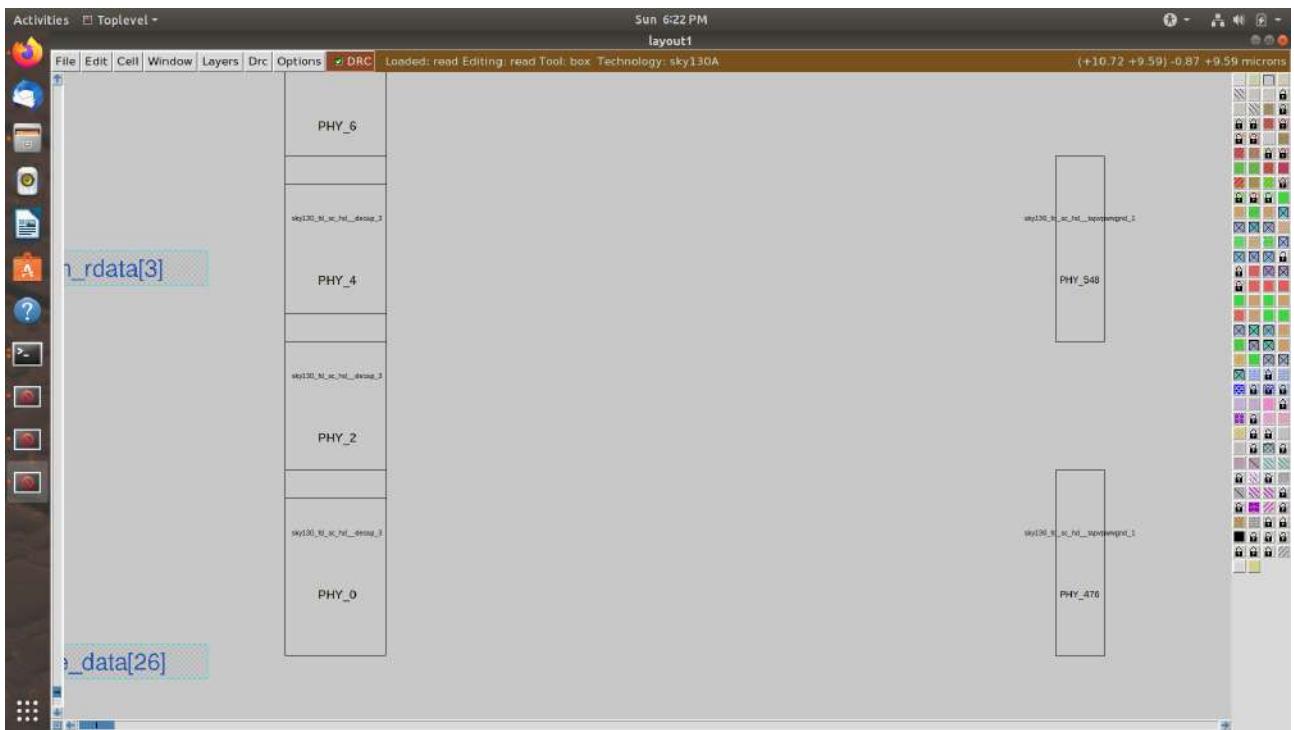
Equidistant placement of ports



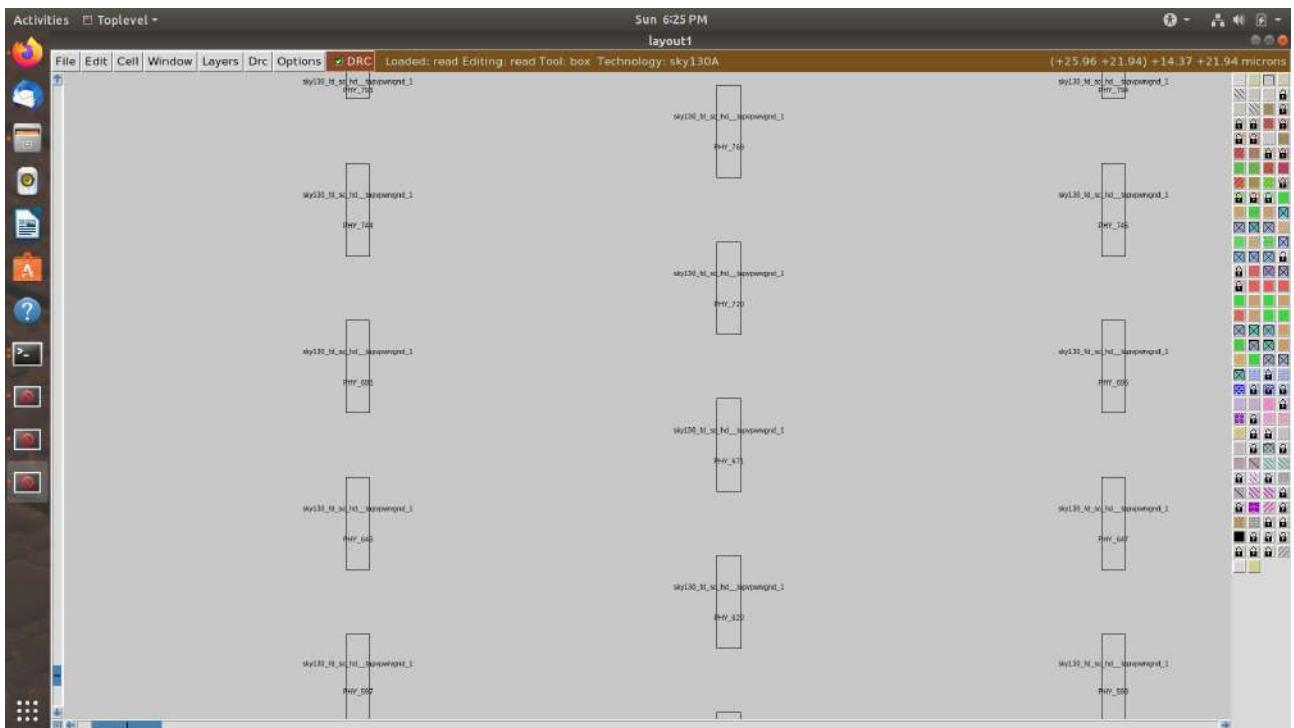
Port layer as set through config.tcl



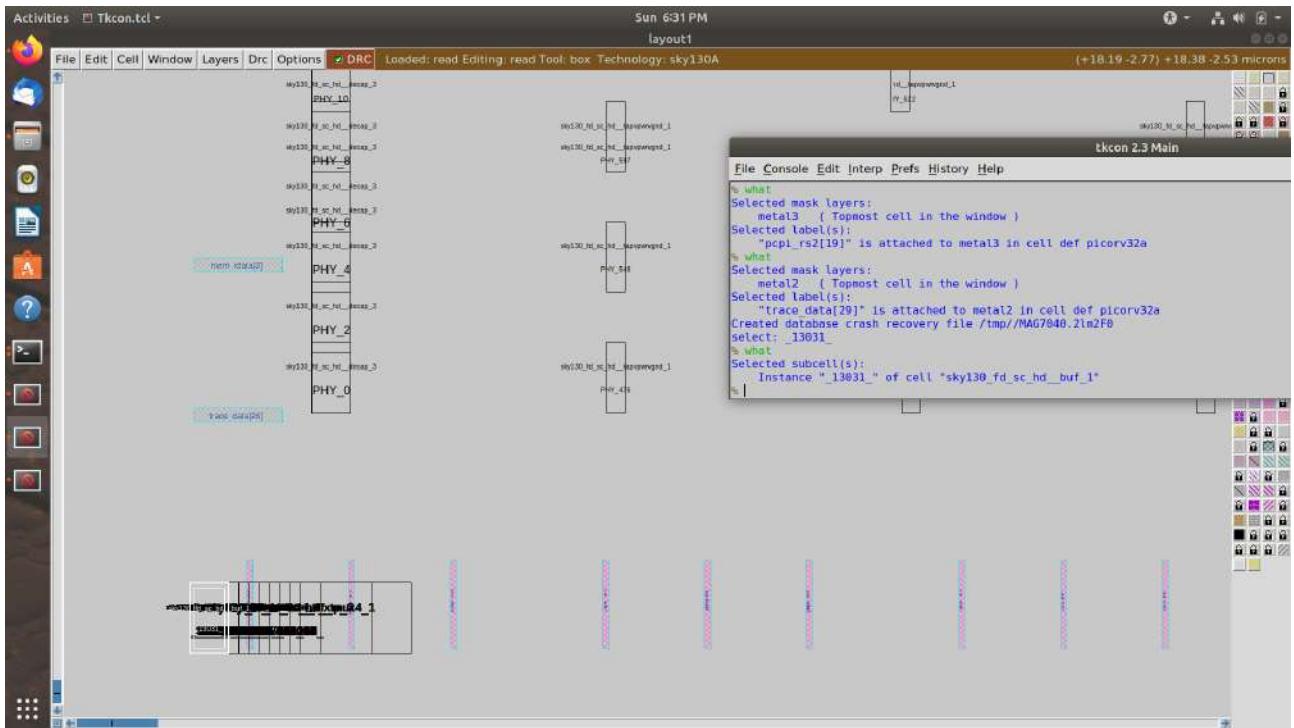
Decap Cells and Tap Cells



Diagonally equidistant Tap cells



Unplaced standard cells at the origin



4. Run 'picorv32a' design congestion aware placement using OpenLANE flow and generate necessary outputs.

Command to run placement

```
# Congestion aware placement by default
```

```
run_placement
```

Screenshots of placement run

```
Activities Terminal - Sun 10:44 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
er stripe. Moving to closest stripe at (567.000um, 103.880um).
[WARNING PSM-0030] Vsrc location at (565.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 257.060um).
[WARNING PSM-0030] Vsrc location at (5.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (145.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
[WARNING PSM-0030] Vsrc location at (425.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 563.420um).
[INFO PSM-0031] Number of nodes on net VGND = 19223.
[INFO PSM-0037] G matrix created sucessfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/floorplan/picorv32a.floorplan.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/floorplan/7-pdn.def
1
::: % run_placement
```

```
Activities Terminal - Sun 10:46 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
legalized HPWL      779196.5 u
delta HPWL          2 %

[INFO DPL-0020] Mirrored 6193 instances
[INFO DPL-0021] HPWL before      779196.5 u
[INFO DPL-0022] HPWL after       766080.0 u
[INFO DPL-0023] HPWL delta      -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/placement/8-resizer.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 12
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
::: %
```

5. Load generated placement def in magic tool and explore the placement.

Commands to load placement def in magic in another terminal

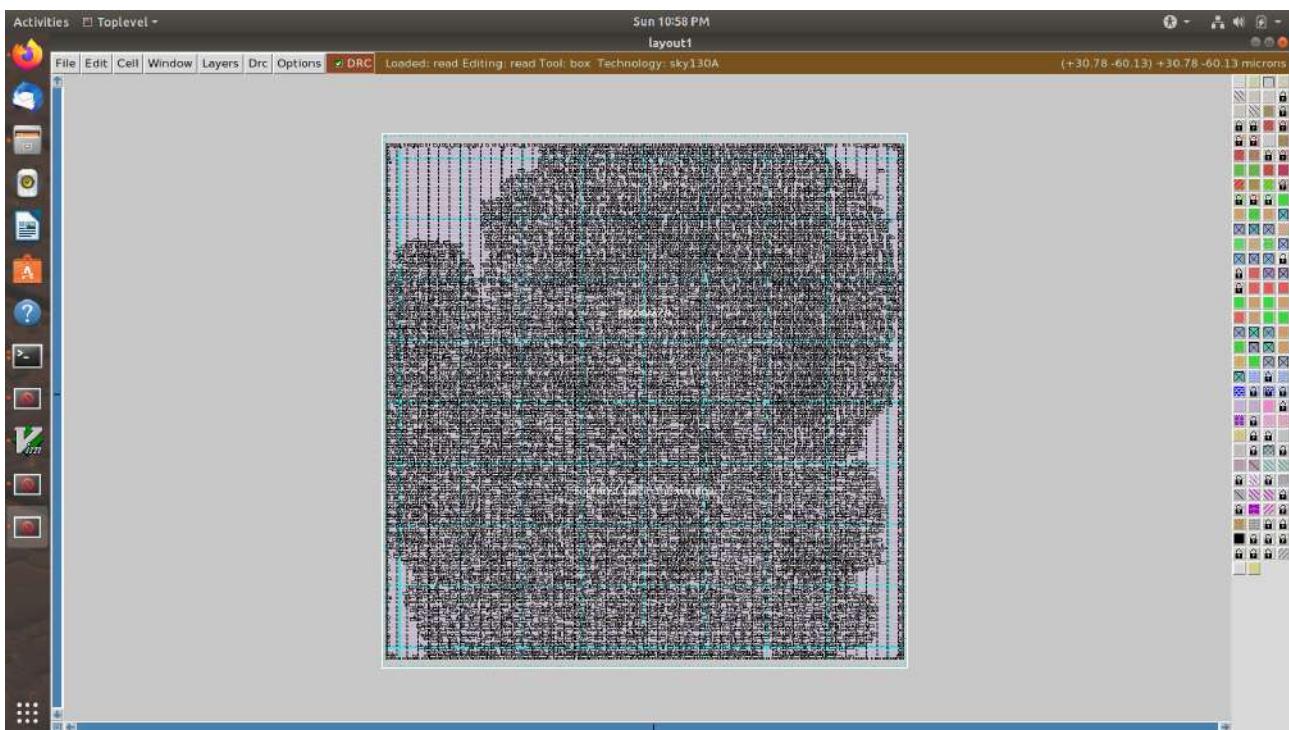
```
# Change directory to path containing generated placement def
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/  
17-03_12-06/results/placement/
```

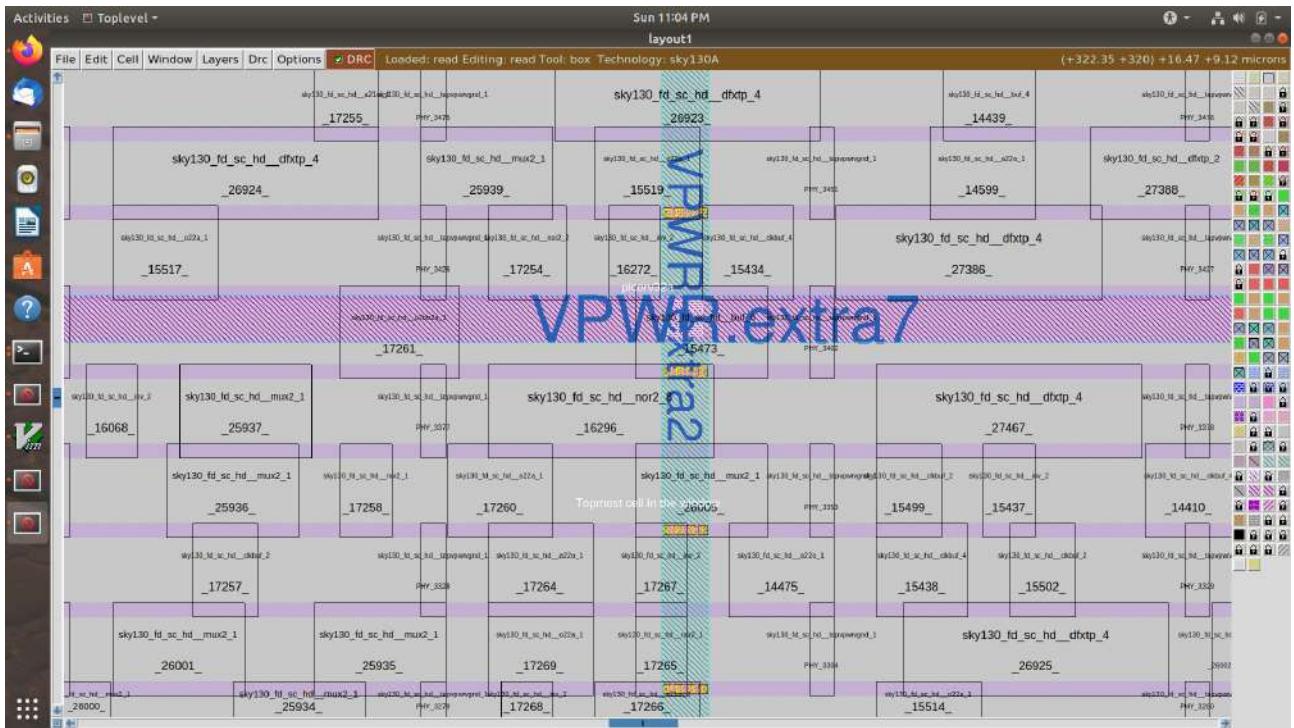
Command to load the placement def in magic tool

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def  
&
```

Screenshots of floorplan def in magic



Standard cells legally placed



Commands to exit from current run

```
# Exit from OpenLANE flow
```

```
exit
```

```
# Exit from OpenLANE flow docker sub-system
```

```
exit
```

Section 3 - Design library cell using Magic Layout and ngspice characterization (18/03/2024 - 21/03/2024)

Theory

Implementation

- **Section 3 tasks:-**
- 6. Clone custom inverter standard cell design from github repository: [Standard cell design and characterization using OpenLANE flow.](#)
- 7. Load the custom inverter layout in magic and explore.
- 8. Spice extraction of inverter in magic.
- 9. Editing the spice model file for analysis through simulation.
- 10. Post-layout ngspice simulations.
- 11. Find problem in the DRC section of the old magic tech file for the skywater process and fix them.
- **Section 3 - Tasks 1 to 5 files, reports and logs can be found in the following folder:**

[Section 3 - Tasks 1 to 5 \(vsdstdcelldesign\)](#)

- **Section 3 - Task 6 files, reports and logs can be found in the following folder:**

[Section 3 - Task 6 \(drc_tests\)](#)

1. Clone custom inverter standard cell design from github repository

```
# Change directory to openlane
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# Clone the repository with custom inverter design
```

```
git clone https://github.com/nickson-jose/vsdstdcelldesign
```

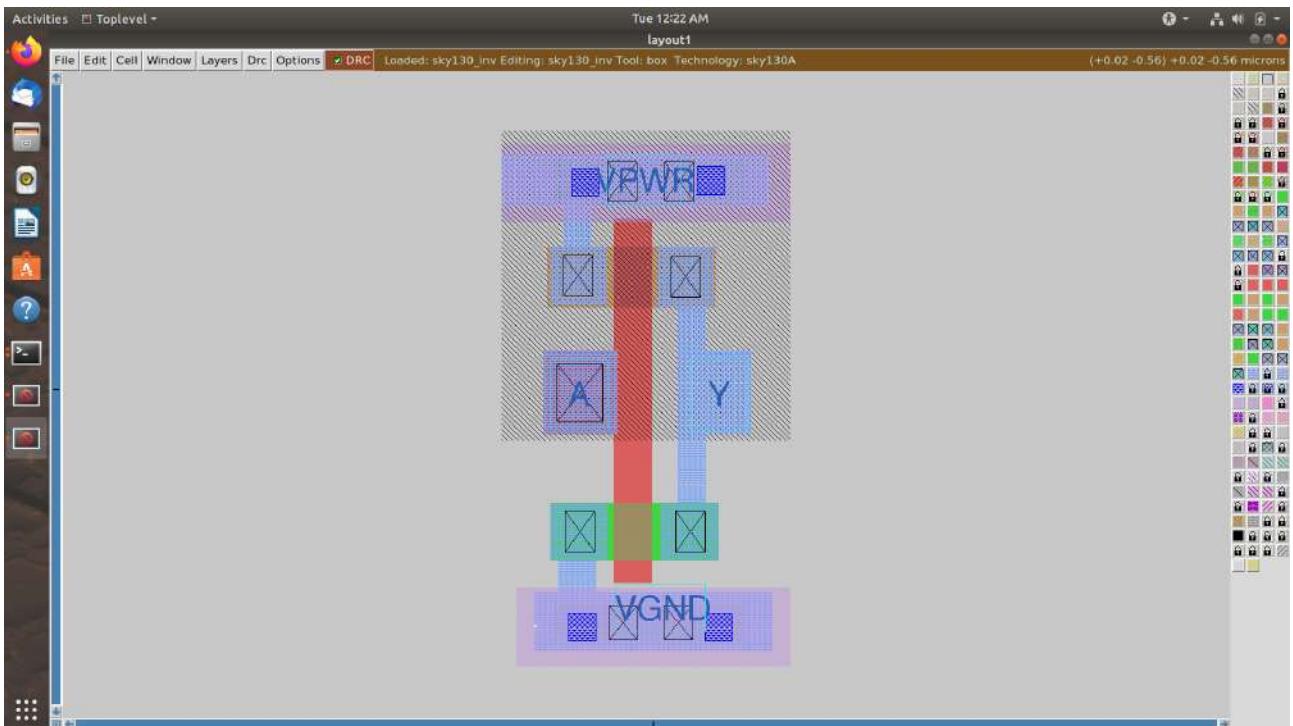
```
# Change into repository directory  
  
cd vsdstdcelldesign  
  
# Copy magic tech file to the repo directory for easy access  
  
cp /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/  
magic/sky130A.tech .  
  
# Check contents whether everything is present  
  
ls  
  
# Command to open custom inverter layout in magic  
  
magic -T sky130A.tech sky130_inv.mag &
```

Screenshot of commands run

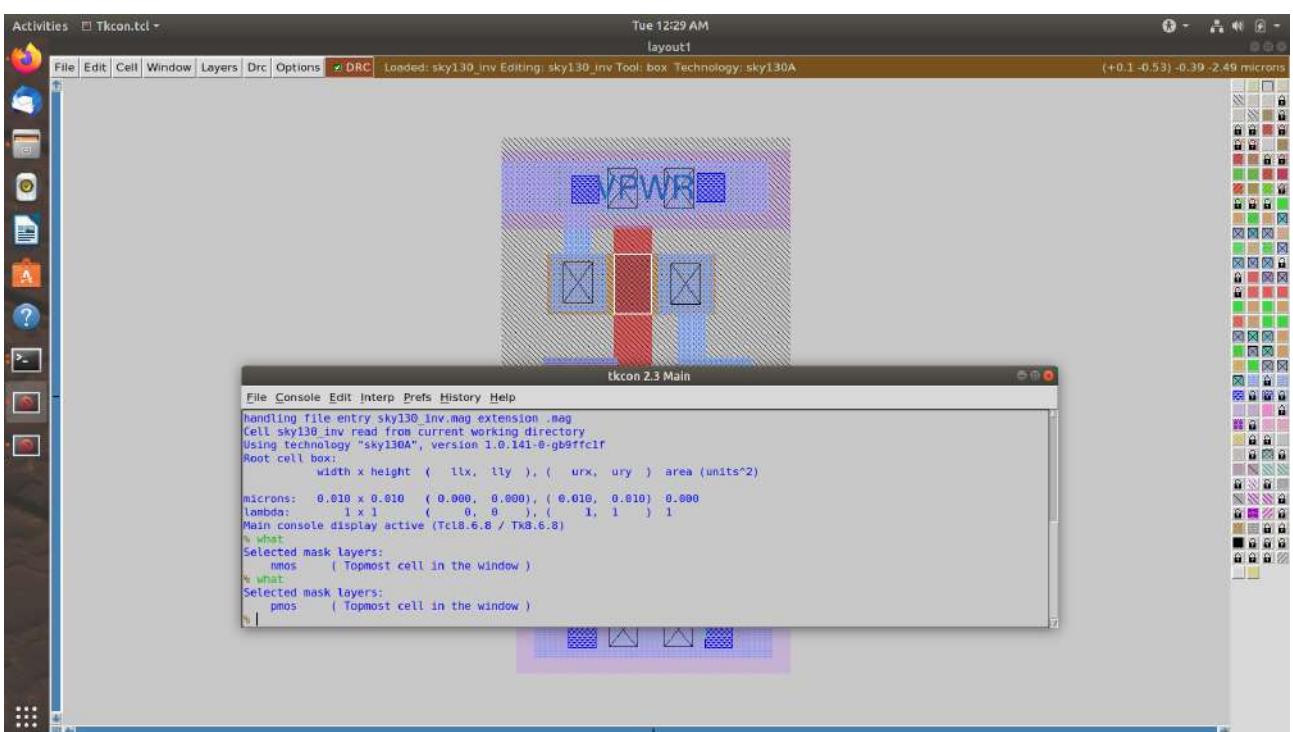
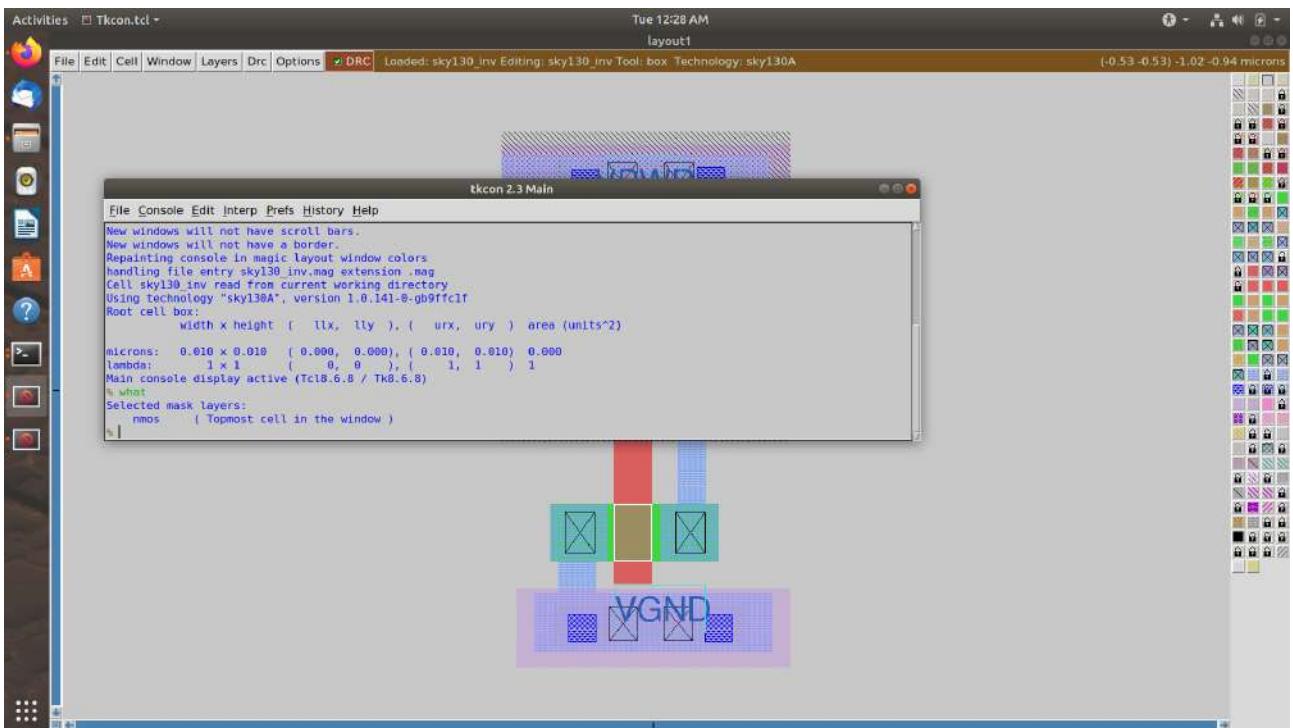
```
Activities Terminal - Tue 12:22 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ git clone https://github.com/nickson-jose/vsdstdcelldesign
Cloning into 'vsdstdcelldesign'...
remote: Enumerating objects: 492, done.
remote: Counting objects: 100% (18/18), done.
remote: Compressing objects: 100% (18/18), done.
remote: Total 492 (delta 7), reused 0 (delta 0), pack-reused 474
Receiving objects: 100% (492/492), 24.08 MiB | 480.00 KiB/s, done.
Resolving deltas: 100% (210/210), done.
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd vsdstdcelldesign
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cp /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/magic/sky130A.tech .
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls
extras Images libs LICENSE README.md sky130A.tech sky130_inv.mag
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ magic -T sky130A.tech sky130_inv.mag &
[1] 4495
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```

2. Load the custom inverter layout in magic and explore.

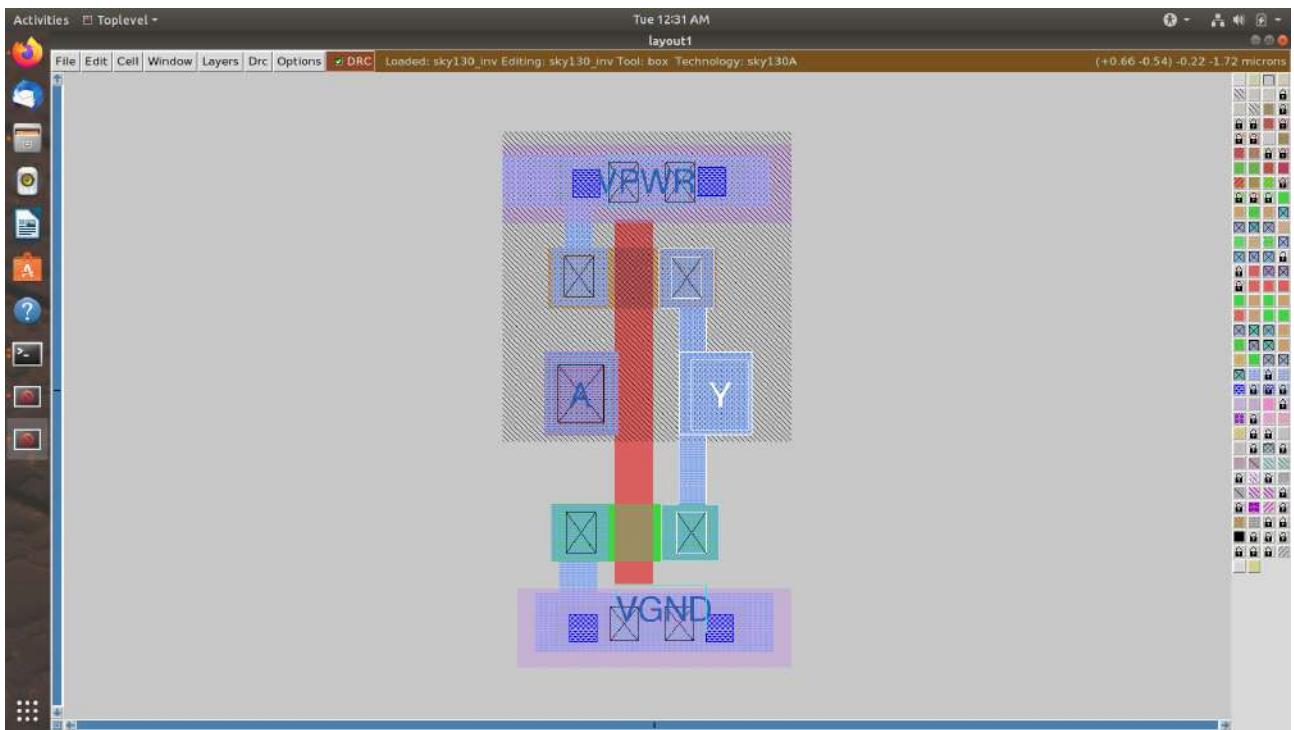
Screenshot of custom inverter layout in magic



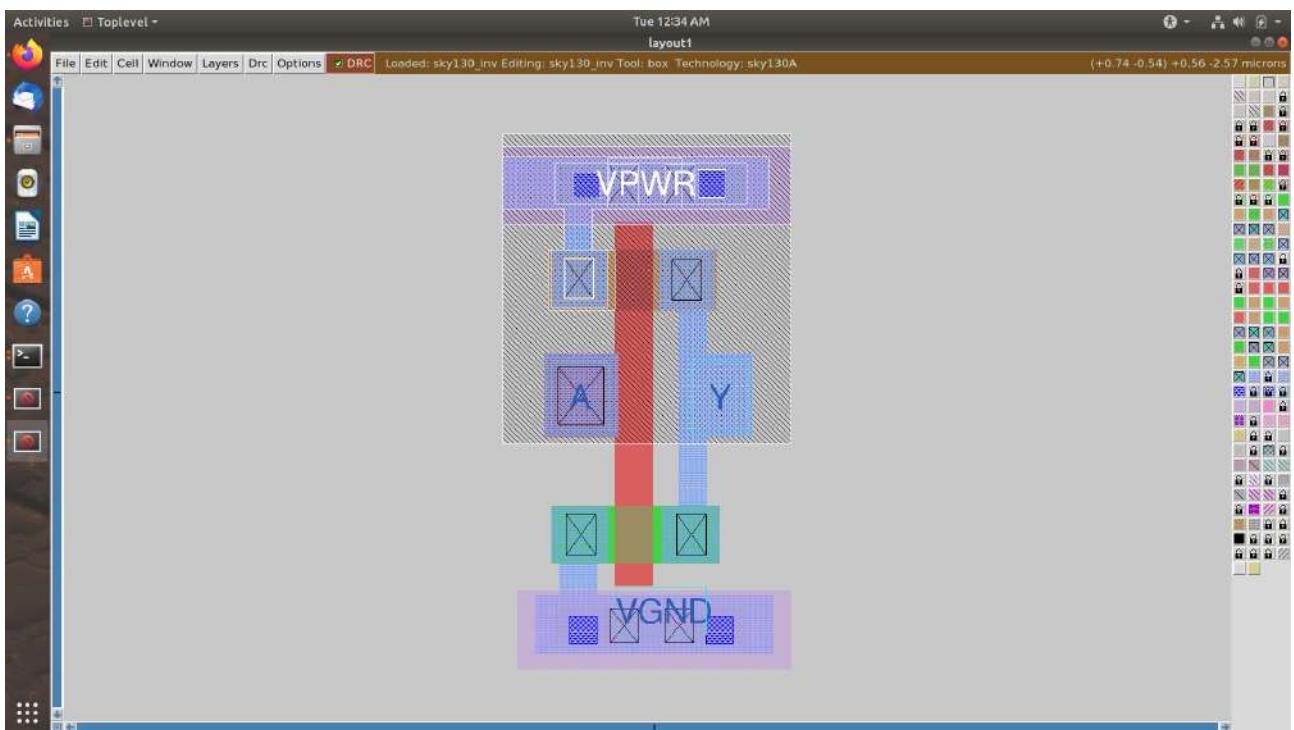
NMOS and PMOS identified



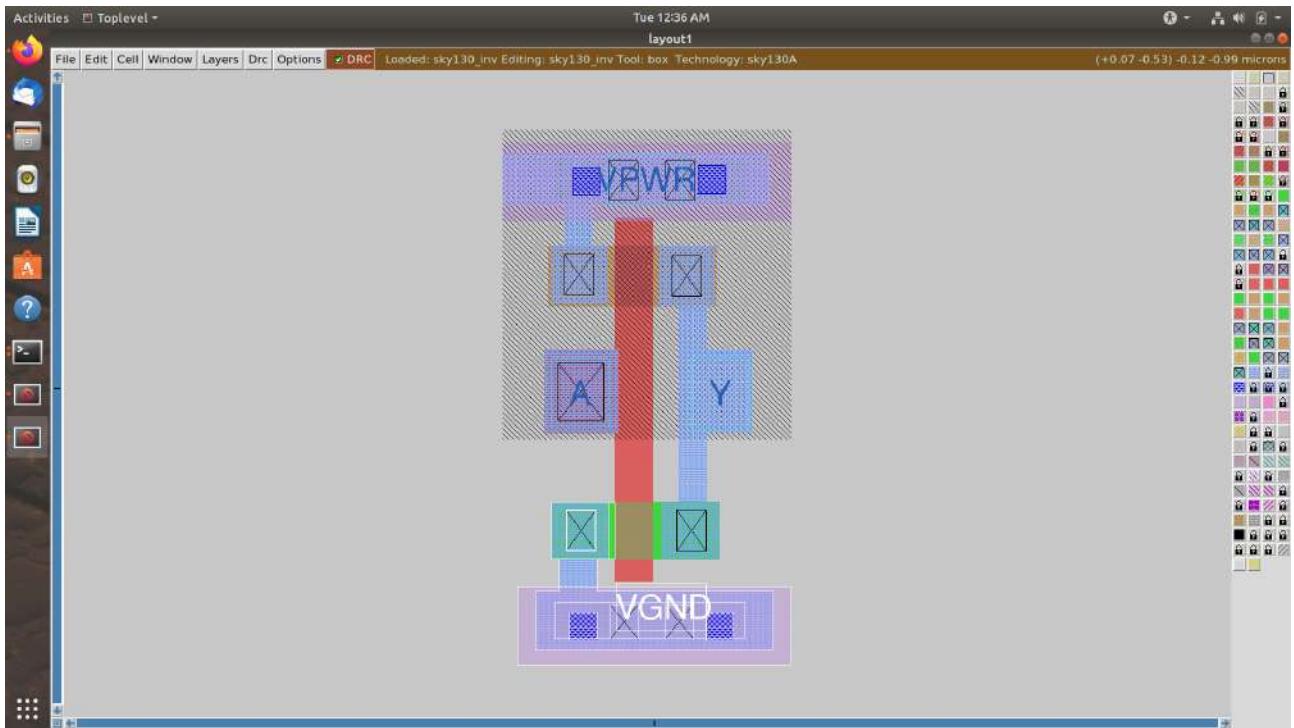
Output Y connectivity to PMOS and NMOS drain verified



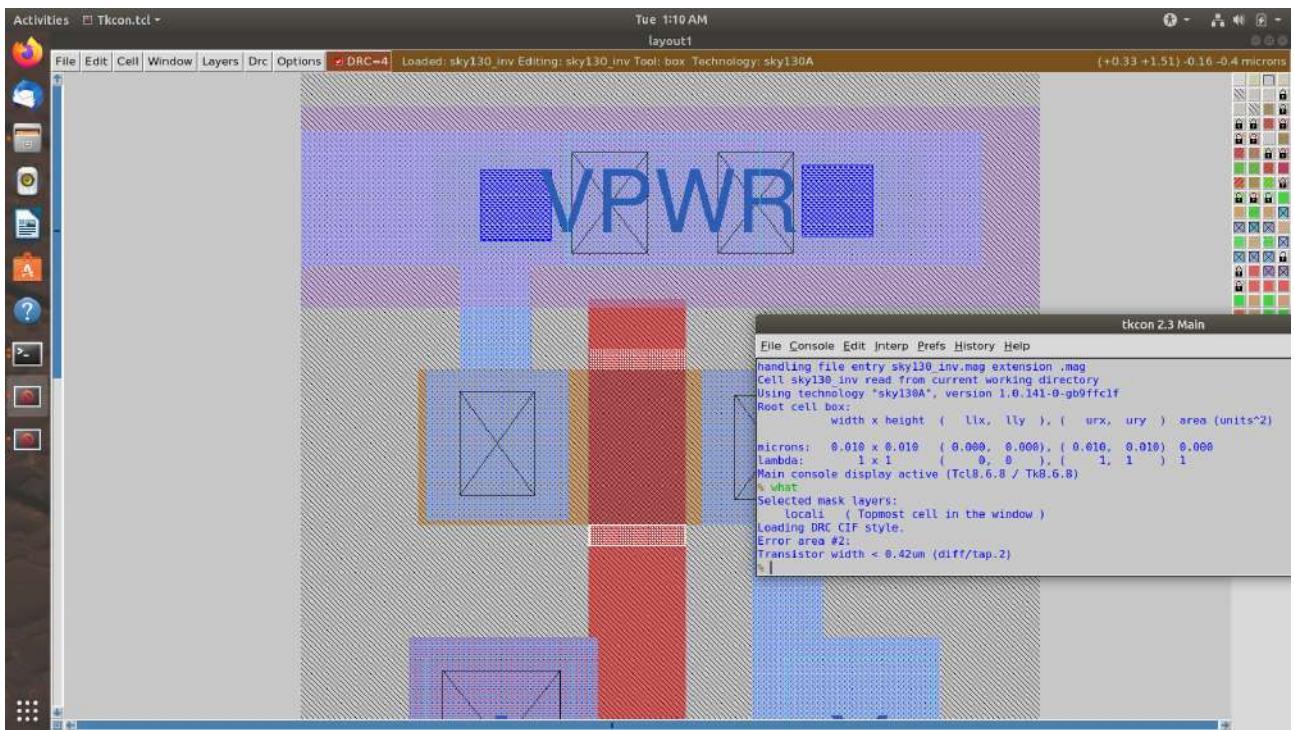
PMOS source connectivity to VDD (here VPWR) verified



NMOS source connectivity to VSS (here VGND) verified



Deleting necessary layout part to see DRC error



3. Spice extraction of inverter in magic.

Commands for spice extraction of the custom inverter layout to be used in tkcon window of magic

```
# Check current directory
```

pwd

```
# Extraction command to extract to .ext format
```

extract all

Before converting ext to spice this command enable the parasitic extraction also

`ext2splice cthresh 0 rthresh 0`

Converting to ext to spice

ext2spice

Screenshot of tkcon window after running above commands

```
Activities □ Tkcon.tcl - Tue 1:24 AM
tkcon 2.3 Main

File Console Edit Interp Prefs History Help
loading history file ... 16 events added
Use openmwrapper to create a new GUI-based layout window
Use closerwrapper to remove a new GUI-based layout window

Magic 8.3 revision 400 - Compiled on Mon May 22 20:58:24 IST 2023.
Starting magic under Tcl Interpreter
Using Tk console window
Using TrueColor, VisualID 0x21 depth 24
Input style sky130(): scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
    nmos obsactive mvobsactive obsl1l obsml obsm2 obsm3 obsm4 obsm5 obsnndl ubm fillblock comment obscomment res8p35 res8p69 reslp41 res2p85 res5p73
Processing system .magicrc file
New windows will not have a title caption.
New windows will not have scroll bars.
New windows will not have a border.
Repainting console in magic layout window colors
handling file entry sky130_inv.mag extension .mag
Cell sky130_inv read from current working directory
Using technology "sky130A", version 1.0.141-0-gb9fffc1f
Root cell box:
    width x height ( llx, lly ),( urx, ury ) area (units^2)
microns: 0.010 x 0.010 ( 0.000, 0.000 ),( 0.010, 0.010 ) 0.000
lambda: 1 x 1 ( 0, 0 ),( 1, 1 ) 1
Main console display active (Tcl8.6.8 / Tk8.6.8)
    ped
/home/vsdsuser/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
    extract all
Extracting sky130_inv into sky130_inv.ext:
% ext2spice cthresh 0 rthresh 0
% ext2spice
ext2spice finished.
%
```

Screenshot of created spice file

Activities ▾ GVim -

Tue 1:27 AM

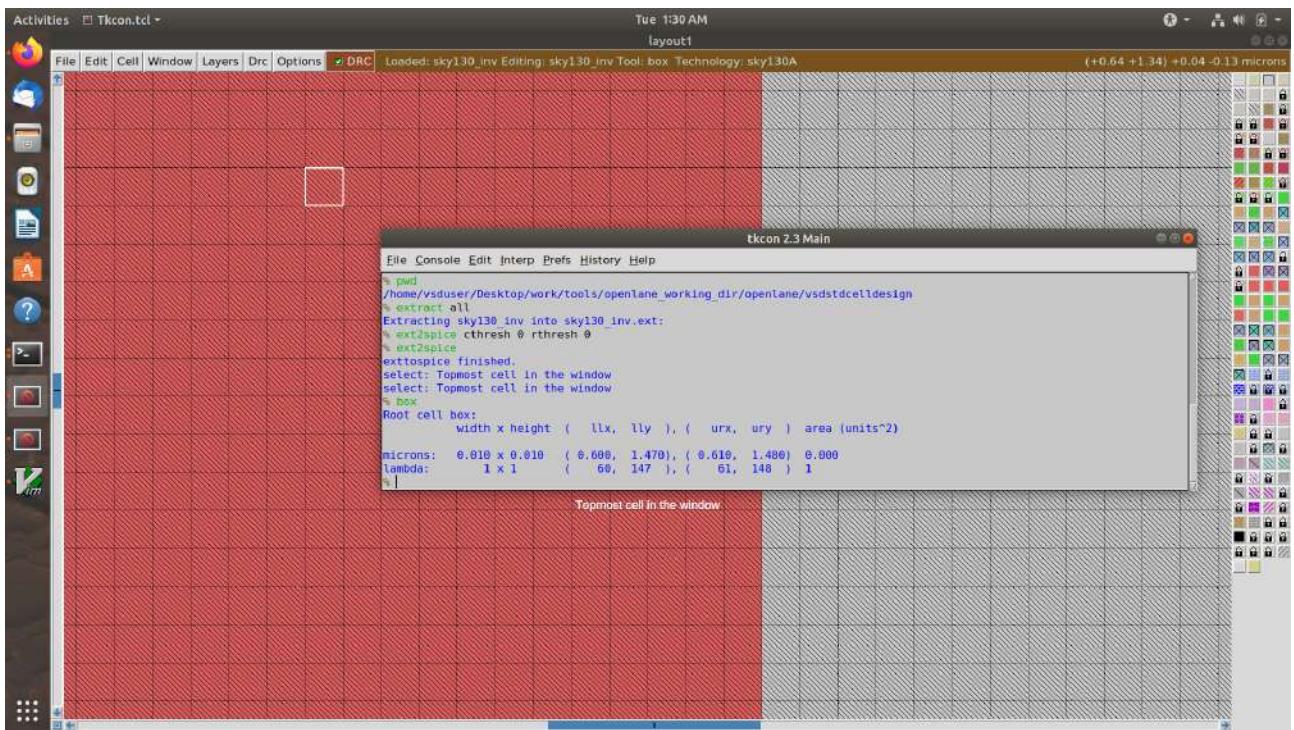
sky130_inv.spice (~/Desktop/work/tools/op...ing_dlr/openlane/vsdstdcelldesign) - GVIM

File Edit Tools Syntax Buffers Window Help

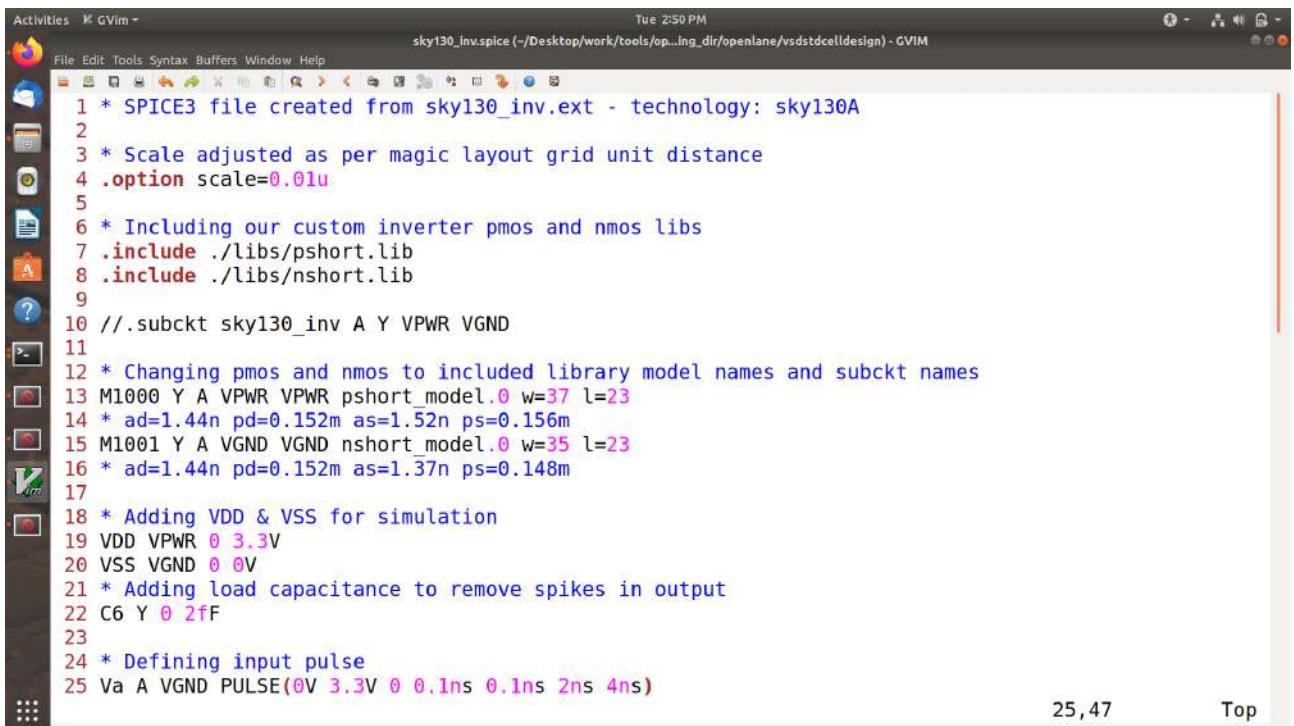
```
1 * SPICE3 file created from sky130_inv.ext - technology: sky130A
2
3 .option scale=10m
4
5 .subckt sky130_inv A Y VPWR VGND
6 X0 Y A VGND VGND sky130_fd_pr_nfet_01v8 ad=1.44n pd=0.152m as=1.37n ps=0.148m w=35 l=23
7 X1 Y A VPWR VPWR sky130_fd_pr_pfet_01v8 ad=1.44n pd=0.152m as=1.52n ps=0.156m w=37 l=23
8 C0 A VPWR 0.0774f
9 C1 Y VPWR 0.117f
10 C2 A Y 0.0754f
11 C3 Y VGND 0.279f
12 C4 A VGND 0.45f
13 C5 VPWR VGND 0.781f
14 .ends
```

4. Editing the spice model file for analysis through simulation.

Measuring unit distance in layout grid

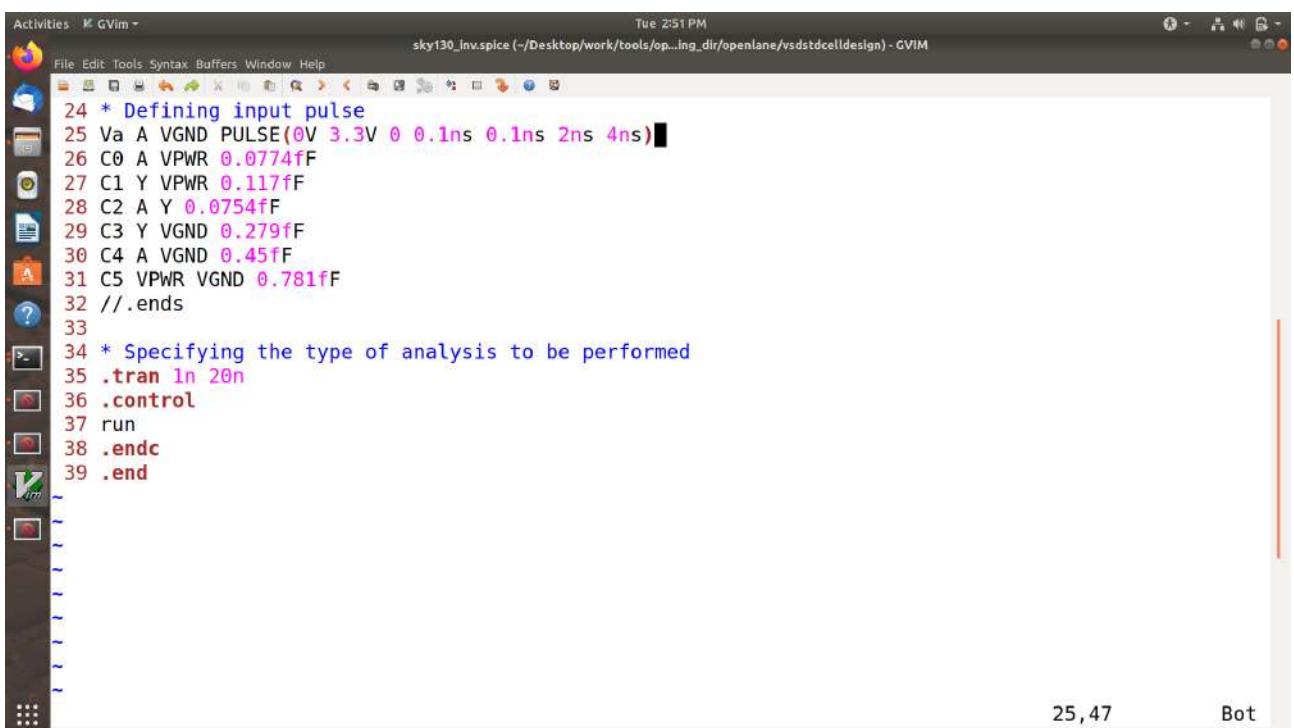


Final edited spice file ready for ngspice simulation



```
Activities  M GVim - Tue 2:50 PM
sky130_inv.spice (~/Desktop/work/tools/op...ng_dir/openlane/vsdstdcelldesign) - GVIM
File Edit Tools Syntax Buffers Window Help
1 * SPICE3 file created from sky130_inv.ext - technology: sky130A
2
3 * Scale adjusted as per magic layout grid unit distance
4 .option scale=0.01u
5
6 * Including our custom inverter pmos and nmos libs
7 .include ./libs/pshort.lib
8 .include ./libs/nshort.lib
9
10 // .subckt sky130_inv A Y VPWR VGND
11
12 * Changing pmos and nmos to included library model names and subckt names
13 M1000 Y A VPWR VPWR pshort_model.0 w=37 l=23
14 * ad=1.44n pd=0.152m as=1.52n ps=0.156m
15 M1001 Y A VGND VGND nshort_model.0 w=35 l=23
16 * ad=1.44n pd=0.152m as=1.37n ps=0.148m
17
18 * Adding VDD & VSS for simulation
19 VDD VPWR 0 3.3V
20 VSS VGND 0 0V
21 * Adding load capacitance to remove spikes in output
22 C6 Y 0 2fF
23
24 * Defining input pulse
25 Va A VGND PULSE(0V 3.3V 0 0.1ns 0.1ns 2ns 4ns)
26
27
28
29
30
31
32 // .ends
33
34 * Specifying the type of analysis to be performed
35 .tran 1n 20n
36 .control
37 run
38 .endc
39 .end
```

25,47 Top



```
Activities  M GVim - Tue 2:51 PM
sky130_inv.spice (~/Desktop/work/tools/op...ng_dir/openlane/vsdstdcelldesign) - GVIM
File Edit Tools Syntax Buffers Window Help
24 * Defining input pulse
25 Va A VGND PULSE(0V 3.3V 0 0.1ns 0.1ns 2ns 4ns)■
26 C0 A VPWR 0.0774fF
27 C1 Y VPWR 0.117fF
28 C2 A Y 0.0754fF
29 C3 Y VGND 0.279fF
30 C4 A VGND 0.45fF
31 C5 VPWR VGND 0.781fF
32 // .ends
33
34 * Specifying the type of analysis to be performed
35 .tran 1n 20n
36 .control
37 run
38 .endc
39 .end
```

25,47 Bot

5. Post-layout ngspice simulations.

Commands for ngspice simulation

Command to directly load spice file for simulation to ngspice

ngspice sky130_inv.spice

```
# Now that we have entered ngspice with the simulation spice file loaded we just have to  
load the plot
```

```
plot y vs time a
```

Screenshots of ngspice run

```

Activities Terminal - vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ngspice sky130_inv.spice
*****
** ngspice-27 : Circuit level simulation program
** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California.
** Please get your ngspice manual from http://ngspice.sourceforge.net/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Tue Dec 26 17:10:20 UTC 2017
*****
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node Voltage
-----
y 3.3
a 0
vpwr 3.3
vgnd 0
va#branch 0

```

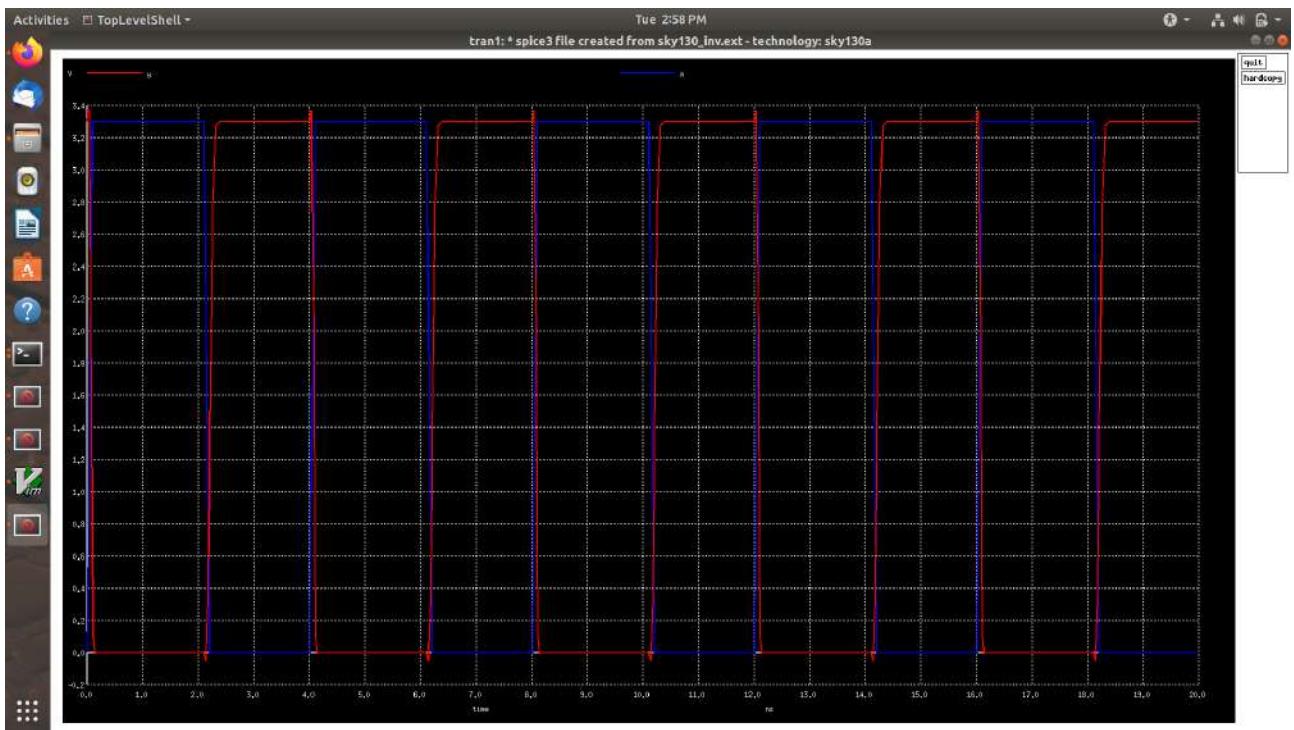
```

Activities TopLevelShell - vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ 
*****
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node Voltage
-----
y 3.3
a 0
vpwr 3.3
vgnd 0
va#branch 0
vss#branch 3.32351e-12
vdd#branch -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
::: ngspice 1 -> 

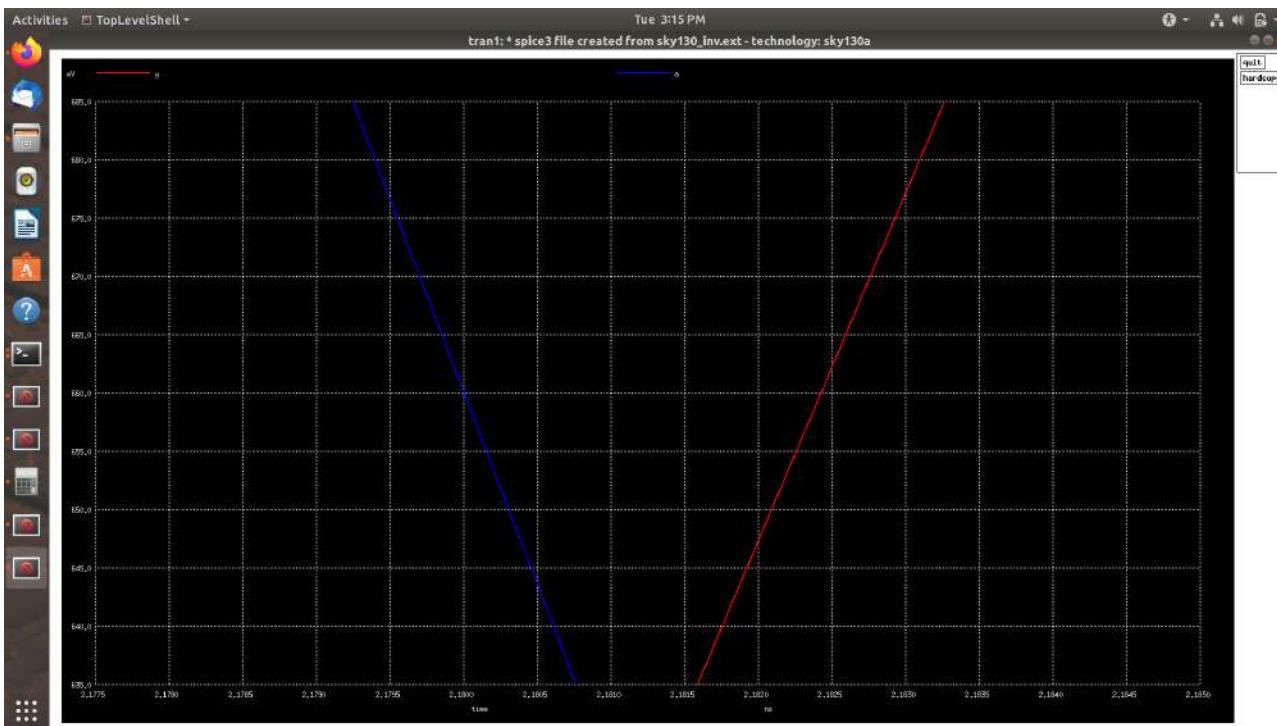
```

Screenshot of generated plot



Rise transition time calculation

20% Screenshots



Activities Terminal -

Tue 3:20 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign

```

File Edit View Search Terminal Help
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a

Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

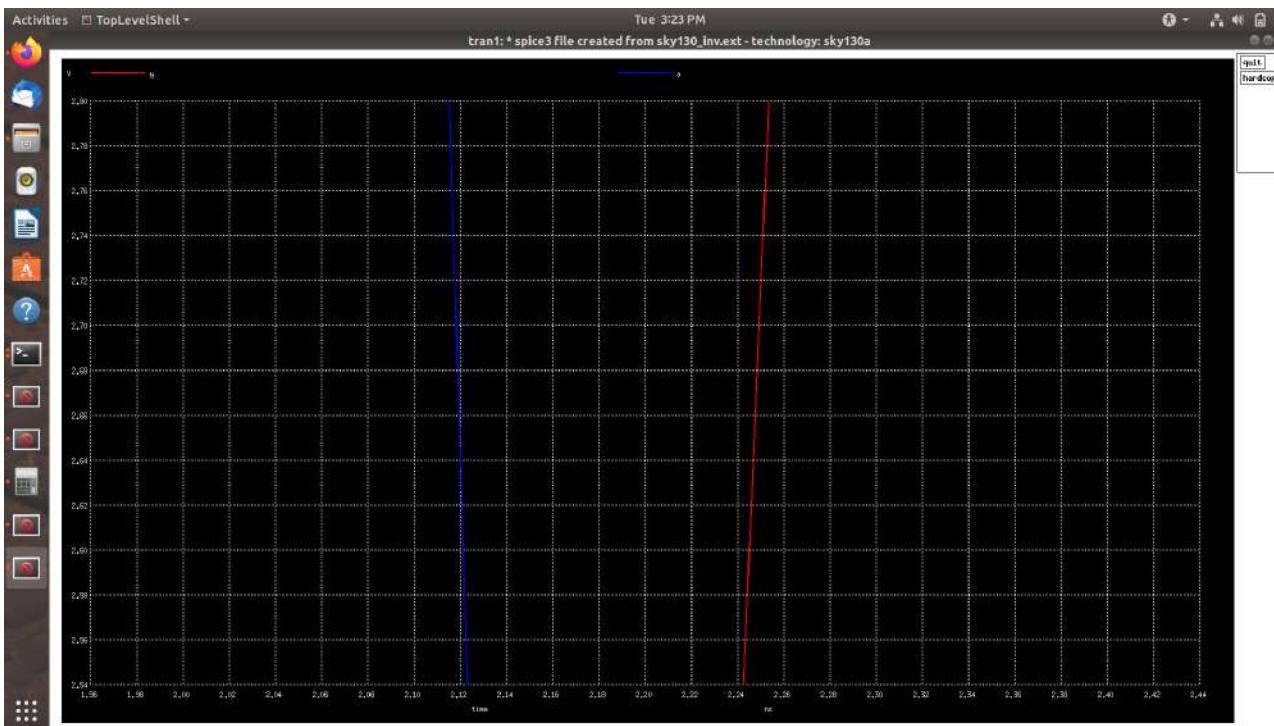
Warning: va: no DC value, transient time 0 value used

Initial Transient Solution
-----
Node          Voltage
---- 
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043

```

80% Screenshots



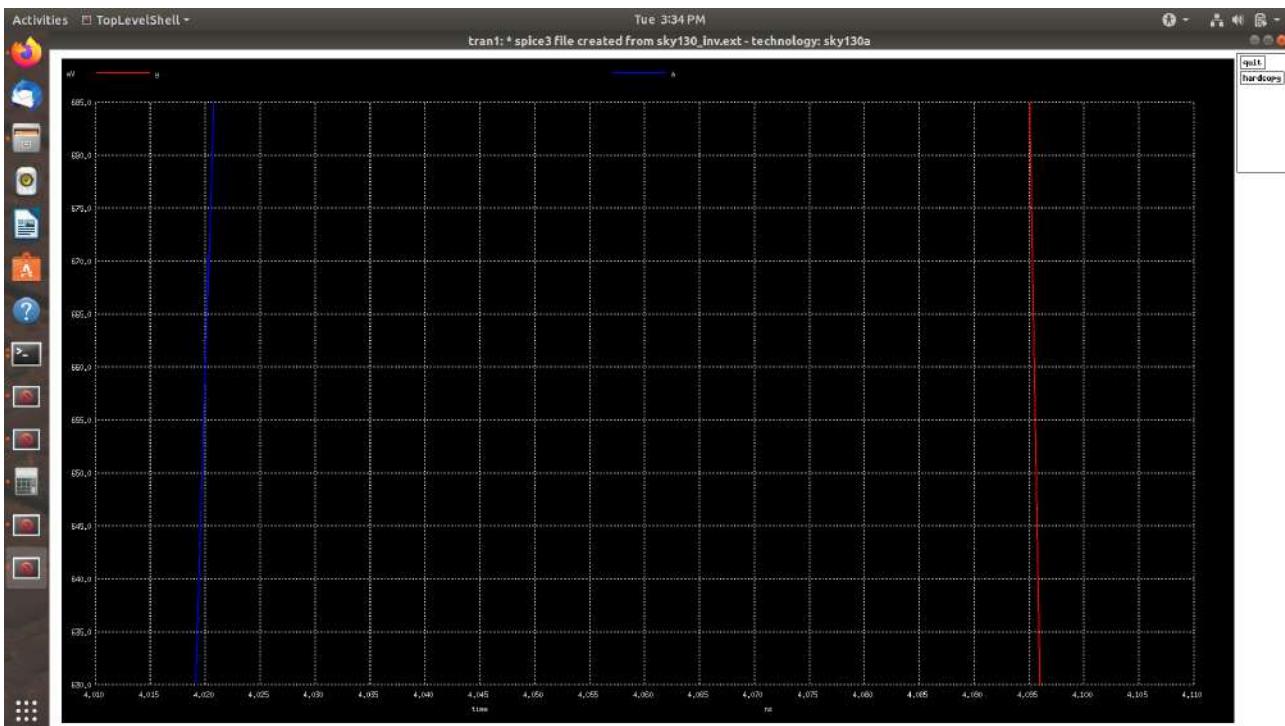
```
Activities Terminal - Tue 3:24 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign

File Edit View Search Terminal Help
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node Voltage
-----
y 3.3
a 0
vpwr 3.3
vgnd 0
va#branch 0
vss#branch 3.32351e-12
vdd#branch -3.32355e-12

No. of Data Rows : 160
ngspice l -> plot y vs time a
ngspice l ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
```

Fall transition time calculation

20% Screenshots



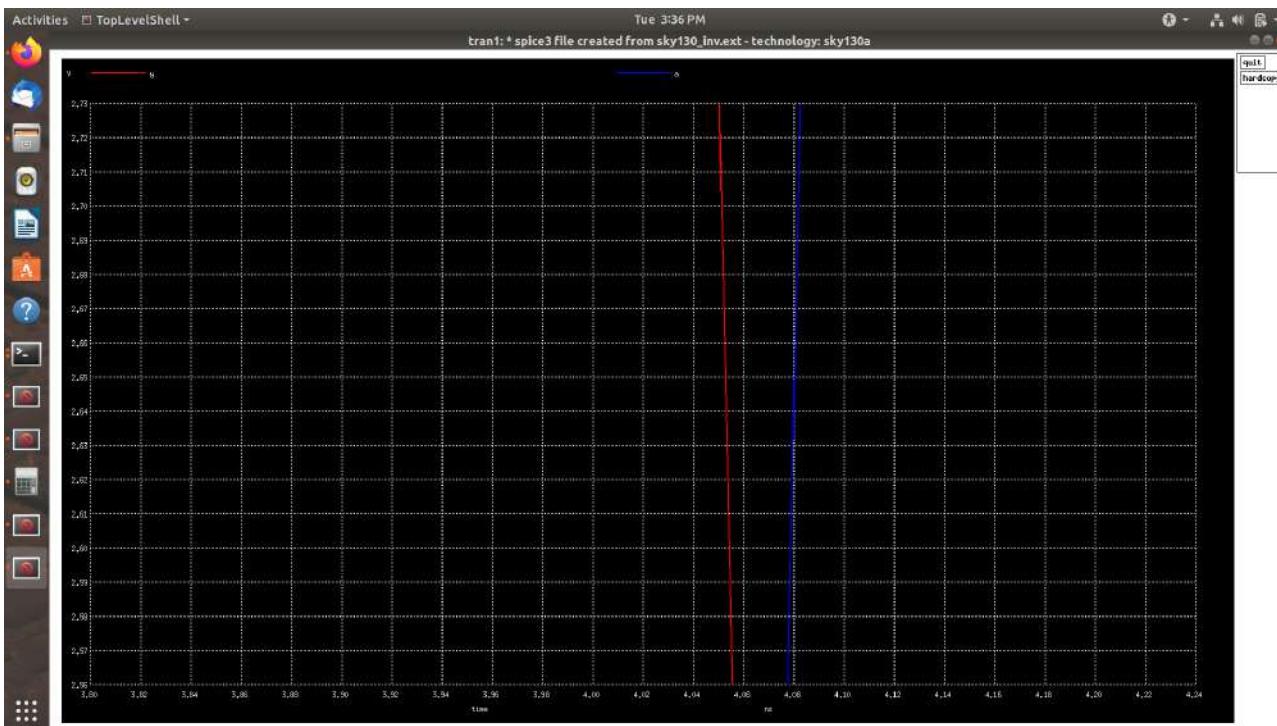
Activities Terminal -

Tue 3:34 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node          Voltage
-----
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
x0 = 4.09555e-09, y0 = 0.660127
```

80% Screenshots



Activities Terminal -

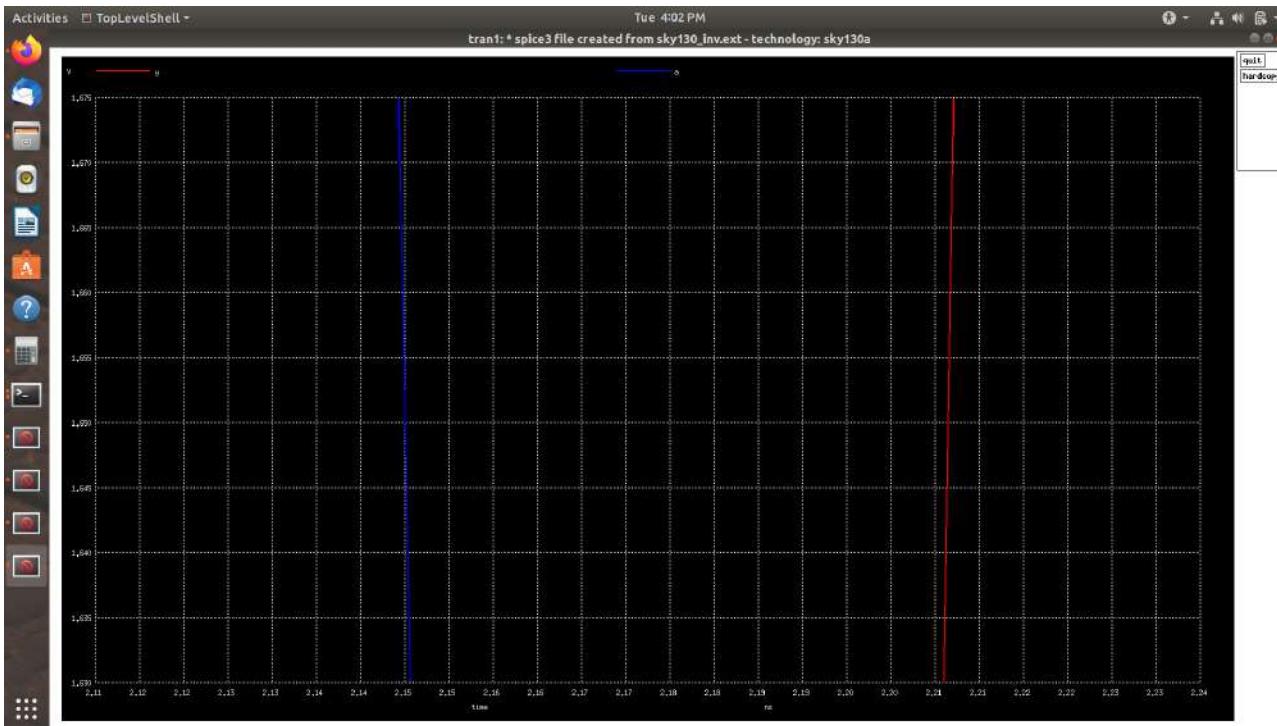
Tue 3:36 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```
Initial Transient Solution
-----
Node          Voltage
-----
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
x0 = 4.09555e-09, y0 = 0.660127
x0 = 4.0536e-09, y0 = 2.64
```

Rise Cell Delay Calculation

50% Screenshots



Activities Terminal

Tue 4:03 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign

```

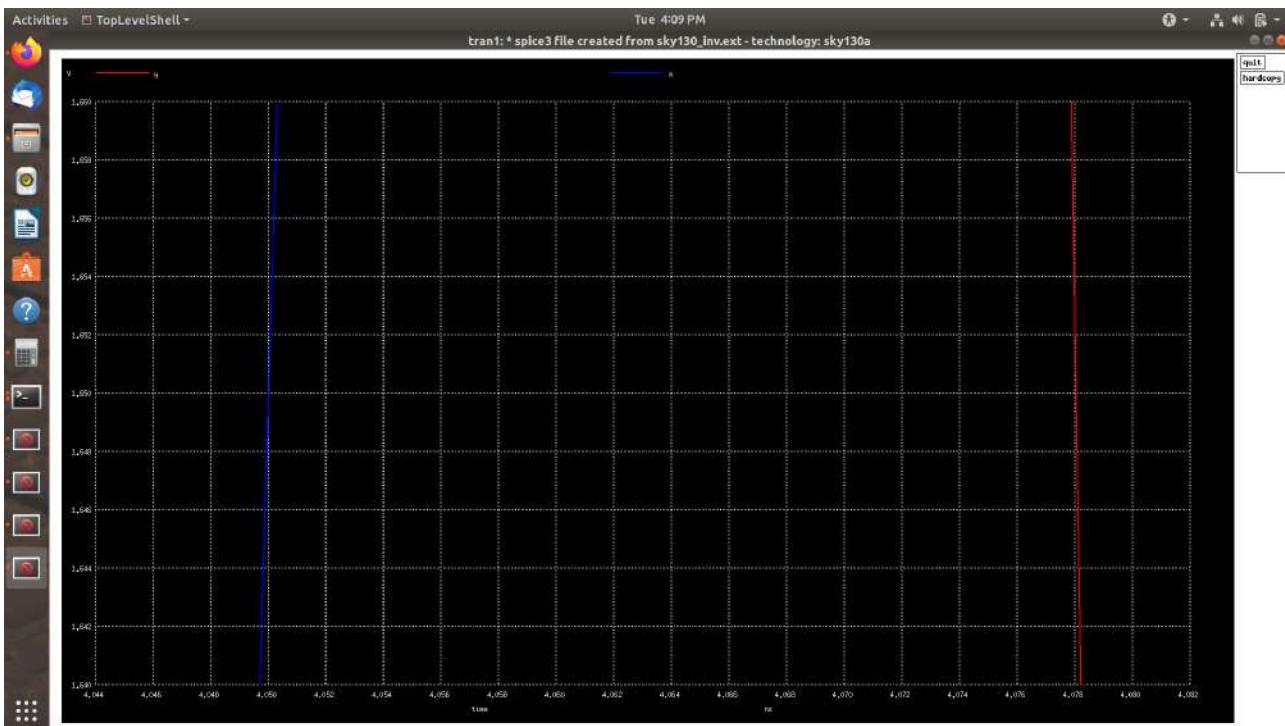
File Edit View Search Terminal Help
Node          Voltage
-----
y             3.3
a             0
vpwr          3.3
vgnd          0
va#branch     0
vss#branch    3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
x0 = 4.09555e-09, y0 = 0.660127
x0 = 4.0536e-09, y0 = 2.64
x0 = 2.21144e-09, y0 = 1.65
x0 = 2.15008e-09, y0 = 1.6501

```

Fall Cell Delay Calculation

50% Screenshots



Activities Terminal Tue 4:10 PM

vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```

File Edit View Search Terminal Help
vpwr          3.3
vgnd          0
va#branch     0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
> x0 = 2.24638e-09, y0 = 2.6403
> x0 = 4.09555e-09, y0 = 0.660127
> x0 = 4.0536e-09, y0 = 2.64
> x0 = 2.21144e-09, y0 = 1.65
> x0 = 2.15008e-09, y0 = 1.6501
> x0 = 4.07807e-09, y0 = 1.65005
> x0 = 4.05e-09, y0 = 1.65002

```

6. Find problem in the DRC section of the old magic tech file for the skywater process and fix them.

Link to Sky130 Periphery rules: <https://skywater-pdk.readthedocs.io/en/main/rules/periphery.html>

Commands to download and view the corrupted skywater process magic tech file and associated files to perform drc corrections

```
# Change to home directory
```

```
cd
```

```
# Command to download the lab files
```

```
wget http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
```

```
# Since lab file is compressed command to extract it
```

```
tar xfz drc_tests.tgz
```

```
# Change directory into the lab folder
```

```
cd drc_tests
```

```
# List all files and directories present in the current directory
```

```
ls -al
```

```
# Command to view .magicrc file
```

```
gvim .magicrc
```

```
# Command to open magic tool in better graphics
```

```
magic -d XR &
```

Screenshots of commands run

Activities Terminal Thu 10:33 PM
vsduser@vsdsquadron:~/drc_tests

```
File Edit View Search Terminal Help
vsduser@vsdsquadron:~$ cd
vsduser@vsdsquadron:~$ wget http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
--2024-03-21 22:31:14-- http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
Resolving opencircuitdesign.com (opencircuitdesign.com)... 69.251.37.208
Connecting to opencircuitdesign.com (opencircuitdesign.com)|69.251.37.208|:80... connected.
HTTP request sent, awaiting response... 200 OK
Length: 41651 (41K) [application/x-gzip]
Saving to: 'drc_tests.tgz'

drc_tests.tgz          100%[=====] 40.67K 160KB/s in 0.3s

2024-03-21 22:31:15 (160 KB/s) - 'drc_tests.tgz' saved [41651/41651]

vsduser@vsdsquadron:~$ tar xfz drc_tests.tgz
vsduser@vsdsquadron:~$ cd drc_tests
vsduser@vsdsquadron:~/drc_tests$ ls -al
total 276
drwxrwxr-x 2 vsduser vsduser 4096 Sep 16 2020 .
drwxr-xr-x 22 vsduser vsduser 4096 Mar 21 22:31 ..
-rw-rw-r-- 1 vsduser vsduser 3178 Sep 15 2020 capm.mag
-rw-rw-r-- 1 vsduser vsduser 3610 Sep 16 2020 difftap.mag
-rw-rw-r-- 1 vsduser vsduser 1535 Sep 16 2020 dnwell.mag
-rw-rw-r-- 1 vsduser vsduser 1684 Sep 15 2020 hvtp.mag
-rw-rw-r-- 1 vsduser vsduser 897 Sep 15 2020 hvtr.mag
-rw-rw-r-- 1 vsduser vsduser 11586 Sep 15 2020 licon.mag
-rw-rw-r-- 1 vsduser vsduser 1480 Sep 15 2020 li.mag
-rw-rw-r-- 1 vsduser vsduser 4648 Sep 15 2020 lvtn.mag
-rw-rw-r-- 1 vsduser vsduser 2565 Sep 15 2020 .magicrc
```

Activities Terminal Thu 10:34 PM
vsduser@vsdsquadron:~/drc_tests

```
File Edit View Search Terminal Help
-rw-rw-r-- 1 vsduser vsduser 11586 Sep 15 2020 licon.mag
-rw-rw-r-- 1 vsduser vsduser 1480 Sep 15 2020 li.mag
-rw-rw-r-- 1 vsduser vsduser 4648 Sep 15 2020 lvtn.mag
-rw-rw-r-- 1 vsduser vsduser 2565 Sep 15 2020 .magicrc
-rw-rw-r-- 1 vsduser vsduser 1198 Sep 15 2020 mcon.mag
-rw-rw-r-- 1 vsduser vsduser 2103 Sep 15 2020 met1.mag
-rw-rw-r-- 1 vsduser vsduser 1799 Sep 15 2020 met2.mag
-rw-rw-r-- 1 vsduser vsduser 1500 Sep 16 2020 met3.mag
-rw-rw-r-- 1 vsduser vsduser 1114 Sep 16 2020 met4.mag
-rw-rw-r-- 1 vsduser vsduser 757 Sep 15 2020 met5.mag
-rw-rw-r-- 1 vsduser vsduser 1948 Sep 15 2020 npc.mag
-rw-rw-r-- 1 vsduser vsduser 2497 Sep 15 2020 nsd.mag
-rw-rw-r-- 1 vsduser vsduser 1351 Sep 16 2020 nwell.mag
-rw-rw-r-- 1 vsduser vsduser 536 Sep 15 2020 pad.mag
-rw-rw-r-- 1 vsduser vsduser 5588 Sep 16 2020 poly.mag
-rw-rw-r-- 1 vsduser vsduser 2565 Sep 15 2020 psd.mag
-rw-rw-r-- 1 vsduser vsduser 3025 Sep 15 2020 rpm.mag
-rw-rw-r-- 1 vsduser vsduser 135962 Sep 16 2020 sky130A.tech
-rw-rw-r-- 1 vsduser vsduser 2476 Sep 16 2020 tunm.mag
-rw-rw-r-- 1 vsduser vsduser 4114 Sep 16 2020 varac.mag
-rw-rw-r-- 1 vsduser vsduser 1271 Sep 15 2020 via2.mag
-rw-rw-r-- 1 vsduser vsduser 1267 Sep 15 2020 via3.mag
-rw-rw-r-- 1 vsduser vsduser 966 Sep 15 2020 via4.mag
-rw-rw-r-- 1 vsduser vsduser 955 Sep 15 2020 via.mag
vsduser@vsdsquadron:~/drc_tests$ gvim .magicrc
vsduser@vsdsquadron:~/drc_tests$ magic -d XR
```

Screenshot of .magicrc file

```

Thu 10:35 PM
.magicrc (~/.drc_tests) - GVIM

File Edit Tools Syntax Buffers Window Help
1 puts stdout "Sourcing design .magicrc for technology sky130A ..."
2
3 # Put grid on 0.005 pitch. This is important, as some commands don't
4 # rescale the grid automatically (such as lef read?).
5
6 set scalefac [tech lambda]
7 if {[lindex $scalefac 1] < 2} {
8     scalegrid 1 2
9 }
10
11 # drc off
12 drc euclidean on
13
14 # Allow override of PDK path from environment variable PDKPATH
15 if {[catch {set PDKPATH $env(PDKPATH)}]} {
16     set PDKPATH "~/cad/pdk/sky130A"
17 }
18
19 # loading technology
20 # tech load $PDKPATH/libs.tech/magic/sky130A.tech
21 tech load sky130A.tech
22
23 # load device generator
24 # source $PDKPATH/libs.tech/magic/sky130A.tcl
25

".magicrc" 74L, 2565C

```

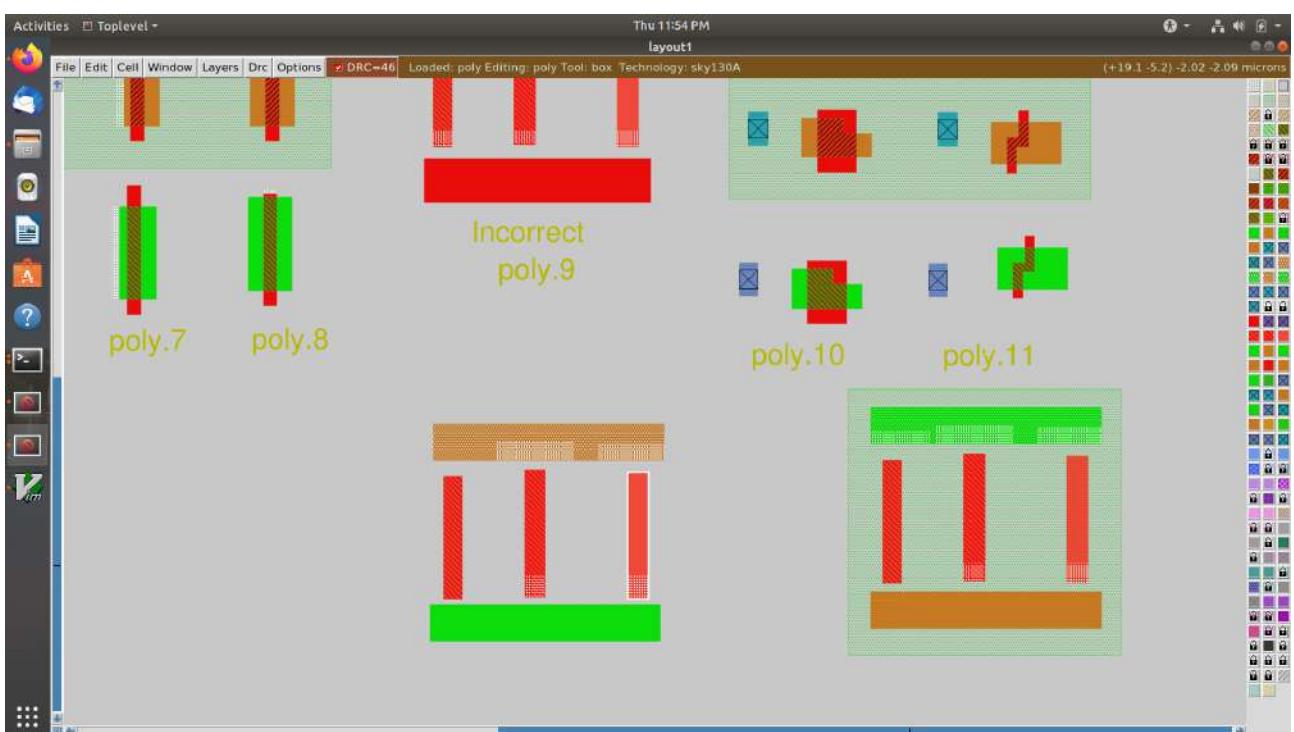
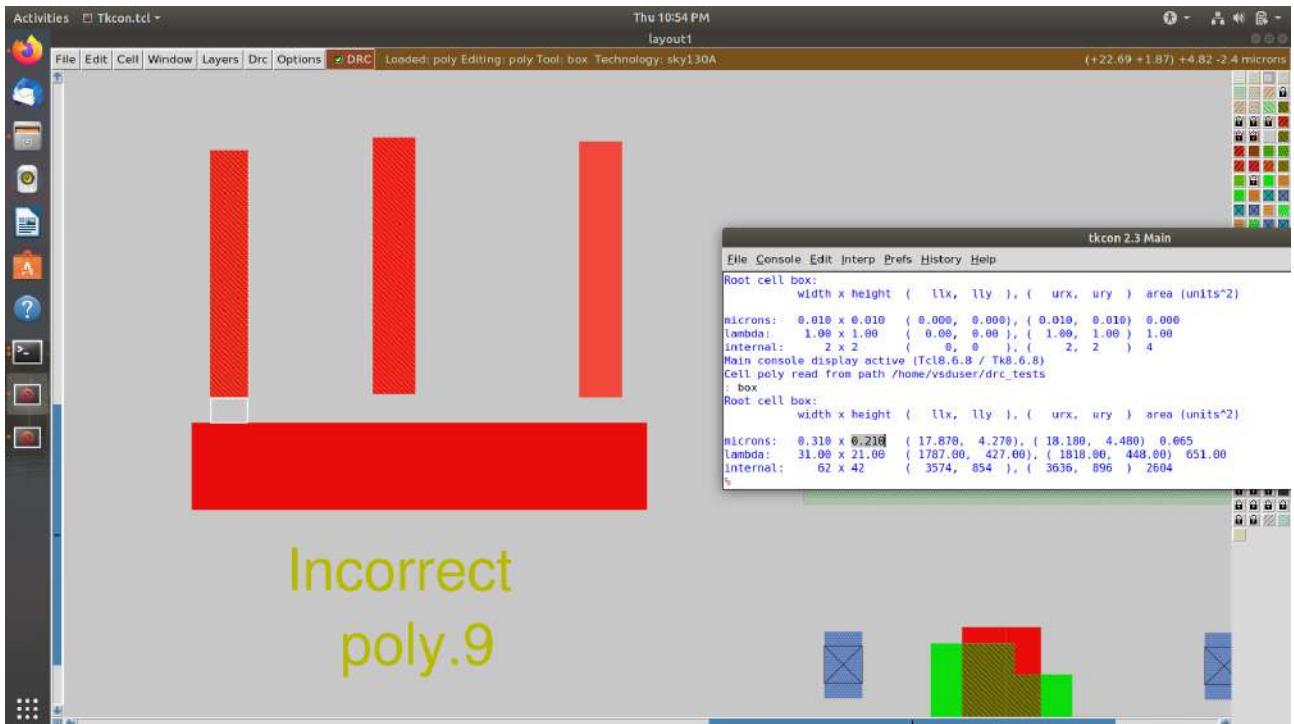
1,1 Top

Incorrectly implemented poly.9 simple rule correction

Screenshot of poly rules

Periphery Rules		Search	google/skywater-pdk
SkyWater SKY130 PDK	(poly.1a)	Width of poly	0.150 μm
Versioning Information	(poly.1b)	Min channel length (poly width) for peft overlapping lvtn (exempt rule for dummy_poly in cells listed on Table H3)	0.350 μm
Current Status	(poly.2)	Spacing of poly to poly except for poly.c2 and poly.c3. Exempt cell: sr_bld_eq where it is same as poly.c2	0.210 μm
Known Issues	(poly.3)	Min poly resistor width	0.330 μm
Design Rules	(poly.4)	Spacing of poly on field to diff (parallel edges only)	P 0.075 μm
PDK Contents	(poly.5)	Spacing of poly on field to tap	P 0.055 μm
Analog Design	(poly.6)	Spacing of poly on diff to abutting tap (min source)	P 0.300 μm
Digital Design	(poly.7)	Extension of diff beyond poly (min drain)	P 0.250
Simulation	(poly.8)	Extension of poly beyond diffusion (endcap)	P 0.130
Physical & Design Verification	(poly.9)	Poly resistor spacing to poly or spacing (no overlap) to diff/tap	0.480 μm
Python API	(poly.10)	Poly can't overlap inner corners of diff	
Previous Nomenclature	(poly.11)	No 90 deg turns of poly on diff	
Glossary	(poly.12)	(Poly NOT (inwell NOT hv)) may not overlap tap: Rule exempted for cell name "g8tge_n_fq2" and gated_rgn and inside UHVL.	P
How to Contribute	(poly.13)	Poly must not overlap diff/rs	
Partners	(poly.14)		
References	(poly.15)		

Incorrectly implemented poly.9 rule no drc violation even though spacing < 0.48μ



New commands inserted in sky130A.tech file to update drc

Activities M GVim Thu 11:58 PM
sky130A.tech (~/.drc_tests) - GVIM

```

4803
4804 variants *
4805
4806 #-----
4807 # POLY
4808 #-----
4809
4810 width allpoly 150 "poly.width < %d (poly.1a)"
4811 spacing allpoly allpoly 210 touching_ok "poly.spacing < %d (poly.2)"
4812 spacing allpolynonfet alldiffvnonfet 75 corner_ok allfets \
    "poly.spacing to Diffusion < %d (poly.4a)"
4813 spacing npres alldiff 480 touching_illegal \
    "poly.resistor spacing to alldiff < %d (poly.9)"
4814 spacing npres allpolynonres 480 touching_illegal \
    "poly.resistor spacing to allpolynonres < %d (poly.9)"
4815 overhang *ndiff,rndiff nfet,scnfet,npd,npass 250 "N-Diffusion overhang of nmos < %d (poly.7)"
4816 overhang *mvndiff,mvrndiff mvnfet,mvnnfet 250 \
    "N-Diffusion overhang of nmos < %d (poly.7)"
4817 overhang *pdifff,rdifff pfet,scpfet,ppu 250 "P-Diffusion overhang of pmos < %d (poly.7)"
4818 overhang *mvpdiff,mvrpdifff mvpfet 250 "P-Diffusion overhang of pmos < %d (poly.7)"
4819 overhang *poly allfets 130 "poly.overhang of transistor < %d (poly.8)"
4820 rect_only allfets "No bends in transistors (poly.11)"
4821 rect_only xhrpoly,uhrpoly "No bends in poly resistors (poly.11)"
4822 extend xpc/a xhrpoly,uhrpoly 2160 \
    "poly.contact extends poly resistor by < %d (lcon.1c + li.5)"
4823
4824 -- VISUAL --
4817,56-63 81%

```

Activities M GVim Thu 11:09 PM
sky130A.tech (~/.drc_tests) - GVIM

```

5168 # xhrpoly (P+ poly resistor)
5169 #-----
5170
5171 width xhrpoly 350 "xhrpoly resistor width < %d (P+ poly.1a)"
5172 # NOTE: xhrpoly resistor requires choice of discrete widths 0.35, 0.69, ... up to 1.27.
5173
5174 #-----
5175 # uhrpoly (P+ poly resistor, 2kOhm/sq)
5176 #-----
5177
5178 width uhrpoly 350 "uhrpoly resistor width < %d"
5179 spacing xhrpoly,uhrpoly,xpc alldiff 480 touching_illegal \
    "xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
5180 spacing xhrpoly,uhrpoly,xpc allpolynonres 480 touching_illegal \
    "xhrpoly/uhrpoly resistor spacing to allpolynonres < %d (poly.9)"
5181
5182
5183
5184
5185 #-----
5186 # MOS Varactor device rules
5187 #-----
5188
5189 overhang *nsd var,varhvt 250 \
    "N-Tap overhang of Varactor < %d (var.4)"
5190
5191
5192 overhang *mvnsd mvvar 250 \
-- VISUAL --
5182,67-74 87%

```

Commands to run in tkcon window

```
# Loading updated tech file
```

```
tech load sky130A.tech
```

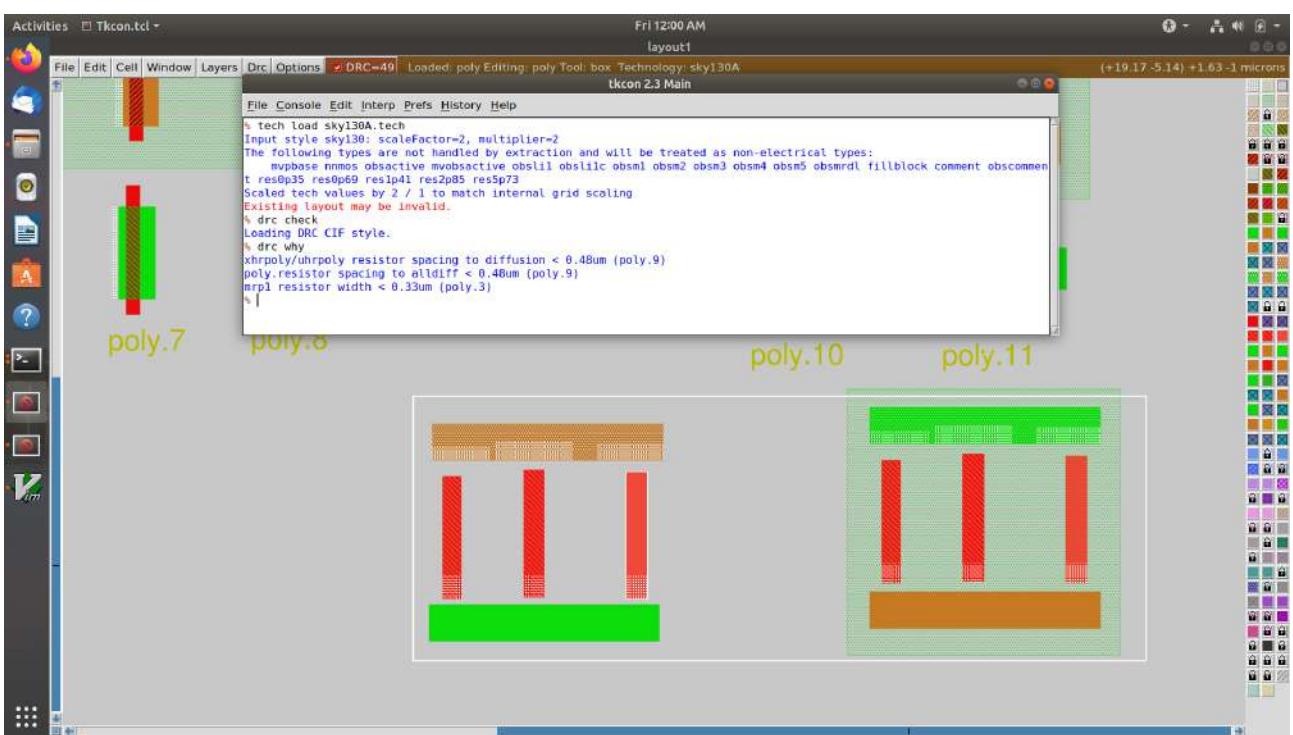
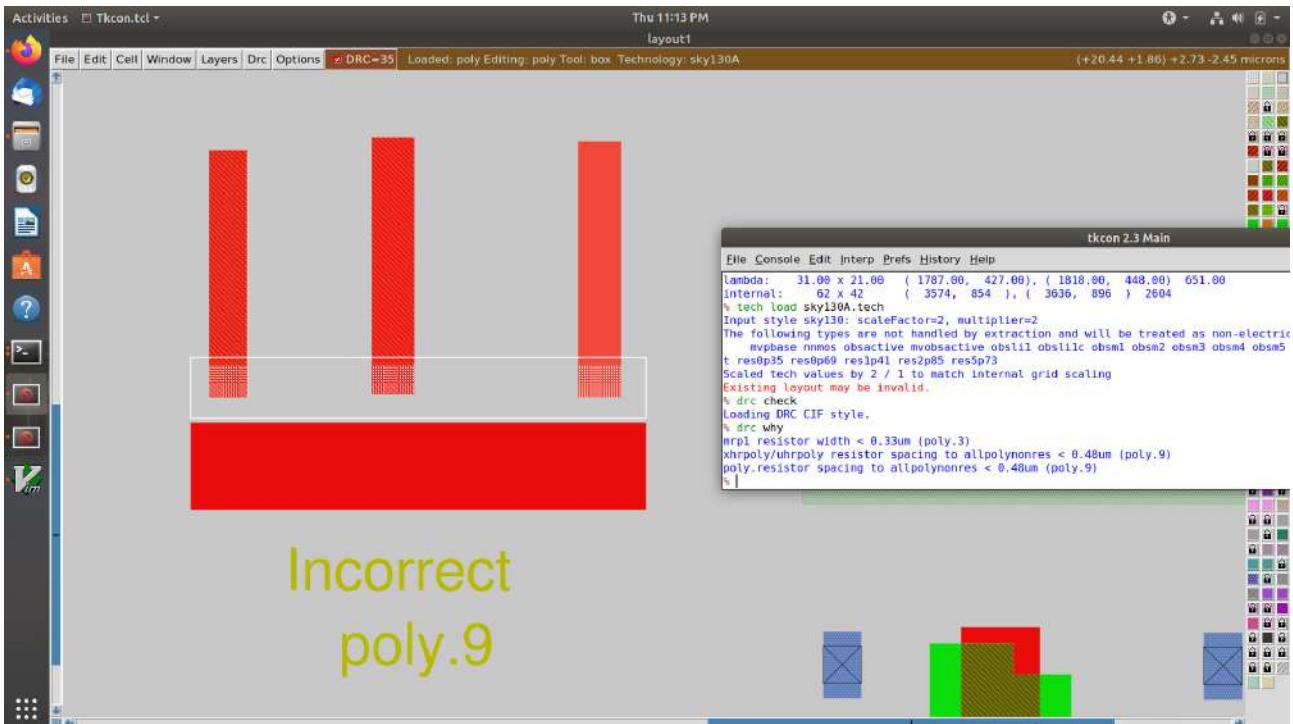
```
# Must re-run drc check to see updated drc errors
```

```
drc check
```

```
# Selecting region displaying the new errors and getting the error messages
```

```
drc why
```

Screenshot of magic window with rule implemented



Incorrectly implemented difftap.2 simple rule correction

Screenshot of difftap rules

Activities Firefox Web Browser Fri 12:14 AM

Editing soc-design-and... yosys-tcl-ui-report/RE... nickson-jose/vsdstdce... Online Clipboard Periphery Rules — Sky... Magic VLSI

<https://skywater-pdk.readthedocs.io/en/main/rules/periphery.html#difftap>

Periphery Rules Search google@skywater-pdk

SkyWater SKY130 PDK

Versioning Information Current Status Known Issues Design Rules PDK Contents Analog Design Digital Design Simulation Physical & Design Verification Python API Previous Nomenclature Glossary How to Contribute Partners References

Name Description Flags Value Unit

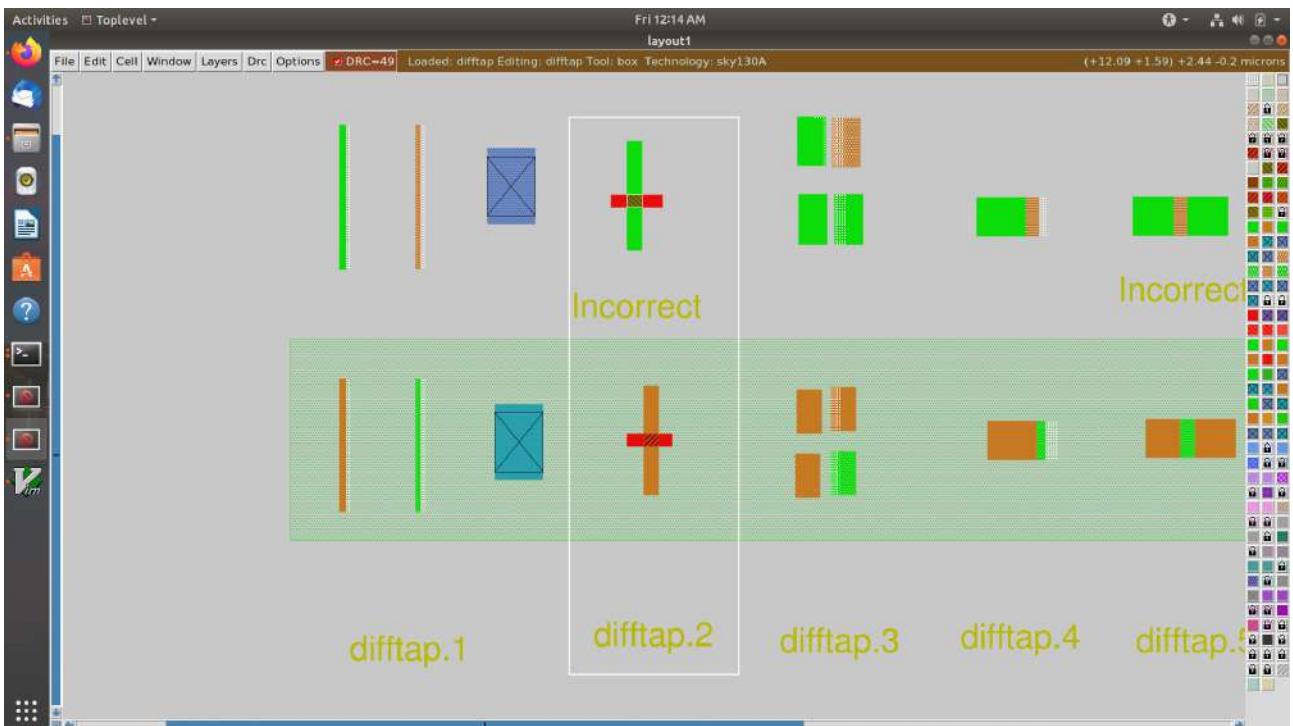
Table 38 Function: Defines active regions and contacts to substrate

Name	Description	Flags	Value	Unit
(difftap.1)	Width of diff or tap	P	0.150	μm
(difftap.2)	Minimum channel width (Diff And Poly) except for FETs inside areaid.sc: Rule exempted in the SP8* flows only, for the cells listed in rule difftap.2a	P	0.420	μm
(difftap.2a)	Minimum channel width (Diff And Poly) for cell names "s8cell_ee_plus_ssein_a", "s8cell_ee_plus_ssein_b", "s8cell_ee_plus_sseip_a", "s8cell_ee_plus_sseip_b", "s8lpls_pl8", "s8lpls_rdrv4", "s8lpls_rdrv4f" and "s8lpls_rdrv8"	P, NA	NA	μm
(difftap.2b)	Minimum channel width (Diff And Poly) for FETs inside areaid.sc	P	0.360	μm
(difftap.3)	Spacing of diff to diff, tap to tap, or non-abutting diff to tap		0.270	μm
(difftap.4)	Min tap bound by one diffusion		0.290	
(difftap.5)	Min tap bound by two diffusions	P	0.400	
(difftap.6)	Diff and tap are not allowed to extend beyond their abutting edge			
(difftap.7)	Spacing of difftap abutting edge to a non-conciding diff or tap edge	NE	0.130	μm
(difftap.8)	Enclosure of (p+) diffusion by N-well. Rule exempted inside UHVI.	DE NE P	0.180	μm
(difftap.9)	Spacing of (n+) diffusion to N-well outside UHVI	DE NE P	0.340	μm
(difftap.10)	Enclosure of (n+) tap by N-well. Rule exempted inside UHVI.	NE P	0.180	μm
Creation of resistors in N-well. Only recommended inside UHVI				
Δ 196 nm				

Contents

- Periphery Rules (x,-) (dnwell,-) (nwell,-) (pwell,-) (pudem,-) (hvtp,-) (hvtr,-) (lvtn,-) (ncm,-) (difftap,-) (tunn,-) (poly,-) (rpm,-) (varac,-) (photo,-) (npc,-) (n/ psd,-) (licon,-) (li,-) (ct,-) (capm,-) (vpp,-) /m1 -

Incorrectly implemented difftap.2 rule no drc violation even though spacing < 0.42μ



New commands inserted in sky130A.tech file to update drc

```
5178 width uhrpoly 350 "uhrpoly resistor width < %d"
5179 spacing xhrpoly,uhrpoly,xpc alldiff 480 touching_illegal \
      "xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
5180 spacing xhrpoly,uhrpoly,xpc allpolynonres 480 touching_illegal \
      "xhrpoly/uhrpoly resistor spacing to allpolynonres < %d (poly.9)"
5181
5182
5183
5184
5185 #-----
5186 # MOS Varactor device rules
5187 #-----
5188
5189 width pmos 420 \
      "mos transistor formed should have minimum width of < %d (difftap.2)"
5190 width nmos 420 \
      "mos transistor formed should have minimum width of < %d (difftap.2)"
5191
5192
5193 overhang *nsd var,varhvt 250 \
      "N-Tap overhang of Varactor < %d (var.4)"
5194
5195 overhang *mvnsd mvvar 250 \
      "N-Tap overhang of Varactor < %d (var.4)"
5196
5197 width var,varhvt,mvvar 180 "Varactor length < %d (var.1)"
5198 extend var,varhvt,mvvar *poly 1000 "Varactor width < %d (var.2)"
5199
5200
5201
5202
```

-- VISUAL -- 5192, 71 88%

Commands to run in tkcon window

```
# Loading updated tech file
```

```
tech load sky130A.tech
```

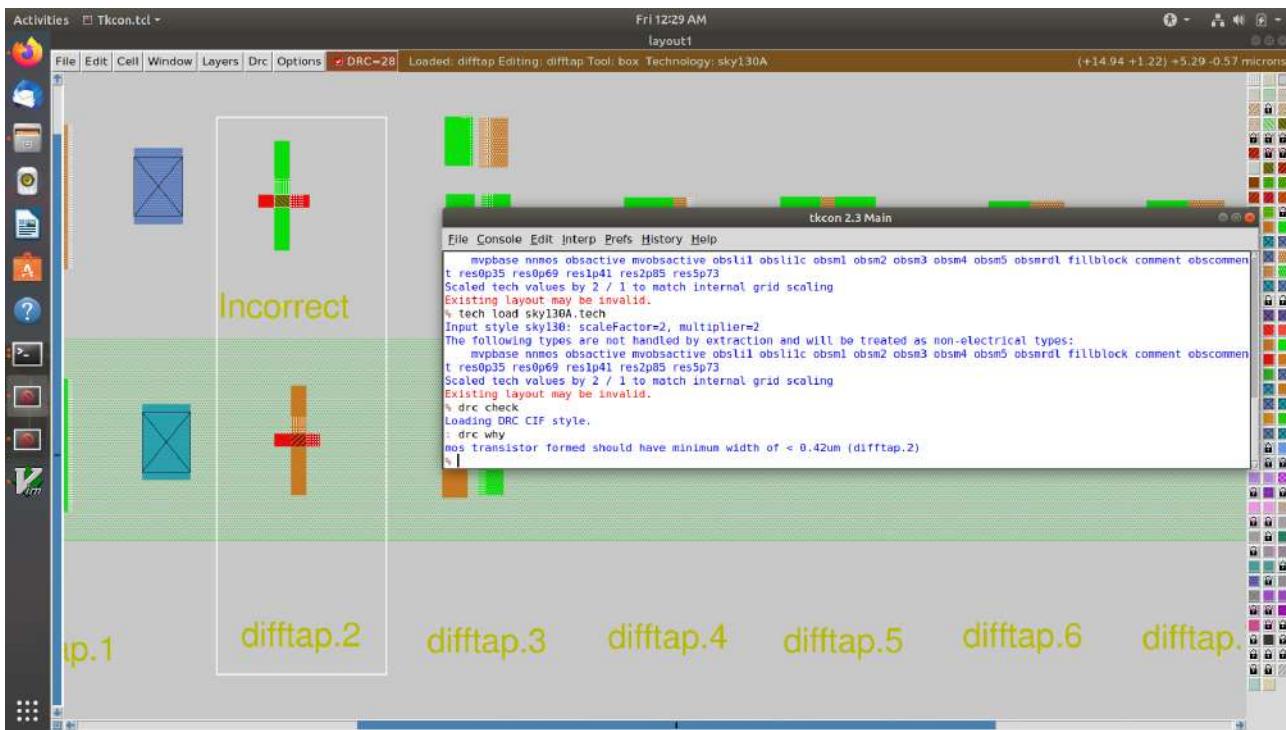
```
# Must re-run drc check to see updated drc errors
```

```
drc check
```

```
# Selecting region displaying the new errors and getting the error messages
```

```
drc why
```

Screenshot of magic window with rule implemented

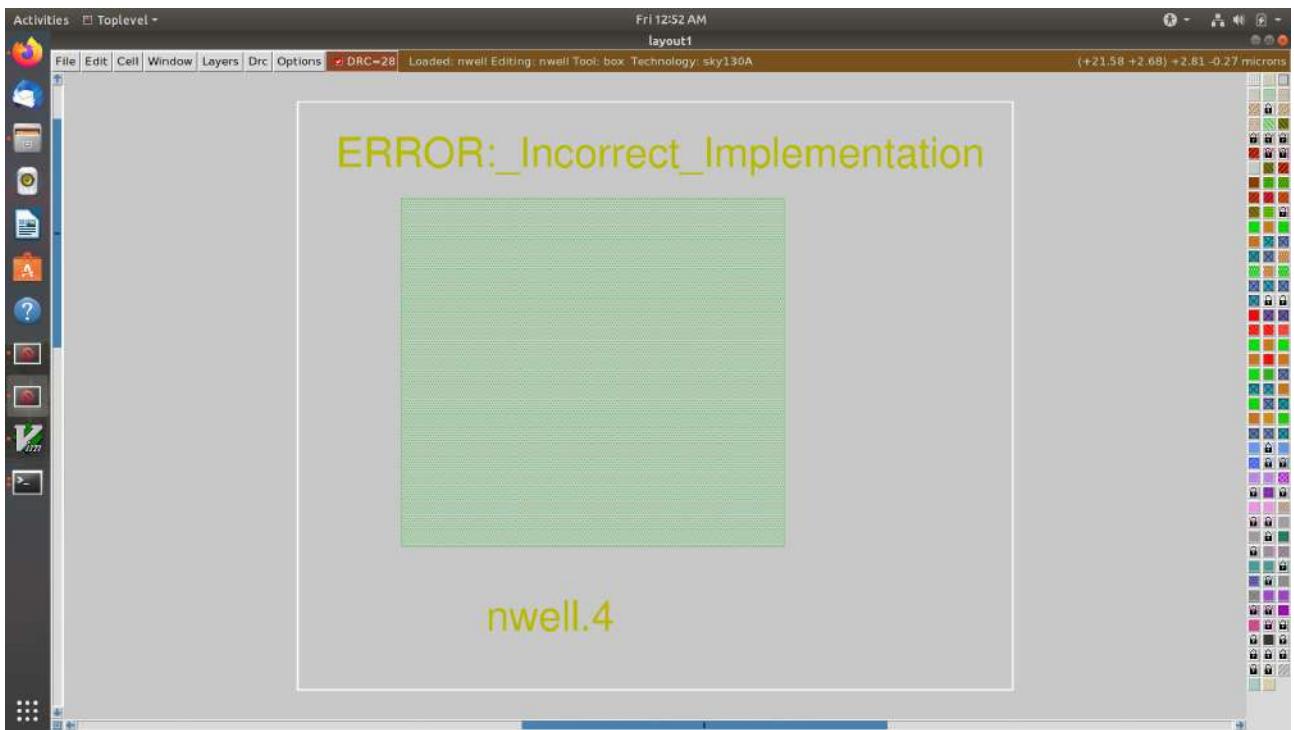


Incorrectly implemented nwell.4 complex rule correction

Screenshot of nwell rules

Table 31 Function: Define nwell implant regions.					
	Name	Description	Flags	Value	Unit
(nwell..1)	Width of nwell			0.840	μm
(nwell..2a)	Spacing between two n-wells			1.270	μm
(nwell..2b)	Manual merge wells if less than minimum				
(nwell..4)	All n-wells will contain metal-contacted tap (rule checks only for icon on top) . Rule exempted from high voltage cells inside UHVI				
(nwell..5)	Deep nwell must be enclosed by nwell by atleast... Exempted inside UHVI or areaid..lw Nwells can merge over deep nwell if spacing too small (as in rule nwell.2)	TC	0.400	μm	
(nwell..5a)	min enclosure of nwell by dnwell inside UHVI		N/A	N/A	
(nwell..5b)	nwell inside UHVI must not be on the same net as nwell outside UHVI		N/A	N/A	
(nwell..6)	Min enclosure of nwell hole by deep nwell outside UHVI	TC	1.030	μm	
(nwell..7)	Min spacing between nwell and deep nwell on separate nets Spacing between nwell and deep nwell on the same net is set by the sum of the rules nwell.2 and nwell.5. By default, DRC run on a cell checks for the separate-net spacing, when nwell and deep nwell nets are separate within the cell hierarchy and are joined in the upper hierarchy. To allow net names to be joined and make the same-net rule applicable in this case, the "joinNets" switch should be turned on. waffle_chip	TC	4.500	μm	

Incorrectly implemented nwell.4 rule no drc violation even though no tap present in nwell



New commands inserted in sky130A.tech file to update drc

Activities M GVim

Fri 1:03 AM
sky130A.tech (~/.drc_tests) - GVIM

```

1230 options calma-permissive-labels
1231
1232 # Ensure nwell overlaps dnwell at least 0.4um outside and 1.03um inside
1233 templayer dnwell_shrink dnwell
1234 shrink 1030
1235
1236 templayer nwell_missing dnwell
1237 grow 400
1238 and-not dnwell_shrink
1239 and-not nwell
1240
1241 templayer nwell_tapped
1242 bloat-all nsc nwell
1243
1244 templayer nwell_untapped nwell
1245 and-not nwell_tapped
1246
1247 # SONOS nFET devices must be in deep nwell
1248 templayer dnwell_missing nsonos
1249 and-not dnwell
1250
1251 # Define MiM cap bottom plate for spacing rule
1252 templayer mim_bottom
1253 bloat-all *mimcap *metal3
1254
-- VISUAL --

```

1245, 22 20%

Activities M GVim

Fri 1:04 AM
sky130A.tech (~/.drc_tests) - GVIM

```

4721 spacing dnwell dnwell 6300 touching_ok "Deep N-well spacing < %d (dnwell.3)"
4722 spacing dnwell allnwell 4500 surround_ok \
4723 "Deep N-well spacing to N-well < %d (nwell.7)"
4724 cifmaxwidth nwell_missing 0 bend_illegal \
4725 "N-well overlap of Deep N-well < 0.4um outside, 1.03um inside (nwell.5a, 7)"
4726 cifmaxwidth dnwell_missing 0 bend_illegal \
4727 "SONOS nFET must be in Deep N-well (tunm.6a)"
4728
4729 #-----
4730 # NWELL
4731 #-----
4732
4733 width allnwell 840 "N-well width < %d (nwell.1)"
4734 spacing allnwell allnwell 1270 touching_ok "N-well spacing < %d (nwell.2a)"
4735
4736 variants (full)
4737 cifmaxwidth nwell_untapped 0 bend_illegal \
4738 "Nwell missing tap (nwell.4)"
4739 variants *
4740
4741 #-----
4742 # DIFF
4743 #-----
@ -- VISUAL --

```

4739, 11 80%

Commands to run in tkcon window

```
# Loading updated tech file
```

```
tech load sky130A.tech
```

```
# Change drc style to drc full
```

```
drc style drc(full)
```

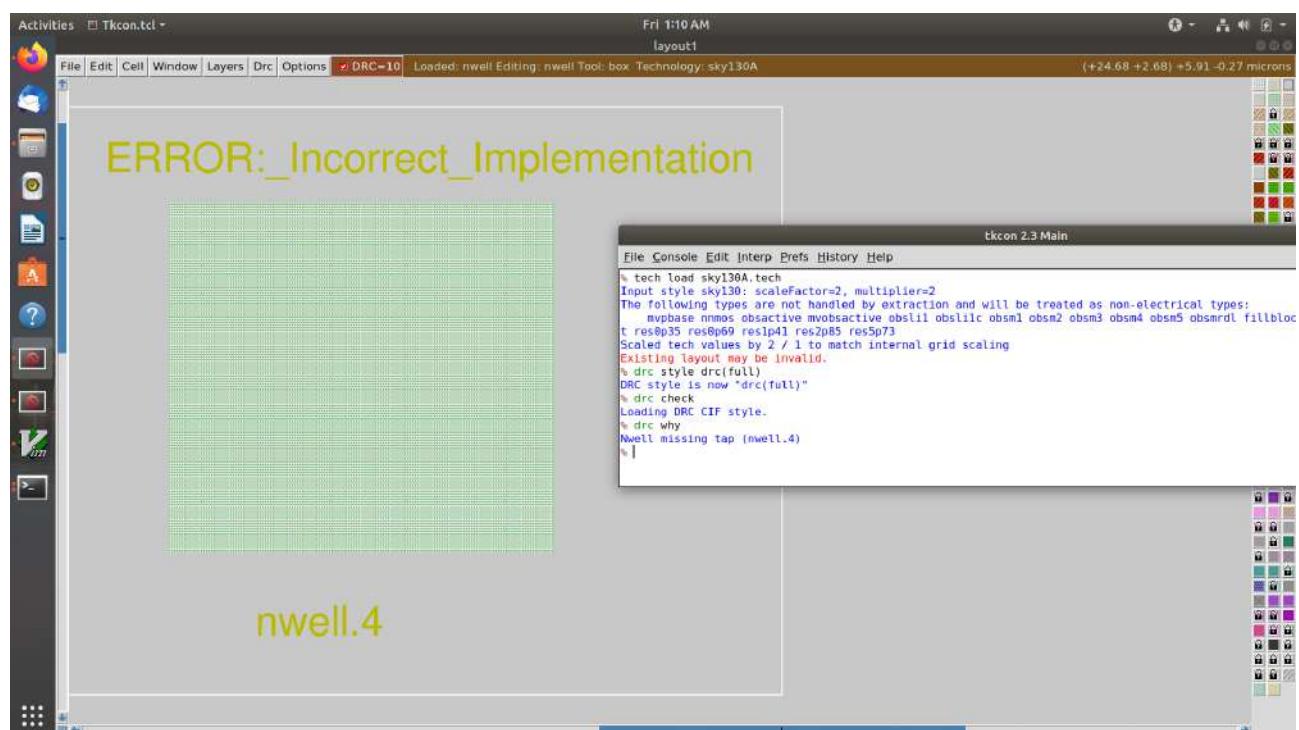
```
# Must re-run drc check to see updated drc errors
```

```
drc check
```

```
# Selecting region displaying the new errors and getting the error messages
```

```
drc why
```

Screenshot of magic window with rule implemented



Section 4 - Pre-layout timing analysis and importance of good clock tree (22/03/2024 - 24/03/2024)

Theory

Implementation

- Section 4 tasks:-
 12. Fix up small DRC errors and verify the design is ready to be inserted into our flow.
 13. Save the finalized layout with custom name and open it.
 14. Generate lef from the layout.
 15. Copy the newly generated lef and associated required lib files to 'picorv32a' design 'src' directory.
 16. Edit 'config.tcl' to change lib file and add the new extra lef into the openlane flow.
 17. Run openlane flow synthesis with newly inserted custom inverter cell.
 18. Remove/reduce the newly introduced violations with the introduction of custom inverter cell by modifying design parameters.
 19. Once synthesis has accepted our custom inverter we can now run floorplan and placement and verify the cell is accepted in PnR flow.
 20. Do Post-Synthesis timing analysis with OpenSTA tool.
 21. Make timing ECO fixes to remove all violations.

22. Replace the old netlist with the new netlist generated after timing ECO fix and implement the floorplan, placement and cts.
23. Post-CTS OpenROAD timing analysis.
24. Explore post-CTS OpenROAD timing analysis by removing 'sky130_fd_sc_hd_clkbuf_1' cell from clock buffer list variable 'CTS_CLK_BUFFER_LIST'.
 - Section 4 - Tasks 1 to 4 files, reports and logs can be found in the following folder:

Section 4 - Tasks 1 to 4 (vsdstdcelldesign)

- Section 4 - Task 4 files, reports and logs can be found in the following folder:

Section 4 - Task 4 (src)

- Section 4 - Task 5 files, reports and logs can be found in the following folder:

Section 4 - Task 5 (picorv32a)

- Section 4 - Tasks 6 to 8 & 11 to 13 logs, reports and results can be found in following run folder:

Section 4 - Tasks 6 to 8 & 11 to 13 Run (24-03_10-03)

- Section 4 - Tasks 9 to 11 logs, reports and results can be found in following run folder:

Section 4 - Tasks 9 to 11 Run (25-03_18-52)

1. Fix up small DRC errors and verify the design is ready to be inserted into our flow.

Conditions to be verified before moving forward with custom designed cell layout:

- Condition 1: The input and output ports of the standard cell should lie on the intersection of the vertical and horizontal tracks.
- Condition 2: Width of the standard cell should be odd multiples of the horizontal track pitch.
- Condition 3: Height of the standard cell should be even multiples of the vertical track pitch.

Commands to open the custom inverter layout

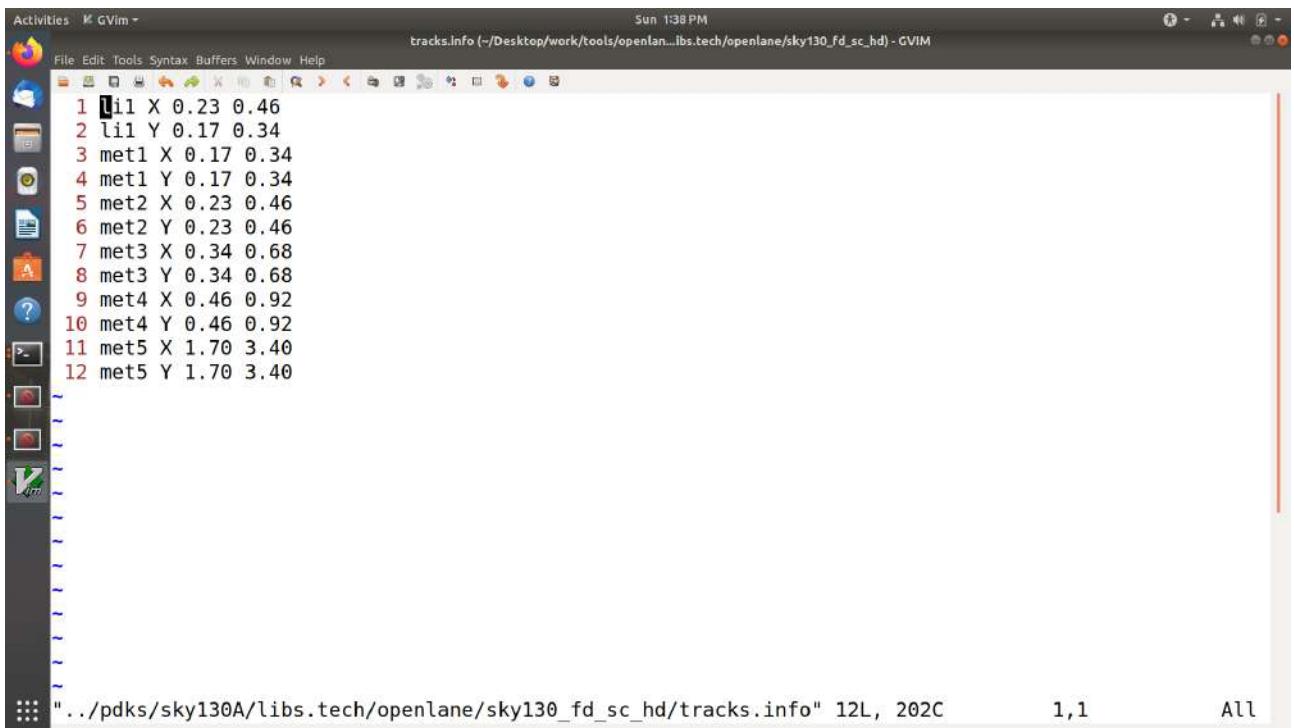
```
# Change directory to vsdstdcelldesign
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
```

```
# Command to open custom inverter layout in magic
```

```
magic -T sky130A.tech sky130_inv.mag &
```

Screenshot of tracks.info of sky130_fd_sc_hd



A screenshot of the GVIM text editor window. The title bar reads "activities K. GVIM" and "tracks.info (~/Desktop/work/tools/openlane/libs.tech/openlane/sky130_fd_sc_hd) - GVIM". The status bar at the bottom shows the path ".../pdks/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tracks.info" and the coordinates "1,1" and "All". The main editor area displays a list of track definitions:

```
1 l1l X 0.23 0.46
2 l1l Y 0.17 0.34
3 met1 X 0.17 0.34
4 met1 Y 0.17 0.34
5 met2 X 0.23 0.46
6 met2 Y 0.23 0.46
7 met3 X 0.34 0.68
8 met3 Y 0.34 0.68
9 met4 X 0.46 0.92
10 met4 Y 0.46 0.92
11 met5 X 1.70 3.40
12 met5 Y 1.70 3.40
```

Commands for tkcon window to set grid as tracks of locali layer

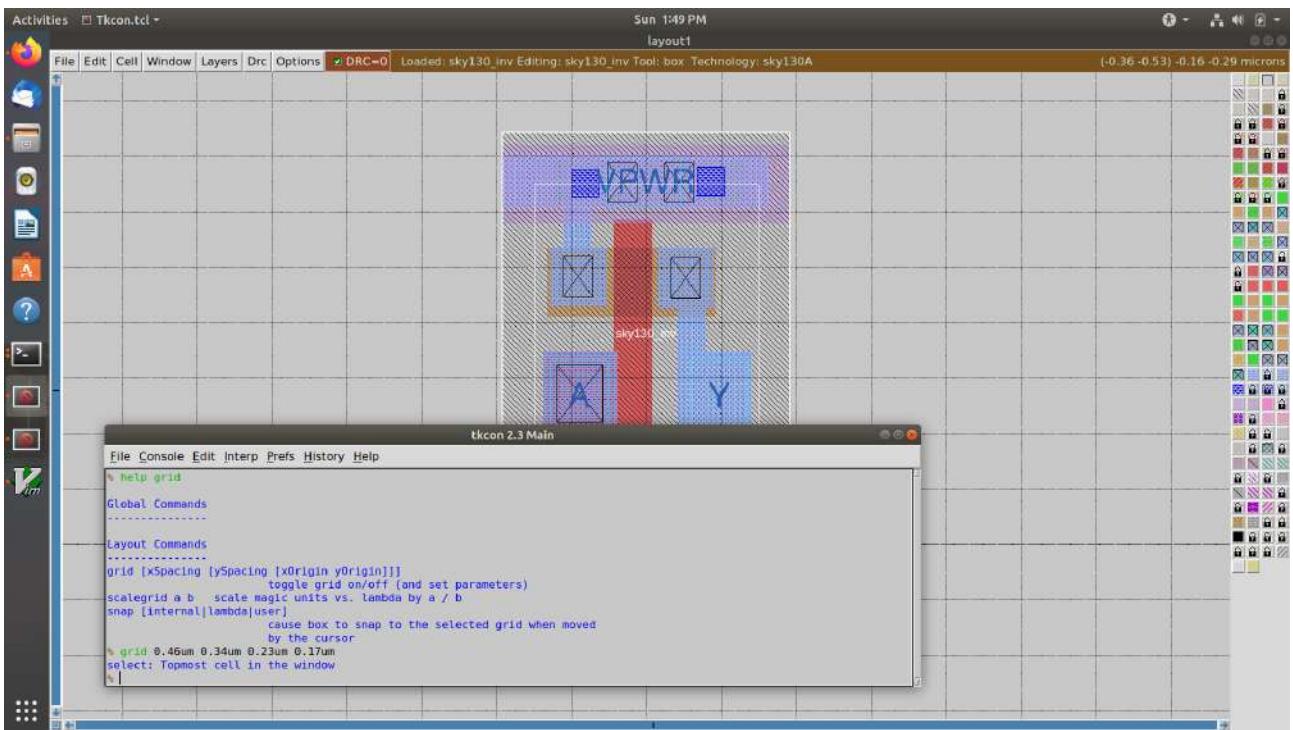
```
# Get syntax for grid command
```

```
help grid
```

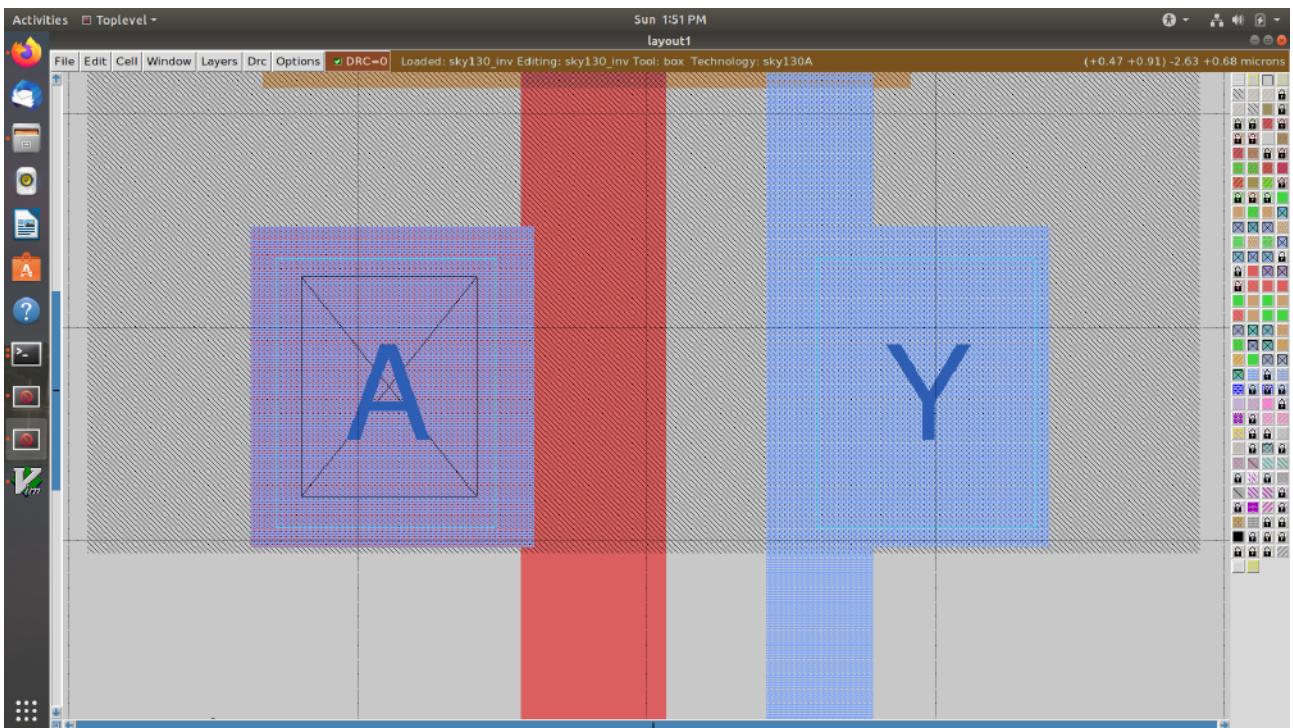
```
# Set grid values accordingly
```

```
grid 0.46um 0.34um 0.23um 0.17um
```

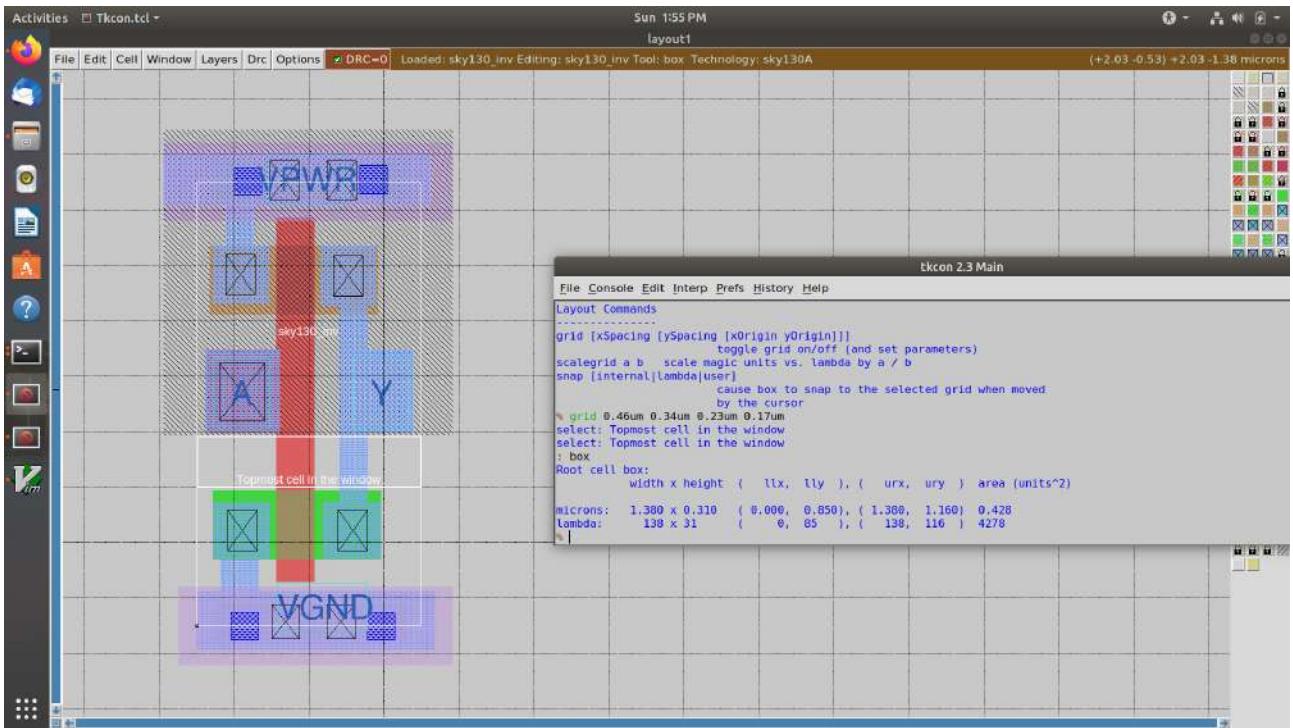
Screenshot of commands run



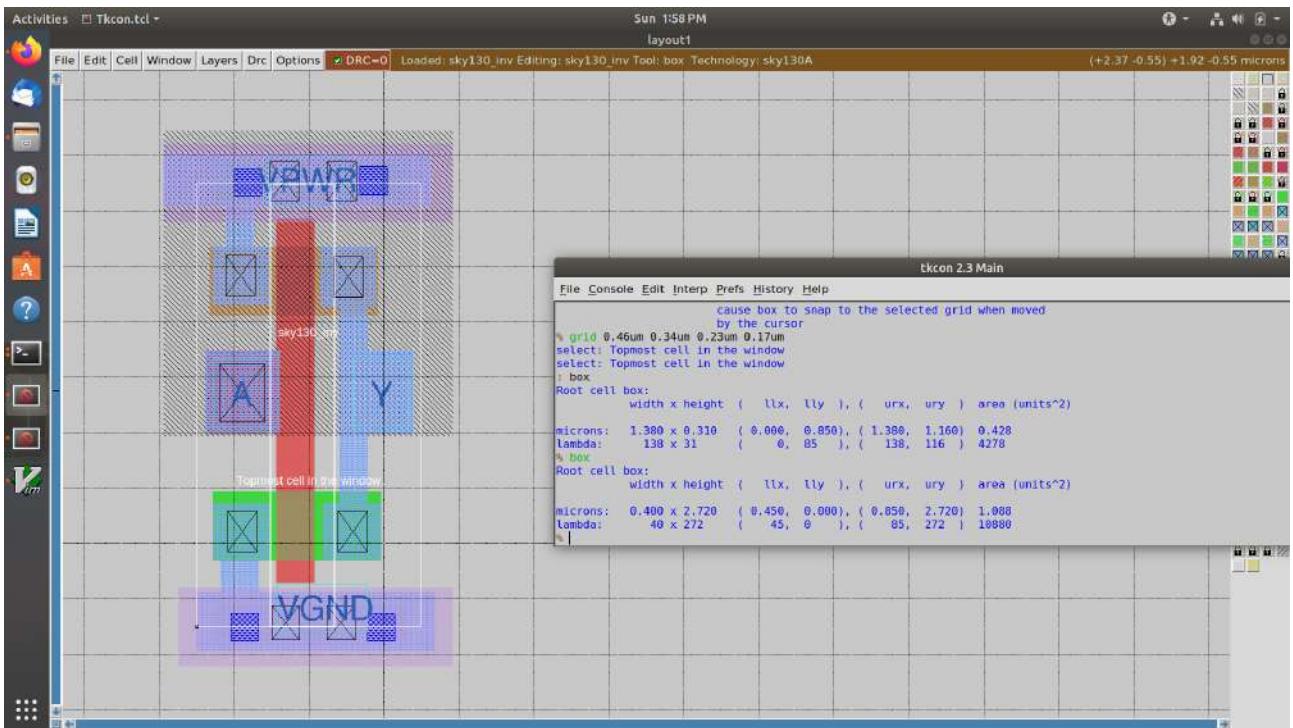
Condition 1 verified



Condition 2 verified



Condition 3 verified



2. Save the finalized layout with custom name and open it.

Command for tkcon window to save the layout with custom name

```
# Command to save as
```

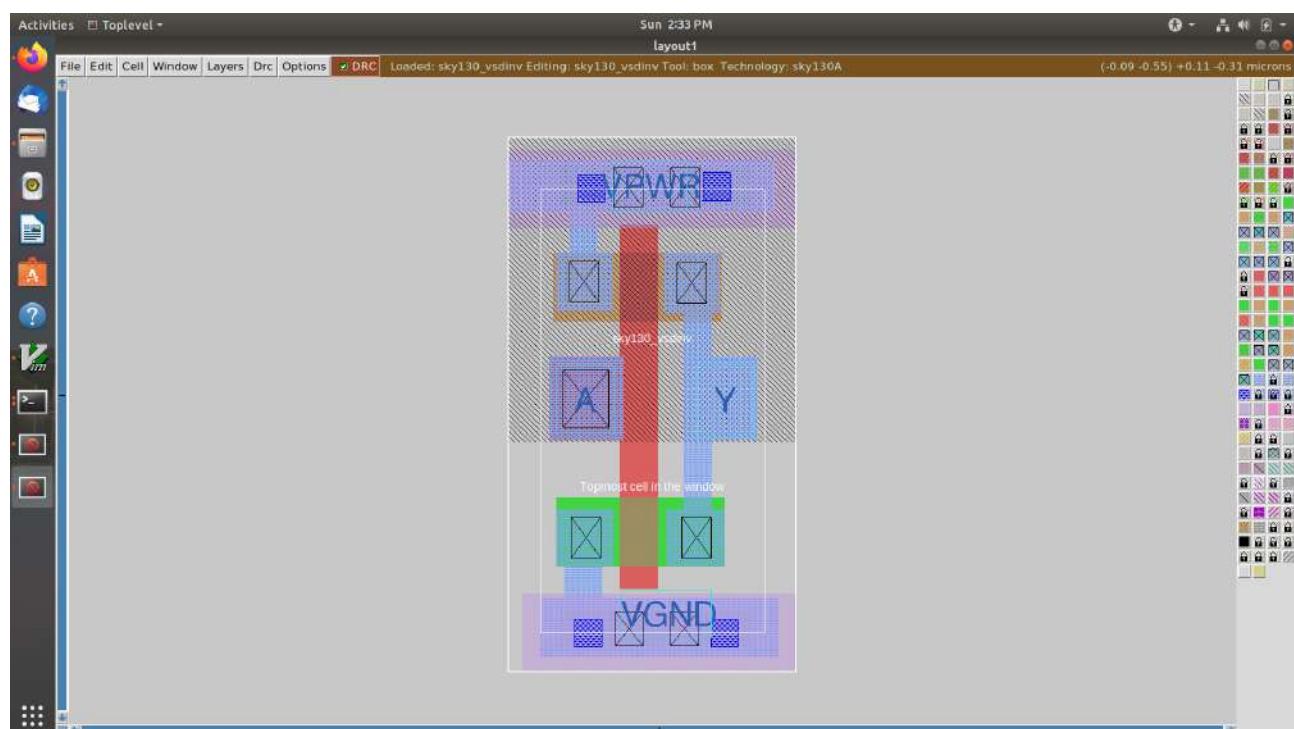
```
save sky130_vsdinv.mag
```

Command to open the newly saved layout

```
# Command to open custom inverter layout in magic
```

```
magic -T sky130A.tech sky130_vsdinv.mag &
```

Screenshot of newly saved layout



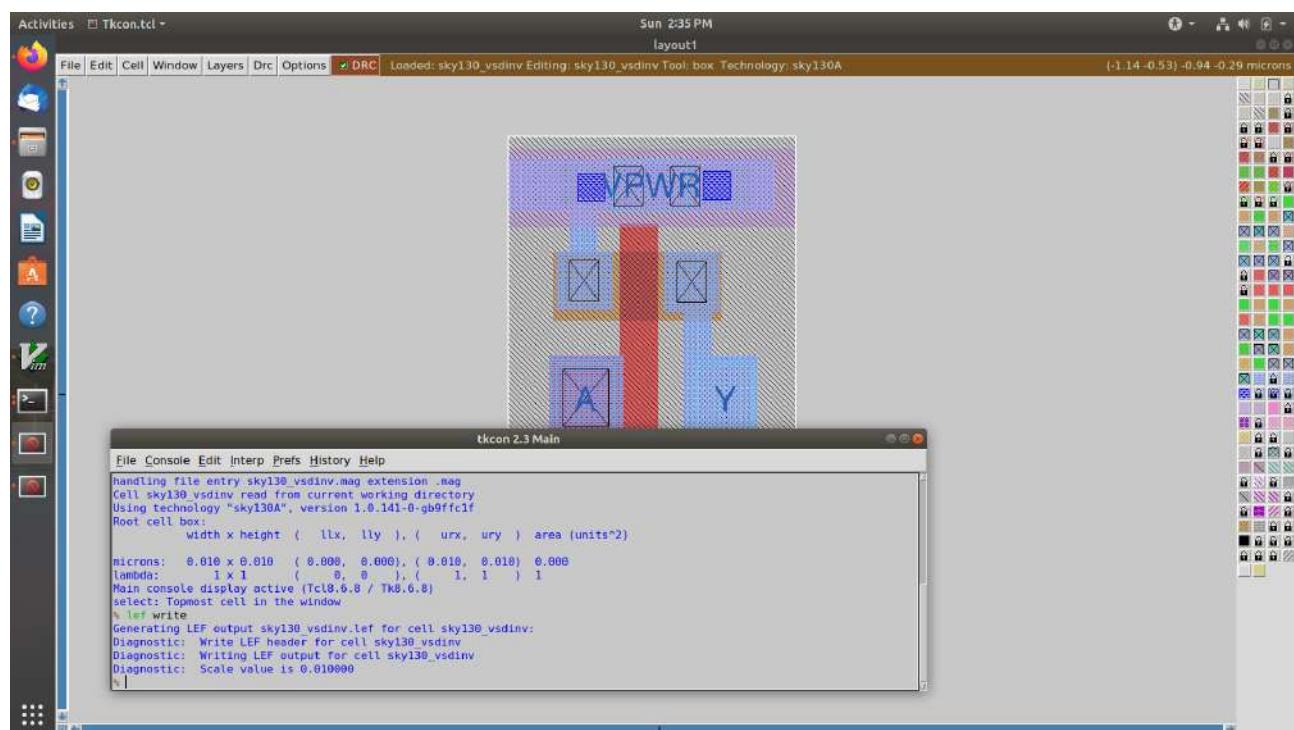
3. Generate lef from the layout.

Command for tkcon window to write lef

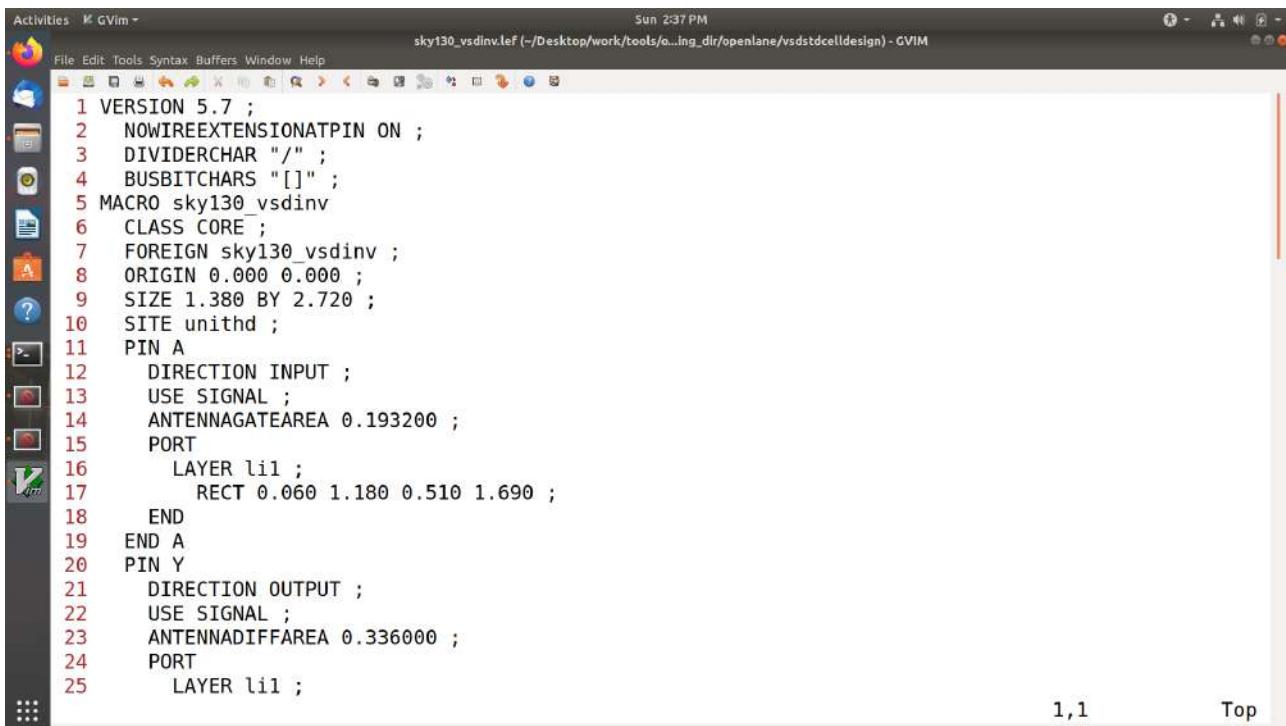
```
# lef command
```

```
lef write
```

Screenshot of command run



Screenshot of newly created lef file



A screenshot of the GVIM text editor window. The title bar reads "Activities K. GVim" and "sky130_vsdinv.lef (~/Desktop/work/tools/openlane/designs/sky130_vsdinv.lef) - GVIM". The status bar shows "Sun 2:37 PM" and "1,1 Top". The main pane displays a LEF (Liberty Cell Format) file with the following content:

```
1 VERSION 5.7 ;
2 NOWIREEXTENSIONATPIN ON ;
3 DIVIDERCHAR "/" ;
4 BUSBITCHARS "[]" ;
5 MACRO sky130_vsdinv
6 CLASS CORE ;
7 FOREIGN sky130_vsdinv ;
8 ORIGIN 0.000 0.000 ;
9 SIZE 1.380 BY 2.720 ;
10 SITE unithd ;
11 PIN A
12     DIRECTION INPUT ;
13     USE SIGNAL ;
14     ANTENNAGATEAREA 0.193200 ;
15     PORT
16         LAYER li1 ;
17         RECT 0.060 1.180 0.510 1.690 ;
18     END
19 END A
20 PIN Y
21     DIRECTION OUTPUT ;
22     USE SIGNAL ;
23     ANTENNADIFFAREA 0.336000 ;
24     PORT
25         LAYER li1 ;
```

4. Copy the newly generated lef and associated required lib files to 'picorv32a' design 'src' directory.

Commands to copy necessary files to 'picorv32a' design 'src' directory

```
# Copy lef file
```

```
cp sky130_vsdinv.lef ~/Desktop/work/tools/openlane_working_dir/openlane/designs/
picorv32a/src/
```

```
# List and check whether it's copied
```

```
ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
```

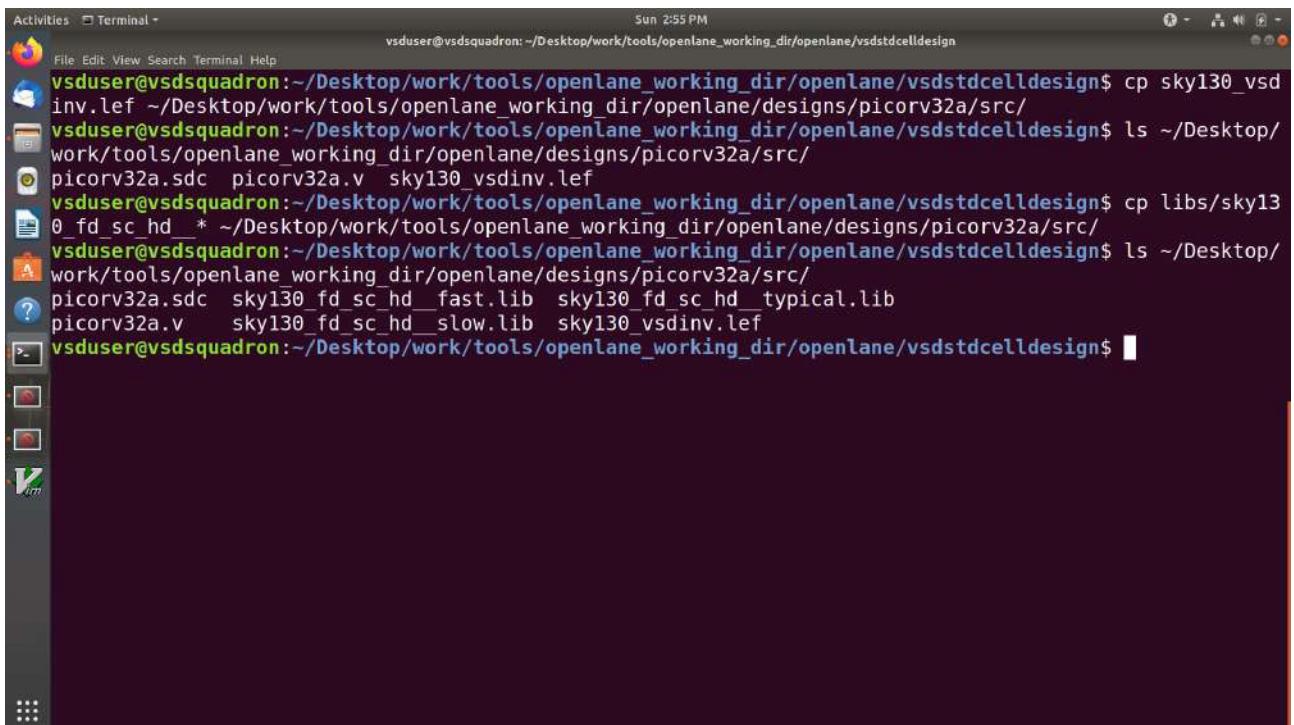
```
# Copy lib files
```

```
cp libs/sky130_fd_sc_hd_* ~/Desktop/work/tools/openlane_working_dir/openlane/designs/
picorv32a/src/
```

```
# List and check whether it's copied
```

```
ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
```

Screenshot of commands run



```
Activities Terminal Sun 2:55 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cp sky130_vsdinv.lef ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
picorv32a.sdc picorv32a.v sky130_vsdinv.lef
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cp libs/sky130_fd_sc_hd_* ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
picorv32a.sdc sky130_fd_sc_hd_fast.lib sky130_fd_sc_hd_typical.lib
picorv32a.v sky130_fd_sc_hd_slow.lib sky130_vsdinv.lef
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```

5. Edit 'config.tcl' to change lib file and add the new extra lef into the openlane flow.

Commands to be added to config.tcl to include our custom cell in the openlane flow

```
set ::env(LIB_SYNTH) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib"

set ::env(LIB_FASTEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib"

set ::env(LIB_SLOWEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib"
```

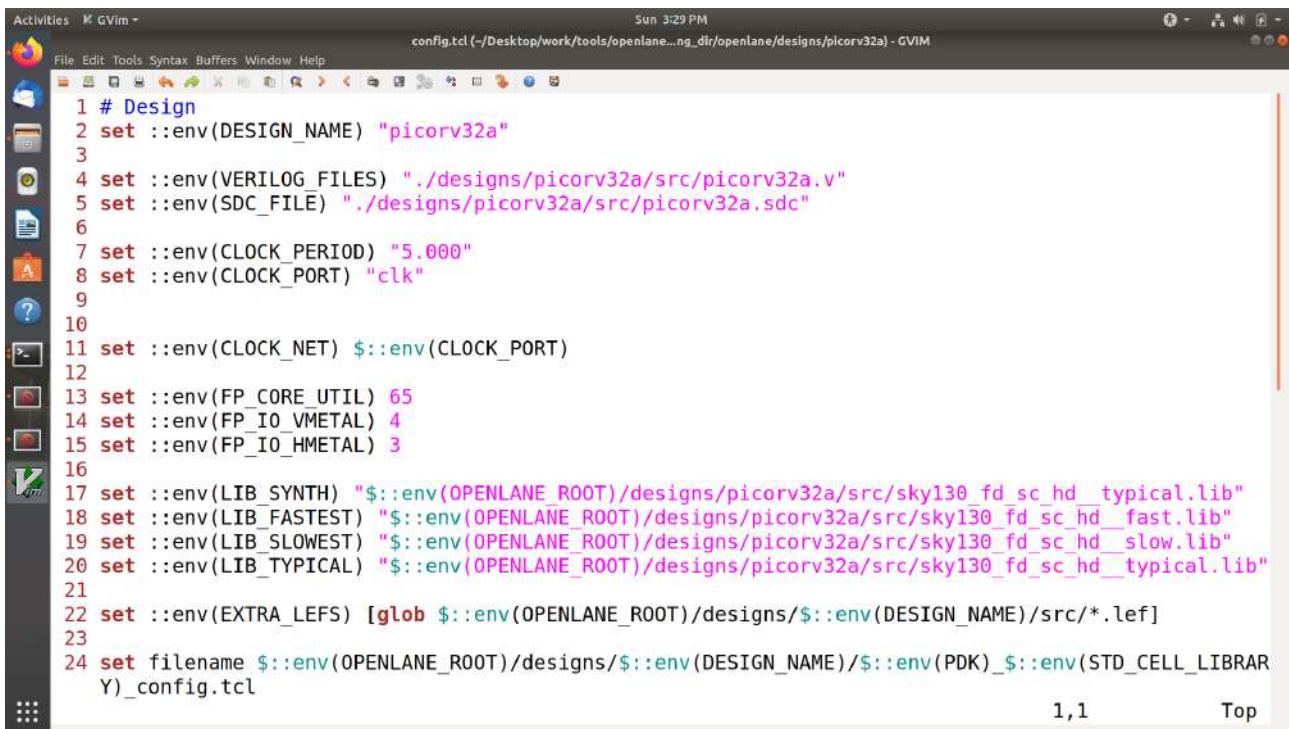
```

set ::env(LIB_TYPICAL) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/
sky130_fd_sc_hd_typical.lib"

set ::env(EXTRA_LEFS) [glob $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/
src/*.lef]

```

Edited config.tcl to include the added lef and change library to ones we added in src directory



```

Activities  M GVIM - Sun 3:29 PM config.tcl (-/Desktop/work/tools/openlane...ng_dir/openlane/designs/picorv32a) - GVIM
File Edit Tools Syntax Buffers Window Help
1 # Design
2 set ::env(DESIGN_NAME) "picorv32a"
3
4 set ::env(VERILOG_FILES) "./designs/picorv32a/src/picorv32a.v"
5 set ::env(SDC_FILE) "./designs/picorv32a/src/picorv32a.sdc"
6
7 set ::env(CLOCK_PERIOD) "5.000"
8 set ::env(CLOCK_PORT) "clk"
9
10
11 set ::env(CLOCK_NET) $::env(CLOCK_PORT)
12
13 set ::env(FP_CORE_UTIL) 65
14 set ::env(FP_IO_VMETAL) 4
15 set ::env(FP_IO_HMETAL) 3
16
17 set ::env(LIB_SYNTH) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib"
18 set ::env(LIB_FASTEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib"
19 set ::env(LIB_SLOWEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib"
20 set ::env(LIB_TYPICAL) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib"
21
22 set ::env(EXTRA_LEFS) [glob $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/src/*.lef]
23
24 set filename $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/$::env(PDK)_$::env(STD_CELL_LIBRARY)_config.tcl
1,1 Top

```

6. Run openlane flow synthesis with newly inserted custom inverter cell.

Commands to invoke the OpenLANE flow include new lef and perform synthesis

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:v0.21'
```

```
# Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command
```

```
docker
```

```
# Now that we have entered the OpenLANE flow contained docker sub-system we can invoke the OpenLANE flow in the Interactive mode using the following command
```

```
./flow.tcl -interactive
```

```
# Now that OpenLANE flow is open we have to input the required packages for proper functionality of the OpenLANE flow
```

```
package require openlane 0.9
```

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the design creating some necessary files and directories for running a specific design which in our case is 'picorv32a'
```

```
prep -design picorv32a
```

```
# Additional commands to include newly added lef to openlane flow
```

```
set lefs [glob ${::env(DESIGN_DIR)}/src/*.lef]
```

```
add_lefs -src $lefs
```

Now that the design is prepped and ready, we can run synthesis using following command

`run_synthesis`

Screenshots of commands run

Activities Terminal Sun 3:36 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```
vsduser@vsdsquadron:~$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ docker
bash-4.2$ ./flow.tcl -interactive
[INFO]:  
  
[INFO]: Version: v0.21
[INFO]: Running interactively
% package require openlane 0.9
% prep -design picorv32a
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
```

Activities Terminal Sun 3:37 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
? sky130_fd_sc_hd.lef: SITEs matched found: 0
? sky130_fd_sc_hd.lef: MACROs matched found: 437
? sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
? sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
? sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
? sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
? sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
? sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
```

```
Activities Terminal - Sun 3:37 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
::: % run_synthesis
```

```
Activities Terminal - Sun 3:45 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
::: %
```

7. Remove/reduce the newly introduced violations with the introduction of custom inverter cell by modifying design parameters.

Noting down current design values generated before modifying parameters to improve timing

```

Activities Terminal - Sun 4:00 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
sky130_fd_sc_hd_o31la_2 8
sky130_fd_sc_hd_o31a_2 19
sky130_fd_sc_hd_o31ai_2 1
sky130_fd_sc_hd_o32a_2 109
sky130_fd_sc_hd_o41a_2 2
sky130_fd_sc_hd_or2_2 1088
sky130_fd_sc_hd_or2b_2 25
sky130_fd_sc_hd_or3_2 68
sky130_fd_sc_hd_or3b_2 5
sky130_fd_sc_hd_or4_2 93
sky130_fd_sc_hd_or4b_2 6
sky130_fd_sc_hd_or4bb_2 2
sky130_vsdinv 1554

Chip area for module '\picorv32a': 147712.918400

29. Executing Verilog backend.
Dumping module '\picorv32a'.

Warnings: 307 unique messages, 307 total
End of script. Logfile hash: ea6f91c309, CPU: user 11.69s system 3.17s, MEM: 95.95 MB peak
Yosys 0.9+3621 (git sha1 84e9fa7, gcc 8.3.1 -fPIC -Os)
Time spent: 57% 2x abc (18 sec), 12% 33x opt_expr (4 sec), ...
[INFO]: Changing netlist from 0 to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis
/picorv32a.synthesis.v
[INFO]: Running Static Timing Analysis...
[INFO]: current step index: 2
OpenSTA 2.2.0-28b40207a8 Copyright (c) 2019 Basilex Software Ltd.

```

```

Activities Terminal - Sun 4:13 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.9460000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.9460000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful

```

Commands to view and change parameters to improve timing and run synthesis

Now once again we have to prep design so as to update variables

prep -design picorv32a -tag 24-03_10-03 -overwrite

```
# Addiitional commands to include newly added lef to openlane flow merged.lef
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to display current value of variable SYNTH_STRATEGY
```

```
echo $::env(SYNTH_STRATEGY)
```

```
# Command to set new value for SYNTH_STRATEGY
```

```
set ::env(SYNTH_STRATEGY) "DELAY 3"
```

```
# Command to display current value of variable SYNTH_BUFFERING to check whether it's  
enabled
```

```
echo $::env(SYNTH_BUFFERING)
```

```
# Command to display current value of variable SYNTH_SIZING
```

```
echo $::env(SYNTH_SIZING)
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Command to display current value of variable SYNTH_DRIVING_CELL to check whether it's the proper cell or not
```

```
echo $::env(SYNTH_DRIVING_CELL)
```

```
# Now that the design is prepped and ready, we can run synthesis using following command
```

```
run_synthesis
```

Screenshot of merged.lef in tmp directory with our custom inverter as macro

```
68236 MACRO Sky130_vsdinv
68237   CLASS CORE ;
68238   FOREIGN sky130_vsdinv ;
68239   ORIGIN 0.000 0.000 ;
68240   SIZE 1.380 BY 2.720 ;
68241   SITE unithd ;
68242   PIN A
68243     DIRECTION INPUT ;
68244     USE SIGNAL ;
68245     ANTENNAGATEAREA 0.193200 ;
68246     PORT
68247       LAYER l1l ;
68248       RECT 0.060 1.180 0.510 1.690 ;
68249     END
68250   END A
68251   PIN Y
68252     DIRECTION OUTPUT ;
68253     USE SIGNAL ;
68254     ANTENNADIFFAREA 0.336000 ;
68255     PORT
68256       LAYER l1l ;
68257       RECT 0.760 1.960 1.100 2.330 ;
68258       RECT 0.880 1.690 1.050 1.960 ;
68259       RECT 0.880 1.180 1.330 1.690 ;
68260       RECT 0.880 0.760 1.050 1.180 ;
```

Screenshots of commands run

```
Activities Terminal Sun 5:09 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% prep -design picorv32a -tag 24-03_10-03 -overwrite
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[WARNING]: Removing existing run /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
::: mergeLef.py : Merging LEFs
::: mergeLef.py : Merging LEFs
```

```
Activities Terminal Sun 5:09 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add lefs -src $lefs
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% echo $::env(SYNTH_STRATEGY)
AREA 0
% set ::env(SYNTH_STRATEGY) "DELAY 3"
DELAY 3
% echo $::env(SYNTH_BUFFERING)
1
% echo $::env(SYNTH_SIZING)
0
% set ::env(SYNTH_SIZING) 1
1
% echo $::env(SYNTH_DRIVING_CELL)
sky130_fd_sc_hd_inv_8
::: % run_synthesis
```

```
Activities Terminal - Sun 5:10 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
::: %
```

Comparing to previously noted run values area has increased and worst negative slack has become 0

```

Activities Terminal - Sun 5:11 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
sky130_fd_sc_hd_o32a_2 9
sky130_fd_sc_hd_o32ai_2 3
sky130_fd_sc_hd_o41ai_2 18
sky130_fd_sc_hd_or2_2 80
sky130_fd_sc_hd_or2b_2 264
sky130_fd_sc_hd_or3_2 6
sky130_fd_sc_hd_or3b_2 5
sky130_fd_sc_hd_or4_2 68
sky130_fd_sc_hd_or4b_2 4
sky130_fd_sc_hd_xnor2_2 700
sky130_fd_sc_hd_xor2_2 1164
sky130_vsdinv 1434

Chip area for module '\picorv32a': 181730.544000

29. Executing Verilog backend.
Dumping module '\picorv32a'.

Warnings: 307 unique messages, 307 total
End of script. Logfile hash: befd735e75, CPU: user 12.56s system 2.87s, MEM: 97.45 MB peak
Yosys 0.9+3621 (git sha1 84e9fa7, gcc 8.3.1 -fPIC -Os)
Time spent: 64% 2x abc (26 sec), 10% 33x opt_expr (4 sec), ...
[INFO]: Changing netlist from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis.v to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis.v
[INFO]: Running Static Timing Analysis...
[INFO]: current step index: 11
OpenSTA 2.2.0-28b10207a8 Copyright (c) 2019, Parallever Software, Inc.

```

```

Activities Terminal - Sun 5:11 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk $all_inputs_wo_clk

# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
[INFO]: % 

```

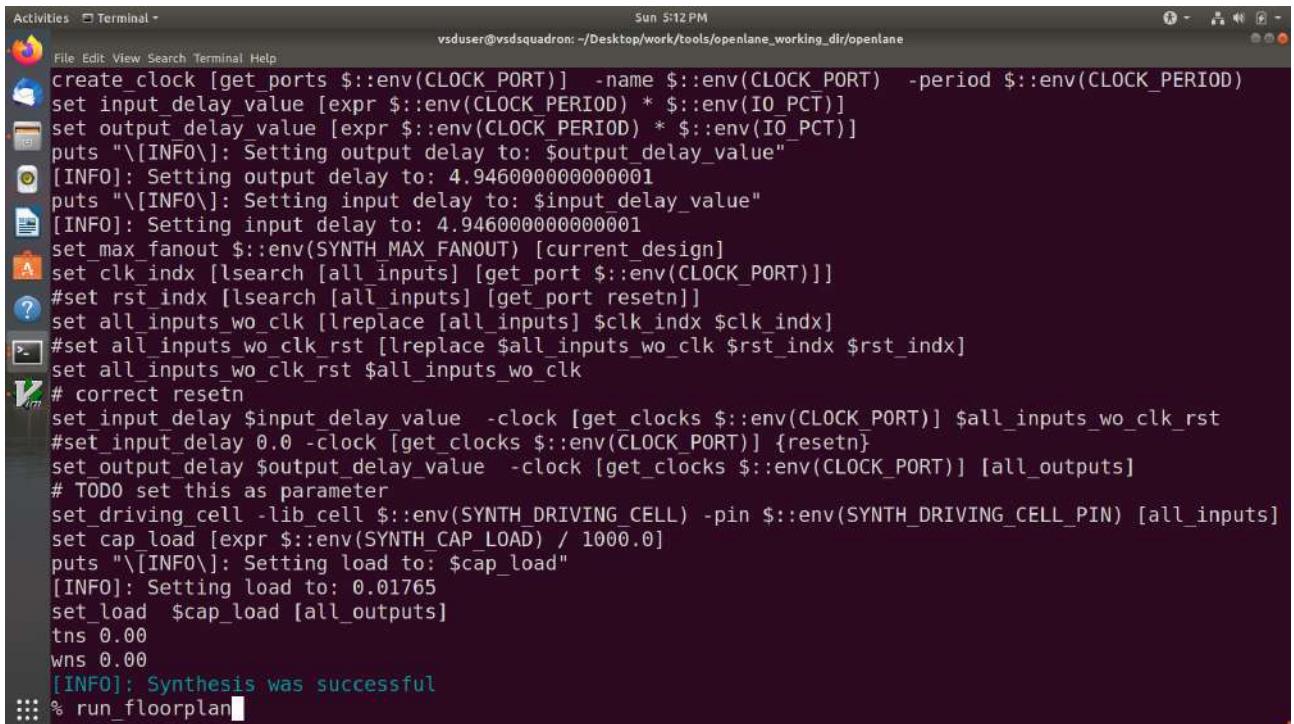
8. Once synthesis has accepted our custom inverter we can now run floorplan and placement and verify the cell is accepted in PnR flow.

Now that our custom inverter is properly accepted in synthesis we can now run floorplan using following command

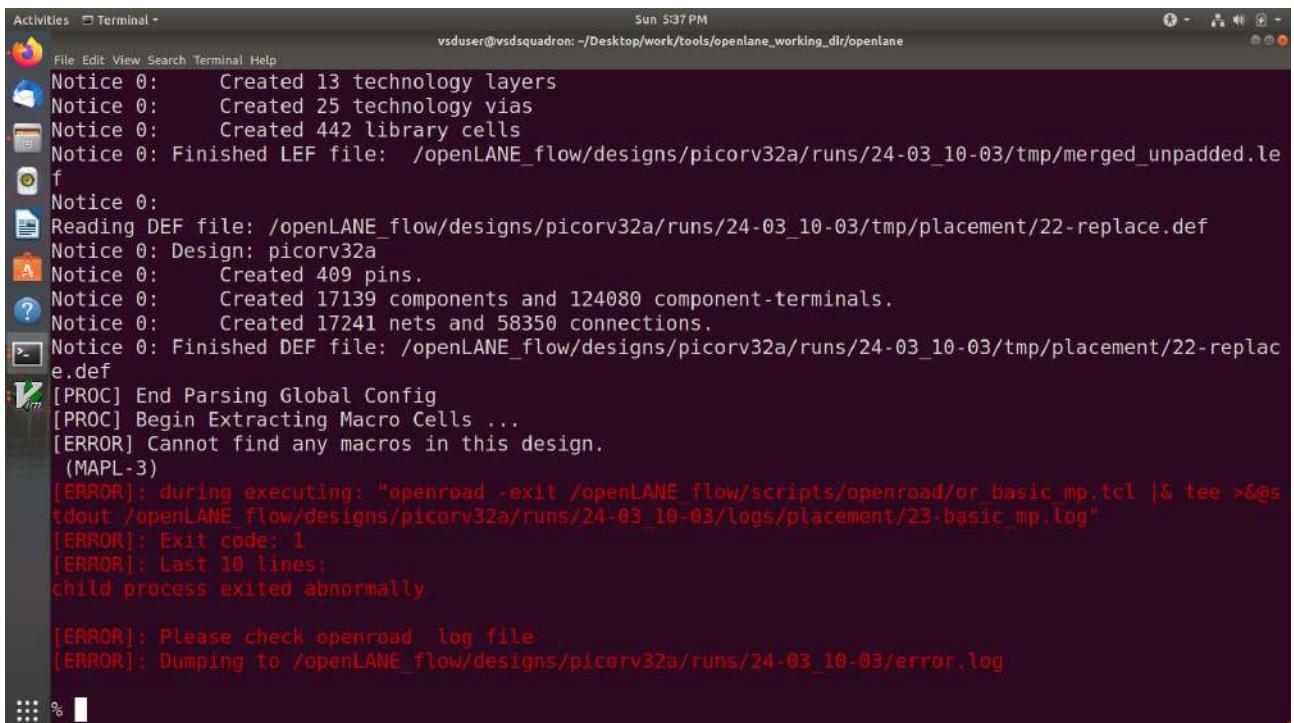
Now we can run floorplan

run_floorplan

Screenshots of command run



```
Activities Terminal Sun 5:12 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
:: % run_floorplan
```



```
Activities Terminal Sun 5:37 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/22-replace.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/22-replace.def
:[PROC] End Parsing Global Config
:[PROC] Begin Extracting Macro Cells ...
[ERROR] Cannot find any macros in this design.
(MAPL-3)
[ERROR]: during executing: "openroad -exit /openLANE_flow/scripts/openroad/or_basic_mp.tcl |& tee >& stdout /openLANE_flow/designs/picorv32a/runs/24-03_10-03/logs/placement/23-basic_mp.log"
[ERROR]: Exit code: 1
[ERROR]: Last 10 lines:
child process exited abnormally

[ERROR]: Please check openroad log file
[ERROR]: Dumping to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/error.log
:: %
```

Since we are facing unexpected un-explainable error while using run_floorplan command, we can instead use the following set of commands available based on information from Desktop/work/tools/openlane_working_dir/openlane/scripts/tcl_commands/floorplan.tcl and also based on Floorplan Commands section in Desktop/work/tools/openlane_working_dir/openlane/docs/source/OpenLANE_commands.md

Following commands are altogether sourced in "run_floorplan" command

init_floorplan

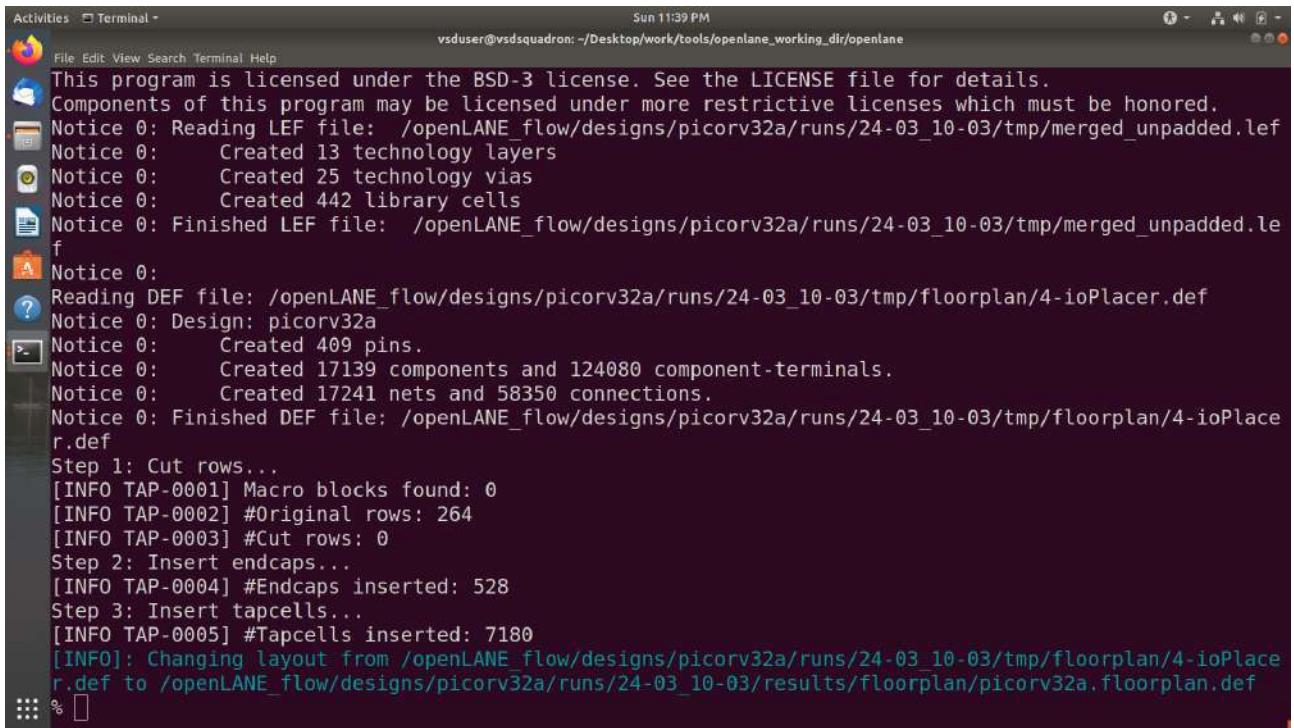
place_io

tap_decap_or

Screenshots of commands run

```
Activities Terminal Sun 11:38 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
% init_floorplan
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 3
OpenROAD 0.9.0 1415572a73
A This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
[INFO IFP-0001] Added 264 rows of 1566 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 731.615 742.335 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/3-verilog2def.die_area.rpt.
[INFO] Floorplanned on a core area of 5.52 10.88 725.88 728.96 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/3-verilog2def.core_area.rpt.
[INFO]: Core area width: 720.36
[INFO]: Core area height: 718.08
[INFO]: Changing layout from 0 to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def
::: % place_io
```

```
Activities Terminal Sun 11:38 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% place_io
[INFO]: Running IO Placement...
[INFO]: current step index: 4
OpenROAD 0.9.0 1415572a73
A This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def
#Macro blocks found: 0
Using 5u default boundaries offset
Random pin placement
RandomMode Even
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
::: % tap_decap_or
```



```
Sun 11:39 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 17139 components and 124080 component-terminals.
Notice 0:     Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Step 1: Cut rows...
[INFO TAP-0001] Macro blocks found: 0
[INFO TAP-0002] #Original rows: 264
[INFO TAP-0003] #Cut rows: 0
Step 2: Insert endcaps...
[INFO TAP-0004] #Endcaps inserted: 528
Step 3: Insert tapcells...
[INFO TAP-0005] #Tapcells inserted: 7180
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/floorplan/picorv32a.floorplan.def
```

Now that floorplan is done we can do placement using following command

Now we are ready to run placement

run_placement

Screenshots of command run

```

Activities Terminal Sun 11:49 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 17139 components and 124080 component-terminals.
Notice 0:     Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Step 1: Cut rows...
[INFO TAP-0001] Macro blocks found: 0
[INFO TAP-0002] #Original rows: 264
[INFO TAP-0003] #Cut rows: 0
Step 2: Insert endcaps...
[INFO TAP-0004] #Endcaps inserted: 528
Step 3: Insert tapcells...
[INFO TAP-0005] #Tapcells inserted: 7180
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/floorplan/picorv32a.floorplan.def
::: % run_placement

```

```

Activities Terminal Sun 11:51 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
legalized HPWL      910806.5 u
delta HPWL           2 %
[INFO DPL-0020] Mirrored 6650 instances
[INFO DPL-0021] HPWL before          910806.5 u
[INFO DPL-0022] HPWL after           895297.0 u
[INFO DPL-0023] HPWL delta           -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/6-resizer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 10
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
::: %

```

Commands to load placement def in magic in another terminal

Change directory to path containing generated placement def

```

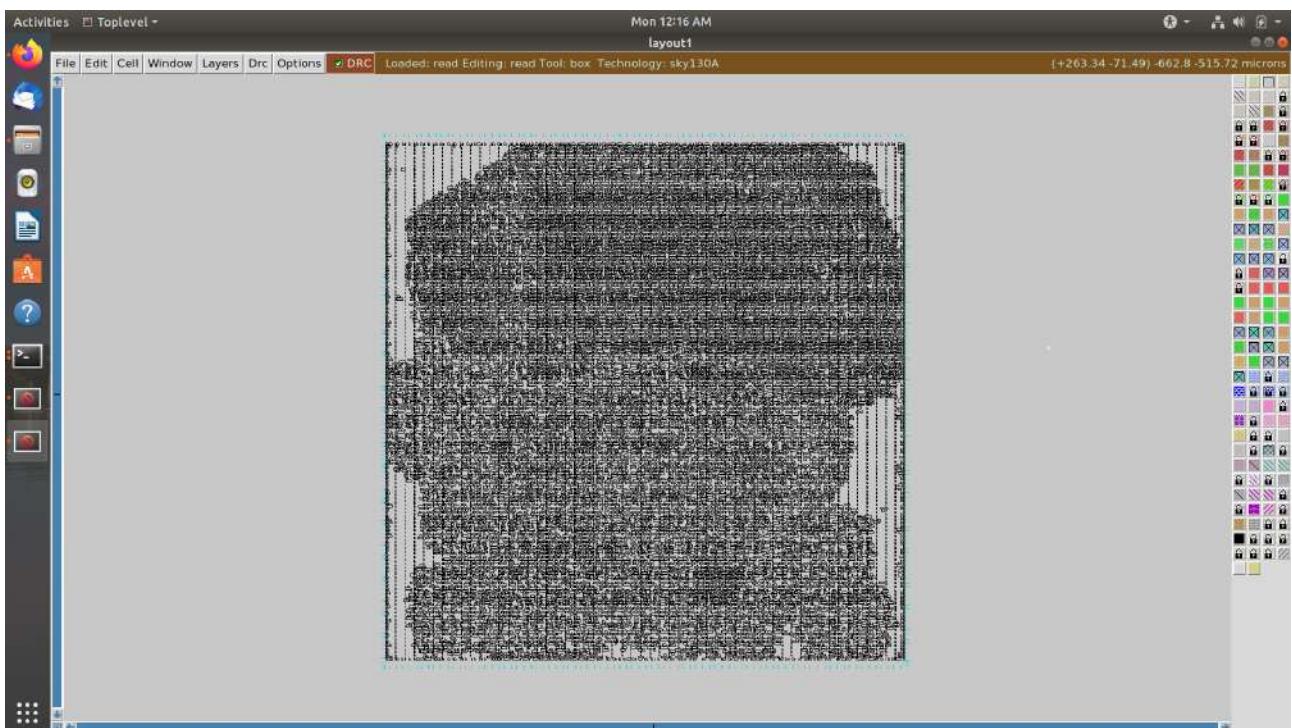
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
24-03_10-03/results/placement/

```

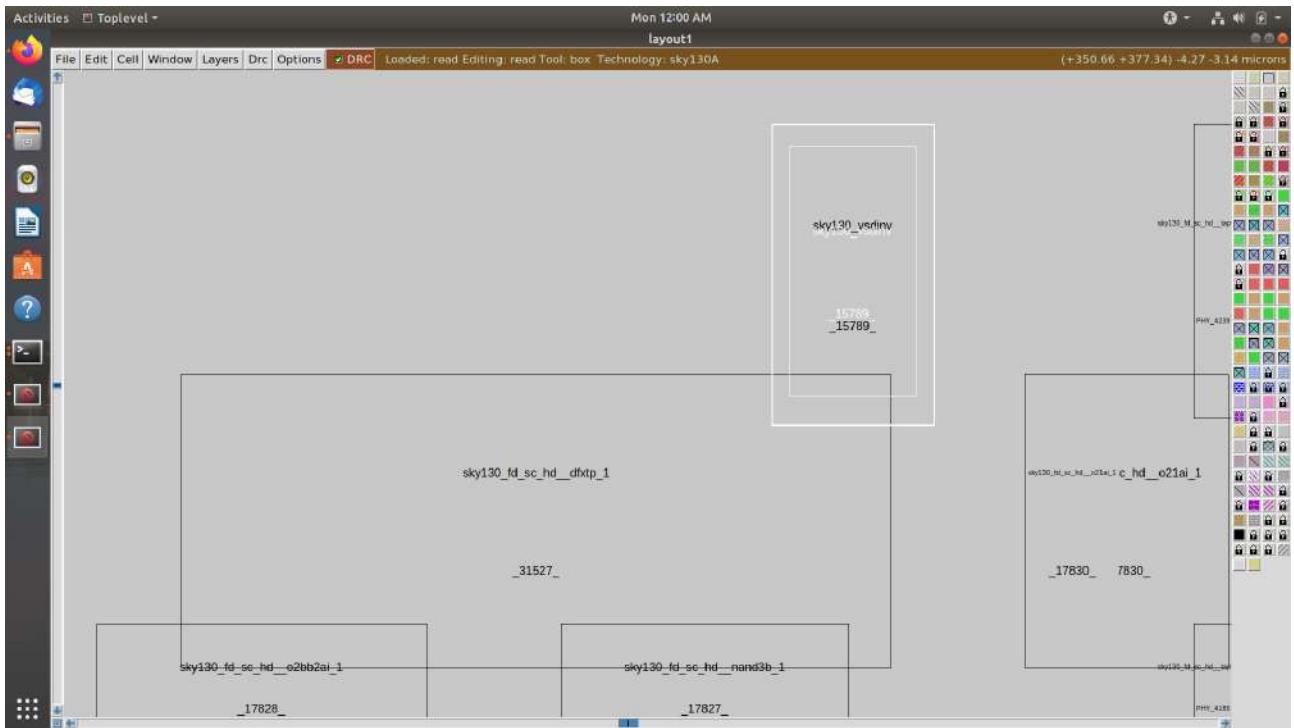
```
# Command to load the placement def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def  
&
```

Screenshot of placement def in magic



Screenshot of custom inverter inserted in placement def with proper abutment

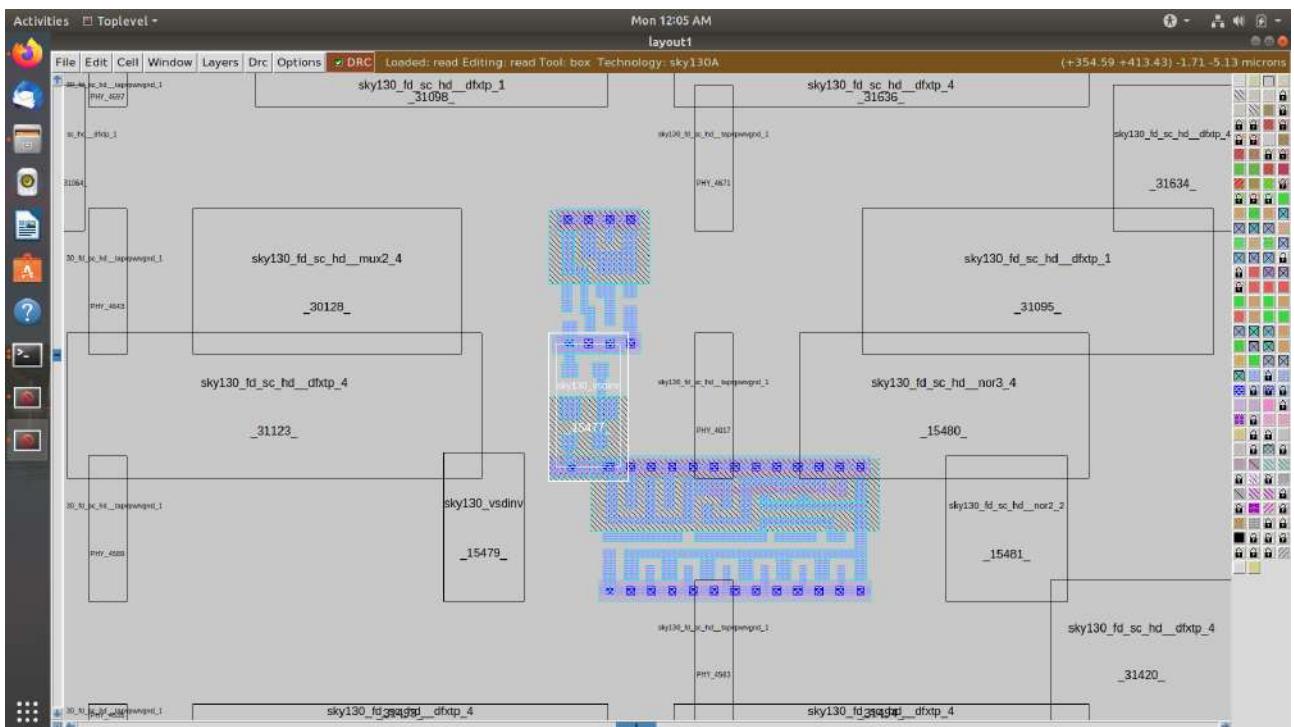
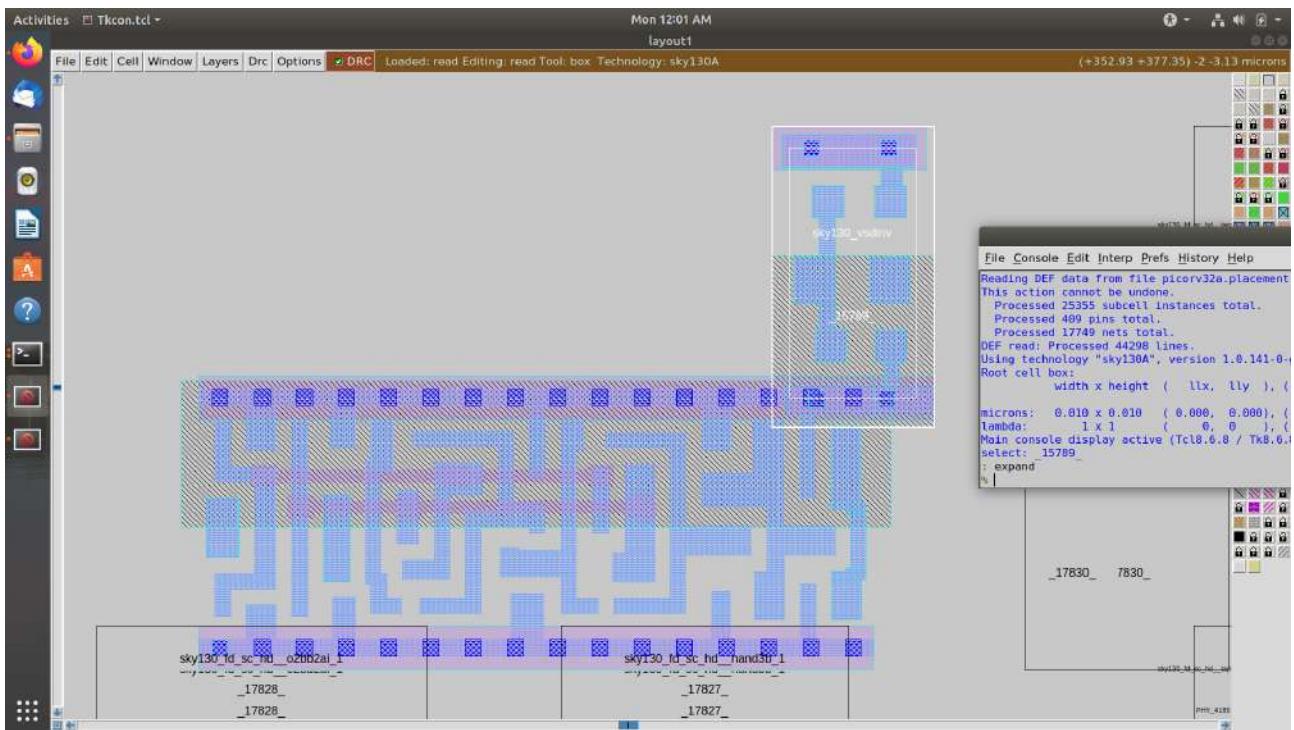


Command for tkcon window to view internal layers of cells

```
# Command to view internal connectivity layers
```

```
expand
```

Abutment of power pins with other cell from library clearly visible



9. Do Post-Synthesis timing analysis with OpenSTA tool.

Since we are having own after improved timing run we are going to do timing analysis on initial run of synthesis which has lots of violations and no parameters were added to improve timing

Commands to invoke the OpenLANE flow include new lef and perform synthesis

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:vo.21'
```

Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command

```
docker
```

Now that we have entered the OpenLANE flow contained docker sub-system we can invoke the OpenLANE flow in the Interactive mode using the following command

```
./flow.tcl -interactive
```

Now that OpenLANE flow is open we have to input the required packages for proper functionality of the OpenLANE flow

```
package require openlane 0.9
```

Now the OpenLANE flow is ready to run any design and initially we have to prep the design creating some necessary files and directories for running a specific design which in our case is 'picorv32a'

```
prep -design picorv32a
```

```
# Additional commands to include newly added lef to openlane flow
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Now that the design is prepped and ready, we can run synthesis using following command
```

```
run_synthesis
```

Commands run final screenshot

```
Activities Terminal Tue 5:52 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
```

Newly created pre_sta.conf for STA analysis in openlane directory

Newly created `my_base.sdc` for STA analysis in `openlane/designs/picorv32a/src` directory based on the file `openlane/scripts/base.sdc`

```
Activities  M GVim - Tue 5:55 AM my_base.sdc (~Desktop/work/tools/openlane/openlane/designs/picorv32a/src) - GVIM1
File Edit Tools Syntax Buffers Window Help
1 set ::env(CLOCK_PORT) cLK
2 set ::env(CLOCK_PERIOD) 24.73
3 #set ::env(SYNTH_DRIVING_CELL) sky130_vsdinv
4 set ::env(SYNTH_DRIVING_CELL) sky130_fd_sc_hd_inv_8
5 set ::env(SYNTH_DRIVING_CELL_PIN) Y
6 set ::env(SYNTH_CAP_LOAD) 17.653
7 set ::env(IO_PCT) 0.2
8 set ::env(SYNTH_MAX_FANOUT) 6
9
10 create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
11 set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
12 set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
13 puts "\[INFO\]: Setting output delay to: $output_delay_value"
14 puts "\[INFO\]: Setting input delay to: $input_delay_value"
15
16 set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
17
18 set clk_idx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
19 #set rst_idx [lsearch [all_inputs] [get_port resetn]]
20 set all_inputs_wo_clk [lreplace [all_inputs] $clk_idx $clk_idx]
21 #set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_idx $rst_idx]
22 set all_inputs_wo_clk_rst $all_inputs_wo_clk
23
24 # correct resetn
```

24,16

Top

```
Activities  M GVim - Tue 5:55 AM my_base.sdc (~Desktop/work/tools/openlane/openlane/designs/picorv32a/src) - GVIM1
File Edit Tools Syntax Buffers Window Help
24 # correct resetn
25 set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
26 #set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
27 set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
28
29 # TODO set this as parameter
30 set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
31 set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
32 puts "\[INFO\]: Setting load to: $cap_load"
33 set_load $cap_load [all_outputs]
```

25,16

Bot

Commands to run STA in another terminal

```
# Change directory to openlane
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# Command to invoke OpenSTA tool with script
```

```
sta pre_sta.conf
```

Screenshots of commands run

```
Activities Terminal Tue 6:04 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ sta pre_sta.conf
OpenSTA 2.4.0 ac3479bc24 Copyright (c) 2021, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type `show copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type `show warranty'.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib line 24, default_fanout_load is 0.0.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib line 23, default_fanout_load is 0.0.
[INFO]: Setting output delay to: 4.946000000000001
[INFO]: Setting input delay to: 4.946000000000001
[INFO]: Setting load to: 0.017653
Startpoint: _26669_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _26669_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _26669/_0 (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.00  0.00  cpuregs[0][0] (net)
          0.03  0.00  0.00 ^ _15938/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _15938/_X (sky130_fd_sc_hd_buf_1)
          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _26669/_D (sky130_fd_sc_hd_dfxtp_2)
          0.02  0.00  0.23  data arrival time

          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  library hold time
          -0.02 -0.02  data required time

          -0.02  data required time
          -0.23  data arrival time

          0.24  slack (MET)
```

```
Activities Terminal Tue 6:05 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _26669/_0 (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.00  0.00  cpuregs[0][0] (net)
          0.03  0.00  0.00 ^ _15938/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _15938/_X (sky130_fd_sc_hd_buf_1)
          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _26669/_D (sky130_fd_sc_hd_dfxtp_2)
          0.02  0.00  0.23  data arrival time

          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  library hold time
          -0.02 -0.02  data required time

          -0.02  data required time
          -0.23  data arrival time

          0.24  slack (MET)

          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  library hold time
          -0.02 -0.02  data required time

          -0.02  data required time
          -0.23  data arrival time

          0.24  slack (MET)

          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  library hold time
          -0.02 -0.02  data required time

          -0.02  data required time
          -0.23  data arrival time

          0.24  slack (MET)
```

```

Activities Terminal - Tue 6:05 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
Startpoint: _27860_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _27762_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
-----
          0.00 0.00 0.00 clock clk (rise edge)
          0.00 0.00 0.00 clock network delay (ideal)
          0.00 0.00 0.00 ^ _27860/_CLK (sky130_fd_sc_hd_dfxtp_2)
          0.10 0.64 0.64 ^ _27860/_Q (sky130_fd_sc_hd_dfxtp_2)
          4   0.01      irq_mask[1] (net)
          0.10 0.00 0.64 ^ _13108/_A (sky130_vsdinv)
          0.13 0.15 0.79 v _13108/_Y (sky130_vsdinv)
          6   0.01      _10510_ (net)
          0.13 0.00 0.79 v _13113/_A1 (sky130_fd_sc_hd_a221o_2)
          0.08 0.65 1.44 v _13113/_X (sky130_fd_sc_hd_a221o_2)
          1   0.00      _10515_ (net)
          0.08 0.00 1.44 v _13132/_A (sky130_fd_sc_hd_or4_2)
          0.21 1.53 2.98 v _13132/_X (sky130_fd_sc_hd_or4_2)
          1   0.00      _10534_ (net)
          0.21 0.00 2.98 v _13160/_A1 (sky130_fd_sc_hd_o2111a_2)
          0.07 0.54 3.52 v _13160/_X (sky130_fd_sc_hd_o2111a_2)
          2   0.00      _10562_ (net)
          0.07 0.00 3.52 v _13161/_C (sky130_fd_sc_hd_or3_2)
          0.17 0.97 4.48 v _13161/_X (sky130_fd_sc_hd_or3_2)
          2   0.00      _10563_ (net)
          0.17 0.00 4.48 v _13164/_A (sky130_fd_sc_hd_or2_2)

```

```

Activities Terminal - Tue 6:08 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
          0.14 0.68 47.22 v _13750/_X (sky130_fd_sc_hd_or2_2)
          3   0.01      10970_ (net)
          0.14 0.00 47.22 v _13751/_B (sky130_fd_sc_hd_or2_2)
          0.12 0.66 47.88 v _13751/_X (sky130_fd_sc_hd_or2_2)
          2   0.00      10971_ (net)
          0.12 0.00 47.88 v _13754/_B2 (sky130_fd_sc_hd_o221a_2)
          0.07 0.44 48.32 v _13754/_X (sky130_fd_sc_hd_o221a_2)
          1   0.00      03928_ (net)
          0.07 0.00 48.32 v _27762/_D (sky130_fd_sc_hd_dfxtp_2)
          48.32 data arrival time
          0.00 24.73 24.73 clock clk (rise edge)
          0.00 24.73 24.73 clock network delay (ideal)
          0.00 24.73 24.73 clock reconvergence pessimism
          24.73 ^ _27762/_CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.29 24.44 library setup time
          24.44 data required time
          24.44 data required time
          -48.32 data arrival time
          -23.89 slack (VIOLATED)

tns -711.59
wns -23.89
%
```

Since more fanout is causing more delay we can add parameter to reduce fanout and do synthesis again

Commands to include new lef and perform synthesis

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the  
design creating some necessary files and directories for running a specific design which in  
our case is 'picorv32a'
```

```
prep -design picorv32a -tag 25-03_18-52 -overwrite
```

```
# Additional commands to include newly added lef to openlane flow
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Command to set new value for SYNTH_MAX_FANOUT
```

```
set ::env(SYNTH_MAX_FANOUT) 4
```

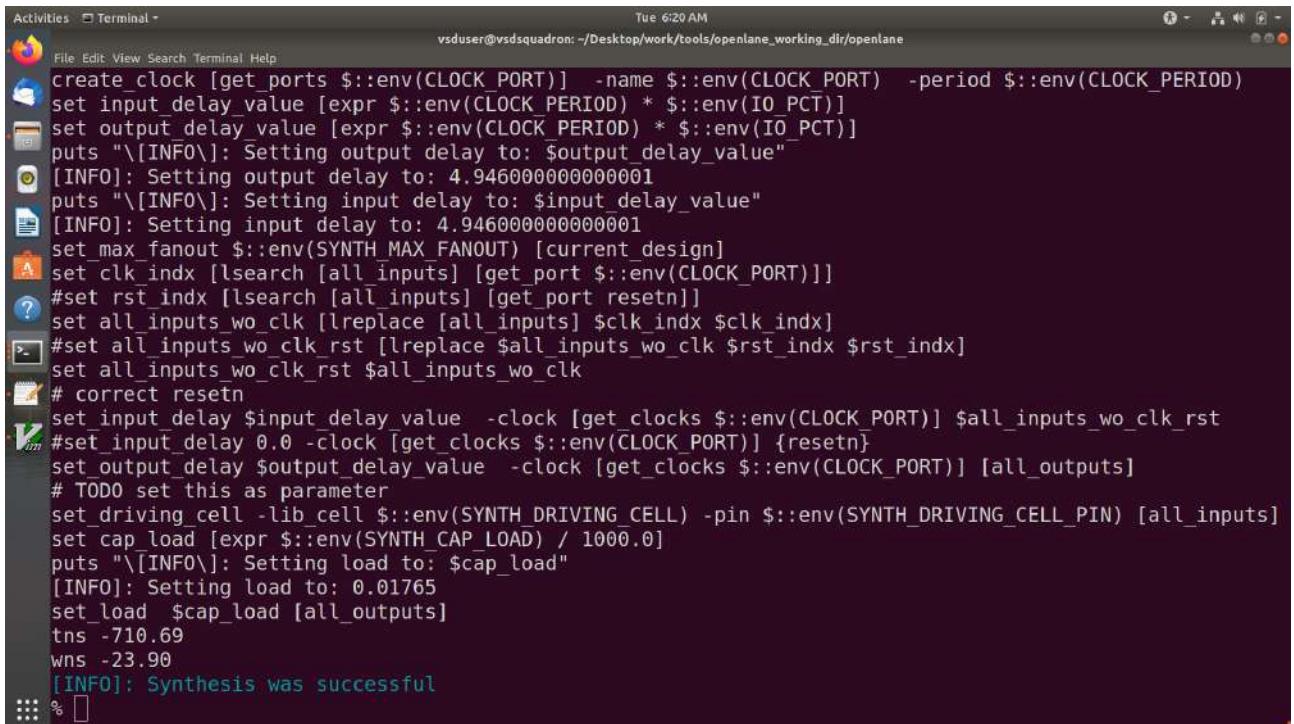
```
# Command to display current value of variable SYNTH_DRIVING_CELL to check whether  
it's the proper cell or not
```

```
echo $::env(SYNTH_DRIVING_CELL)
```

```
# Now that the design is prepped and ready, we can run synthesis using following  
command
```

run_synthesis

Commands run final screenshot



A screenshot of a terminal window titled "Terminal". The window shows a series of commands being run and their corresponding output. The commands relate to setting clock ports, input and output delays, and driving cell parameters. The output includes several "[INFO]" messages indicating the progress of the synthesis process, such as "Setting output delay to: 4.946000000000001" and "Synthesis was successful". The terminal window has a dark background with light-colored text.

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -710.69
wns -23.90
[INFO]: Synthesis was successful
```

Commands to run STA in another terminal

```
# Change directory to openlane
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# Command to invoke OpenSTA tool with script
```

```
sta pre_sta.conf
```

Screenshots of commands run

```

Activities Terminal - Tue 6:22 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ sta pre_sta.conf
OpenSTA 2.4.0 ac3479bc24 Copyright (c) 2021, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type `show copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type `show warranty'.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib line 24, default_fanout_load is 0.0.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib line 23, default_fanout_load is 0.0.
[INFO]: Setting output delay to: 4.9460000000000001
[INFO]: Setting input delay to: 4.9460000000000001
[INFO]: Setting load to: 0.017653
Startpoint: _29347_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _29347_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _29347_/Q (sky130_fd_sc_hd_dfxtp_2)
          2   0.00          cpuregs[0][0] (net)
          0.02  0.00  0.10 ^ _17885/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _17885/_X (sky130_fd_sc_hd_buf_1)
          1   0.00          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _29347/_D (sky130_fd_sc_hd_dfxtp_2)
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data required time
          -0.23 -0.23  0.00  data arrival time
          0.24  slack (MET)

```

```

Activities Terminal - Tue 6:22 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _29347_/Q (sky130_fd_sc_hd_dfxtp_2)
          2   0.00          cpuregs[0][0] (net)
          0.03  0.00  0.18 ^ _17885/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _17885/_X (sky130_fd_sc_hd_buf_1)
          1   0.00          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _29347/_D (sky130_fd_sc_hd_dfxtp_2)
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data required time
          -0.23 -0.23  0.00  data arrival time
          0.24  slack (MET)

```

Activities Terminal - Tue 6:22 AM
 vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```

Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00 ^ _29052_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.06  0.58  0.58 v _29052/_Q (sky130_fd_sc_hd_dfxtp_2)
          4   0.01           irq_pending[3] (net)
          0.06  0.00  0.58 v _14460/_A (sky130_vsdinv)
          0.19  0.17  0.75 ^ _14460/_Y (sky130_vsdinv)
          3   0.01           _11622_ (net)
          0.19  0.00  0.75 ^ _14461/_B2 (sky130_fd_sc_hd_o22ai_2)
          0.09  0.14  0.89 v _14461/_Y (sky130_fd_sc_hd_o22ai_2)
          1   0.00           _11623_ (net)
          0.09  0.00  0.89 v _14462/_C1 (sky130_fd_sc_hd_a221o_2)
          0.08  0.55  1.44 v _14462/_X (sky130_fd_sc_hd_a221o_2)
          1   0.00           _11624_ (net)
          0.08  0.00  1.44 v _14481/_A (sky130_fd_sc_hd_or4_2)
          0.21  1.53  2.97 v _14481/_X (sky130_fd_sc_hd_or4_2)
          1   0.00           _11643_ (net)
          0.21  0.00  2.97 v _14509/_A1 (sky130_fd_sc_hd_o2111a_2)
          0.07  0.54  3.51 v _14509/_X (sky130_fd_sc_hd_o2111a_2)
          2   0.00
  
```

Activities Terminal - Tue 6:23 AM
 vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```

          0.14  0.68  47.23 v _15226/_X (sky130_fd_sc_hd_or2_2)
          3   0.01           _12208_ (net)
          0.14  0.00  47.23 v _15227/_B (sky130_fd_sc_hd_or2_2)
          0.12  0.66  47.89 v _15227/_X (sky130_fd_sc_hd_or2_2)
          2   0.00           _12209_ (net)
          0.12  0.00  47.89 v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
          0.07  0.44  48.33 v _15230/_X (sky130_fd_sc_hd_o221a_2)
          1   0.00           _03928_ (net)
          0.07  0.00  48.33 v _30440/_D (sky130_fd_sc_hd_dfxtp_2)
          48.33 data arrival time
          0.00  24.73  24.73  clock clk (rise edge)
          0.00  24.73  24.73  clock network delay (ideal)
          0.00  24.73  24.73  clock reconvergence pessimism
          24.73 ^ _30440_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.29 24.44  24.44  library setup time
          24.44 24.44  24.44  data required time
          24.44 data required time
          -48.33 data arrival time
  ----- -23.90 slack (VIOLATED)

tns -710.69
wns -23.90
  
```

10. Make timing ECO fixes to remove all violations.

OR gate of drive strength 2 is driving 4 fanouts

Activities Terminal Tue 6:55 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

		0.19	0.00	0.75	^ _14461 /B2 (sky130_fd_sc_hd_o22ai_2)
1	0.00	0.09	0.14	0.89 v	_14461 /Y (sky130_fd_sc_hd_o22ai_2)
					11623 (net)
		0.09	0.00	0.89 v	_14462 /C1 (sky130_fd_sc_hd_a22lo_2)
1	0.00	0.08	0.55	1.44 v	_14462 /X (sky130_fd_sc_hd_a22lo_2)
					11624 (net)
		0.08	0.00	1.44 v	_14481 /A (sky130_fd_sc_hd_or4_2)
1	0.00	0.21	1.53	2.97 v	_14481 /X (sky130_fd_sc_hd_or4_2)
					11643 (net)
		0.21	0.00	2.97 v	_14509 /A1 (sky130_fd_sc_hd_o2111a_2)
2	0.00	0.07	0.54	3.51 v	_14509 /X (sky130_fd_sc_hd_o2111a_2)
					11671 (net)
		0.07	0.00	3.51 v	_14510 /C (sky130_fd_sc_hd_or3_2)
4	0.01	0.21	1.04	4.55 v	_14510 /X (sky130_fd_sc_hd_or3_2)
					11672 (net)
		0.21	0.00	4.55 v	_14513 /A (sky130_fd_sc_hd_or2_2)
2	0.00	0.11	0.71	5.26 v	_14513 /X (sky130_fd_sc_hd_or2_2)
					11674 (net)
		0.11	0.00	5.26 v	_14514 /C (sky130_fd_sc_hd_or3_2)
4	0.01	0.20	1.03	6.29 v	_14514 /X (sky130_fd_sc_hd_or3_2)
					11675 (net)
		0.20	0.00	6.29 v	_15166 /B (sky130_fd_sc_hd_or2_2)
2	0.00	0.11	0.67	6.96 v	_15166 /X (sky130_fd_sc_hd_or2_2)
					12148 (net)
		0.11	0.00	6.96 v	_15167 /C (sky130_fd_sc_hd_or3_2)
2	0.00	0.17	0.98	7.94 v	_15167 /X (sky130_fd_sc_hd_or3_2)
					12149 (net)
		0.17	0.00	7.94 v	_15168 /B (sky130_fd_sc_hd_or2_2)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

report_net -connections _11672_

Checking command syntax

help replace_cell

Replacing cell

replace_cell _14510_ sky130_fd_sc_hd_or3_4

Generating custom timing report

```
report_checks -fields {net cap slew input_pins} -digits 4
```

Result - slack reduced

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
----- [-23.90 slack (VIOLATED)]
tns -710.69
wns -23.90
% report_net -connections _11672_
Net _11672_
Driver pins
_14510 /X output (sky130_fd_sc_hd_or3_2)
Load pins
_14513 /A input (sky130_fd_sc_hd_or2_2)
_15505 /B input (sky130_fd_sc_hd_or2_2)
_18231 /A input (sky130_fd_sc_hd_buf_1)
_18326 /B input (sky130_fd_sc_hd_nand2_2)

% help replace_cell
replace_cell instance lib_cell
% replace_cell _14510_ sky130_fd_sc_hd_or3_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Fanout Cap Slew Delay Time Description
```

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Fanout Cap Slew Delay Time Description
-----[clock clk (rise edge)
          0.0000 0.0000 0.0000
          0.0000 0.0000 0.0000 ^ _29052/_CLK (sky130_fd_sc_hd_dfxtp_2)
          0.0572 0.5830 0.5830 v _29052/_Q (sky130_fd_sc_hd_dfxtp_2)
          irq_pending[3] (net)
          4 0.0067
          0.0572 0.0000 0.5830 v _14460/_A (sky130_vsdinv)
          0.1856 0.1667 0.7497 ^ _14460/_Y (sky130_vsdinv)
          11622_ (net)
          3 0.0138
          0.1856 0.0000 0.7497 ^ _14461/_B2 (sky130_fd_sc_hd_o22ai_2)
          0.0878 0.1436 0.8933 v _14461/_Y (sky130_fd_sc_hd_o22ai_2)
          11623_ (net)
          1 0.0021
          0.0878 0.0000 0.8933 v _14462/_C1 (sky130_fd_sc_hd_a221o_2)
          0.0784 0.5469 1.4402 v _14462/_X (sky130_fd_sc_hd_a221o_2)
          11624_ (net)
          1 0.0013
          0.0784 0.0000 1.4402 v _14481/_A (sky130_fd_sc_hd_or4_2)
          0.2106 1.5344 2.9746 v _14481/_X (sky130_fd_sc_hd_or4_2)
          11643_ (net)
          1 0.0024
          0.2106 0.0000 2.9746 v _14509/_A1 (sky130_fd_sc_hd_o2111a_2)
          0.0792 0.5466 3.5212 v _14509/_X (sky130_fd_sc_hd_o2111a_2)
          11671_ (net)]
```

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

Tue 9:42 AM

3	0.0138	0.1856	0.0000	0.7497	^ _11622_ (net)
		0.0878	0.1436	0.8933	v _14461/_B2 (sky130_fd_sc_hd_o22ai_2)
1	0.0021	0.0878	0.0000	0.8933	v _14461/_Y (sky130_fd_sc_hd_o22ai_2)
		0.0784	0.5469	1.4402	v _11623_ (net)
1	0.0013	0.0784	0.0000	1.4402	v _14462/_C1 (sky130_fd_sc_hd_a221o_2)
		0.2106	1.5344	2.9746	v _14462/_X (sky130_fd_sc_hd_a221o_2)
1	0.0024	0.2106	0.0000	2.9746	v _11624_ (net)
		0.0792	0.5466	3.5212	v _14481/_A (sky130_fd_sc_hd_or4_2)
2	0.0044	0.0792	0.0000	3.5212	v _14481/_X (sky130_fd_sc_hd_or4_2)
		0.1349	0.6755	4.1967	v _11643_ (net)
4	0.0089	0.1349	0.0000	4.1967	v _14509/_A1 (sky130_fd_sc_hd_o2111a_2)
		0.1121	0.6770	4.8737	v _14509/_X (sky130_fd_sc_hd_o2111a_2)
2	0.0025	0.1121	0.0000	4.8737	v _11671_ (net)
		0.1967	1.0321	5.9057	v _14514/_C (sky130_fd_sc_hd_or3_2)
4	0.0070	0.1967	0.0000	5.9057	v _14514/_X (sky130_fd_sc_hd_or3_2)
		0.1148	0.6684	6.5742	v _11675_ (net)
2	0.0032	0.1148	0.0000	6.5742	v _15166/_B (sky130_fd_sc_hd_or2_2)
		0.1692	0.9831	7.5573	v _15166/_X (sky130_fd_sc_hd_or2_2)
2	0.0025	0.0000	0.0000	7.5573	v _12148_ (net)
		0.0000	0.0000	7.5573	v _15167/_C (sky130_fd_sc_hd_or3_2)
		0.0000	0.0000	7.5573	v _15167/_X (sky130_fd_sc_hd_or3_2)
		0.0000	0.0000	7.5573	v _12149_ (net)

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

Tue 7:07 AM

2	0.0035	0.1162	0.0000	46.1648	v _12207_ (net)
		0.1421	0.6813	46.8462	v _15226/_B (sky130_fd_sc_hd_or2_2)
3	0.0079	0.1421	0.0000	46.8462	v _15226/_X (sky130_fd_sc_hd_or2_2)
		0.1228	0.6610	47.5072	v _12208_ (net)
2	0.0044	0.1228	0.0000	47.5072	v _15227/_B (sky130_fd_sc_hd_or2_2)
		0.0713	0.4381	47.9453	v _15227/_X (sky130_fd_sc_hd_or2_2)
1	0.0016	0.0713	0.0000	47.9453	v _12209_ (net)
		0.0000	24.7300	24.7300	v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
		0.0000	24.7300	24.7300	v _15230/_X (sky130_fd_sc_hd_o221a_2)
		0.0000	24.7300	24.7300	v _03928_ (net)
		0.0000	24.7300	24.7300	v _30440/_D (sky130_fd_sc_hd_dfxtip_2)
		0.0000	24.7300	24.7300	v data arrival time
		0.0000	24.7300	24.7300	v clock clk (rise edge)
		0.0000	24.7300	24.7300	v clock network delay (ideal)
		0.0000	24.7300	24.7300	v clock reconvergence pessimism
		24.7300	24.7300	24.7300	v ^ _30440/_CLK (sky130_fd_sc_hd_dfxtip_2)
		-0.2939	24.4361	24.4361	v library setup time
		-0.2939	24.4361	24.4361	v data required time
		24.4361	24.4361	24.4361	v data arrival time
		24.4361	24.4361	24.4361	v slack (VIOLATED)
		-47.9453	-47.9453	-47.9453	v -23.5092 slack (VIOLATED)

OR gate of drive strength 2 is driving 4 fanouts

Activities Terminal Tue 9:46 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

		0.2106	1.5344	2.9746 v	_14481/_X (sky130_fd_sc_hd_or4_2)
1	0.0024				11643 (net)
		0.2106	0.0000	2.9746 v	_14509/_A1 (sky130_fd_sc_hd_o2111a_2)
		0.0792	0.5466	3.5212 v	_14509/_X (sky130_fd_sc_hd_o2111a_2)
2	0.0044				11671 (net)
		0.0792	0.0000	3.5212 v	_14510/_C (sky130_fd_sc_hd_or3_4)
		0.1349	0.6755	4.1967 v	_14510/_X (sky130_fd_sc_hd_or3_4)
4	0.0089				11672 (net)
		0.1349	0.0000	4.1967 v	_14513/_A (sky130_fd_sc_hd_or2_2)
		0.1121	0.6770	4.8737 v	_14513/_X (sky130_fd_sc_hd_or2_2)
2	0.0025				11674 (net)
		0.1121	0.0000	4.8737 v	_14514/_C (sky130_fd_sc_hd_or3_2)
		0.1967	1.0321	5.9057 v	_14514/_X (sky130_fd_sc_hd_or3_2)
4	0.0070				11675 (net)
		0.1967	0.0000	5.9057 v	_15166/_B (sky130_fd_sc_hd_or2_2)
		0.1148	0.6684	6.5742 v	_15166/_X (sky130_fd_sc_hd_or2_2)
2	0.0032				12148 (net)
		0.1148	0.0000	6.5742 v	_15167/_C (sky130_fd_sc_hd_or3_2)
		0.1692	0.9831	7.5573 v	_15167/_X (sky130_fd_sc_hd_or3_2)
2	0.0035				12149 (net)
		0.1692	0.0000	7.5573 v	_15168/_B (sky130_fd_sc_hd_or2_2)
		0.1422	0.7026	8.2599 v	_15168/_X (sky130_fd_sc_hd_or2_2)
3	0.0079				12150 (net)
		0.1422	0.0000	8.2599 v	_15169/_B (sky130_fd_sc_hd_or2_2)
		0.1162	0.6492	8.9091 v	_15169/_X (sky130_fd_sc_hd_or2_2)
2	0.0035				12151 (net)
		0.1162	0.0000	8.9091 v	_15170/_B (sky130_fd_sc_hd_or2_2)
		0.1422	0.6817	9.5904 v	_15170/_X (sky130_fd_sc_hd_or2_2)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

```
# Reports all the connections to a net
```

```
report_net -connections _11675_
```

```
# Replacing cell
```

```
replace_cell _14514_ sky130_fd_sc_hd_or3_4
```

```
# Generating custom timing report
```

```
report_checks -fields {net cap slew input_pins} -digits 4
```

Result - slack reduced

```

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Tue 9:49 AM
-47.9453  data arrival time
-----
-23.5092  slack (VIOLATED)

% report_net -connections _11675_
Net _11675_
Driver pins
_14514/_X output (sky130_fd_sc_hd_or3_2)
Load pins
_14515/_A input (sky130_vsdinv)
_14521/_B2 input (sky130_fd_sc_hd_o221a_2)
_14662/_B input (sky130_fd_sc_hd_or2_2)
_15166/_B input (sky130_fd_sc_hd_or2_2)

% replace_cell _14514_ sky130_fd_sc_hd_or3_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout      Cap      Slew      Delay      Time      Description
-----      -----      -----      -----      -----      -----
          0.0000  0.0000  0.0000  clock clk (rise edge)
          0.0000  0.0000  slack network delay (ideal)

```

Tue 9:50 AM						
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane						
Fanout	Cap	Slew	Delay	Time	Description	
1	0.0013				11624_ (net)	
		0.0784	0.0000	1.4402	v 14481/_A (sky130_fd_sc_hd_or4_2)	
		0.2106	1.5344	2.9746	v 14481/_X (sky130_fd_sc_hd_or4_2)	
1	0.0024				11643_ (net)	
		0.2106	0.0000	2.9746	v 14509/_A1 (sky130_fd_sc_hd_o2111a_2)	
		0.0792	0.5466	3.5212	v 14509/_X (sky130_fd_sc_hd_o2111a_2)	
2	0.0044				11671_ (net)	
		0.0792	0.0000	3.5212	v 14510/_C (sky130_fd_sc_hd_or3_4)	
		0.1349	0.6755	4.1967	v 14510/_X (sky130_fd_sc_hd_or3_4)	
4	0.0089				11672_ (net)	
		0.1349	0.0000	4.1967	v 14513/_A (sky130_fd_sc_hd_or2_2)	
		0.1182	0.6880	4.8847	v 14513/_X (sky130_fd_sc_hd_or2_2)	
2	0.0034				11674_ (net)	
		0.1182	0.0000	4.8847	v 14514/_C (sky130_fd_sc_hd_or3_4)	
		0.1290	0.6794	5.5641	v 14514/_X (sky130_fd_sc_hd_or3_4)	
4	0.0070				11675_ (net)	
		0.1290	0.0000	5.5641	v 15166/_B (sky130_fd_sc_hd_or2_2)	
		0.1148	0.6414	6.2055	v 15166/_X (sky130_fd_sc_hd_or2_2)	
2	0.0032				12148_ (net)	
		0.1148	0.0000	6.2055	v 15167/_C (sky130_fd_sc_hd_or3_2)	
		0.1692	0.9831	7.1886	v 15167/_X (sky130_fd_sc_hd_or3_2)	
2	0.0035				12149_ (net)	
		0.1692	0.0000	7.1886	v 15168/_B (sky130_fd_sc_hd_or2_2)	
		0.1422	0.7026	7.8912	v 15168/_X (sky130_fd_sc_hd_or2_2)	
3	0.0079				12150_ (net)	
		0.1422	0.0000	7.8912	v 15169/_B (sky130_fd_sc_hd_or2_2)	
		0.1162	0.6492	8.5404	v 15169/_X (sky130_fd_sc_hd_or2_2)	
2	0.0025				12151_ (net)	

```

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
2 0.0035
          0.1162 0.0000 45.7962 v _12207_(net)
          0.1421 0.6813 46.4775 v _15226/_B(sky130_fd_sc_hd_or2_2)
          0.1421 0.0000 46.4775 v _15226/_X(sky130_fd_sc_hd_or2_2)
          0.1228 0.6610 47.1385 v _12208_(net)
          0.1228 0.0000 47.1385 v _15227/_B(sky130_fd_sc_hd_or2_2)
          0.0713 0.4381 47.5766 v _15227/_X(sky130_fd_sc_hd_o221a_2)
          0.0713 0.0000 47.5766 v _03928_(net)
          0.0713 0.0000 47.5766 v _30440/_D(sky130_fd_sc_hd_dfxtpl_2)
                                     data arrival time
          0.0000 24.7300 24.7300 clock clk (rise edge)
          0.0000 24.7300 clock network delay (ideal)
          0.0000 24.7300 clock reconvergence pessimism
          -0.2939 24.4361 ^ _30440/_CLK(sky130_fd_sc_hd_dfxtpl_2)
          24.4361 library setup time
          24.4361 data required time
          -----
          24.4361 data required time
          -47.5766 data arrival time
          -----
          -23.1405 slack (VIOLATED)

```

OR gate of drive strength 2 driving OA gate has more delay

```

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Fanout Cap Slew Delay Time Description
-----+
          0.0000 0.0000 0.0000 clock clk (rise edge)
          0.0000 0.0000 0.0000 clock network delay (ideal)
          0.0000 0.0000 ^ _29052/_CLK(sky130_fd_sc_hd_dfxtpl_2)
          0.0572 0.5830 0.5830 v _29052/_Q(sky130_fd_sc_hd_dfxtpl_2)
          4 0.0067           irq_pending[3] (net)
          0.0572 0.0000 0.5830 v _14460/_A(sky130_vsdinv)
          0.1856 0.1667 0.7497 ^ _14460/_Y(sky130_vsdinv)
          3 0.0138           11622_(net)
          0.1856 0.0000 0.7497 ^ _14461/_B2(sky130_fd_sc_hd_o22ai_2)
          0.0878 0.1436 0.8933 v _14461/_Y(sky130_fd_sc_hd_o22ai_2)
          1 0.0021           11623_(net)
          0.0878 0.0000 0.8933 v _14462/_C1(sky130_fd_sc_hd_a221o_2)
          0.0784 0.5469 1.4402 v _14462/_X(sky130_fd_sc_hd_a221o_2)
          1 0.0013           11624_(net)
          0.0784 0.0000 1.4402 v _14481/_A(sky130_fd_sc_hd_or4_2)
          0.2106 1.5344 2.9746 v _14481/_X(sky130_fd_sc_hd_or4_2)
          1 0.0024           11643_(net)
          0.2106 0.0000 2.9746 v _14509/_A1(sky130_fd_sc_hd_o2111a_2)
          0.0792 0.5466 3.5212 v _14509/_X(sky130_fd_sc_hd_o2111a_2)
          2 0.0044           11671_(net)
          0.0792 0.0000 3.5212 v _14510/_C(sky130_fd_sc_hd_or3_4)
          0.1349 0.6755 4.1967 v _14510/_X(sky130_fd_sc_hd_or3_4)
          4 0.0089           11672_(net)
          0.1349 0.0000 4.1967 v _14513/_A(sky130_fd_sc_hd_or2_2)
          0.1182 0.6880 4.8847 v _14513/_X(sky130_fd_sc_hd_or2_2)
          2 0.0024           11674_(net)

```

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

```
report_net -connections _11643_
```

```
# Replacing cell
```

```
replace_cell _14481_ sky130_fd_sc_hd__or4_4
```

```
# Generating custom timing report
```

```
report_checks -fields {net cap slew input_pins} -digits 4
```

Result - slack reduced

```

Activities Terminal - Tue 10:29 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
-47.5766  data arrival time
-----
-23.1405  slack (VIOLATED)

% report_net -connections _11643_
Net _11643_
Driver pins
_14481 /X output (sky130_fd_sc_hd_or4_2)
Load pins
_14509 /A1 input (sky130_fd_sc_hd_o2111a_2)
% replace_cell _14481_ sky130_fd_sc_hd_or4_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29043_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout      Cap      Slew      Delay      Time      Description
-----
          0.0000  0.0000  0.0000  clock clk (rise edge)
          0.0000  0.0000  0.0000  clock network delay (ideal)
          0.0000  0.0000  0.0000 ^ _29043/_CLK (sky130_fd_sc_hd_dfxtp_2)
          0.0581  0.5838  0.5838 v _29043/_Q (sky130_fd_sc_hd_dfxtp_2)
          1.0000  0.0000  0.0000   _29043_ (net)
-----
```

```

Activities Terminal - Tue 10:29 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
2  0.0035
          0.1162  0.0000  45.7918 v _12207_(net)
          0.1421  0.6813  46.4731 v _15226/_B (sky130_fd_sc_hd_or2_2)
          0.1421  0.0000  46.4731 v _15226/_X (sky130_fd_sc_hd_or2_2)
          0.1228  0.6610  47.1341 v _12208_(net)
          0.1228  0.0000  47.1341 v _15227/_B (sky130_fd_sc_hd_or2_2)
          0.1228  0.0000  47.1341 v _15227/_X (sky130_fd_sc_hd_or2_2)
          0.0713  0.4381  47.5723 v _12209_(net)
          0.0713  0.0000  47.5723 v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
          0.0713  0.0000  47.5723 v _15230/_X (sky130_fd_sc_hd_o221a_2)
          0.0713  0.0000  47.5723 v _03928_(net)
          0.0713  0.0000  47.5723 v _30440/_D (sky130_fd_sc_hd_dfxtp_2)
          0.0713  0.0000  47.5723 v data arrival time
          0.0000  24.7300  24.7300  clock clk (rise edge)
          0.0000  24.7300  24.7300  clock network delay (ideal)
          0.0000  24.7300  24.7300  clock reconvergence pessimism
          0.0000  24.7300  24.7300 ^ _30440/_CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.2939  24.4361  library setup time
          0.0000  24.4361  24.4361  data required time
          0.0000  24.4361  24.4361  data arrival time
-----
-23.1362  slack (VIOLATED)
```

OR gate of drive strength 2 driving OA gate has more delay

Activities Terminal Tue 10:32 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

				irq_pending[12] (net)
4	0.0069	0.0581	0.0000	0.5838 v _14484 /A (sky130_vsdinv)
		0.1864	0.1676	0.7515 ^ _14484 /Y (sky130_vsdinv)
3	0.0139	0.1864	0.0000	11646 (net)
		0.0878	0.1674	0.7515 ^ _14486 /A2 (sky130_fd_sc_hd_o22ai_2)
1	0.0021	0.0878	0.0000	0.9189 v _14486 /Y (sky130_fd_sc_hd_o22ai_2)
		0.0784	0.5469	11648 (net)
1	0.0013	0.0784	0.0000	1.4658 v _14487 /C1 (sky130_fd_sc_hd_a22lo_2)
		0.2092	1.5317	11649 (net)
1	0.0023	0.2092	0.0000	2.9975 v _14506 /A (sky130_fd_sc_hd_or4_2)
		0.0792	0.5193	11668 (net)
2	0.0044	0.0792	0.0000	3.5168 v _14509 /A2 (sky130_fd_sc_hd_o2111a_2)
		0.1349	0.6755	11671 (net)
4	0.0089	0.1349	0.0000	3.5168 v _14510 /C (sky130_fd_sc_hd_or3_4)
		0.1182	0.6880	4.1923 v _14510 /X (sky130_fd_sc_hd_or3_4)
2	0.0034	0.1182	0.0000	11672 (net)
		0.1290	0.6794	4.8803 v _14513 /A (sky130_fd_sc_hd_or2_2)
4	0.0070	0.1290	0.0000	4.8803 v _14513 /X (sky130_fd_sc_hd_or2_2)
		0.1148	0.6414	11674 (net)
2	0.0022	0.1148	0.0000	5.5597 v _14514 /C (sky130_fd_sc_hd_or3_4)
		0.1290	0.6414	5.5597 v _14514 /X (sky130_fd_sc_hd_or3_4)
4	0.0070	0.1290	0.0000	11675 (net)
		0.1148	0.6414	6.2011 v _15166 /B (sky130_fd_sc_hd_or2_2)
2	0.0022	0.1148	0.0000	6.2011 v _15166 /X (sky130_fd_sc_hd_or2_2)
		0.1290	0.6414	11676 (net)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

report_net -connections _11668_

Replacing cell

replace_cell _14506_ sky130_fd_sc_hd_or4_4

Generating custom timing report

report_checks -fields {net cap slew input_pins} -digits 4

Result - slack reduced

```

Activities Terminal - Tue 10:36 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
-47.5723  data arrival time
-----  

-23.1362  slack (VIOLATED)

% report_net -connections _11668_
Net _11668
Driver pins
_14506 /X output (sky130_fd_sc_hd_or4_2)
Load pins
_14509 /A2 input (sky130_fd_sc_hd_o2111a_2)

% replace_cell _14506_ sky130_fd_sc_hd_or4_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout      Cap      Slew      Delay      Time      Description
-----  

          0.0000  0.0000  0.0000  clock clk (rise edge)
          0.0000  0.0000  0.0000  clock network delay (ideal)
          0.0000  0.0000  0.0000 ^ _29052 /CLK (sky130_fd_sc_hd_dfxtp_2)
          0.0572  0.5830  0.5830 v _29052 /Q (sky130_fd_sc_hd_dfxtp_2)
           0.0067  


```

```

Activities Terminal - Tue 10:37 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
2  0.0035
          0.1162  0.0000  45.2729 v _12207_ (net)
          0.1421  0.6813  45.9542 v _15226 /B (sky130_fd_sc_hd_or2_2)
          0.1421  0.0000  45.9542 v _15226 /X (sky130_fd_sc_hd_or2_2)
          0.1228  0.6610  46.6153 v _12208_ (net)
          0.1228  0.0000  46.6153 v _15227 /B (sky130_fd_sc_hd_or2_2)
          0.1228  0.0000  46.6153 v _15227 /X (sky130_fd_sc_hd_or2_2)
          0.0713  0.4381  47.0534 v _12209_ (net)
          0.0713  0.0000  47.0534 v _15230 /B2 (sky130_fd_sc_hd_o221a_2)
          0.0713  0.0000  47.0534 v _15230 /X (sky130_fd_sc_hd_o221a_2)
          0.0713  0.0000  47.0534 v _03928_ (net)
          0.0713  0.0000  47.0534 v _30440 /D (sky130_fd_sc_hd_dfxtp_2)
          0.0713  0.0000  47.0534 data arrival time
          0.0000  24.7300  24.7300  clock clk (rise edge)
          0.0000  24.7300  24.7300  clock network delay (ideal)
          0.0000  24.7300  24.7300  clock reconvergence pessimism
          0.0000  24.7300  24.7300 ^ _30440 /CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.2939  24.4361  library setup time
          24.4361  data required time
          24.4361  data arrival time
-----  

-22.6173  slack (VIOLATED)

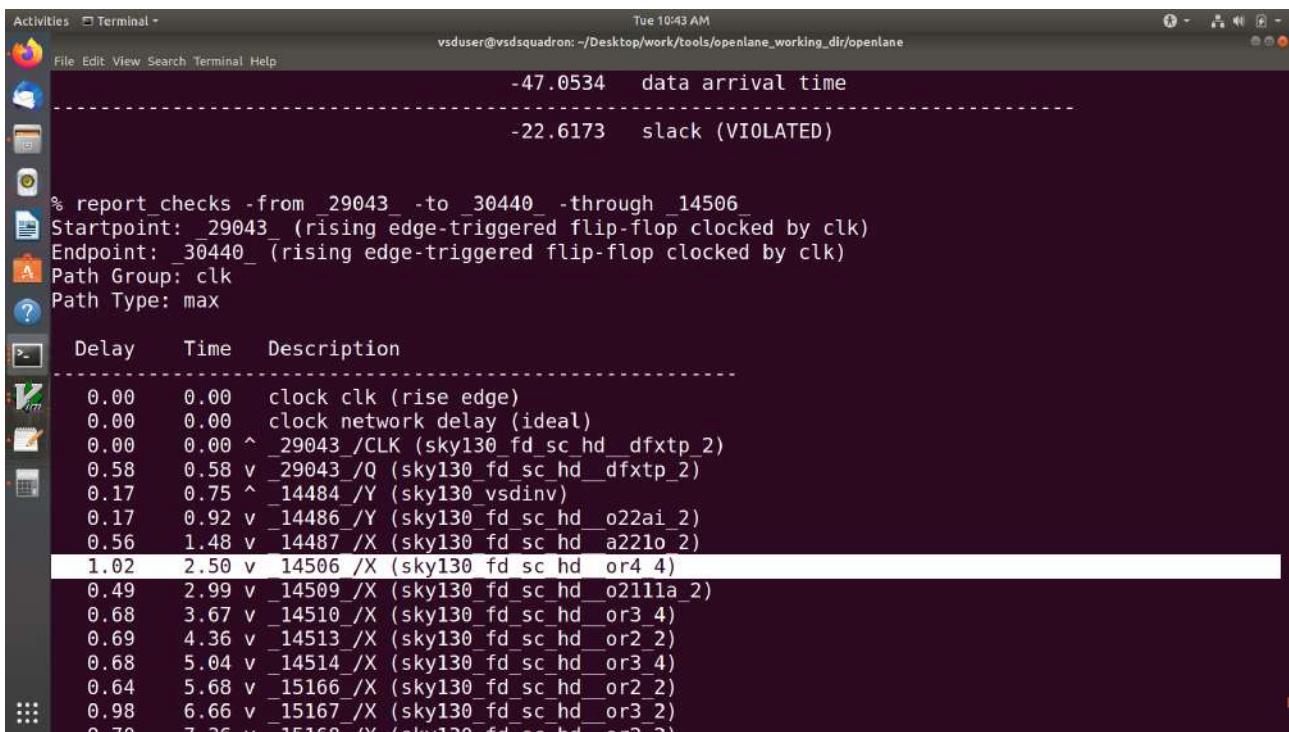
```

Commands to verify instance _14506_ is replaced with sky130_fd_sc_hd_or4_4

Generating custom timing report

report_checks -from _29043_ -to _30440_ -through _14506_

Screenshot of replaced instance



The screenshot shows a terminal window with the following output:

```
Tue 10:43 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
-47.0534  data arrival time
-----
-22.6173  slack (VIOLATED)

% report_checks -from 29043 -to 30440 -through 14506
Startpoint: 29043 (rising edge-triggered flip-flop clocked by clk)
Endpoint: 30440 (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Delay      Time      Description
-----
0.00      0.00      clock clk (rise edge)
0.00      0.00      clock network delay (ideal)
0.00      0.00 ^ 29043 /CLK (sky130_fd_sc_hd_dfxtpl_2)
0.58      0.58 v 29043 /Q (sky130_fd_sc_hd_dfxtpl_2)
0.17      0.75 ^ 14484 /Y (sky130_vsdinv)
0.17      0.92 v 14486 /Y (sky130_fd_sc_hd_o22ai_2)
0.56      1.48 v 14487 /X (sky130_fd_sc_hd_a22lo_2)
1.02      2.50 v 14506 /X (sky130_fd_sc_hd_or4_4)
0.49      2.99 v 14509 /X (sky130_fd_sc_hd_o2111a_2)
0.68      3.67 v 14510 /X (sky130_fd_sc_hd_or3_4)
0.69      4.36 v 14513 /X (sky130_fd_sc_hd_or2_2)
0.68      5.04 v 14514 /X (sky130_fd_sc_hd_or3_4)
0.64      5.68 v 15166 /X (sky130_fd_sc_hd_or2_2)
0.98      6.66 v 15167 /X (sky130_fd_sc_hd_or3_2)
0.70      7.26 v 15168 /X (sky130_fd_sc_hd_or2_2)
```

We started ECO fixes at wns -23.9000 and now we stand at wns -22.6173 we reduced around 1.2827 ns of violation

11. Replace the old netlist with the new netlist generated after timing ECO fix and implement the floorplan, placement and cts.

Now to insert this updated netlist to PnR flow and we can use write_verilog and overwrite the synthesis netlist but before that we are going to make a copy of the old old netlist

Commands to make copy of netlist

```
# Change from home directory to synthesis results directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
25-03_18-52/results/synthesis/
```

```
# List contents of the directory
```

```
ls
```

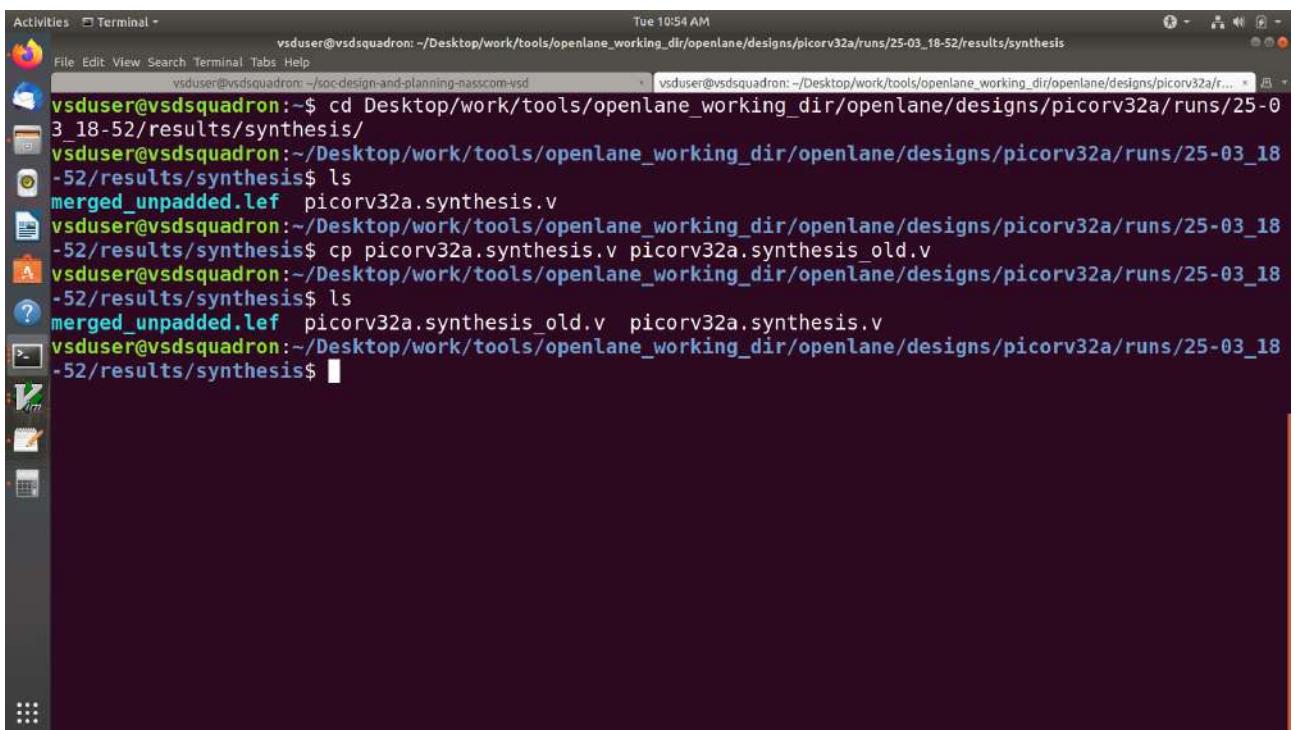
```
# Copy and rename the netlist
```

```
cp picorv32a.synthesis.v picorv32a.synthesis_old.v
```

```
# List contents of the directory
```

```
ls
```

Screenshot of commands run



The screenshot shows a terminal window titled "Terminal" with a dark theme. The window title bar includes the text "Activities Terminal" and the date "Tue 10:54 AM". The terminal window displays a command-line session:

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$ ls
merged_unpadded.lef picorv32a.synthesis.v
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$ cp picorv32a.synthesis.v picorv32a.synthesis_old.v
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$ ls
merged_unpadded.lef picorv32a.synthesis_old.v picorv32a.synthesis.v
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$
```

Commands to write verilog

```
# Check syntax
```

```
help write_verilog
```

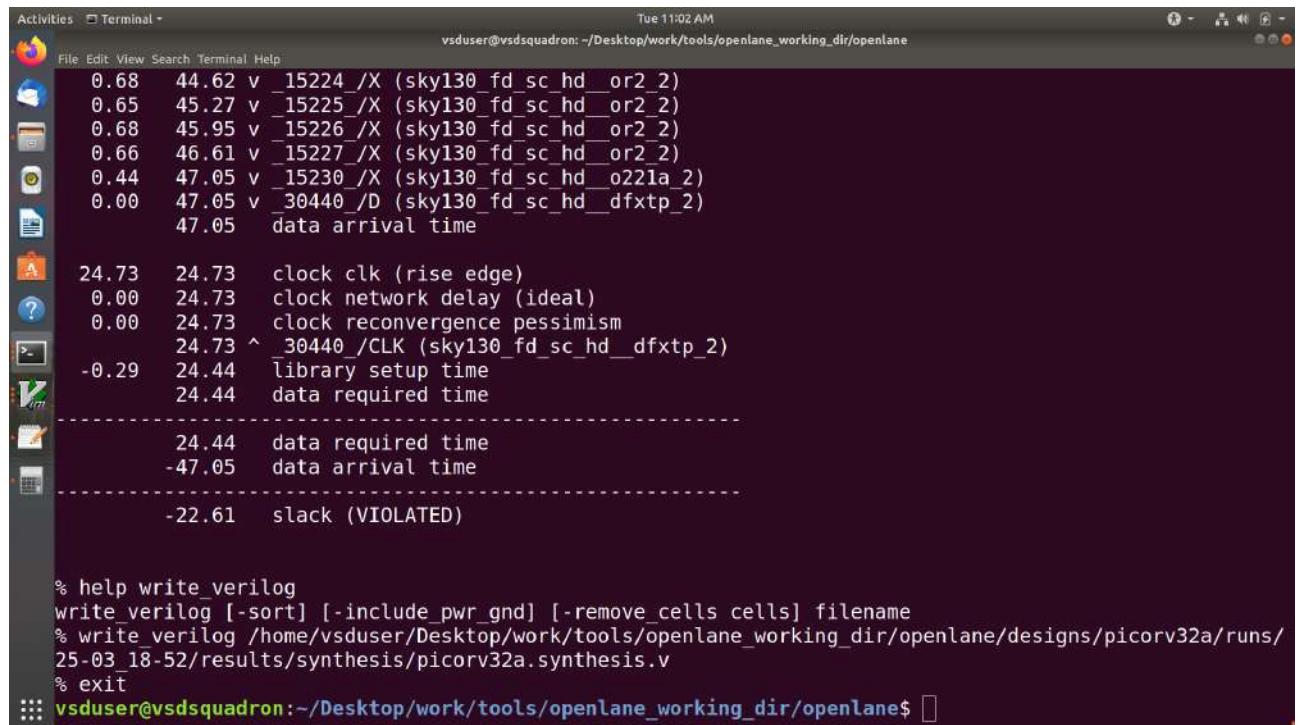
```
# Overwriting current synthesis netlist
```

```
write_verilog /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis/picorv32a.synthesis.v
```

```
# Exit from OpenSTA since timing analysis is done
```

```
exit
```

Screenshot of commands run



The screenshot shows a terminal window with the following content:

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
Tue 11:02 AM
File Edit View Search Terminal Help
0.68 44.62 v _15224_X (sky130_fd_sc_hd_or2_2)
0.65 45.27 v _15225_X (sky130_fd_sc_hd_or2_2)
0.68 45.95 v _15226_X (sky130_fd_sc_hd_or2_2)
0.66 46.61 v _15227_X (sky130_fd_sc_hd_or2_2)
0.44 47.05 v _15230_X (sky130_fd_sc_hd_o221a_2)
0.00 47.05 v _30440_D (sky130_fd_sc_hd_dfxtp_2)
47.05 data arrival time

24.73 24.73 clock clk (rise edge)
0.00 24.73 clock network delay (ideal)
0.00 24.73 clock reconvergence pessimism
24.73 ^ _30440_CLK (sky130_fd_sc_hd_dfxtp_2)
-0.29 24.44 library setup time
24.44 data required time
-----
24.44 data required time
-47.05 data arrival time
-----
-22.61 slack (VIOLATED)

% help write_verilog
write_verilog [-sort] [-include_pwr_gnd] [-remove_cells cells] filename
% write_verilog /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis/picorv32a.synthesis.v
% exit
::: vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$
```

Verified that the netlist is overwritten by checking that instance `_14506_` is replaced with `sky130_fd_sc_hd_or4_4`

```

Activities  M. GVim -
Tue 11:01 AM
picorv32a.synthesis.v (~-/Desktop/work/toolbox/25-03_18-52/results/synthesis) - GVIM2
File Edit Tools Syntax Buffers Window Help
16359     .Y(_11665_));
16360   sky130_fd_sc_hd_o22ai_2 _14504_ (.A1(\irq_mask[21]),
16361     .A2(_11664),
16362     .B1(\irq_mask[23]),
16363     .B2(_11665),
16364     .Y(_11666));
16365   sky130_fd_sc_hd_a221o_2 _14505_ (.A1(_11662),
16366     .A2(\irq_pending[20]),
16367     .B1(_11663),
16368     .B2(\irq_pending[22]),
16369     .C1(_11666),
16370     .X(_11667));
16371   sky130_fd_sc_hd_or4_4 _14506_ (.A(_11649),
16372     .B(_11655),
16373     .C(_11661),
16374     .D(_11667),
16375     .X(_11668));
16376   sky130_vsdinv _14507_ (.A(irq_active),
16377     .Y(_11669));
16378   sky130_vsdinv _14508_ (.A(irq_delay),
16379     .Y(_11670));
16380   sky130_fd_sc_hd_o2111a_2 _14509_ (.A1(_11643),
16381     .A2(_11668),
16382     .B1(_11669),
16383     .C1(_11670),
hlsearch
16371,25      21%

```

Since we confirmed that netlist is replaced and will be loaded in PnR but since we want to follow up on the earlier o violation design we are continuing with the clean design to further stages

Commands load the design and run necessary stages

```
# Now once again we have to prep design so as to update variables
```

```
prep -design picorv32a -tag 24-03_10-03 -overwrite
```

```
# Additional commands to include newly added lef to openlane flow merged.lef
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_STRATEGY
```

```
set ::env(SYNTH_STRATEGY) "DELAY 3"

# Command to set new value for SYNTH_SIZING

set ::env(SYNTH_SIZING) 1

# Now that the design is prepped and ready, we can run synthesis using following command

run_synthesis

# Following commands are altogether sourced in "run_floorplan" command

init_floorplan

place_io

tap_decap_or

# Now we are ready to run placement

run_placement

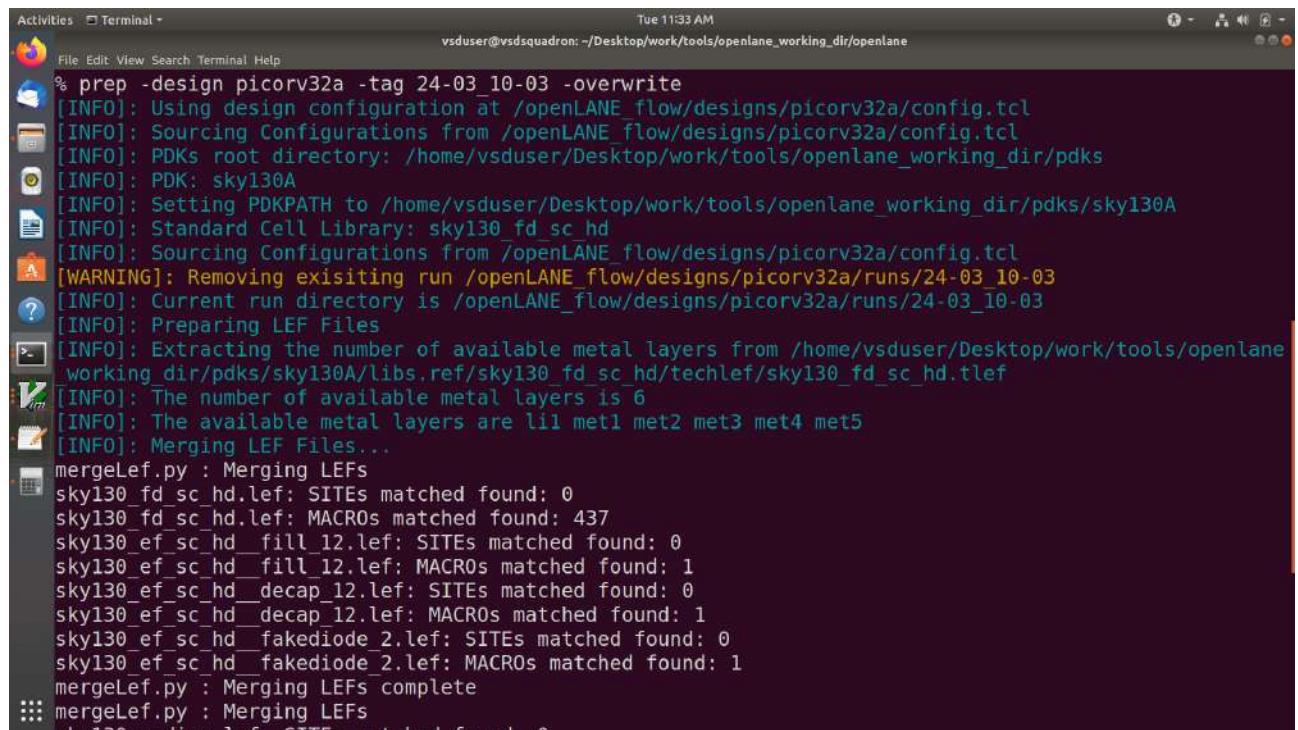
# Incase getting error

unset ::env(LIB_CTS)
```

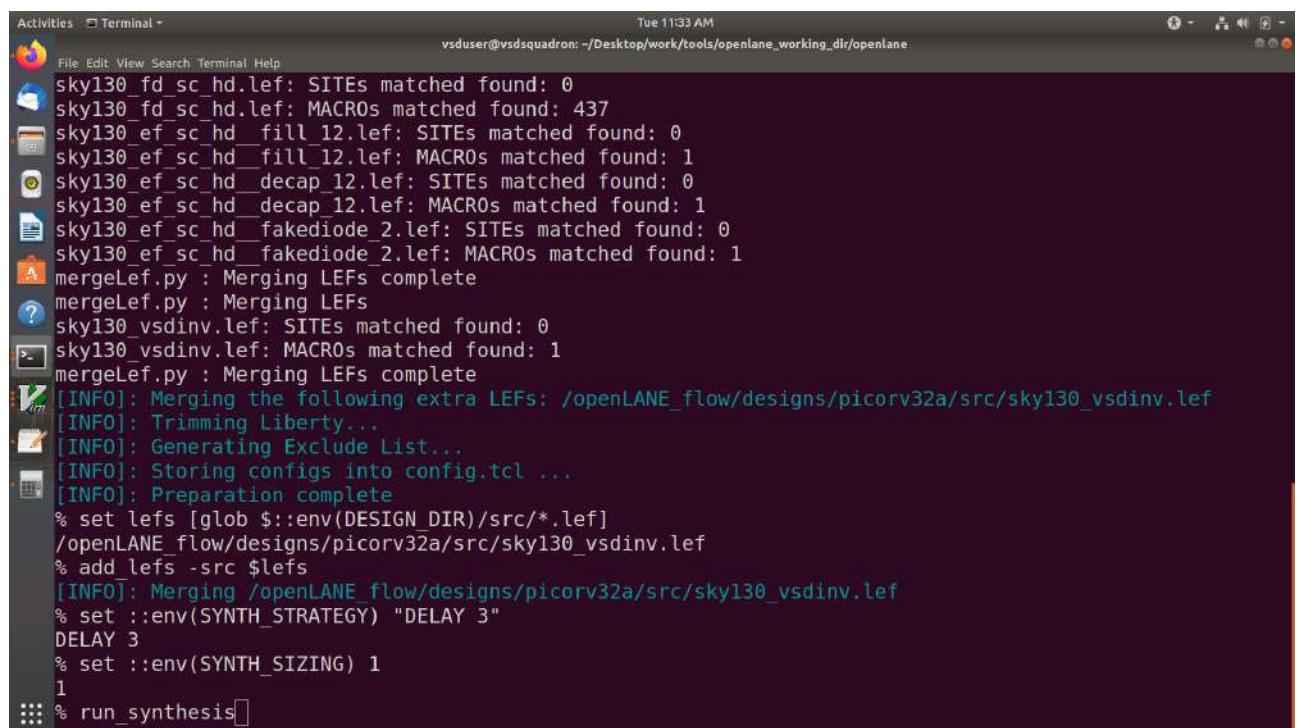
```
# With placement done we are now ready to run CTS
```

```
run_cts
```

Screenshots of commands run



```
Activities Terminal Tue 11:33 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% prep -design picorv32a -tag 24-03_10-03 -overwrite
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130 fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[WARNING]: Removing existing run /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.tlef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1l met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
::: mergeLef.py : Merging LEFs
    120 SITEs and 15 MACROs
```



```
Activities Terminal Tue 11:33 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% set ::env(SYNTH_STRATEGY) "DELAY 3"
DELAY 3
% set ::env(SYNTH_SIZING) 1
1
::: % run_synthesis
```

```
Activities Terminal - Tue 11:35 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
::: % init_floorplan
```

```
Activities Terminal - Tue 11:36 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
% init_floorplan
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 8
OpenROAD 0.9.0 1415572a73
A This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
[INFO IFP-0001] Added 264 rows of 1566 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 731.615 742.335 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/8-verilog2def.die_area.rpt.
[INFO] Floorplanned on a core area of 5.52 10.88 725.88 728.96 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/8-verilog2def.core_area.rpt.
[INFO]: Core area width: 720.36
[INFO]: Core area height: 718.08
[INFO]: Changing layout from 0 to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def
::: % place_io
```

```
Activities Terminal - Tue 11:37 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% place_io
[INFO]: Running IO Placement...
[INFO]: current step index: 9
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def
#Macro blocks found: 0
Using 5u default boundaries offset
Random pin placement
RandomMode Even
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def
::: % tap_decap_or
```

```
Activities Terminal - Tue 11:38 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% place_io
[INFO]: Running IO Placement...
[INFO]: current step index: 9
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def
Step 1: Cut rows...
[INFO TAP-0001] Macro blocks found: 0
[INFO TAP-0002] #Original rows: 264
[INFO TAP-0003] #Cut rows: 0
Step 2: Insert endcaps...
[INFO TAP-0004] #Endcaps inserted: 528
Step 3: Insert tapcells...
[INFO TAP-0005] #Tapcells inserted: 7180
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/floorplan/picorv32a.floorplan.def
::: % run_placement
```

```
Activities Terminal - Tue 11:39 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
legalized HPWL      910806.5 u
delta HPWL          2 %

[INFO DPL-0020] Mirrored 6650 instances
[INFO DPL-0021] HPWL before      910806.5 u
[INFO DPL-0022] HPWL after       895297.0 u
[INFO DPL-0023] HPWL delta      -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/11-resize.r.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 15
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
% run_cts
```

```
Activities Terminal - Tue 12:00 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 25690 components and 145610 component-terminals.
Notice 0:     Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
[INFO]: Changing netlist from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis_optimized.v to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis_cts.v
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 19
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def.png'
Done
[INFO]: Screenshot taken.
% 
```

12. Post-CTS OpenROAD timing analysis.

Commands to be run in OpenLANE flow to do OpenROAD timing analysis with integrated OpenSTA in OpenROAD

```
# Command to run OpenROAD tool
```

```
openroad
```

```
# Reading lef file
```

```
read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
```

```
# Reading def file
```

```
read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
```

```
# Creating an OpenROAD database to work with
```

```
write_db pico_cts.db
```

```
# Loading the created database in OpenROAD
```

```
read_db pico_cts.db
```

```
# Read netlist post CTS
```

```
read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/  
picorv32a.synthesis_cts.v
```

```
# Read library for design
```

```
read_liberty $::env(LIB_SYNTH_COMPLETE)
```

```
# Link design and library

link_design picorv32a

# Read in the custom sdc we created

read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc

# Setting all cloks as propagated clocks

set_propagated_clock [all_clocks]

# Check syntax of 'report_checks' command

help report_checks

# Generating custom timing report

report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format
full_clock_expanded -digits 4

# Exit to OpenLANE flow

exit
```

Screenshots of commands run and timing report generated

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane Tue 12:55 PM

```
% openroad
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
% read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
% read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 25690 components and 145610 component-terminals.
Notice 0: Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
% write_db pico_cts.db
% read_db pico_cts.db
% read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis_cts.v
% read_liberty $::env(LIB_SYNTH_COMPLETE)
1
% link_design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_tapvprvgnd_1 has no liberty cell.
.
```

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane Tue 12:57 PM

```
% read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
[INFO]: Setting output delay to: 4.946000000000001
[INFO]: Setting input delay to: 4.946000000000001
[INFO]: Setting load to: 0.017653
% set_propagated_clock [all_clocks]
% help report_checks
report_checks
report_checks [-from from_list]-rise_from from_list[-fall_from from_list] [-through through_list]-rise_through through_list[-fall_through through_list] [-to to_list]-rise_to to_list[-fall_to to_list] [-unconstrained] [-path_delay min|min_rise|min_fall|max|max_rise|max_fall|min_max] [-corner corner_name] [-group_count path_count] [-endpoint_count path_count] [-unique_paths_to_endpoint] [-slack_max slack_max] [-slack_min slack_min] [-sort_by slack] [-path_group group_name] [-format full|full_clock|full_clock_expanded|short|end|summary] [-fields [capacitance|slew|input_pin|net]] [-digits digits] [-no_line_splits] [> filename] [>> filename]
% report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
Startpoint: _30990_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30955_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----.
. 0.0000 0.0000 clock clk (rise edge)
. 0.0000 0.0000 clock source latency
. 0.0225 0.0100 0.0100 ^ clk (in)
. . . . . clk (net)
. 1 0.0079 . . . .
```

```

Activities Terminal - Tue 12:58 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
11 0.0206
    0.0650  0.0000  1.6203 ^ _30955/_CLK (sky130_fd_sc_hd_dfxtp_2)
    0.0000  1.6203  clock reconvergence pessimism
   -0.0263  1.5941  library hold time
    1.5941  data required time
-----
    1.5941  data required time
   -1.8059  data arrival time
-----
    0.2119  slack (MET)

Startpoint: resetn (input port clocked by clk)
Endpoint: mem_la_read (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
----- 0.0000 0.0000 0.0000 0.0000 clock clk (rise edge)
          0.0000 0.0000 4.9460 4.9460 ^ input external delay
          0.0172 0.0055 4.9515 ^ resetn (in)
          0.0042 0.0172 0.0000 4.9515 ^ input101/A (sky130_fd_sc_hd_clkbuf_8)
          0.0582 0.1265 5.0780 ^ input101/X (sky130_fd_sc_hd_clkbuf_8)
          0.0234 0.0582 0.0000 5.0780 ^ net101 (net)

```

```

Activities Terminal - Tue 11:09 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
6 0.0270
    0.0947  0.0000  5.2526 ^ 12638_(net)
    0.1284  0.1277  5.3802 v 17093/_C (sky130_fd_sc_hd_nand3_4)
          0.1284  0.0000  5.3802 v 17093/_Y (sky130_fd_sc_hd_nand3_4)
          0.0799  0.1239  5.5041 ^ 13857_(net)
          0.0023 0.0799 0.0000 5.5041 ^ 18867/_B1 (sky130_fd_sc_hd_a21oi_4)
          0.0799  0.0000 5.5041 ^ 18867/_Y (sky130_fd_sc_hd_a21oi_4)
          0.0177 0.1052 0.1596 5.6637 ^ net199_(net)
          0.1052 0.0000 5.6637 ^ output199/A (sky130_fd_sc_hd_clkbuf_2)
          0.1052 0.0000 5.6637 ^ output199/X (sky130_fd_sc_hd_clkbuf_2)
          0.0000 0.0000 24.7300 24.7300 clock clk (rise edge)
          0.0000 0.0000 24.7300 24.7300 clock network delay (propagated)
          0.0000 0.0000 24.7300 24.7300 clock reconvergence pessimism
         -4.9460 19.7840 19.7840 output external delay
         19.7840 19.7840 data required time
         -5.6637 14.1203 14.1203 data arrival time
-----
         19.7840 14.1203 slack (MET)

% exit
%
```

**13. Explore post-CTS OpenROAD timing analysis by removing
'sky130_fd_sc_hd_clkbuf_1' cell from clock buffer list variable
'CTS_CLK_BUFFER_LIST'.**

**Commands to be run in OpenLANE flow to do OpenROAD timing analysis after
changing CTS_CLK_BUFFER_LIST**

```
# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)

# Removing 'sky130_fd_sc_hd_clkbuf_1' from the list

set ::env(CTS_CLK_BUFFER_LIST) [lreplace $::env(CTS_CLK_BUFFER_LIST) 0 0]

# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)

# Checking current value of 'CURRENT_DEF'

echo $::env(CURRENT_DEF)

# Setting def as placement def

set ::env(CURRENT_DEF) /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/
placement/picorv32a.placement.def

# Run CTS again

run_cts

# Checking current value of 'CTS_CLK_BUFFER_LIST'
```

```
echo $::env(CTS_CLK_BUFFER_LIST)

# Command to run OpenROAD tool

openroad

# Reading lef file

read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef

# Reading def file

read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def

# Creating an OpenROAD database to work with

write_db pico_cts1.db

# Loading the created database in OpenROAD

read_db pico_cts.db

# Read netlist post CTS

read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/
picorv32a.synthesis_cts.v
```

```
# Read library for design

read_liberty $::env(LIB_SYNTH_COMPLETE)

# Link design and library

link_design picorv32a

# Read in the custom sdc we created

read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc

# Setting all cloks as propagated clocks

set_propagated_clock [all_clocks]

# Generating custom timing report

report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format
full_clock_expanded -digits 4

# Report hold skew

report_clock_skew -hold
```

```
# Report setup skew

report_clock_skew -setup

# Exit to OpenLANE flow

exit

# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)

# Inserting 'sky130_fd_sc_hd__clkbuf_1' to first index of list

set ::env(CTS_CLK_BUFFER_LIST) [linsert $::env(CTS_CLK_BUFFER_LIST) 0
sky130_fd_sc_hd__clkbuf_1]

# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)
```

Screenshots of commands run and timing report generated

```
Activities Terminal - Tue 1:42 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_
8
% set ::env(CTS_CLK_BUFFER_LIST) [lreplace $::env(CTS_CLK_BUFFER_LIST) 0 0]
sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
% set ::env(CURRENT_DEF) /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
% run_cts
[INFO]: Running TritonCTS...
[INFO]: current step index: 20
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Done
```

```
Activities Terminal - Tue 1:45 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def.png'
Done
[INFO]: Screenshot taken.
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% openroad
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
% read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
% read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 25690 components and 145610 component-terminals.
Notice 0: Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
% write_db pico_cts1.db
% read_db pico_cts.db
```

```

Activities Terminal - Tue 1:48 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% write_db pico_cts1.db
% read_db pico_cts.db
% read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis
_cts.v
% read_liberty $::env(LIB_SYNTH_COMPLETE)
1
% link_design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_tapvpwrvgnd_1 has no liberty cell.
% read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
[INFO]: Setting output delay to: 4.946000000000001
[INFO]: Setting input delay to: 4.946000000000001
[INFO]: Setting load to: 0.017653
% set_propagated_clock [all_clocks]
% report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
Startpoint: _30990_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30955_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----  

1 0.0079 0.0225 0.0000 0.0100 ^ clkbuf_0_clk/A (sky130_fd_sc_hd_clkbuf_16)  

0.0225 0.0000 0.0100 ^ clkbuf_0_clk/X (sky130_fd_sc_hd_clkbuf_16)

```

```

Activities Terminal - Tue 1:48 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% report_checks -path_delay max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
0.0520 0.0000 1.2459 ^ _30955/_CLK (sky130_fd_sc_hd_dfxtpl_2)
0.0000 1.2459 clock reconvergence pessimism
-0.0280 1.2179 library hold time
1.2179 data required time
-----  

1.2179 data required time
-1.5305 data arrival time
-----  

0.3125 slack (MET)

Startpoint: resetn (input port clocked by clk)
Endpoint: mem_la_read (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
-----  

1 0.0042 0.0172 0.0000 4.9515 ^ resetn/in
0.0000 0.0000 4.9460 ^ input external delay
0.0172 0.0055 4.9515 ^ resetn/net
0.0172 0.0000 4.9515 ^ input101/A (sky130_fd_sc_hd_clkbuf_8)
1 0.0234 0.0582 0.1265 5.0780 ^ input101/X (sky130_fd_sc_hd_clkbuf_8)
0.0582 0.0000 5.0780 ^ net101/net
0.0582 0.0000 5.0780 ^ 15304/A (sky130_fd_sc_hd_clkbuf_4)
0.0042 0.0000 5.2526 ^ 15304/X (sky130_fd_sc_hd_clkbuf_4)

```

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      Tue 1:50 PM
          -4.9460  19.7840  output external delay
          19.7840  data required time
          19.7840  data required time
          -5.6637  data arrival time
          14.1203  slack (MET)

% report_clock_skew -hold
Clock clk
Latency CRPR Skew
_31226 /CLK ^
    1.36
_32416 /CLK ^
    0.94    0.00    0.42

% report_clock_skew -setup
Clock clk
Latency CRPR Skew
_31226 /CLK ^
    1.36
_32416 /CLK ^
    0.94    0.00    0.42

% exit
%
```

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      Tue 1:53 PM
          % echo $::env(CTS_CLK_BUFFER_LIST)
          sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
          % set ::env(CTS_CLK_BUFFER_LIST) [linsert $::env(CTS_CLK_BUFFER_LIST) 0 sky130_fd_sc_hd_clkbuf_1]
          sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_
          8
          % echo $::env(CTS_CLK_BUFFER_LIST)
          sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_
          8
%
```

Section 5 - Final steps for RTL2GDS using tritonRoute and openSTA (25/03/2024 - 26/03/2024)

Theory

Implementation

- **Section 5 tasks:-**
25. Perform generation of Power Distribution Network (PDN) and explore the PDN layout.
 26. Perform detailed routing using TritonRoute.
 27. Post-Route parasitic extraction using SPEF extractor.
 28. Post-Route OpenSTA timing analysis with the extracted parasitics of the route.
- All section 5 logs, reports and results can be found in following run folder:

Section 5 Run - 26-03_08-45

1. Perform generation of Power Distribution Network (PDN) and explore the PDN layout.

Commands to perform all necessary stages up until now

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:vo.21'
```

```
# Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command
```

```
docker
```

```
# Now that we have entered the OpenLANE flow contained docker sub-system we can  
invoke the OpenLANE flow in the Interactive mode using the following command
```

```
./flow.tcl -interactive
```

```
# Now that OpenLANE flow is open we have to input the required packages for proper  
functionality of the OpenLANE flow
```

```
package require openlane 0.9
```

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the  
design creating some necessary files and directories for running a specific design which in  
our case is 'picorv32a'
```

```
prep -design picorv32a
```

```
# Additional commands to include newly added lef to openlane flow merged.lef
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_STRATEGY
```

```
set ::env(SYNTH_STRATEGY) "DELAY 3"
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Now that the design is prepped and ready, we can run synthesis using following command
```

```
run_synthesis
```

```
# Following commands are altogether sourced in "run_floorplan" command
```

```
init_floorplan
```

```
place_io
```

```
tap_decap_or
```

```
# Now we are ready to run placement
```

```
run_placement
```

```
# Incase getting error
```

```
unset ::env(LIB_CTS)
```

```
# With placement done we are now ready to run CTS
```

```
run_cts
```

Now that CTS is done we can do power distribution network

gen_pdn

Screenshots of power distribution network run

```
Activities Terminal Tue 2:22 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: Screenshot taken.
% gen pdn
[INFO]: Generating PDN...
[INFO]: current step index: 14
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 25690 components and 145610 component-terminals.
Notice 0:     Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/cts/picorv32a.cts.def
[INFO] [PDNG-0016] Power Delivery Network Generator: Generating PDN
[INFO] [PDNG-0016] config: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdkss/sky130A/libs.tech/openlane/common_pdn.tcl
[INFO] [PDNG-0008] Design Name is picorv32a
[INFO] [PDNG-0009] Reading technology data
[INFO] [PDNG-0011] ***** INFO *****
Tunne: stdcell -mid
```

```
Activities Terminal Tue 2:22 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[WARNING PSM-0030] Vsrc location at (705.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
[WARNING PSM-0030] Vsrc location at (425.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 563.420um).
[WARNING PSM-0030] Vsrc location at (705.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 710.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 716.600um).
[WARNING PSM-0030] Vsrc location at (705.520um, 710.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 716.600um).
[INFO PSM-0031] Number of nodes on net VGND = 24383.
[INFO PSM-0037] G matrix created successfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/cts/picorv32a.cts.def to /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
% 
```

Commands to load PDN def in magic in another terminal

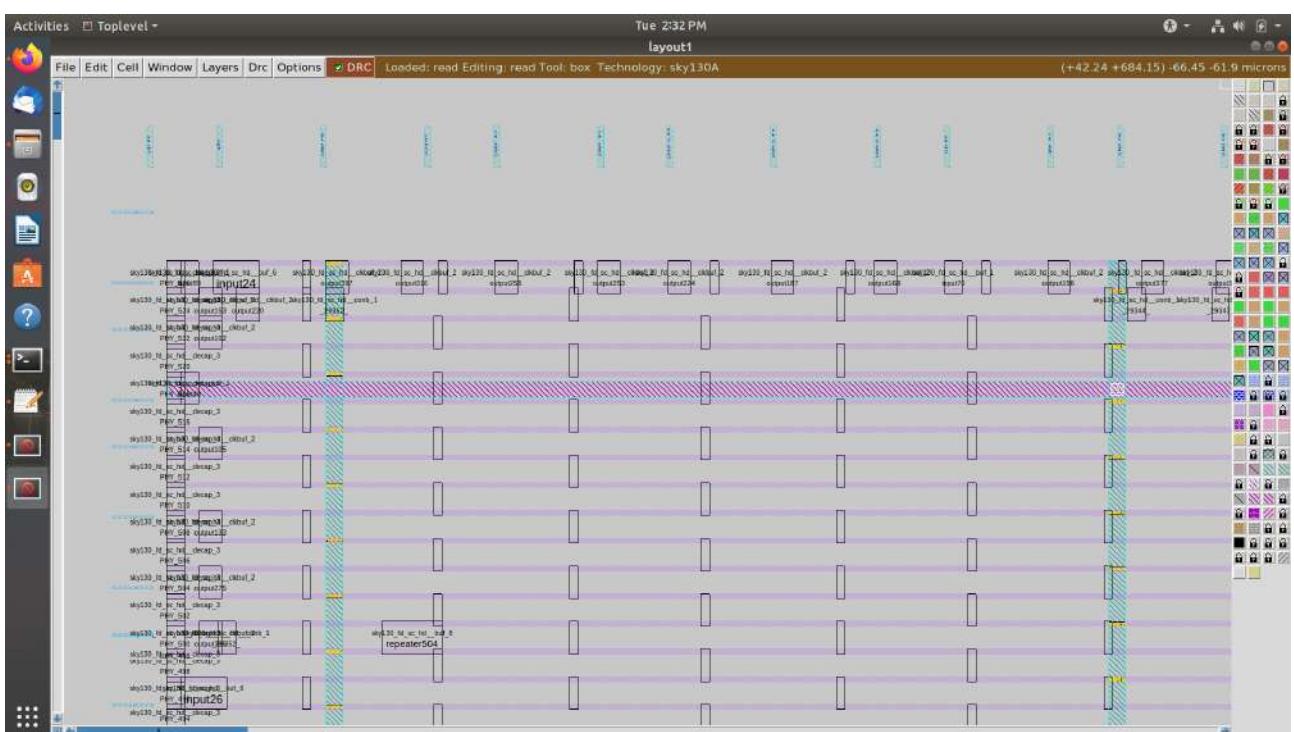
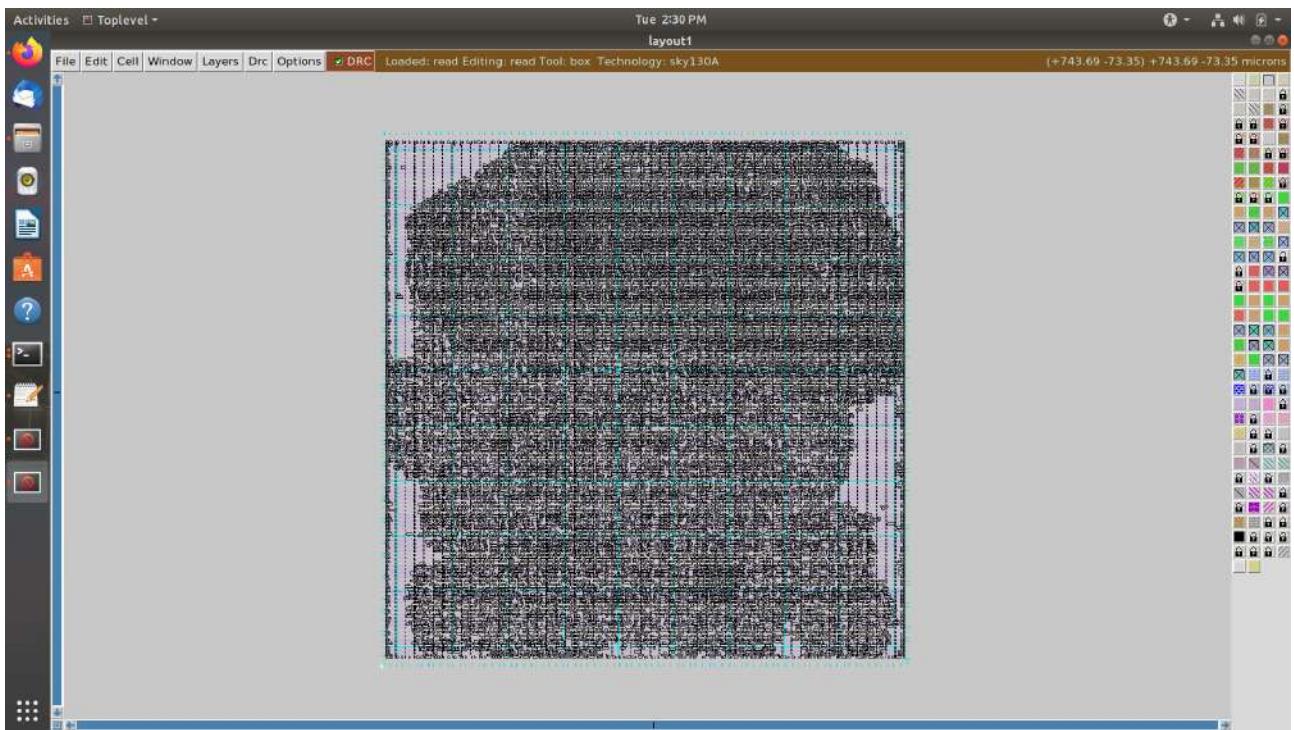
```
# Change directory to path containing generated PDN def
```

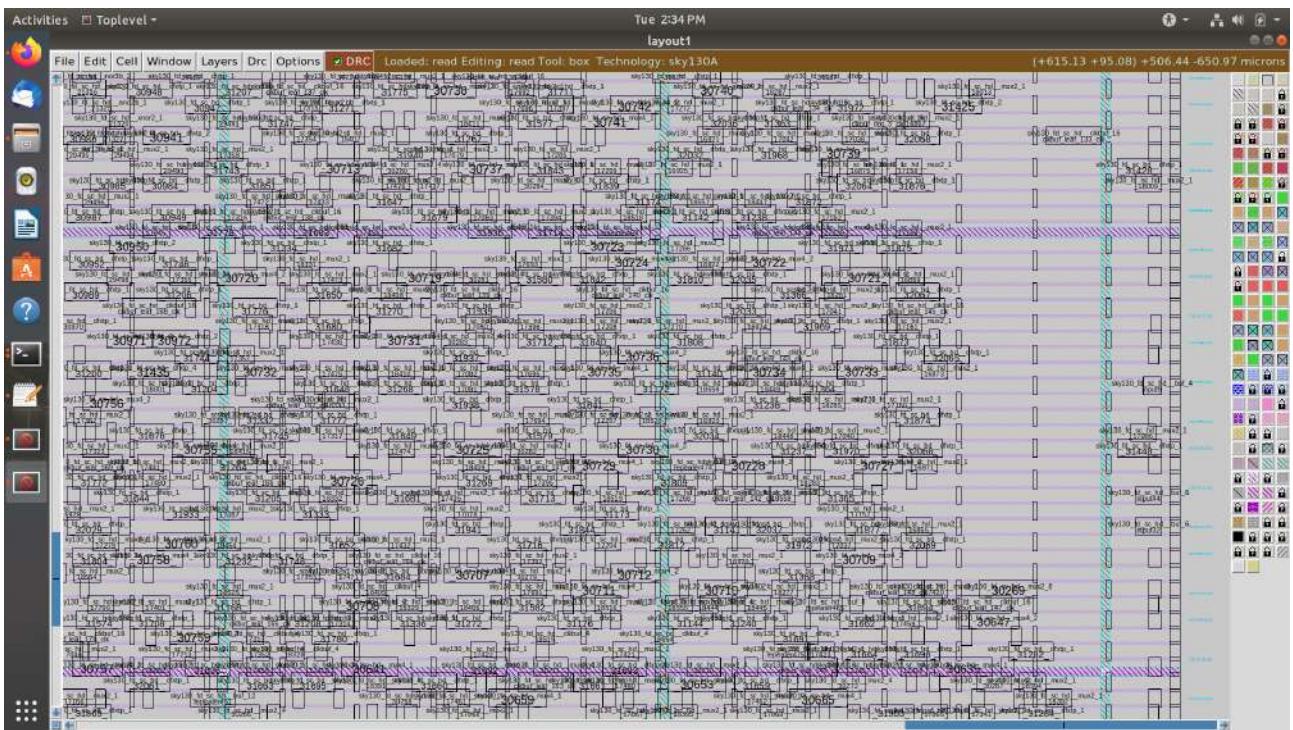
```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/  
26-03_08-45/tmp/floorplan/
```

```
# Command to load the PDN def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read 14-pdn.def &
```

Screenshots of PDN def





2. Perform detailed routing using TritonRoute and explore the routed layout.

Command to perform routing

```
# Check value of 'CURRENT_DEF'
```

```
echo $::env(CURRENT_DEF)
```

```
# Check value of 'ROUTING_STRATEGY'
```

```
echo $::env(ROUTING_STRATEGY)
```

```
# Command for detailed route using TritonRoute
```

```
run_routing
```

Screenshots of routing run

```
Activities Terminal - Tue 2:48 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
% echo $::env(ROUTING_STRATEGY)
can't read "::env(ROUTING_STRATEGY)": no such variable
% run_routing
[INFO]: Routing...
[INFO]: Running Global Routing...
[INFO]: current step index: 15
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
Notice 0: Design: picorv32a
Notice 0: Created 411 pins.
Notice 0: Created 25690 components and 145610 component-terminals.
Notice 0: Created 2 special nets and 0 connections.
Notice 0: Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
Min routing layer: 2
Max routing layer: 6
```

```
Activities Terminal - Tue 3:38 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
elapsed time = 00:00:08, memory = 782.73 (MB)
completing 60% with 0 violations
elapsed time = 00:00:10, memory = 782.73 (MB)
completing 70% with 0 violations
elapsed time = 00:00:12, memory = 782.73 (MB)
completing 80% with 0 violations
elapsed time = 00:00:14, memory = 782.73 (MB)
completing 90% with 0 violations
elapsed time = 00:00:15, memory = 782.73 (MB)
completing 100% with 0 violations
elapsed time = 00:00:17, memory = 782.73 (MB)
number of violations = 0
cpu time = 00:00:16, elapsed time = 00:00:17, memory = 782.73 (MB), peak = 854.19 (MB)
total wire length = 1103187 um
total wire length on LAYER l1l = 2639 um
total wire length on LAYER met1 = 483058 um
total wire length on LAYER met2 = 482317 um
total wire length on LAYER met3 = 122196 um
total wire length on LAYER met4 = 12976 um
total wire length on LAYER met5 = 0 um
total number of vias = 145509
up-via summary (total 145509):

-----
FR_MASTERSLICE      0
      l1l    60472
      met1   78129
      met2   6540
```

```
Tue 3:29 PM  
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane  
File Edit View Search Terminal Help  
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]  
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]  
puts "[INFO]: Setting output delay to: $output_delay_value"  
[INFO]: Setting output delay to: 4.946000000000001  
puts "[INFO]: Setting input delay to: $input_delay_value"  
[INFO]: Setting input delay to: 4.946000000000001  
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]  
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]  
#set rst_indx [lsearch [all_inputs] [get_port resetn]]  
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]  
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]  
set all_inputs_wo_clk_rst $all_inputs_wo_clk  
# correct resetn  
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst  
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}  
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]  
# TODO set this as parameter  
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]  
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]  
puts "[INFO]: Setting load to: $cap_load"  
[INFO]: Setting load to: 0.01765  
set_load $cap_load [all_outputs]  
tns 0.00  
wns 0.00  
[INFO]: Calculating Runtime From the Start...  
[INFO]: Routing completed for picorv32a/26-03_08-45 in 1h7m11s  
::: %
```

Commands to load routed def in magic in another terminal

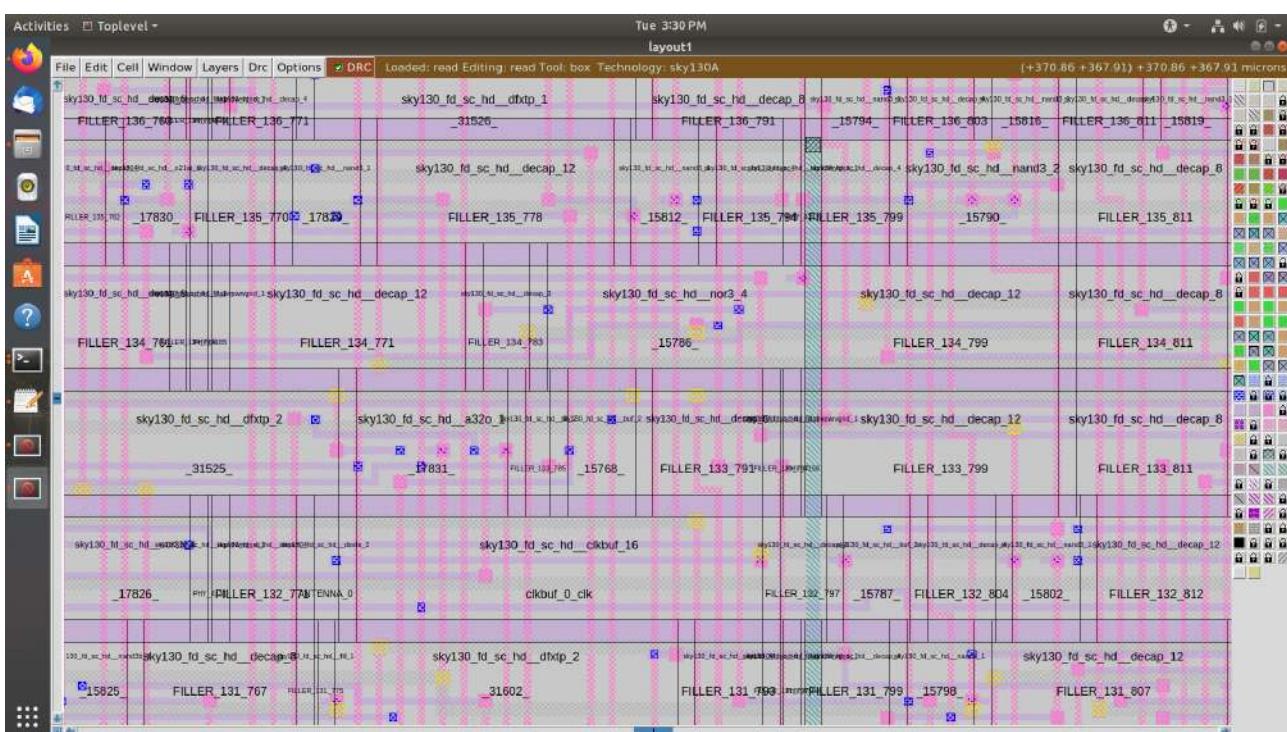
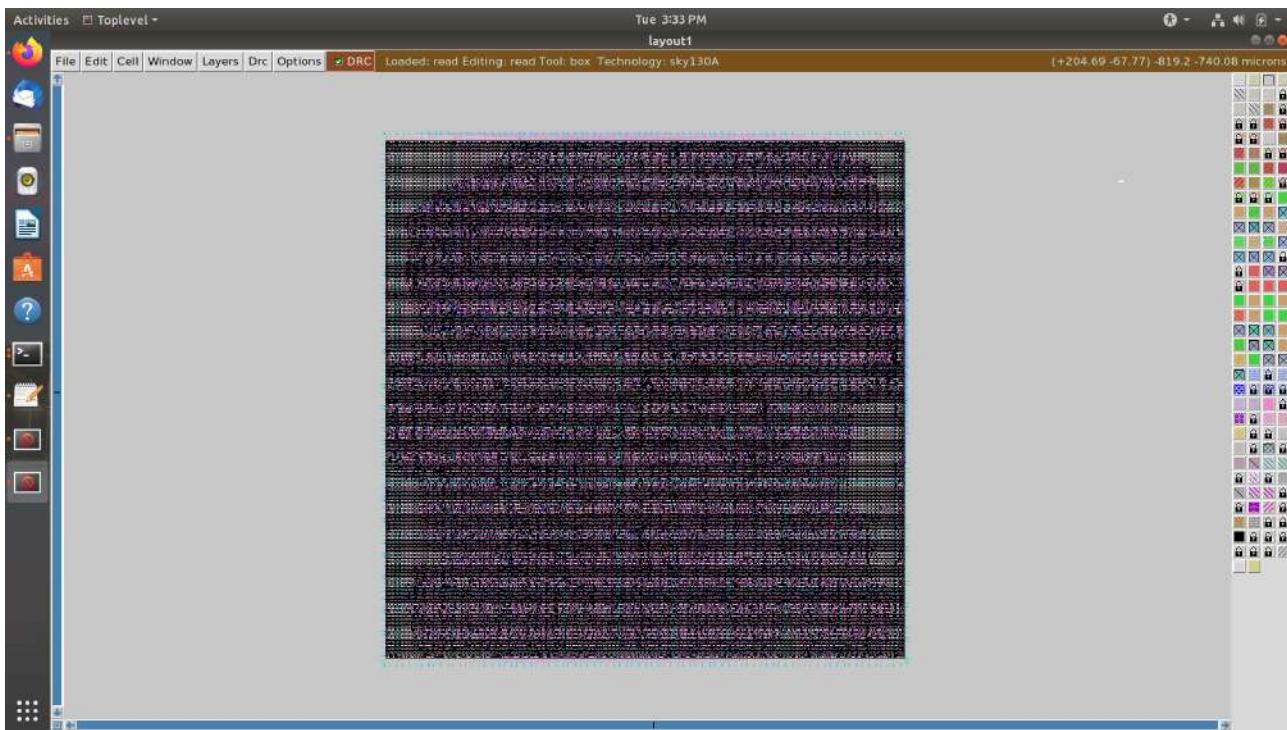
Change directory to path containing routed def

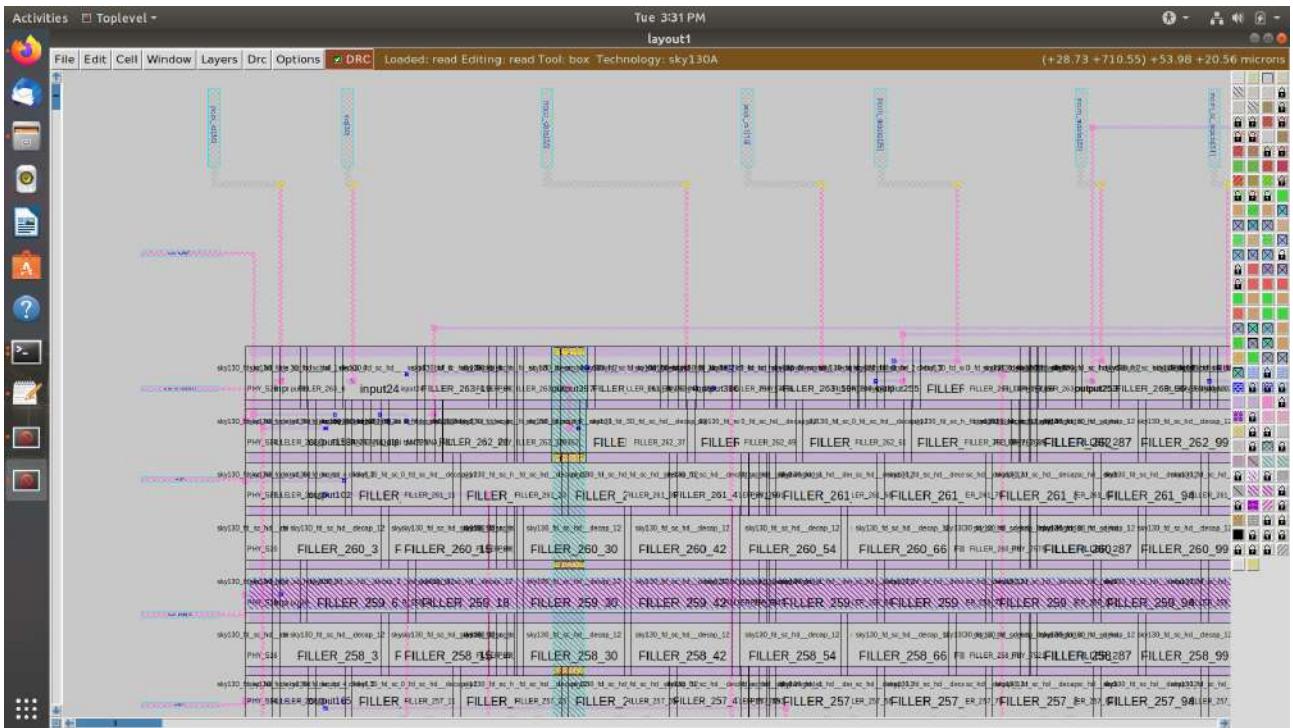
```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/  
26-03_08-45/results/routing/
```

Command to load the routed def in magic tool

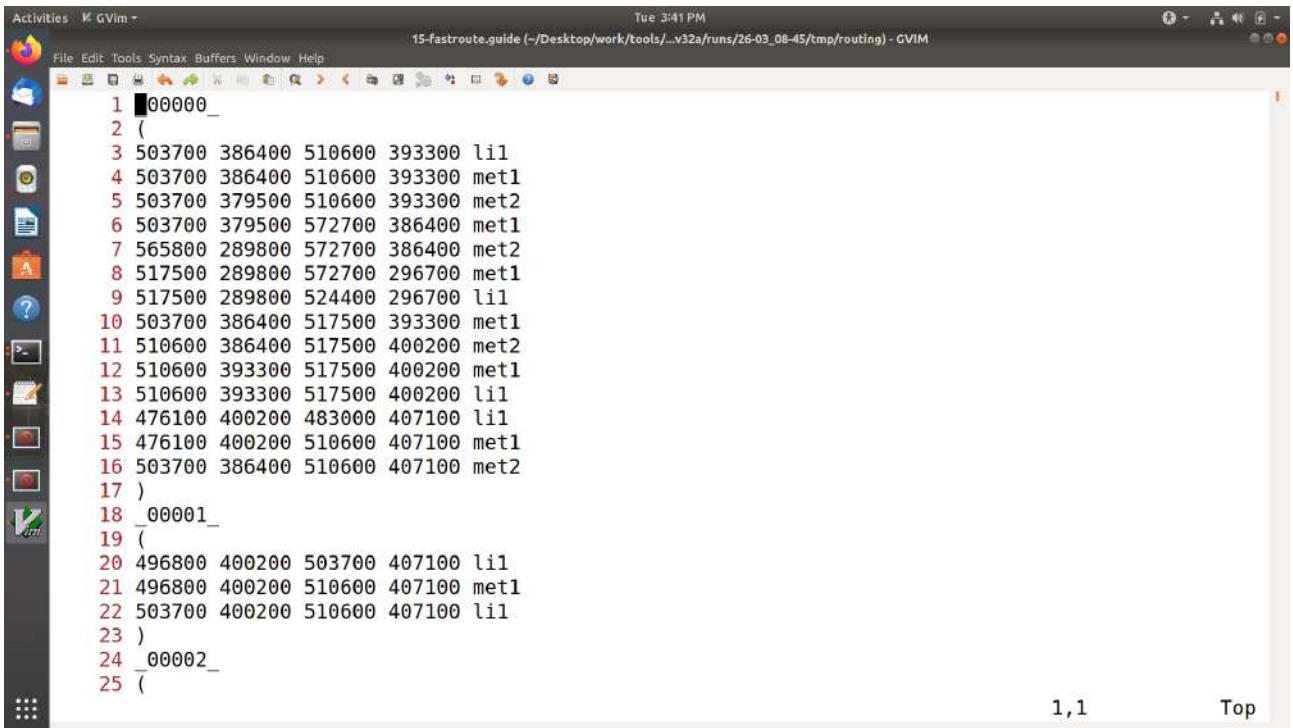
```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.def &
```

Screenshots of routed def





Screenshot of fast route guide present in openlane/designs/picorv32a/runs/26-03_08-45/tmp/routing directory



The screenshot shows a terminal window titled "Activities" with "GVim" selected. The title bar displays "15-fastroute.guide (~/Desktop/work/tools/...v32a/runs/26-03_08-45/tmp/routing) - GVIM" and the date and time "Tue 3:41 PM". The GVim interface includes a toolbar with icons for file operations like Open, Save, and Print, and a menu bar with File, Edit, Tools, Syntax, Buffers, Window, and Help. The main editor area contains the following text:

```
1 _00000_
2 (
3 503700 386400 510600 393300 l1l
4 503700 386400 510600 393300 met1
5 503700 379500 510600 393300 met2
6 503700 379500 572700 386400 met1
7 565800 289800 572700 386400 met2
8 517500 289800 572700 296700 met1
9 517500 289800 524400 296700 l1l
10 503700 386400 517500 393300 met1
11 510600 386400 517500 400200 met2
12 510600 393300 517500 400200 met1
13 510600 393300 517500 400200 l1l
14 476100 400200 483000 407100 l1l
15 476100 400200 510600 407100 met1
16 503700 386400 510600 407100 met2
17 )
18 _00001_
19 (
20 496800 400200 503700 407100 l1l
21 496800 400200 510600 407100 met1
22 503700 400200 510600 407100 l1l
23 )
24 _00002_
25 )
```

The status bar at the bottom right shows "1,1" and "Top".

3. Post-Route parasitic extraction using SPEF extractor.

Commands for SPEF extraction using external tool

```
# Change directory
```

```
cd Desktop/work/tools/SPEF_EXTRACTOR
```

```
# Command extract spef
```

```
python3 main.py /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/
designs/picorv32a/runs/26-03_08-45/tmp/merged.lef /home/vsduser/Desktop/work/tools/
openlane_working_dir/openlane/designs/picorv32a/runs/26-03_08-45/results/routing/
picorv32a.def
```

4. Post-Route OpenSTA timing analysis with the extracted parasitics of the route.

Commands to be run in OpenLANE flow to do OpenROAD timing analysis with integrated OpenSTA in OpenROAD

```
# Command to run OpenROAD tool
```

```
openroad
```

```
# Reading lef file
```

```
read_lef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
```

```
# Reading def file
```

```
read_def /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/  
picorv32a.def
```

```
# Creating an OpenROAD database to work with
```

```
write_db pico_route.db
```

```
# Loading the created database in OpenROAD
```

```
read_db pico_route.db
```

```
# Read netlist post CTS
```

```
read_verilog /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/synthesis/  
picorv32a.synthesis_preroute.v
```

```
# Read library for design

read_liberty $::env(LIB_SYNTH_COMPLETE)

# Link design and library

link_design picorv32a

# Read in the custom sdc we created

read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc

# Setting all cloks as propagated clocks

set_propagated_clock [all_clocks]

# Read SPEF

read_spef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/
picorv32a.spef

# Generating custom timing report

report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format
full_clock_expanded -digits 4
```

```
# Exit to OpenLANE flow
```

```
exit
```

Screenshots of commands run and timing report generated

```

Activities Terminal - Tue 11:16 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% openroad
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
% read_lef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
% read_def /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.def
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.def
Notice 0: Design: picorv32a
Notice 0: Created 429 pins.
Notice 0: Created 65617 components and 305814 component-terminals.
Notice 0: Created 2 special nets and 0 connections.
Notice 0: Created 18084 nets and 60532 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.def
% write_db pico_route.db
% read_db pico_route.db
% read_verilog /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/synthesis/picorv32a.synthesis_preroute.v
% read_liberty /openLANE_flow/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib
1
::: % link design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_fill_1 has no liberty cell.

```

```

Activities Terminal - Tue 11:17 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% link_design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_fill_1 has no liberty cell.
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_fill_2 has no liberty cell.
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_tapvpwrvrnd_1 has no liberty cell.
% read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
[INFO]: Setting output delay to: 4.9460000000000001
[INFO]: Setting input delay to: 4.9460000000000001
[INFO]: Setting load to: 0.017653
% set_propagated_clock [all_clocks]
% read_spef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.spef
1
% report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
Startpoint: _30900_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30910_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----
                           0.0000  0.0000  clock clk (rise edge)
                           0.0000  0.0000  clock source latency
                           0.0897  0.0624  0.0624 ^ clk (in)
                           0.0563          clk (net)
                           0.0900  0.0000  0.0624 ^ clkbuf_0_clk/A (sky130_fd_sc_hd_clkbuff_16)
                           0.0371  0.1366  0.1990 ^ clkbuf_0_clk/X (sky130_fd_sc_hd_clkbuff_16)
                           2     0.0143          clknet_0_clk (net)

```

```

Activities Terminal - Tue 11:17 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      5  0.0099
      0.0596  0.0002  2.3273 ^ clknet_leaf_220_clk (net)
      0.0000  2.3273  clock reconvergence pessimism
      -0.0274  2.2998  library hold time
      2.2998  data required time
      2.2998  data required time
      -1.9092  data arrival time
      -0.3907  slack (VIOLATED)

Startpoint: resetn (input port clocked by clk)
Endpoint: mem_la_read (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout   Cap     Slew     Delay    Time   Description
-----+-----+-----+-----+-----+
          0.0000  0.0000  clock clk (rise edge)
          0.0000  0.0000  clock network delay (propagated)
          4.9460  4.9460 ^ input external delay
          0.0172  0.0055  4.9515 ^ resetn (in)
          1  0.0042   resetn (net)
          0.0172  0.0000  4.9515 ^ input101/A (sky130_fd_sc_hd_clkbuf_8)
          0.0662  0.1329  5.0843 ^ input101/X (sky130_fd_sc_hd_clkbuf_8)
          7  0.0299   net101 (net)

```

```

Activities Terminal - Tue 11:17 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      6  0.0211
      0.0760  0.0002  5.2498 ^ 12638_(net)
      0.0933  0.0927  5.3425 v 17093/_C (sky130_fd_sc_hd_nand3_4)
      4  0.0143
      0.0933  0.0001  5.3426 v 17093/_Y (sky130_fd_sc_hd_nand3_4)
      0.4344  0.3758  5.7184 ^ 13857_(net)
      2  0.0603
      0.4349  0.0115  5.7299 ^ 18867/_B1 (sky130_fd_sc_hd_a21oi_4)
      0.1189  0.2493  5.9793 ^ 18867/_Y (sky130_fd_sc_hd_a21oi_4)
      1  0.0177
      0.1189  0.0002  5.9795 ^ net199 (net)
      0.1189  0.0002  5.9795 ^ mem_la_read (net)
      24.7300  24.7300  clock clk (rise edge)
      0.0000  24.7300  clock network delay (propagated)
      0.0000  24.7300  clock reconvergence pessimism
      -4.9460  19.7840  output external delay
      19.7840  data required time
      -5.9795  data arrival time
      13.8045  slack (MET)

% exit
%
```

About

2 Week digital VLSI SoC design and planning workshop with complete RTL2GDSII flow organised by VSD in collaboration with NASSCOM (Advanced Physical Design using OpenLANE/Sky130)

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Folders and files

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Latest commit



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History

--	--	--

Desktop/work/tools/ openlane working dir	Add files via upload	
--	--	--

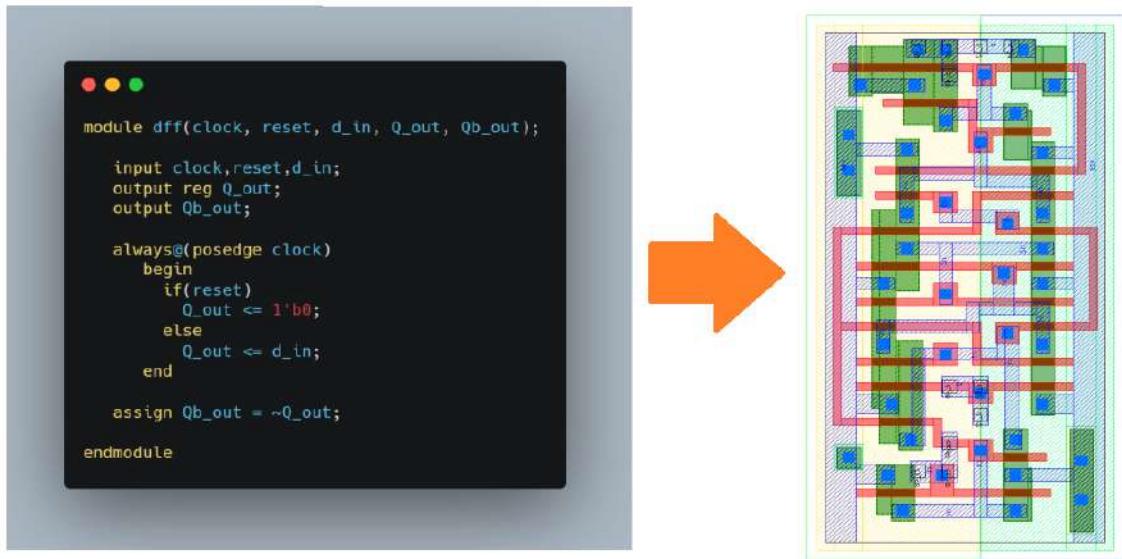
drc test	Add files via upload	
--------------------------	--	--

README.m d	Update README.md	
--------------------------------	--------------------------------------	--

drc tests.tg z	Add files via upload	
------------------------------------	--	--

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Digital VLSI SoC Design & Planning (RTL2GDSII Flow)

Digital VLSI SoC Design and Planning

OS linux

EDA Tools OpenLANE-Flow, Yosys, abc, OpenROAD, TritonRoute, OpenSTA, magic, netgen, GUNA

languages verilog, bash, TCL last commit last wednesday languages 12

verilog 96.2% repo size 179 MB code size 32.9 MB files 4

2 Week digital VLSI SoC design and planning workshop with complete RTL2GDSII flow organised by VSD in collaboration with NASSCOM

Section 1 - Inception of open-source EDA, OpenLANE and Sky130 PDK (14/03/2024 - 15/03/2024)

Theory

Expand or Collapse

Implementation

Section 1 tasks:-

1. Run 'picorv32a' design synthesis using OpenLANE flow and generate necessary outputs.
2. Calculate the flop ratio.

- All section 1 logs, reports and results can be found in following run folder:

Section 1 Run - 15-03_15-51

1. Run 'picorv32a' design synthesis using OpenLANE flow and generate necessary outputs.

Commands to invoke the OpenLANE flow and perform synthesis

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:vo.21'
```

```
# Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command
```

```
docker
```

```
# Now that we have entered the OpenLANE flow contained docker sub-system we can  
invoke the OpenLANE flow in the Interactive mode using the following command
```

```
./flow.tcl -interactive
```

```
# Now that OpenLANE flow is open we have to input the required packages for proper  
functionality of the OpenLANE flow
```

```
package require openlane 0.9
```

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the  
design creating some necessary files and directories for running a specific design which in  
our case is 'picorv32a'
```

```
prep -design picorv32a
```

```
# Now that the design is prepped and ready, we can run synthesis using following  
command
```

```
run_synthesis
```

```
# Exit from OpenLANE flow
```

```
exit
```

```
# Exit from OpenLANE flow docker sub-system
```

`exit`

Screenshots of running each commands

Activities Terminal Fri 9:23 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
vsduser@vsdsquadron:~$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ docker
bash-4.2$ ./flow.tcl -interactive
[INFO]:
[INFO]: Version: v0.21
[INFO]: Running interactively
% package require openlane 0.9
0.9
% prep -design picorv32a
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/15-03_15-51
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane
```

Activities Terminal Fri 9:24 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/15-03_15-51
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.tlef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1l met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
[INFO]: % run_synthesis[]
```

```
Activities Terminal Fri 9:29 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -759.46
wns -24.89
[INFO]: Synthesis was successful
::: %
```

2. Calculate the flop ratio.

Screenshots of synthesis statistics report file with required values highlighted

Activities M GVim Fri 10:02 PM

File Edit Tools Syntax Buffers Window Help

```

1 28. Printing statistics.
2
3 === picorv32a ===
4
5     Number of wires:          14596
6     Number of wire bits:      14978
7     Number of public wires:   1565
8     Number of public wire bits: 1947
9
10    Number of memories:       0
11    Number of memory bits:    0
12    Number of processes:      0
13    Number of cells:          14876
14        sky130_fd_sc_hd_a2111o_2      1
15        sky130_fd_sc_hd_a211o_2      35
16        sky130_fd_sc_hd_a211oi_2     60
17        sky130_fd_sc_hd_a21bo_2      149
18        sky130_fd_sc_hd_a21boi_2     8
19        sky130_fd_sc_hd_a21o_2       57
20        sky130_fd_sc_hd_a21oi_2      244
21        sky130_fd_sc_hd_a221o_2      86
22        sky130_fd_sc_hd_a22o_2       1013
23        sky130_fd_sc_hd_a2bb2o_2     1748
24        sky130_fd_sc_hd_a2bb2oi_2    81
25        sky130_fd_sc_hd_a311o_2      2

```

hlsearch 25, 38 Top

Activities M GVIM Fri 10:03 PM

File Edit Tools Syntax Buffers Window Help

```

25    sky130_fd_sc_hd_a311o_2      2
26    sky130_fd_sc_hd_a31o_2       49
27    sky130_fd_sc_hd_a31oi_2      7
28    sky130_fd_sc_hd_a32o_2       46
29    sky130_fd_sc_hd_a41o_2       1
30    sky130_fd_sc_hd_and2_2       157
31    sky130_fd_sc_hd_and3_2       58
32    sky130_fd_sc_hd_and4_2       345
33    sky130_fd_sc_hd_and4b_2      1
34    sky130_fd_sc_hd_buf_1        1656
35    sky130_fd_sc_hd_buf_2        8
36    sky130_fd_sc_hd_conb_1       42
37    sky130_fd_sc_hd_dfxtp_2      1613
38    sky130_fd_sc_hd_inv_2        1615
39    sky130_fd_sc_hd_mux2_1       1224
40    sky130_fd_sc_hd_mux2_2       2
41    sky130_fd_sc_hd_mux4_1       221
42    sky130_fd_sc_hd_nand2_2      78
43    sky130_fd_sc_hd_nor2_2       524
44    sky130_fd_sc_hd_nor2b_2      1
45    sky130_fd_sc_hd_nor3_2       42
46    sky130_fd_sc_hd_nor4_2       1
47    sky130_fd_sc_hd_o2111a_2     2
48    sky130_fd_sc_hd_o211a_2      69
49    sky130_fd_sc_hd_o211ai_2     6

```

search hit BOTTOM, continuing at TOP 49, 38 48%

Calculation of Flop Ratio and DFF % from synthesis statistics report file

Section 2 - Good floorplan vs bad floorplan and introduction to library cells (16/03/2024 - 17/03/2024)

Theory

Implementation

Section 2 tasks:-

1. Run 'picorv32a' design floorplan using OpenLANE flow and generate necessary outputs.
 2. Calculate the die area in microns from the values in floorplan def.
 3. Load generated floorplan def in magic tool and explore the floorplan.
 4. Run 'picorv32a' design congestion aware placement using OpenLANE flow and generate necessary outputs.
 5. Load generated placement def in magic tool and explore the placement.
-
- All section 2 logs, reports and results can be found in following run folder:

Section 2 Run - 17-03_12-06

1. Run 'picorv32a' design floorplan using OpenLANE flow and generate necessary outputs.

Commands to invoke the OpenLANE flow and perform floorplan

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:v0.21'
```

Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command

```
docker
```

Now that we have entered the OpenLANE flow contained docker sub-system we can invoke the OpenLANE flow in the interactive mode using the following command

```
./flow.tcl -interactive
```

Now that OpenLANE flow is open we have to input the required packages for proper functionality of the OpenLANE flow

```
package require openlane 0.9
```

Now the OpenLANE flow is ready to run any design and initially we have to prep the design creating some necessary files and directories for running a specific design which in our case is 'picorv32a'

```
prep -design picorv32a
```

Now that the design is prepped and ready, we can run synthesis using following command

```
run_synthesis
```

```
# Now we can run floorplan
```

```
run_floorplan
```

Screenshot of floorplan run

```
Activities Terminal Sun 6:06 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: Synthesis was successful
% run_floorplan
[INFO]: Running Floorplanning...
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 3
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/l
ib/sky130_fd_sc_hd_tt_025C_lv80.lib line 31, default_operating_condition tt_025C_lv80 not found.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/merged_unpadded.le
f
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 440 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/merged_unpadded.le
f
[INFO IFP-0001] Added 238 rows of 1412 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 660.685 671.405 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/reports/floorplan/3-verilog2def.die_area.rpt.
[INFO] Floorplanned on a core area of 5.52 10.88 655.04 658.24 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/reports/floorplan/3-verilog2def.core_area.rpt.
[INFO]: Core area width: 649.52
[INFO]: Core area height: 647.36
[INFO]: Changing layout from 0 to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/floorplan/3-ve
rilog2def_openroad.def
[INFO]: Running IO Placement...
[INFO]: success! step index: 3
```

```
Activities Terminal Sun 6:06 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
er stripe. Moving to closest stripe at (567.000um, 103.880um).
[WARNING PSM-0030] Vsrc location at (565.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 257.060um).
[WARNING PSM-0030] Vsrc location at (5.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (145.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
[WARNING PSM-0030] Vsrc location at (425.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 563.420um).
[INFO PSM-0031] Number of nodes on net VGND = 19223.
[INFO PSM-0037] G matrix created sucessfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/floorplan/picorv32a.floorplan.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/floorplan/7-pdn.def
1
% [ ]
```

2. Calculate the die area in microns from the values in floorplan def.

Screenshot of contents of floorplan def

```

1 VERSION 5.8 ;
2 DIVIDERCHAR "/";
3 BUSBITCHARS "[]";
4 DESIGN picorv32a ;
5 UNITS DISTANCE MICRONS 1000 ;
6 DIEAREA ( 0 0 ) ( 660685 671405 ) ;
7 ROW ROW_0 unithd 5520 10880 FS DO 1412 BY 1 STEP 460 0 ;
8 ROW ROW_1 unithd 5520 13600 N DO 1412 BY 1 STEP 460 0 ;
9 ROW ROW_2 unithd 5520 16320 FS DO 1412 BY 1 STEP 460 0 ;
10 ROW ROW_3 unithd 5520 19040 N DO 1412 BY 1 STEP 460 0 ;
11 ROW ROW_4 unithd 5520 21760 FS DO 1412 BY 1 STEP 460 0 ;
12 ROW ROW_5 unithd 5520 24480 N DO 1412 BY 1 STEP 460 0 ;
13 ROW ROW_6 unithd 5520 27200 FS DO 1412 BY 1 STEP 460 0 ;
14 ROW ROW_7 unithd 5520 29920 N DO 1412 BY 1 STEP 460 0 ;
15 ROW ROW_8 unithd 5520 32640 FS DO 1412 BY 1 STEP 460 0 ;
16 ROW ROW_9 unithd 5520 35360 N DO 1412 BY 1 STEP 460 0 ;
17 ROW ROW_10 unithd 5520 38080 FS DO 1412 BY 1 STEP 460 0 ;
18 ROW ROW_11 unithd 5520 40800 N DO 1412 BY 1 STEP 460 0 ;
19 ROW ROW_12 unithd 5520 43520 FS DO 1412 BY 1 STEP 460 0 ;
20 ROW ROW_13 unithd 5520 46240 N DO 1412 BY 1 STEP 460 0 ;
21 ROW ROW_14 unithd 5520 48960 FS DO 1412 BY 1 STEP 460 0 ;
22 ROW ROW_15 unithd 5520 51680 N DO 1412 BY 1 STEP 460 0 ;
23 ROW ROW_16 unithd 5520 54400 FS DO 1412 BY 1 STEP 460 0 ;
24 ROW ROW_17 unithd 5520 57120 N DO 1412 BY 1 STEP 460 0 ;
25 ROW ROW_18 unithd 5520 59840 FS DO 1412 BY 1 STEP 460 0 ;

```

According to floorplan def

3. Load generated floorplan def in magic tool and explore the floorplan.

Commands to load floorplan def in magic in another terminal

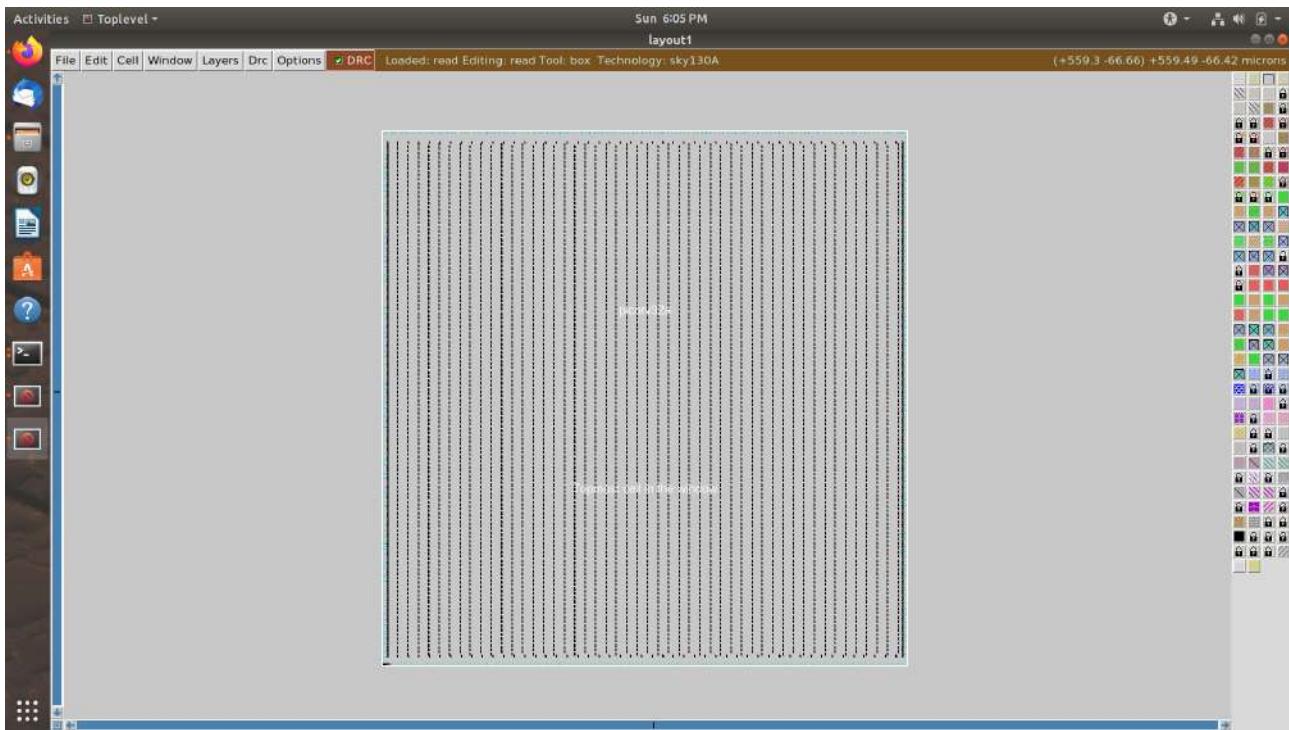
```
# Change directory to path containing generated floorplan def
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
17-03_12-06/results/floorplan/
```

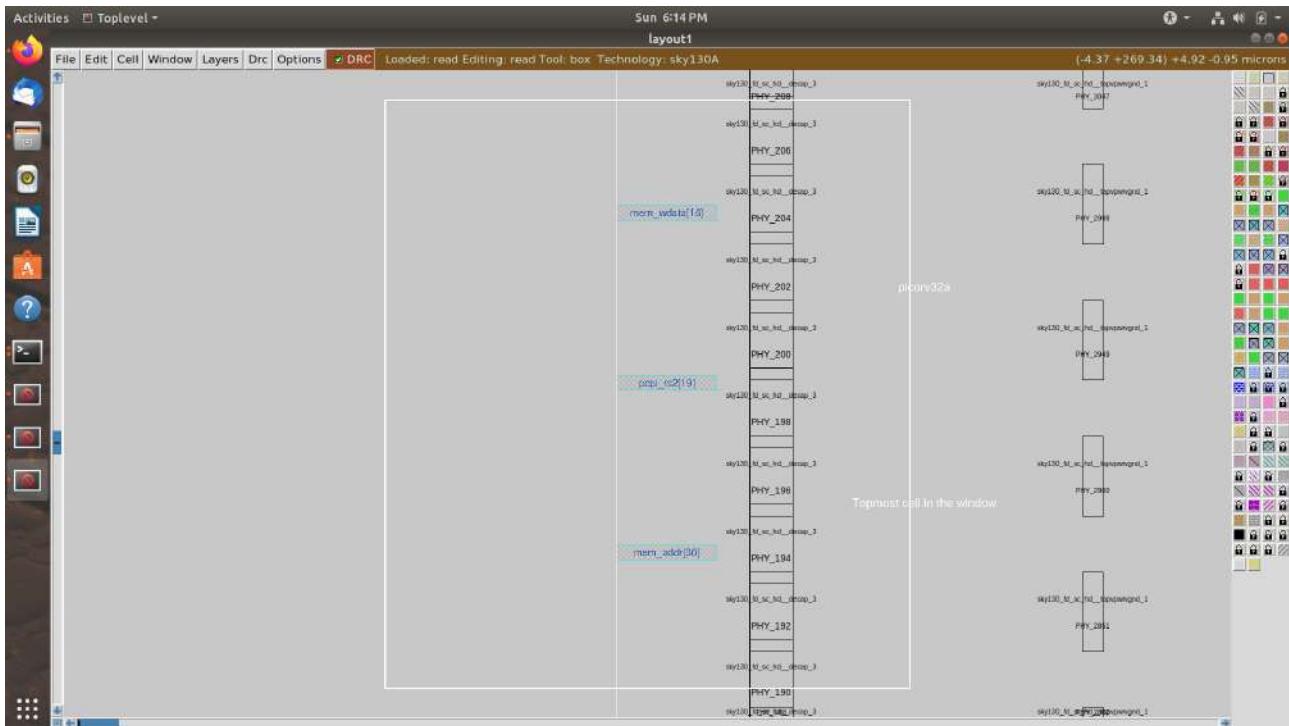
```
# Command to load the floorplan def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.floorplan.def &
```

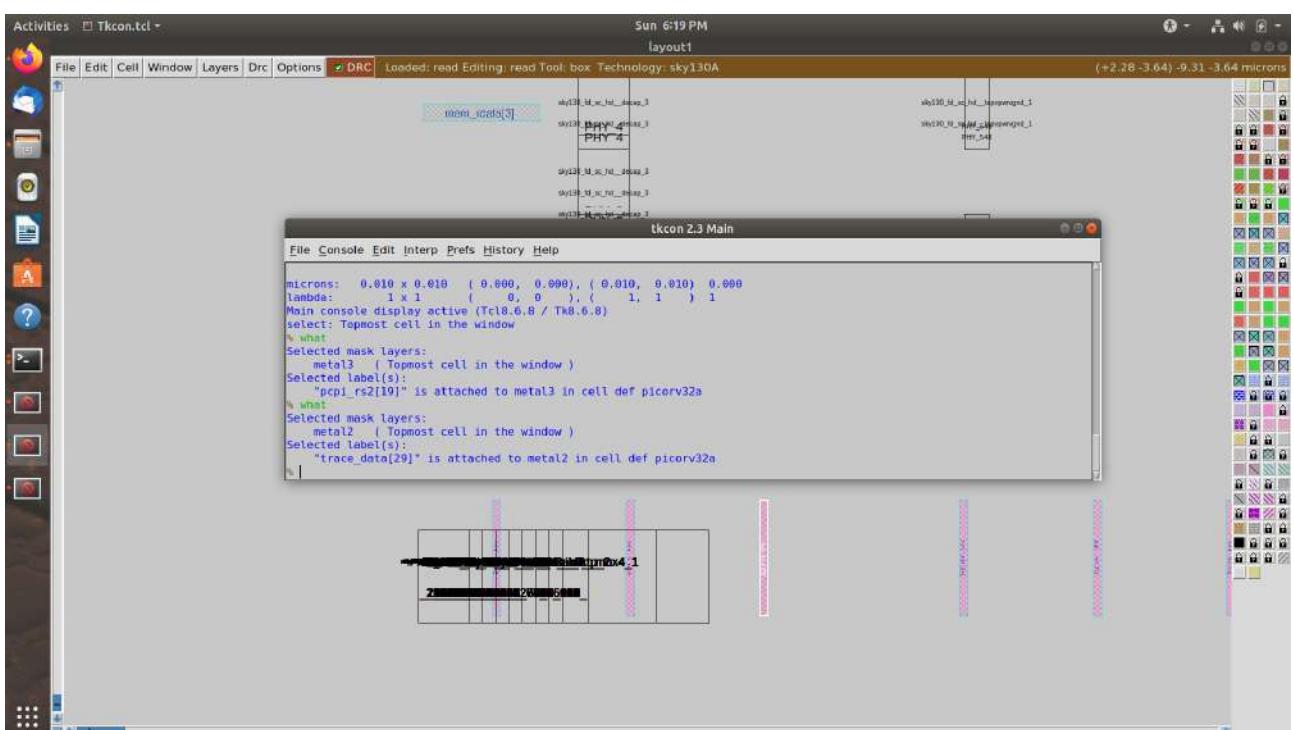
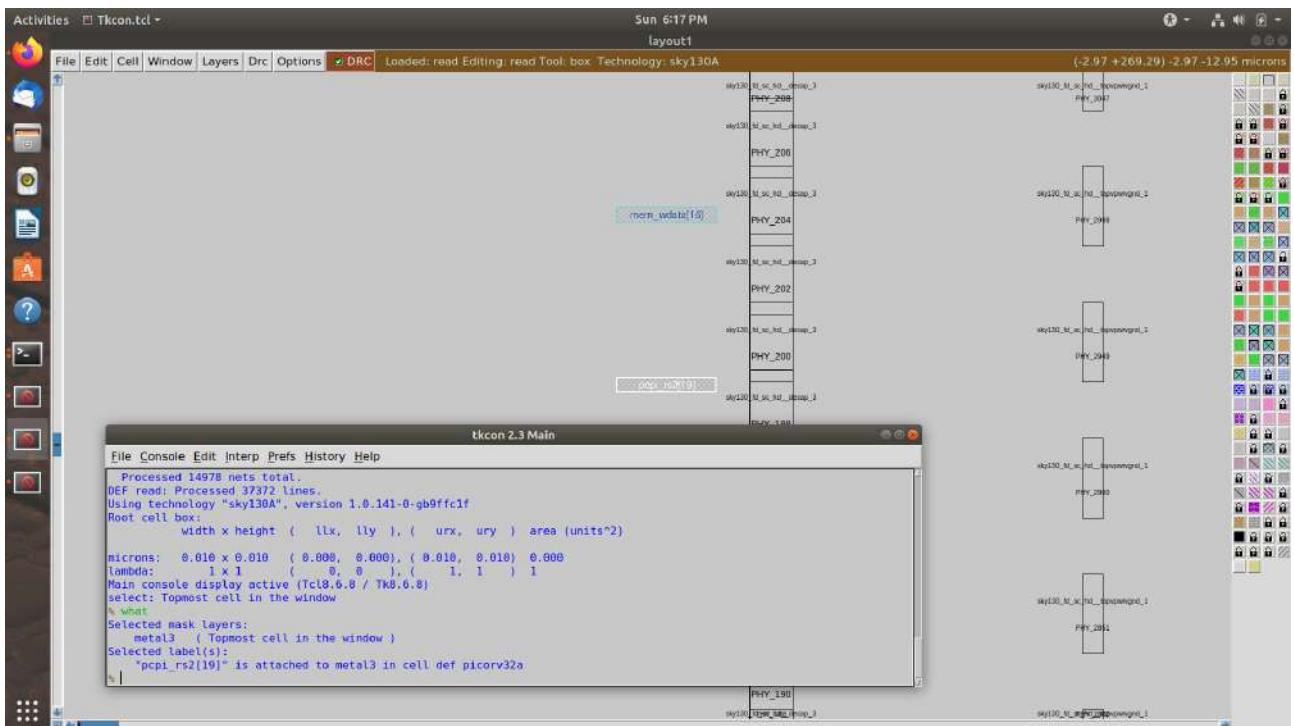
Screenshots of floorplan def in magic



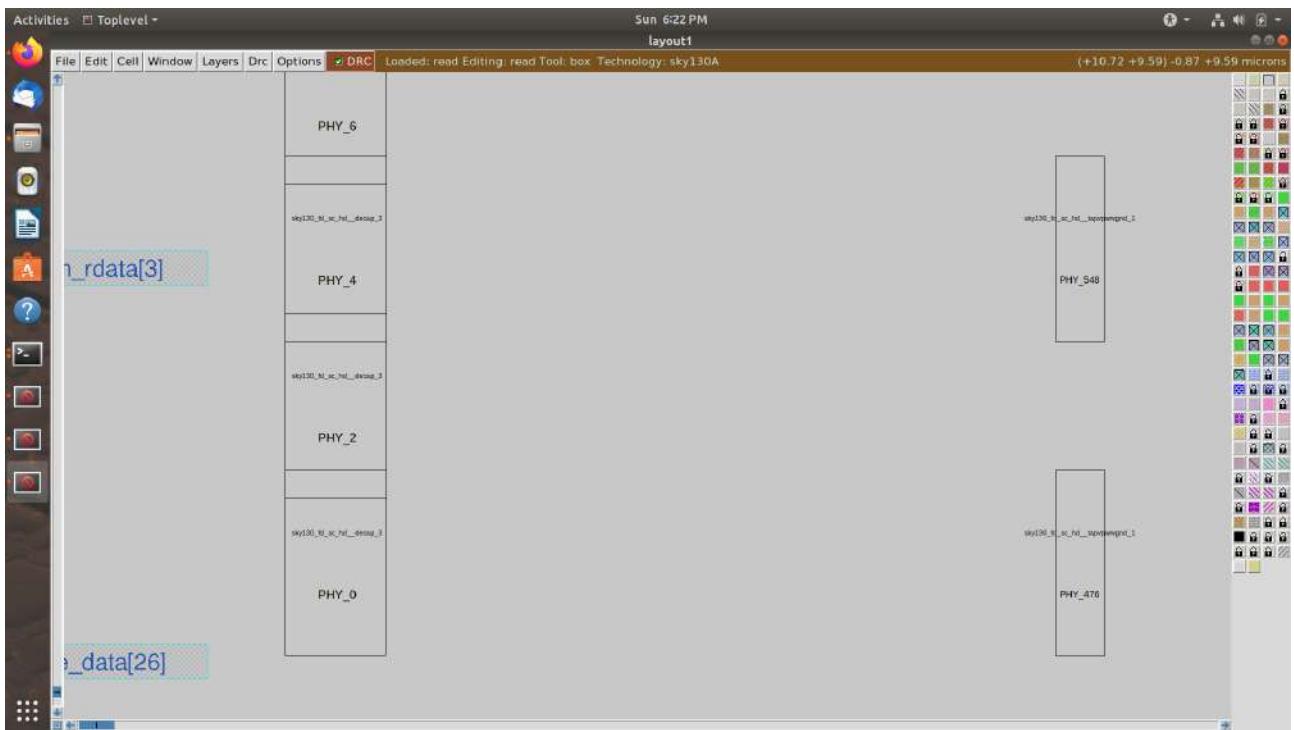
Equidistant placement of ports



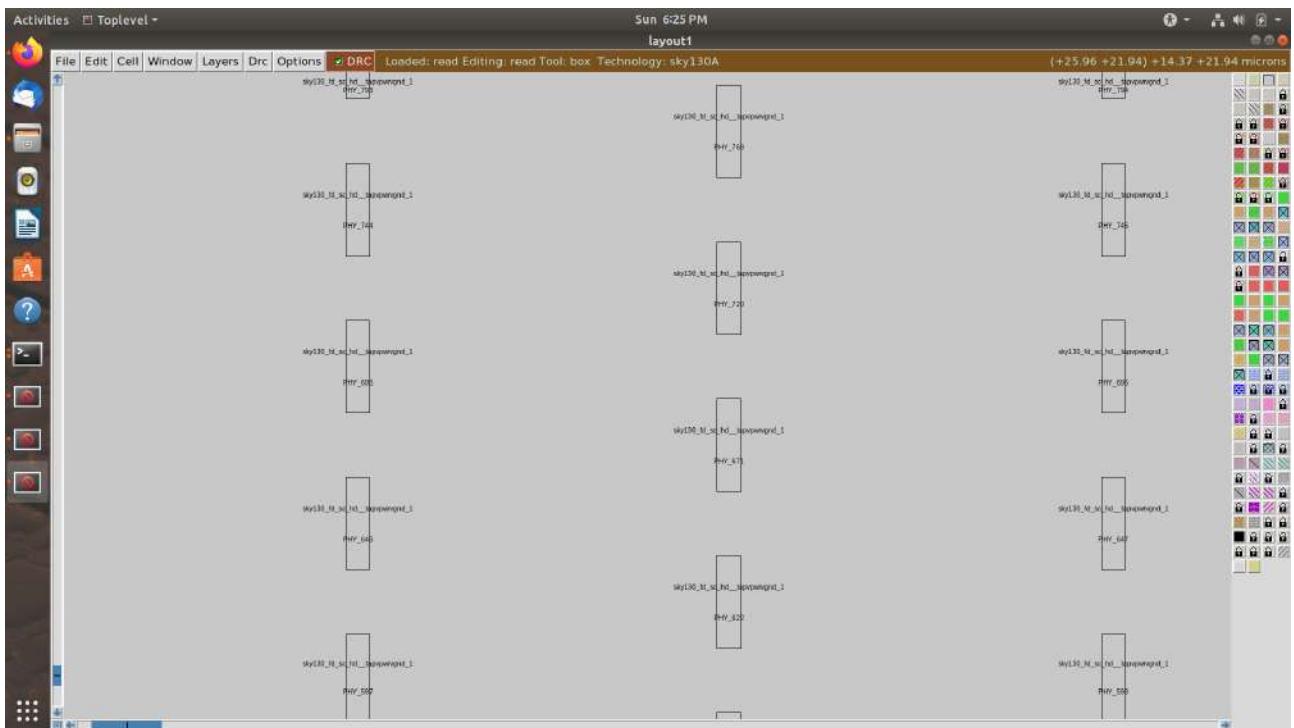
Port layer as set through config.tcl



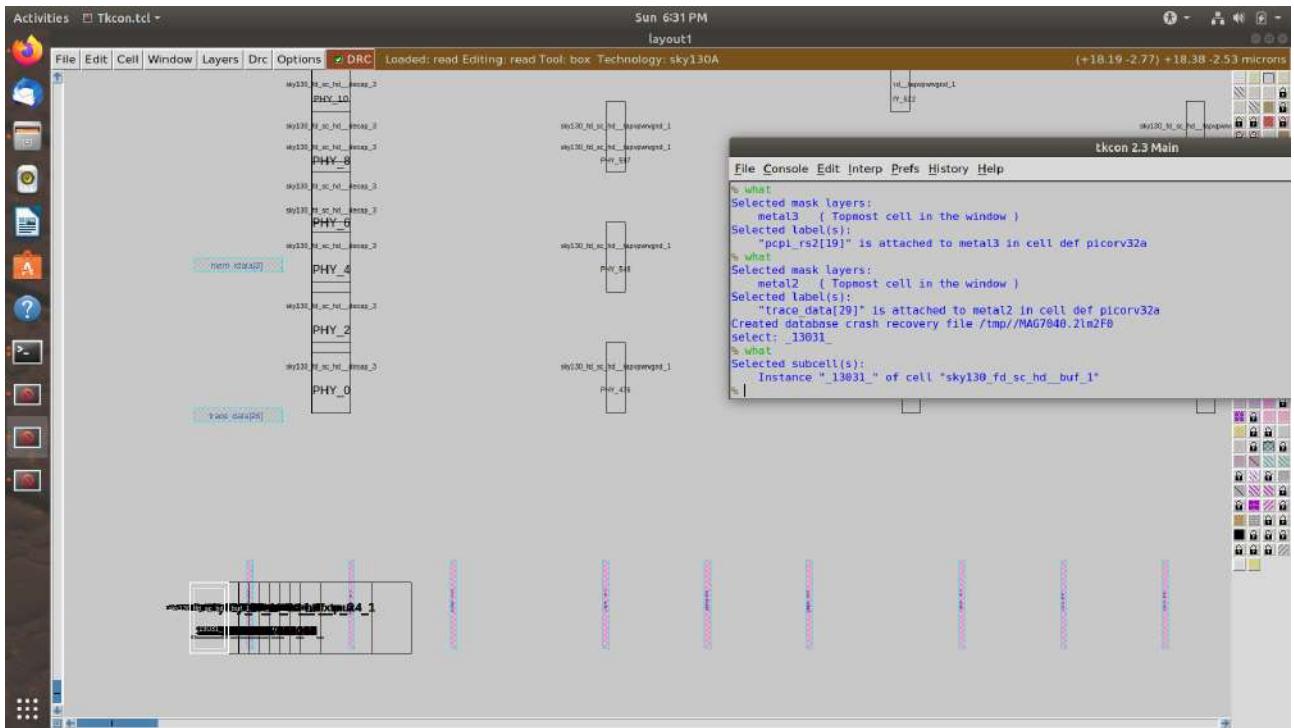
Decap Cells and Tap Cells



Diagonally equidistant Tap cells



Unplaced standard cells at the origin



4. Run 'picorv32a' design congestion aware placement using OpenLANE flow and generate necessary outputs.

Command to run placement

```
# Congestion aware placement by default
```

```
run_placement
```

Screenshots of placement run

```
Activities Terminal - Sun 10:44 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
er stripe. Moving to closest stripe at (567.000um, 103.880um).
[WARNING PSM-0030] Vsrc location at (565.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 257.060um).
[WARNING PSM-0030] Vsrc location at (5.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (145.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
[WARNING PSM-0030] Vsrc location at (425.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 563.420um).
[INFO PSM-0031] Number of nodes on net VGND = 19223.
[INFO PSM-0037] G matrix created sucessfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/floorplan/picorv32a.floorplan.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/floorplan/7-pdn.def
1
::: % run_placement
```

```
Activities Terminal - Sun 10:46 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
legalized HPWL      779196.5 u
delta HPWL          2 %

[INFO DPL-0020] Mirrored 6193 instances
[INFO DPL-0021] HPWL before      779196.5 u
[INFO DPL-0022] HPWL after       766080.0 u
[INFO DPL-0023] HPWL delta      -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/placement/8-resizer.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 12
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
::: %
```

5. Load generated placement def in magic tool and explore the placement.

Commands to load placement def in magic in another terminal

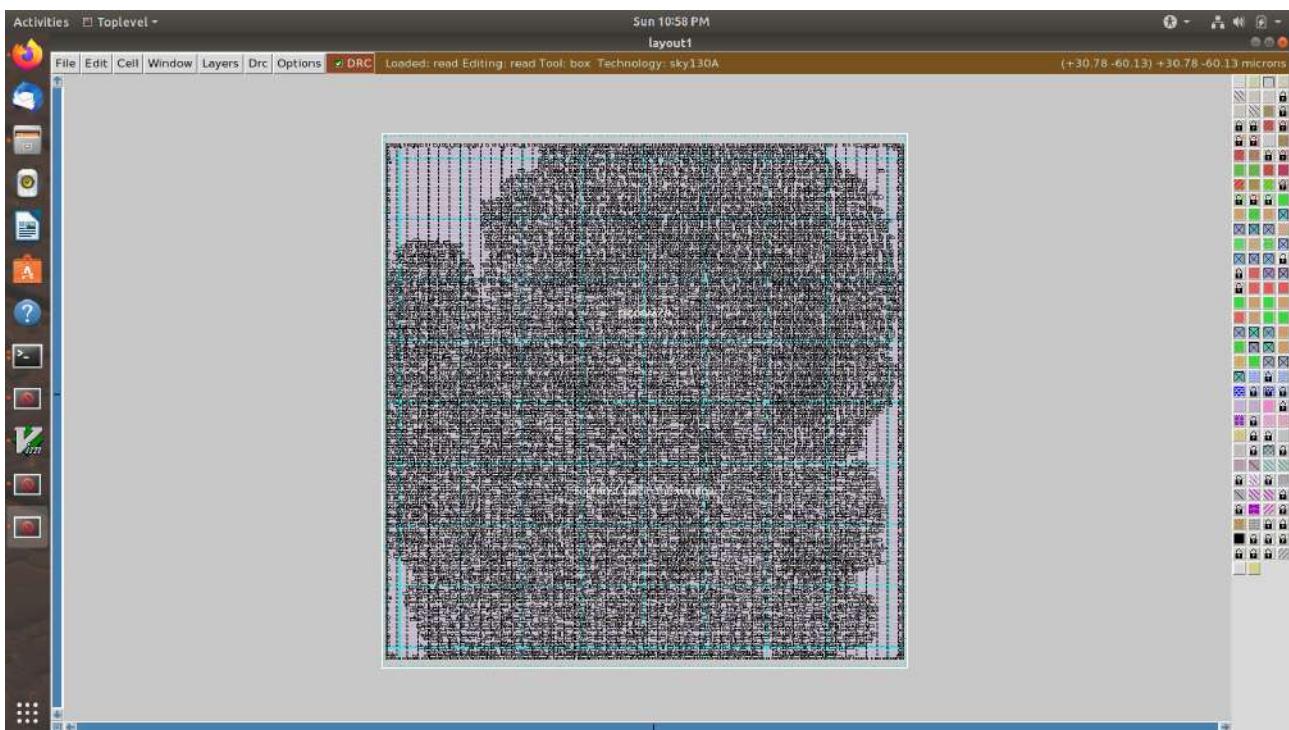
```
# Change directory to path containing generated placement def
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/  
17-03_12-06/results/placement/
```

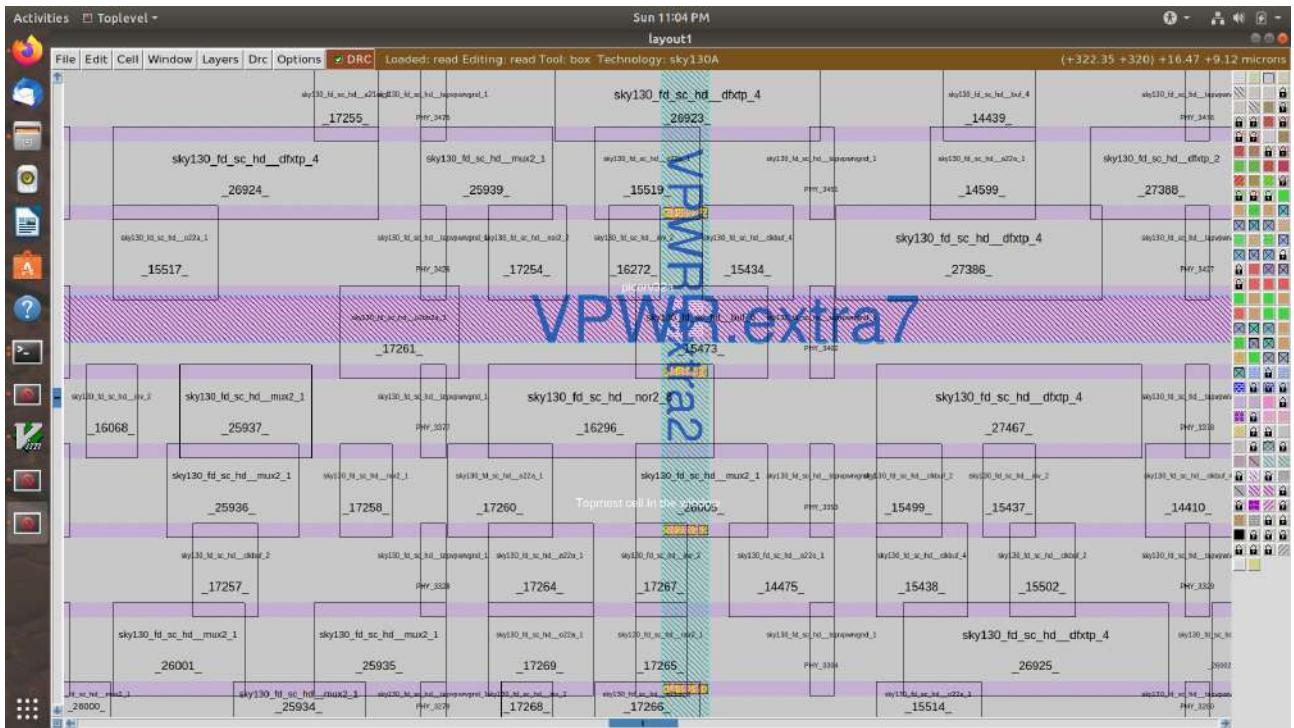
Command to load the placement def in magic tool

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def  
&
```

Screenshots of floorplan def in magic



Standard cells legally placed



Commands to exit from current run

```
# Exit from OpenLANE flow
```

```
exit
```

```
# Exit from OpenLANE flow docker sub-system
```

```
exit
```

Section 3 - Design library cell using Magic Layout and ngspice characterization (18/03/2024 - 21/03/2024)

Theory

Implementation

- **Section 3 tasks:-**
- 6. Clone custom inverter standard cell design from github repository: [Standard cell design and characterization using OpenLANE flow.](#)
- 7. Load the custom inverter layout in magic and explore.
- 8. Spice extraction of inverter in magic.
- 9. Editing the spice model file for analysis through simulation.
- 10. Post-layout ngspice simulations.
- 11. Find problem in the DRC section of the old magic tech file for the skywater process and fix them.
- Section 3 - Tasks 1 to 5 files, reports and logs can be found in the following folder:

[Section 3 - Tasks 1 to 5 \(vsdstdcelldesign\)](#)

- Section 3 - Task 6 files, reports and logs can be found in the following folder:

[Section 3 - Task 6 \(drc_tests\)](#)

1. Clone custom inverter standard cell design from github repository

```
# Change directory to openlane
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# Clone the repository with custom inverter design
```

```
git clone https://github.com/nickson-jose/vsdstdcelldesign
```

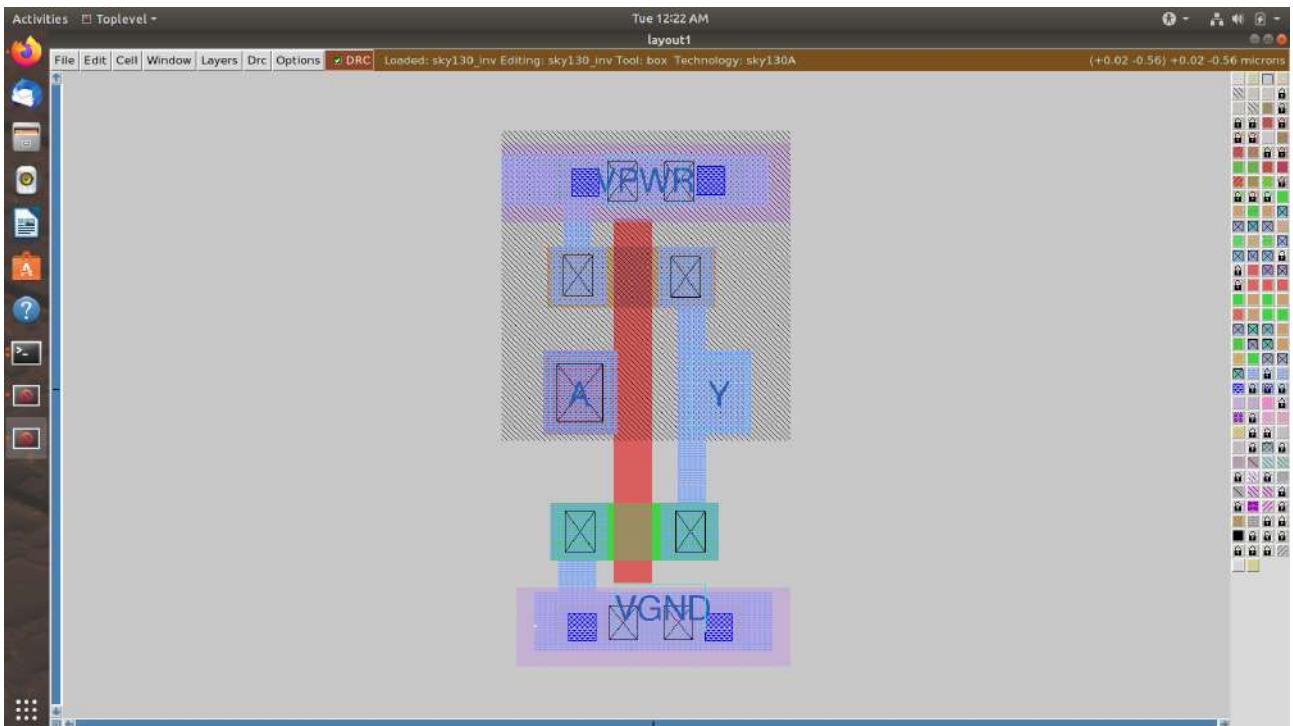
```
# Change into repository directory  
  
cd vsdstdcelldesign  
  
# Copy magic tech file to the repo directory for easy access  
  
cp /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/  
magic/sky130A.tech .  
  
# Check contents whether everything is present  
  
ls  
  
# Command to open custom inverter layout in magic  
  
magic -T sky130A.tech sky130_inv.mag &
```

Screenshot of commands run

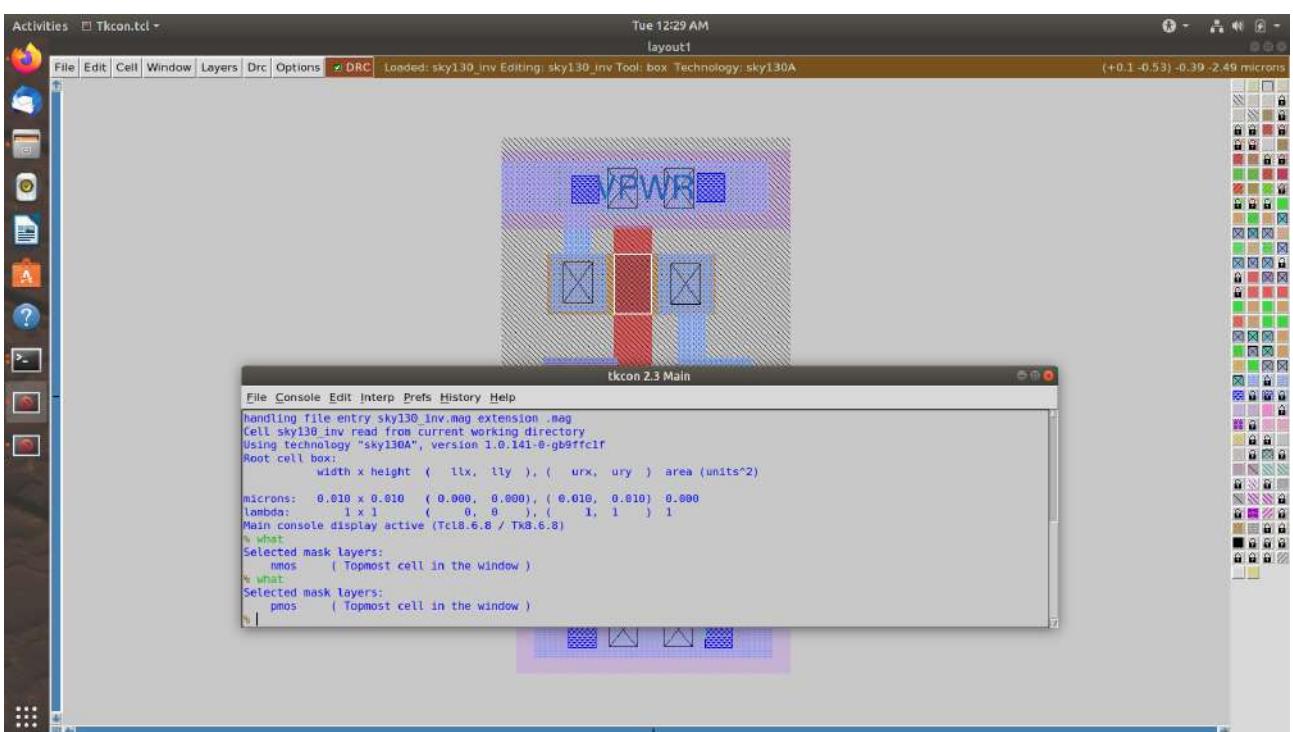
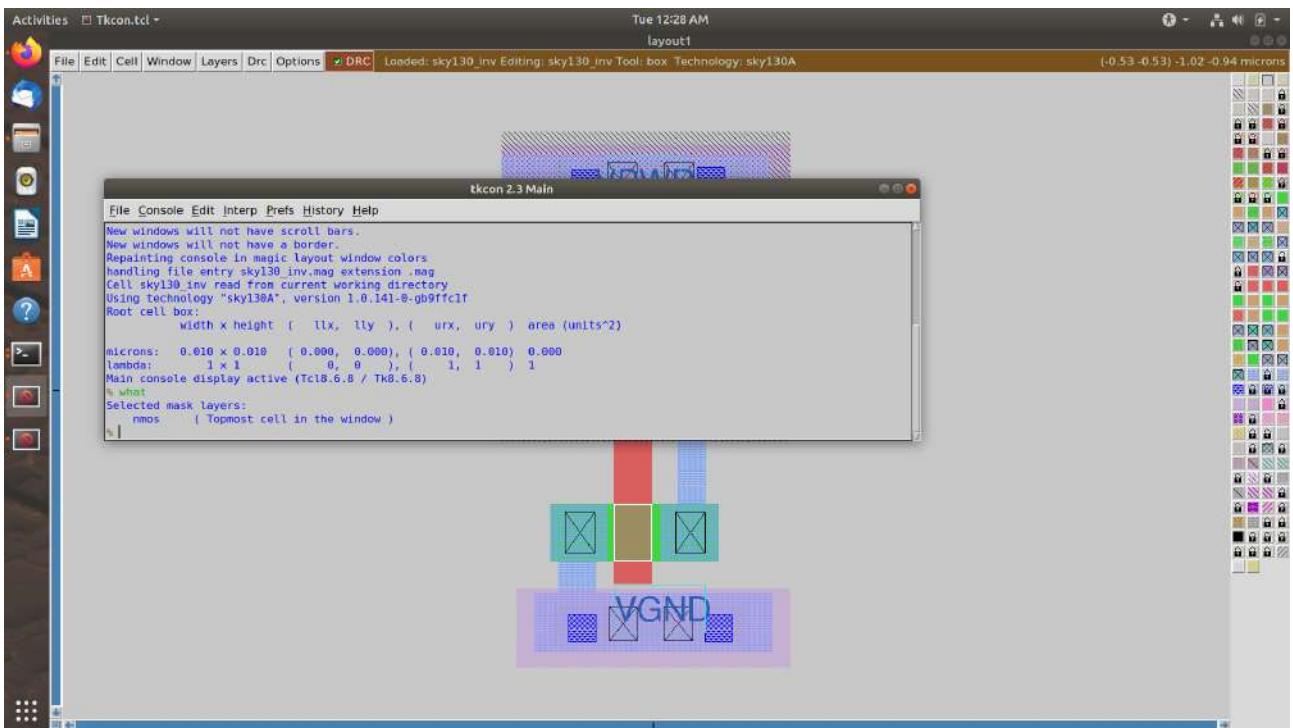
```
Activities Terminal - Tue 12:22 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ git clone https://github.com/nickson-jose/vsdstdcelldesign
Cloning into 'vsdstdcelldesign'...
remote: Enumerating objects: 492, done.
remote: Counting objects: 100% (18/18), done.
remote: Compressing objects: 100% (18/18), done.
remote: Total 492 (delta 7), reused 0 (delta 0), pack-reused 474
Receiving objects: 100% (492/492), 24.08 MiB | 480.00 KiB/s, done.
Resolving deltas: 100% (210/210), done.
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd vsdstdcelldesign
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cp /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/magic/sky130A.tech .
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls
extras Images libs LICENSE README.md sky130A.tech sky130_inv.mag
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ magic -T sky130A.tech sky130_inv.mag &
[1] 4495
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```

2. Load the custom inverter layout in magic and explore.

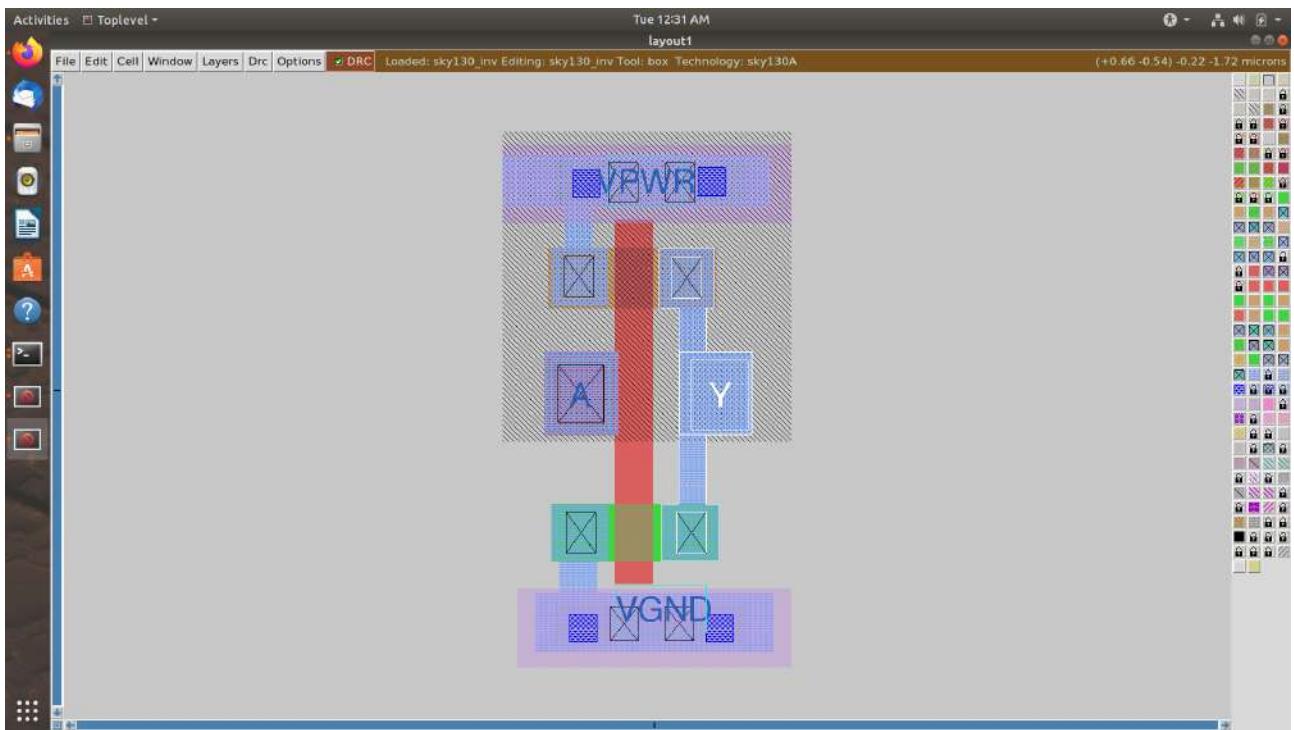
Screenshot of custom inverter layout in magic



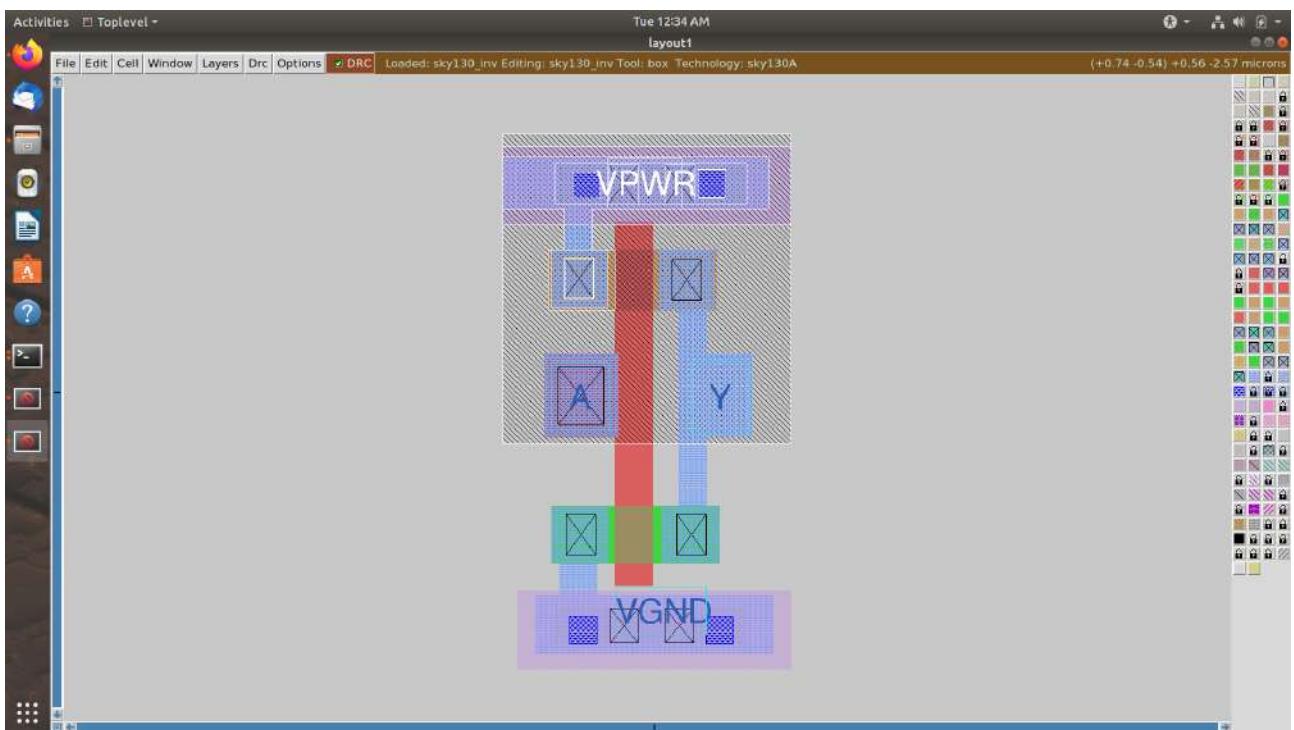
NMOS and PMOS identified



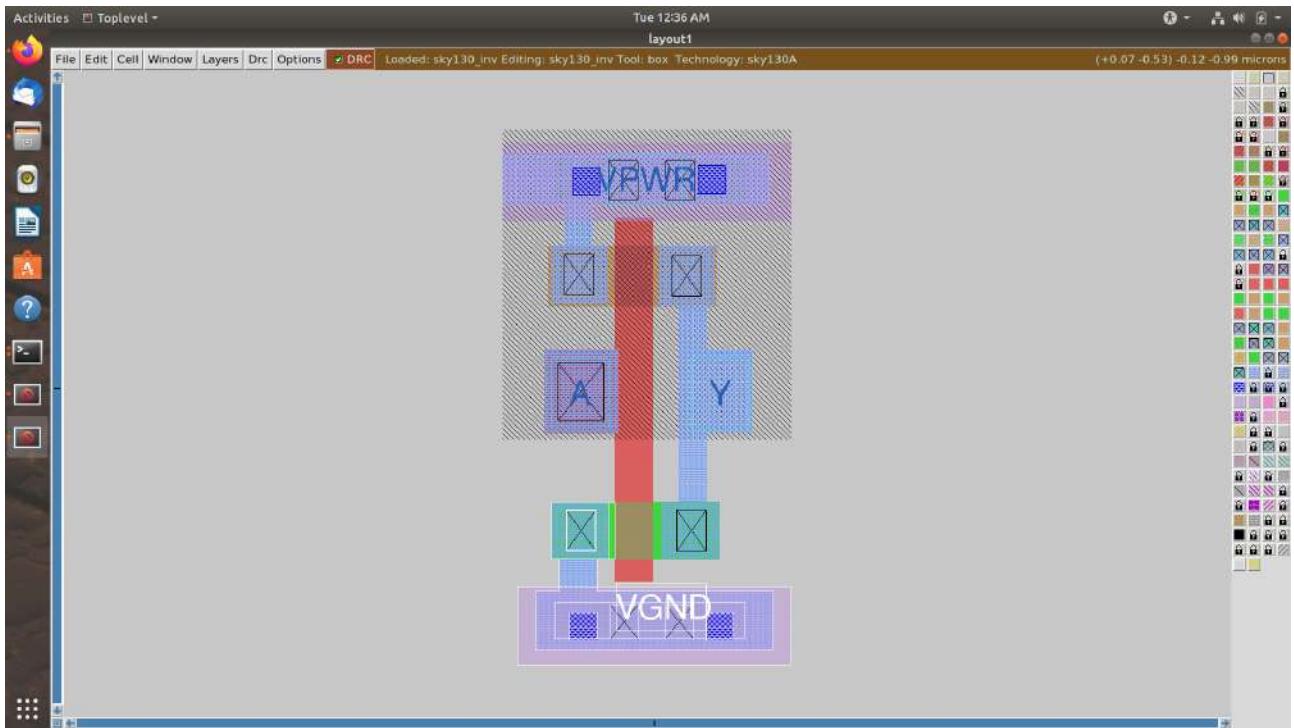
Output Y connectivity to PMOS and NMOS drain verified



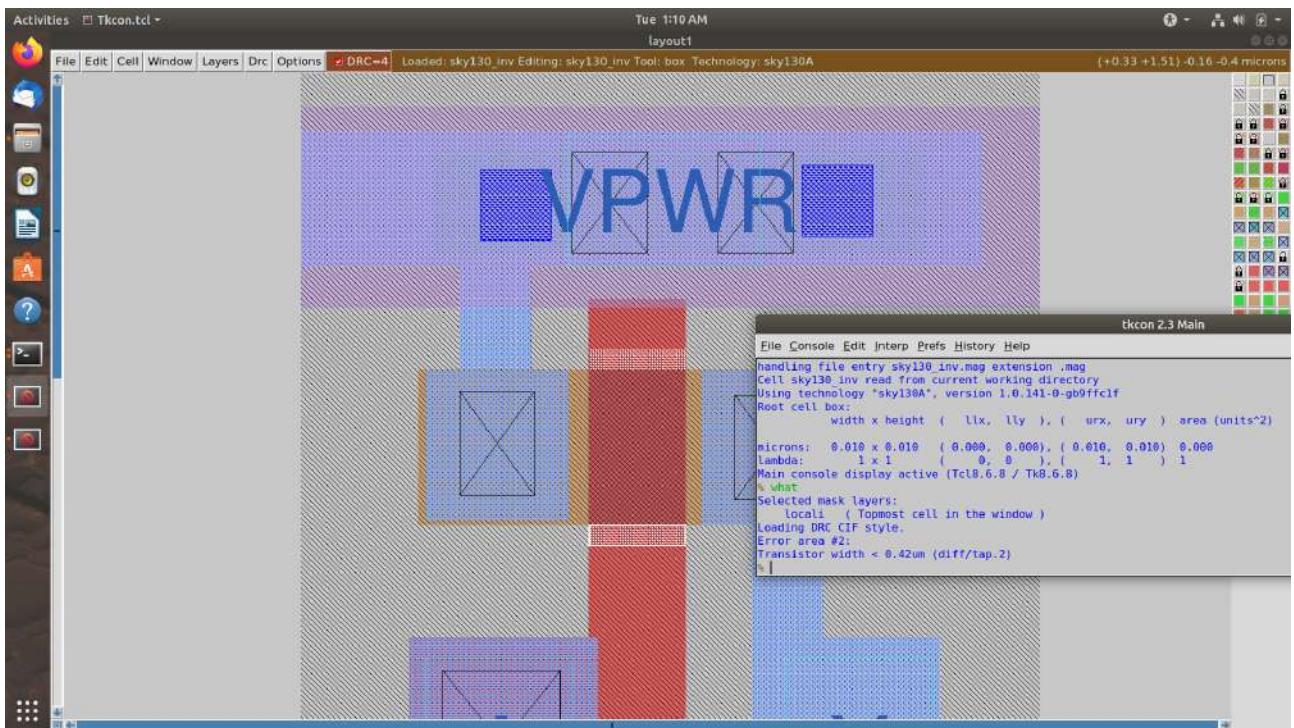
PMOS source connectivity to VDD (here VPWR) verified



NMOS source connectivity to VSS (here VGND) verified



Deleting necessary layout part to see DRC error



3. Spice extraction of inverter in magic.

Commands for spice extraction of the custom inverter layout to be used in tkcon window of magic

```
# Check current directory
```

pwd

```
# Extraction command to extract to .ext format
```

extract all

Before converting ext to spice this command enable the parasitic extraction also

`ext2splice cthresh 0 rthresh 0`

Converting to ext to spice

ext2spice

Screenshot of tkcon window after running above commands

```
Activities □ Tkcon.tcl - Tue 1:24 AM
tkcon 2.3 Main

File Console Edit Interp Prefs History Help
Loading history file ... 16 events added
Use openwrapper to create a new GUI-based layout window
Use closerwrapper to remove a new GUI-based layout window

Magic 8.3 revision 400 - Compiled on Mon May 22 20:58:24 IST 2023.
Starting magic under Tcl Interpreter
Using Tk console window
Using TrueColor, VisualID 0x21 depth 24
Input style sky130(): scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
    nmosc obsactive mvbsactive obsl11 obsm1 obsm2 obsm3 obsm4 obsm5 obsmndl ubm fillblock comment obscomment res0p35 res0p69 reslp41 res2p85 res5p73
Processing system .magicrc file
New windows will not have a title caption.
New windows will not have scroll bars.
New windows will not have a border.
Repainting console in magic layout window colors
handling file entry sky130_inv.mag extension .mag
Cell sky130_inv read from current working directory
Using technology "sky130A", version 1.0.141-0-gb9ffcf
Root cell box:
    width x height ( llx, lly ),( urx, ury ) area (units^2)
microns:  0.010 x 0.010  ( 0.000, 0.000), ( 0.010, 0.010) 0.000
lambda:   1 x 1  ( 0, 0 ), ( 1, 1 ) 1
Main console display active (Tcl8.6.8 / Tk8.6.8)
> .pmf
> /home/vsdsuser/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
> extract all
Extracting sky130_inv into sky130_inv.ext:
% ext2spice cthresh 0 rthresh 0
% ext2spice
ext2spice finished.
%
```

Screenshot of created spice file

Activities GVim -

Tue 11:27 AM
sky130_inv.spice (~/Desktop/work/tools/op...ing_dir/openlane/vsdstdcelldesign) - GVIM

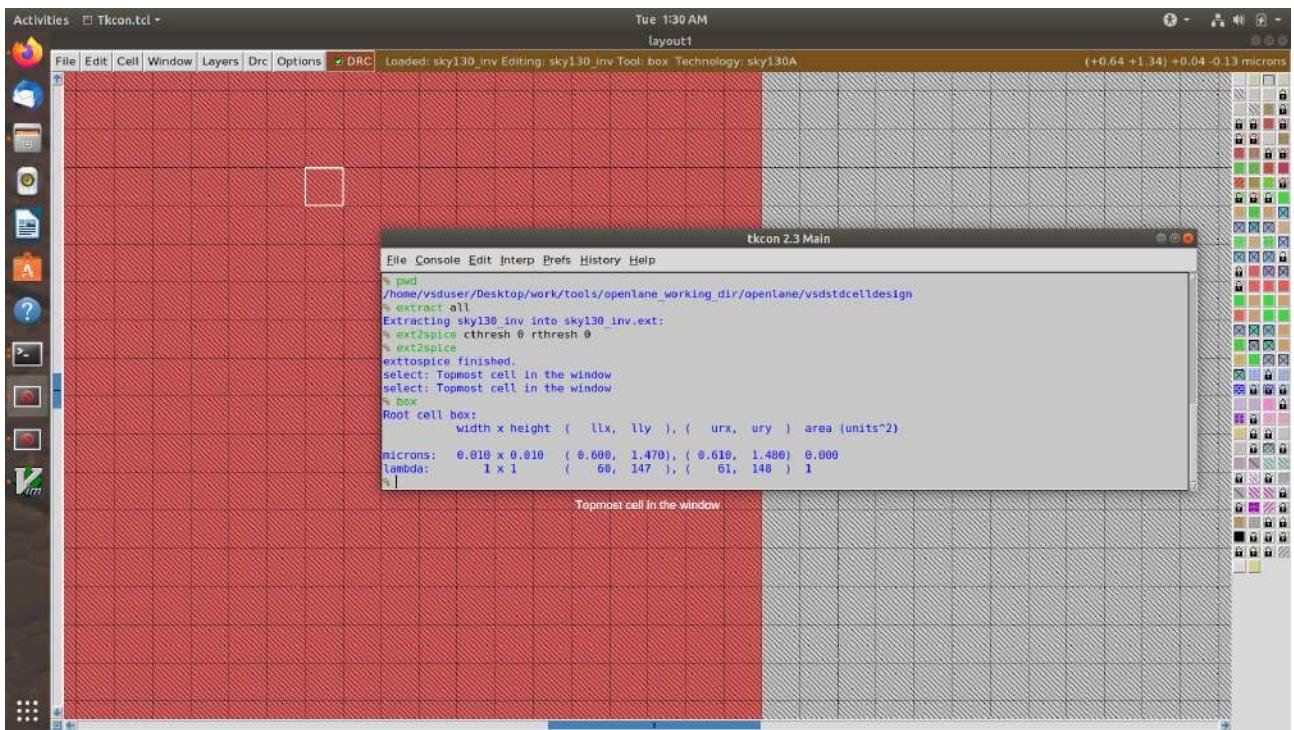
File Edit Tools Syntax Buffers Window Help

1 * SPICE3 file created from sky130_inv.ext - technology: sky130A
2
3 .option scale=10m
4
5 .subckt sky130_inv A Y VPWR VGND
6 X0 Y A VGND VGND sky130_fd_pr_nfet_01v8 ad=1.44n pd=0.152m as=1.37n ps=0.148m w=35 l=23
7 X1 Y A VPWR VPWR sky130_fd_pr_pfet_01v8 ad=1.44n pd=0.152m as=1.52n ps=0.156m w=37 l=23
8 C0 A VPWR 0.0774f
9 C1 Y VPWR 0.117f
10 C2 A Y 0.0754f
11 C3 Y VGND 0.279f
12 C4 A VGND 0.45f
13 C5 VPWR VGND 0.781f
14 .ends

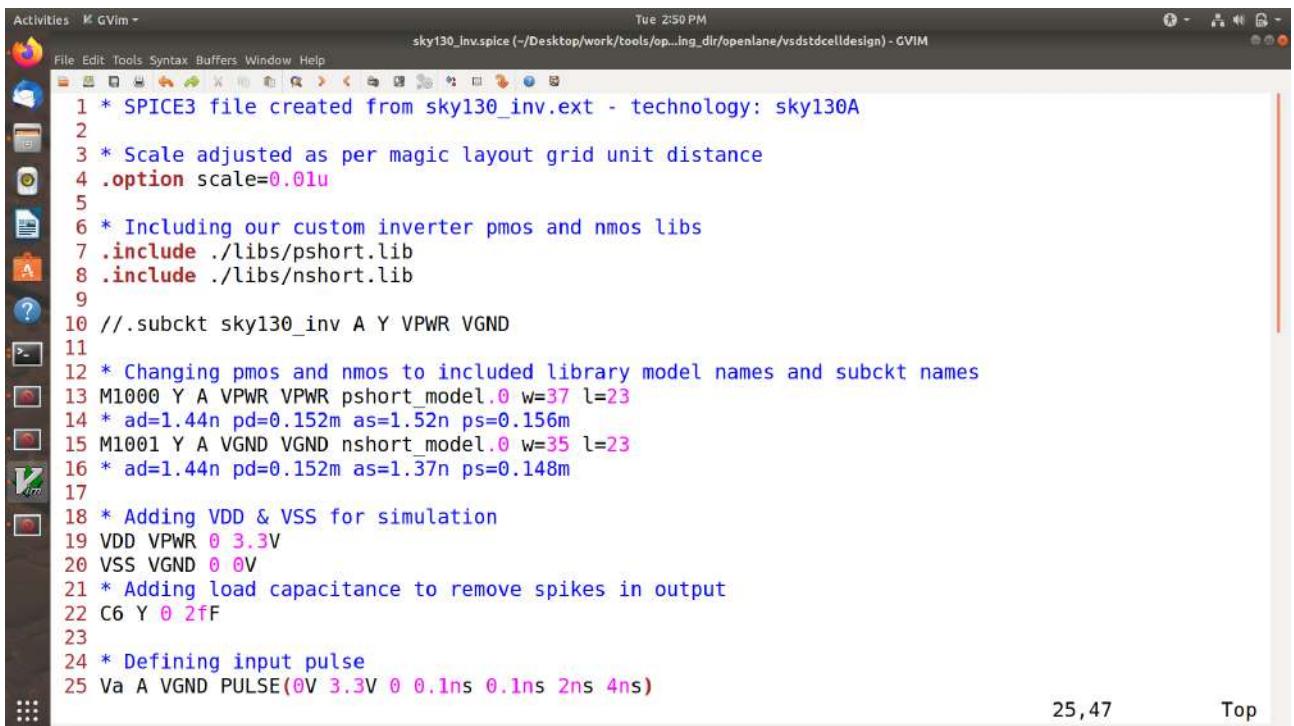
"sky130_inv.spice" 14L, 404C 1,1 All

4. Editing the spice model file for analysis through simulation.

Measuring unit distance in layout grid

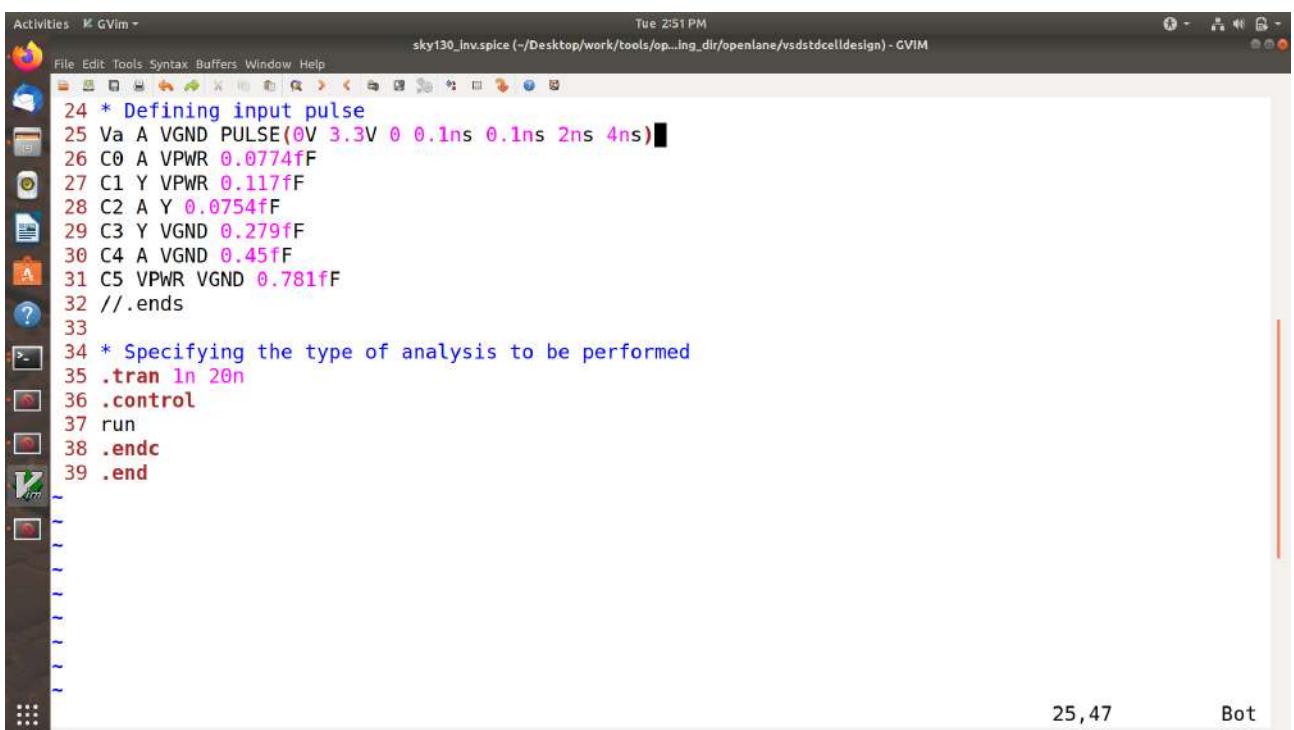


Final edited spice file ready for ngspice simulation



```
Activities  M GVim - Tue 2:50 PM
sky130_inv.spice (~/Desktop/work/tools/op...ing_dir/openlane/vsdstdcelldesign) - GVIM
File Edit Tools Syntax Buffers Window Help
1 * SPICE3 file created from sky130_inv.ext - technology: sky130A
2
3 * Scale adjusted as per magic layout grid unit distance
4 .option scale=0.01u
5
6 * Including our custom inverter pmos and nmos libs
7 .include ./libs/pshort.lib
8 .include ./libs/nshort.lib
9
10 // .subckt sky130_inv A Y VPWR VGND
11
12 * Changing pmos and nmos to included library model names and subckt names
13 M1000 Y A VPWR VPWR pshort_model.0 w=37 l=23
14 * ad=1.44n pd=0.152m as=1.52n ps=0.156m
15 M1001 Y A VGND VGND nshort_model.0 w=35 l=23
16 * ad=1.44n pd=0.152m as=1.37n ps=0.148m
17
18 * Adding VDD & VSS for simulation
19 VDD VPWR 0 3.3V
20 VSS VGND 0 0V
21 * Adding load capacitance to remove spikes in output
22 C6 Y 0 2fF
23
24 * Defining input pulse
25 Va A VGND PULSE(0V 3.3V 0 0.1ns 0.1ns 2ns 4ns)
26
27
28
29
30
31
32 // .ends
33
34 * Specifying the type of analysis to be performed
35 .tran 1n 20n
36 .control
37 run
38 .endc
39 .end
```

25,47 Top



```
Activities  M GVim - Tue 2:51 PM
sky130_inv.spice (~/Desktop/work/tools/op...ing_dir/openlane/vsdstdcelldesign) - GVIM
File Edit Tools Syntax Buffers Window Help
24 * Defining input pulse
25 Va A VGND PULSE(0V 3.3V 0 0.1ns 0.1ns 2ns 4ns)■
26 C0 A VPWR 0.0774fF
27 C1 Y VPWR 0.117fF
28 C2 A Y 0.0754fF
29 C3 Y VGND 0.279fF
30 C4 A VGND 0.45fF
31 C5 VPWR VGND 0.781fF
32 // .ends
33
34 * Specifying the type of analysis to be performed
35 .tran 1n 20n
36 .control
37 run
38 .endc
39 .end
```

25,47 Bot

5. Post-layout ngspice simulations.

Commands for ngspice simulation

Command to directly load spice file for simulation to ngspice

ngspice sky130_inv.spice

```
# Now that we have entered ngspice with the simulation spice file loaded we just have to  
load the plot
```

```
plot y vs time a
```

Screenshots of ngspice run

```

Activities Terminal - vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ngspice sky130_inv.spice
*****
** ngspice-27 : Circuit level simulation program
** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California.
** Please get your ngspice manual from http://ngspice.sourceforge.net/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Tue Dec 26 17:10:20 UTC 2017
*****
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node Voltage
-----
y 3.3
a 0
vpwr 3.3
vgnd 0
va#branch 0

```

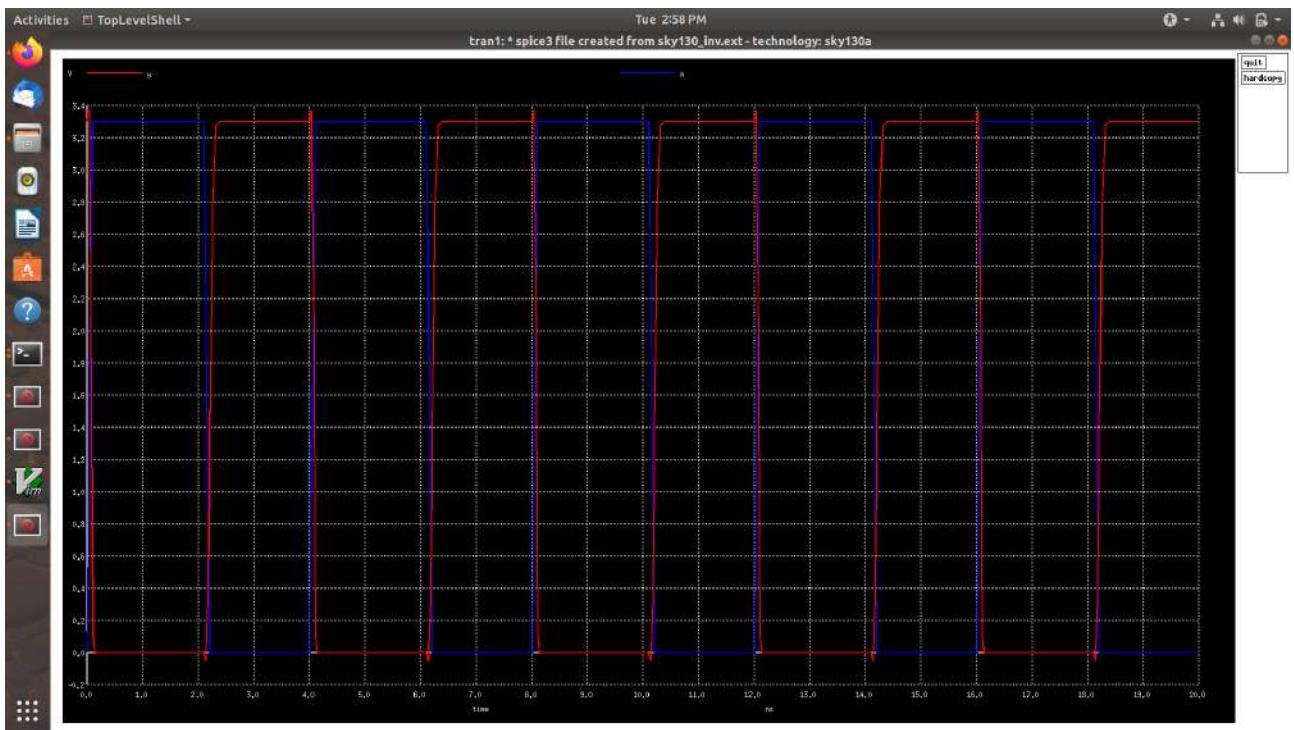
```

Activities TopLevelShell - vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ 
*****
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node Voltage
-----
y 3.3
a 0
vpwr 3.3
vgnd 0
va#branch 0
vss#branch 3.32351e-12
vdd#branch -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
::: ngspice 1 -> 

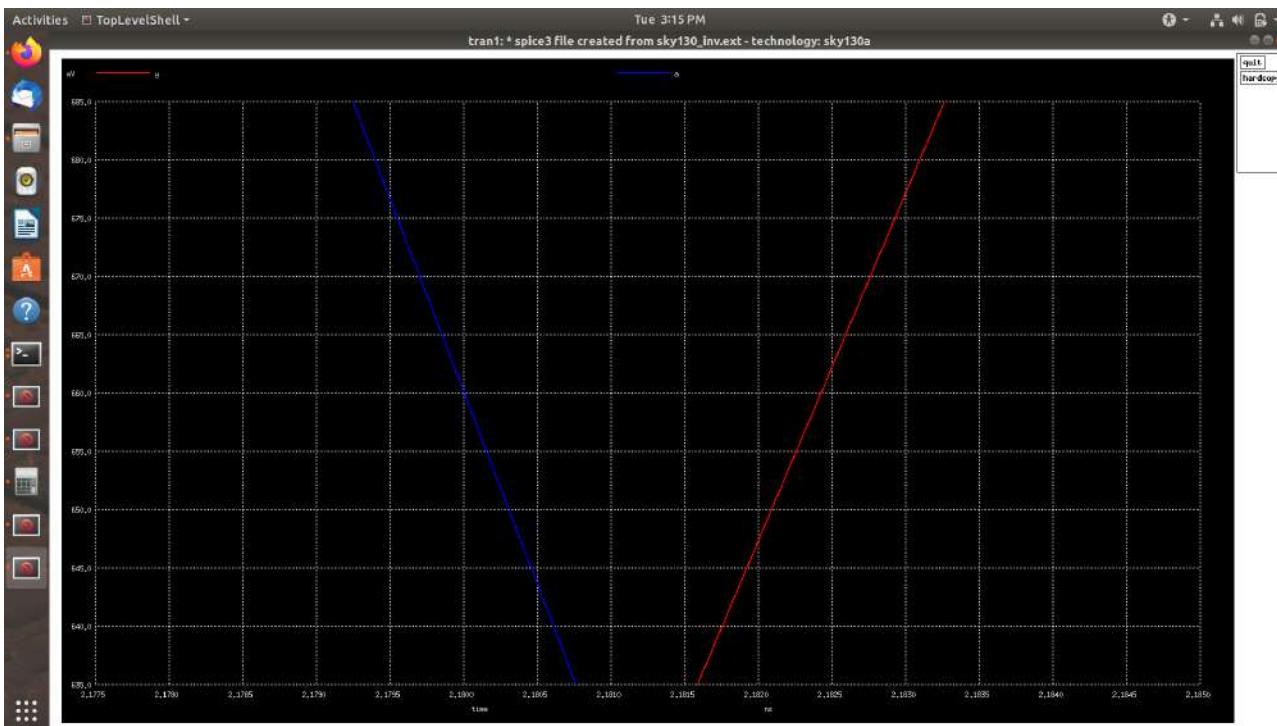
```

Screenshot of generated plot



Rise transition time calculation

20% Screenshots



Activities Terminal -

Tue 3:20 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign

```

File Edit View Search Terminal Help
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a

Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

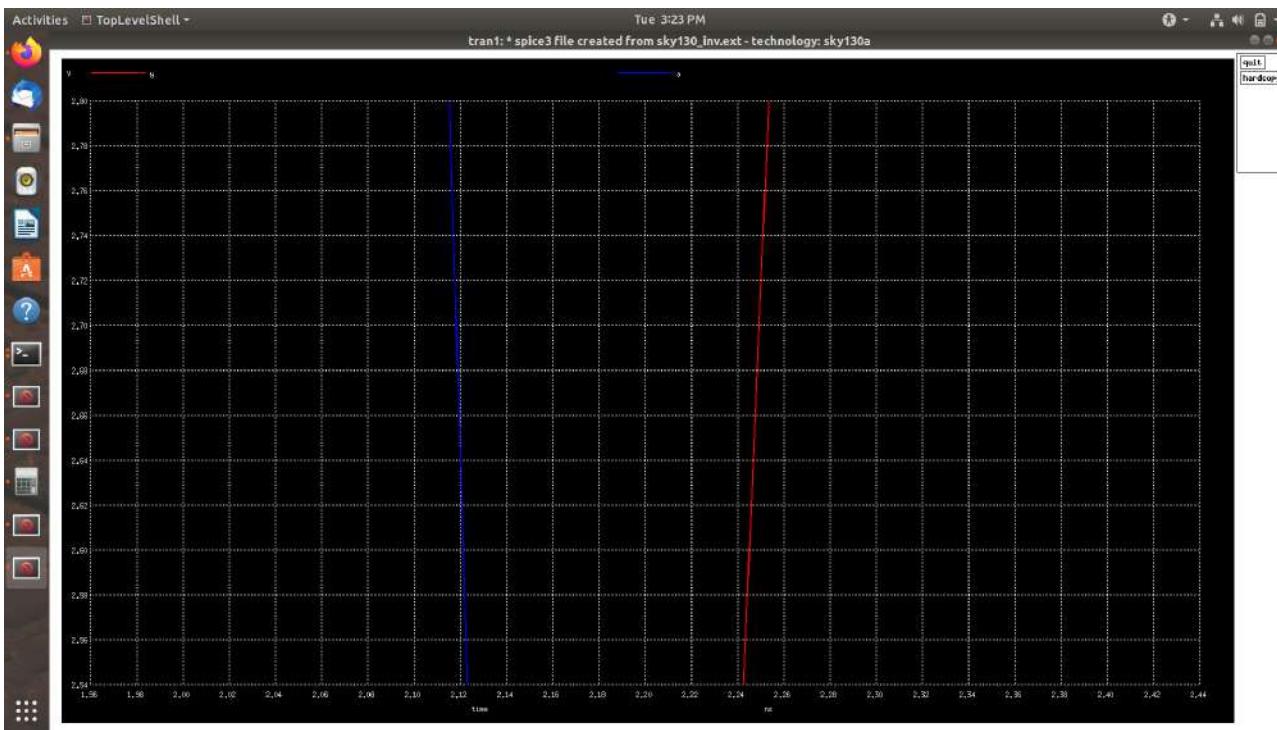
Warning: va: no DC value, transient time 0 value used

Initial Transient Solution
-----
Node          Voltage
---- 
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043

```

80% Screenshots



Activities Terminal -

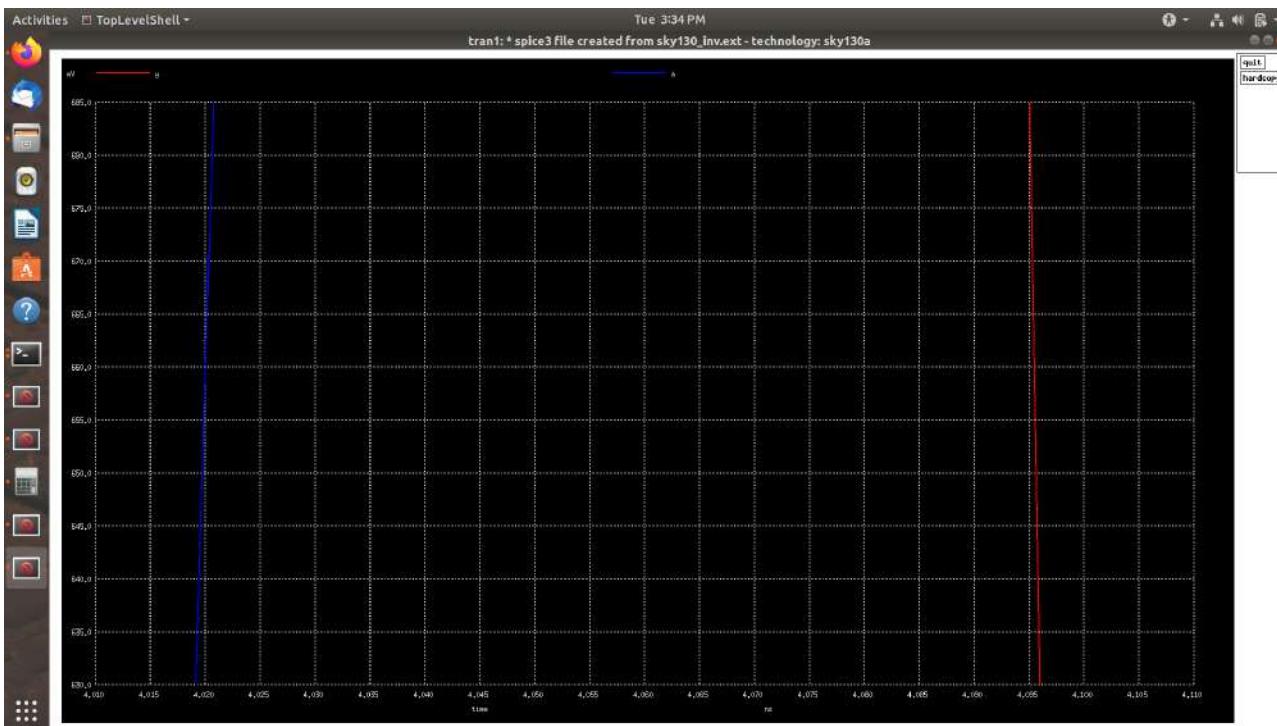
Tue 3:24 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```
File Edit View Search Terminal Help
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node          Voltage
-----
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
```

Fall transition time calculation

20% Screenshots



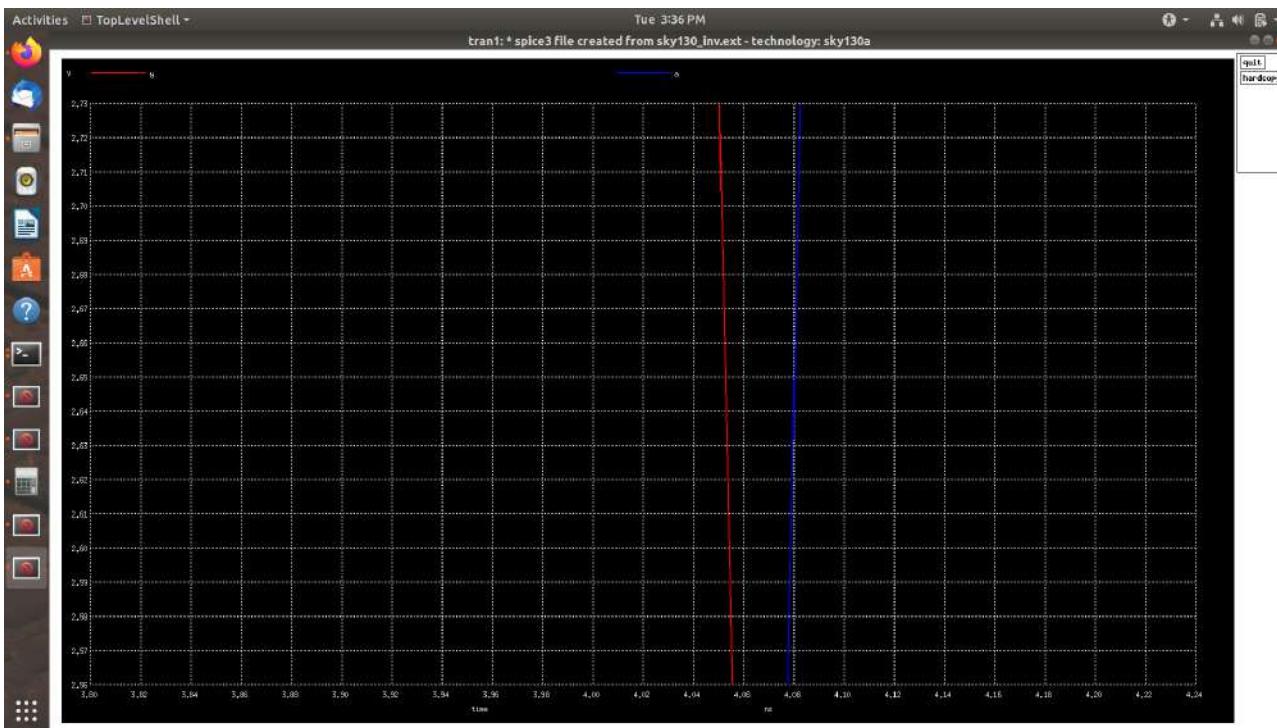
Activities Terminal -

Tue 3:34 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node          Voltage
-----
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
x0 = 4.09555e-09, y0 = 0.660127
```

80% Screenshots



Activities Terminal -

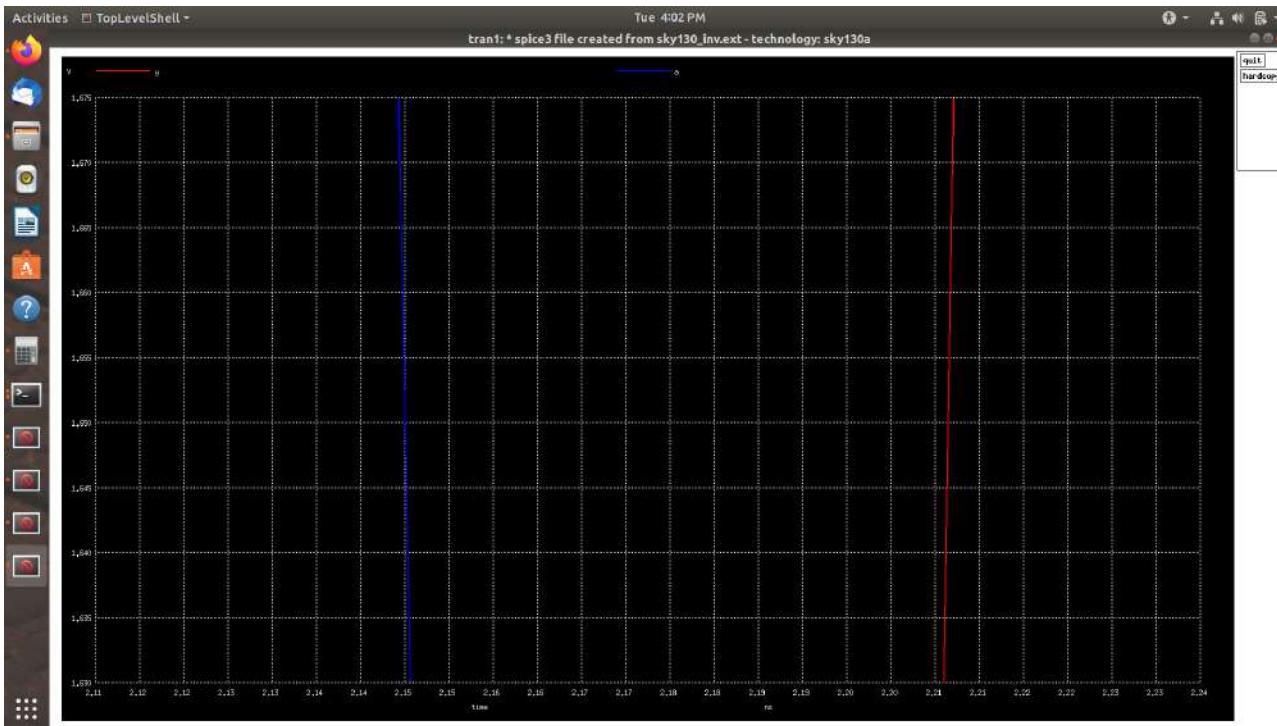
Tue 3:36 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign

```
Initial Transient Solution
-----
Node          Voltage
-----
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
x0 = 4.09555e-09, y0 = 0.660127
x0 = 4.0536e-09, y0 = 2.64
```

Rise Cell Delay Calculation

50% Screenshots



Activities Terminal

Tue 4:03 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign

```

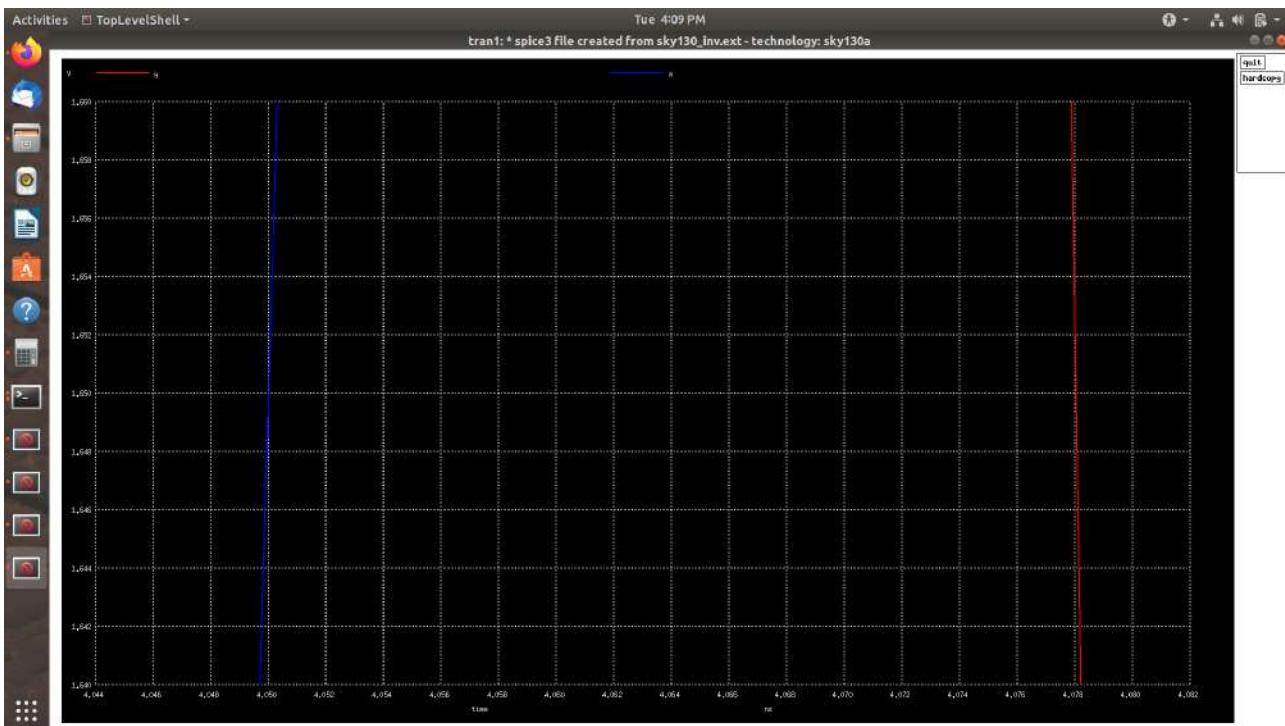
File Edit View Search Terminal Help
Node          Voltage
-----
y             3.3
a             0
vpwr          3.3
vgnd          0
va#branch     0
vss#branch    3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
x0 = 4.09555e-09, y0 = 0.660127
x0 = 4.0536e-09, y0 = 2.64
x0 = 2.21144e-09, y0 = 1.65
x0 = 2.15008e-09, y0 = 1.6501

```

Fall Cell Delay Calculation

50% Screenshots



Activities Terminal Tue 4:10 PM

vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```

File Edit View Search Terminal Help
vpwr          3.3
vgnd          0
va#branch     0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
> x0 = 2.24638e-09, y0 = 2.6403
> x0 = 4.09555e-09, y0 = 0.660127
> x0 = 4.0536e-09, y0 = 2.64
> x0 = 2.21144e-09, y0 = 1.65
> x0 = 2.15008e-09, y0 = 1.6501
> x0 = 4.07807e-09, y0 = 1.65005
> x0 = 4.05e-09, y0 = 1.65002

```

6. Find problem in the DRC section of the old magic tech file for the skywater process and fix them.

Link to Sky130 Periphery rules: <https://skywater-pdk.readthedocs.io/en/main/rules/periphery.html>

Commands to download and view the corrupted skywater process magic tech file and associated files to perform drc corrections

```
# Change to home directory
```

```
cd
```

```
# Command to download the lab files
```

```
wget http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
```

```
# Since lab file is compressed command to extract it
```

```
tar xfz drc_tests.tgz
```

```
# Change directory into the lab folder
```

```
cd drc_tests
```

```
# List all files and directories present in the current directory
```

```
ls -al
```

```
# Command to view .magicrc file
```

```
gvim .magicrc
```

```
# Command to open magic tool in better graphics
```

```
magic -d XR &
```

Screenshots of commands run

Activities Terminal Thu 10:33 PM
vsduser@vsdsquadron:~/drc_tests

```
File Edit View Search Terminal Help
vsduser@vsdsquadron:~$ cd
vsduser@vsdsquadron:~$ wget http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
--2024-03-21 22:31:14-- http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
Resolving opencircuitdesign.com (opencircuitdesign.com)... 69.251.37.208
Connecting to opencircuitdesign.com (opencircuitdesign.com)|69.251.37.208|:80... connected.
HTTP request sent, awaiting response... 200 OK
Length: 41651 (41K) [application/x-gzip]
Saving to: 'drc_tests.tgz'

drc_tests.tgz          100%[=====] 40.67K 160KB/s in 0.3s

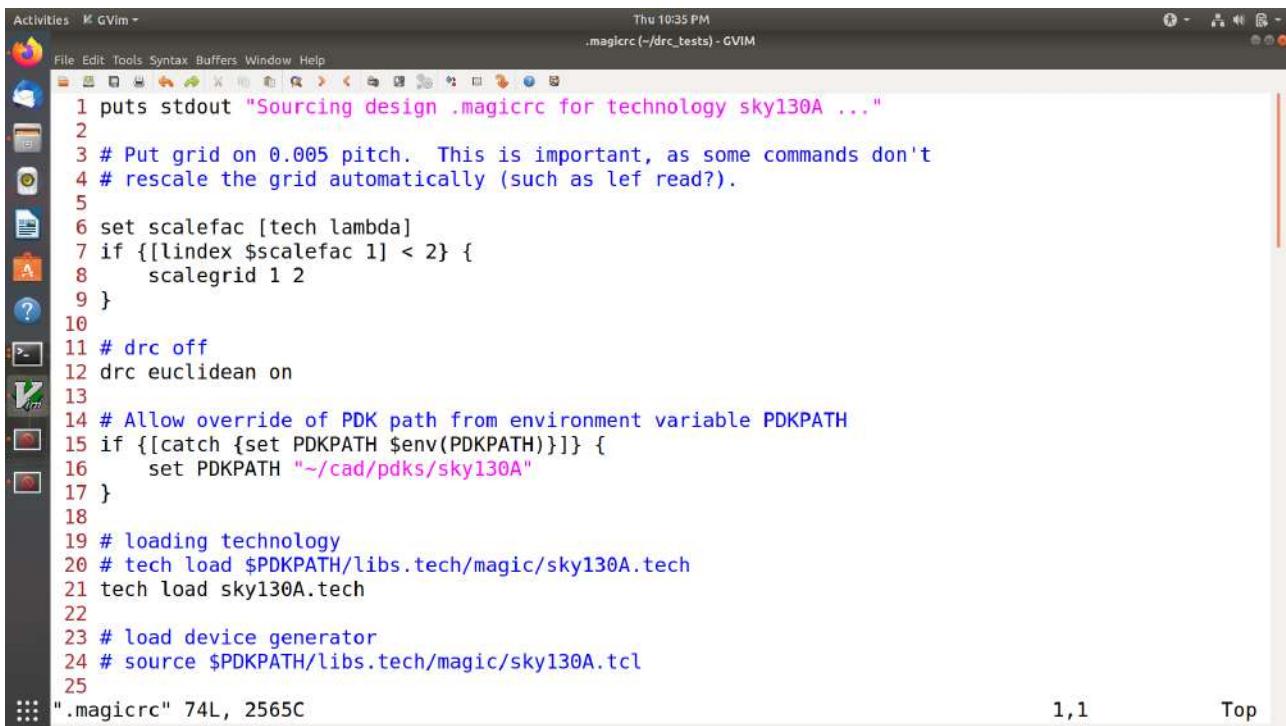
2024-03-21 22:31:15 (160 KB/s) - 'drc_tests.tgz' saved [41651/41651]

vsduser@vsdsquadron:~$ tar xfz drc_tests.tgz
vsduser@vsdsquadron:~$ cd drc_tests
vsduser@vsdsquadron:~/drc_tests$ ls -al
total 276
drwxrwxr-x 2 vsduser vsduser 4096 Sep 16 2020 .
drwxr-xr-x 22 vsduser vsduser 4096 Mar 21 22:31 ..
-rw-rw-r-- 1 vsduser vsduser 3178 Sep 15 2020 capm.mag
-rw-rw-r-- 1 vsduser vsduser 3610 Sep 16 2020 difftap.mag
-rw-rw-r-- 1 vsduser vsduser 1535 Sep 16 2020 dnwell.mag
-rw-rw-r-- 1 vsduser vsduser 1684 Sep 15 2020 hvtp.mag
-rw-rw-r-- 1 vsduser vsduser 897 Sep 15 2020 hvtr.mag
-rw-rw-r-- 1 vsduser vsduser 11586 Sep 15 2020 licon.mag
-rw-rw-r-- 1 vsduser vsduser 1480 Sep 15 2020 li.mag
-rw-rw-r-- 1 vsduser vsduser 4648 Sep 15 2020 lvtn.mag
-rw-rw-r-- 1 vsduser vsduser 2565 Sep 15 2020 .magicrc
```

Activities Terminal Thu 10:34 PM
vsduser@vsdsquadron:~/drc_tests

```
File Edit View Search Terminal Help
-rw-rw-r-- 1 vsduser vsduser 11586 Sep 15 2020 licon.mag
-rw-rw-r-- 1 vsduser vsduser 1480 Sep 15 2020 li.mag
-rw-rw-r-- 1 vsduser vsduser 4648 Sep 15 2020 lvtn.mag
-rw-rw-r-- 1 vsduser vsduser 2565 Sep 15 2020 .magicrc
-rw-rw-r-- 1 vsduser vsduser 1198 Sep 15 2020 mcon.mag
-rw-rw-r-- 1 vsduser vsduser 2103 Sep 15 2020 met1.mag
-rw-rw-r-- 1 vsduser vsduser 1799 Sep 15 2020 met2.mag
-rw-rw-r-- 1 vsduser vsduser 1500 Sep 16 2020 met3.mag
-rw-rw-r-- 1 vsduser vsduser 1114 Sep 16 2020 met4.mag
-rw-rw-r-- 1 vsduser vsduser 757 Sep 15 2020 met5.mag
-rw-rw-r-- 1 vsduser vsduser 1948 Sep 15 2020 npc.mag
-rw-rw-r-- 1 vsduser vsduser 2497 Sep 15 2020 nsd.mag
-rw-rw-r-- 1 vsduser vsduser 1351 Sep 16 2020 nwell.mag
-rw-rw-r-- 1 vsduser vsduser 536 Sep 15 2020 pad.mag
-rw-rw-r-- 1 vsduser vsduser 5588 Sep 16 2020 poly.mag
-rw-rw-r-- 1 vsduser vsduser 2565 Sep 15 2020 psd.mag
-rw-rw-r-- 1 vsduser vsduser 3025 Sep 15 2020 rpm.mag
-rw-rw-r-- 1 vsduser vsduser 135962 Sep 16 2020 sky130A.tech
-rw-rw-r-- 1 vsduser vsduser 2476 Sep 16 2020 tunm.mag
-rw-rw-r-- 1 vsduser vsduser 4114 Sep 16 2020 varac.mag
-rw-rw-r-- 1 vsduser vsduser 1271 Sep 15 2020 via2.mag
-rw-rw-r-- 1 vsduser vsduser 1267 Sep 15 2020 via3.mag
-rw-rw-r-- 1 vsduser vsduser 966 Sep 15 2020 via4.mag
-rw-rw-r-- 1 vsduser vsduser 955 Sep 15 2020 via.mag
vsduser@vsdsquadron:~/drc_tests$ gvim .magicrc
vsduser@vsdsquadron:~/drc_tests$ magic -d XR
```

Screenshot of .magicrc file



```

Thu 10:35 PM
.magicrc (~/.drc_tests) - GVIM

File Edit Tools Syntax Buffers Window Help
1 puts stdout "Sourcing design .magicrc for technology sky130A ..."
2
3 # Put grid on 0.005 pitch. This is important, as some commands don't
4 # rescale the grid automatically (such as lef read?).
5
6 set scalefac [tech lambda]
7 if {[lindex $scalefac 1] < 2} {
8     scalegrid 1 2
9 }
10
11 # drc off
12 drc euclidean on
13
14 # Allow override of PDK path from environment variable PDKPATH
15 if {[catch {set PDKPATH $env(PDKPATH)}]} {
16     set PDKPATH "~/cad/pdk/sky130A"
17 }
18
19 # loading technology
20 # tech load $PDKPATH/libs.tech/magic/sky130A.tech
21 tech load sky130A.tech
22
23 # load device generator
24 # source $PDKPATH/libs.tech/magic/sky130A.tcl
25

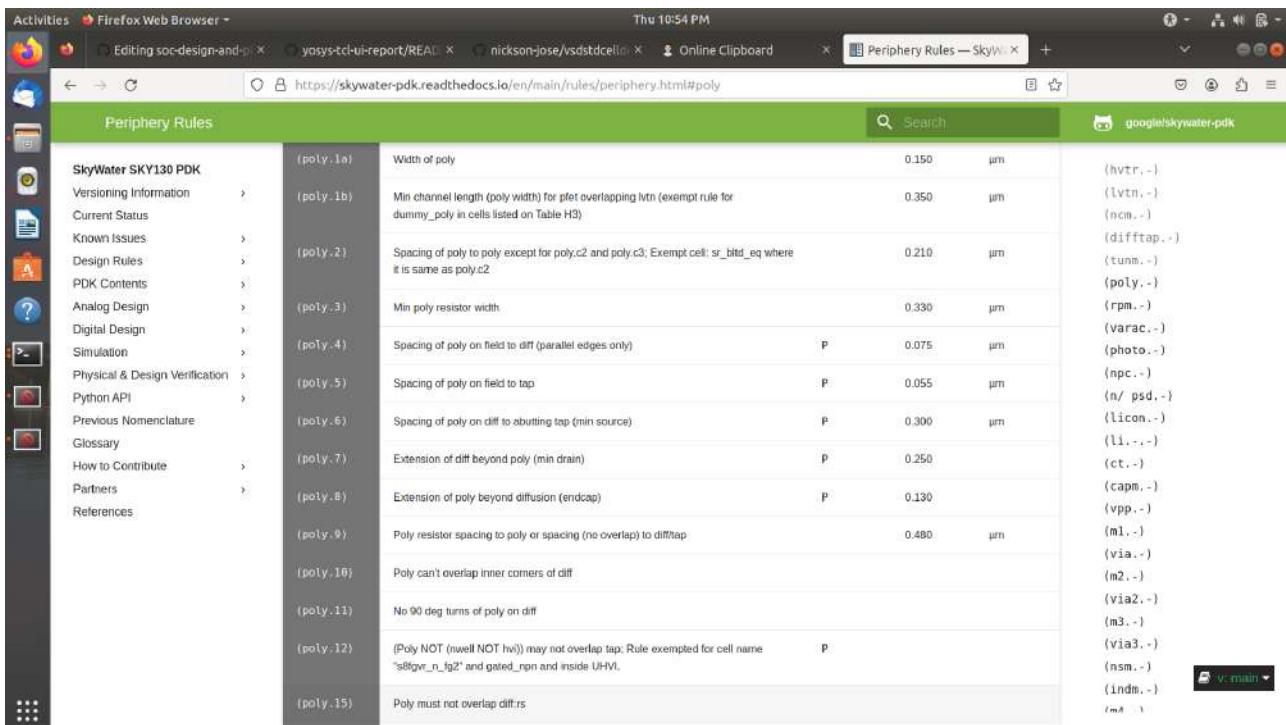
".magicrc" 74L, 2565C

```

1,1 Top

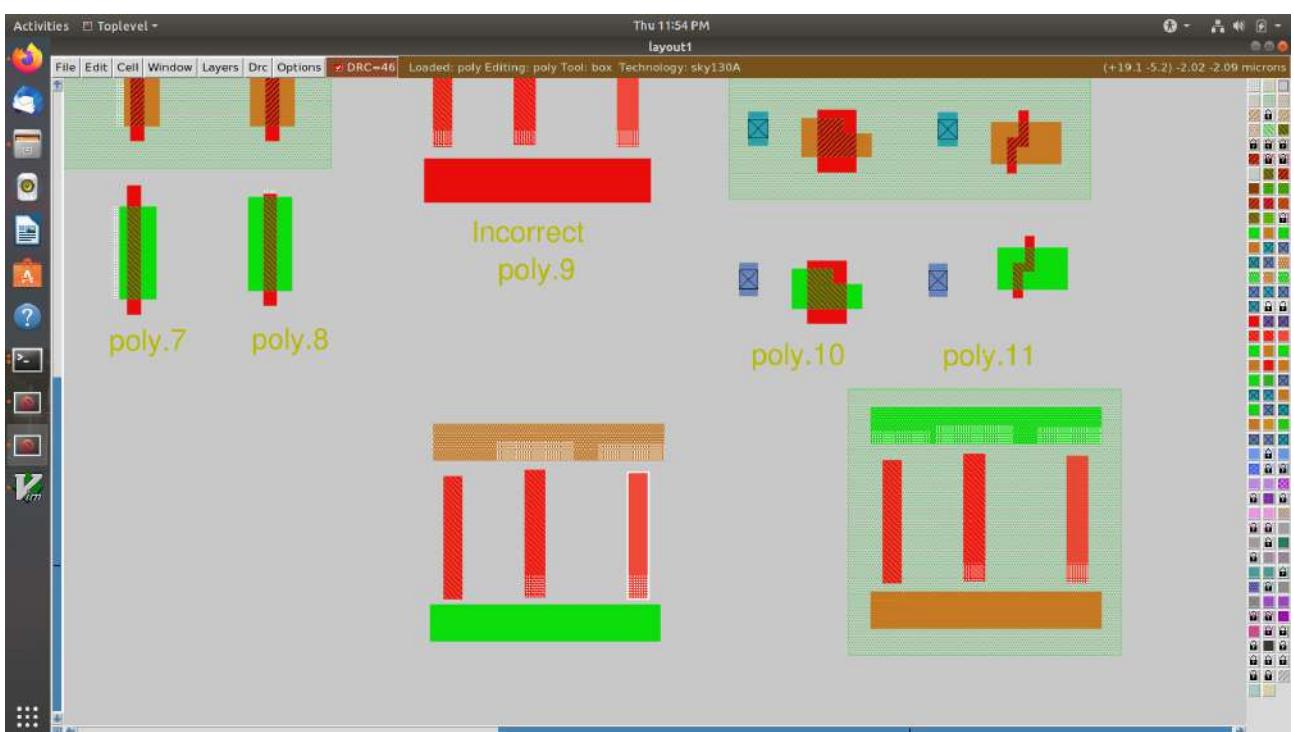
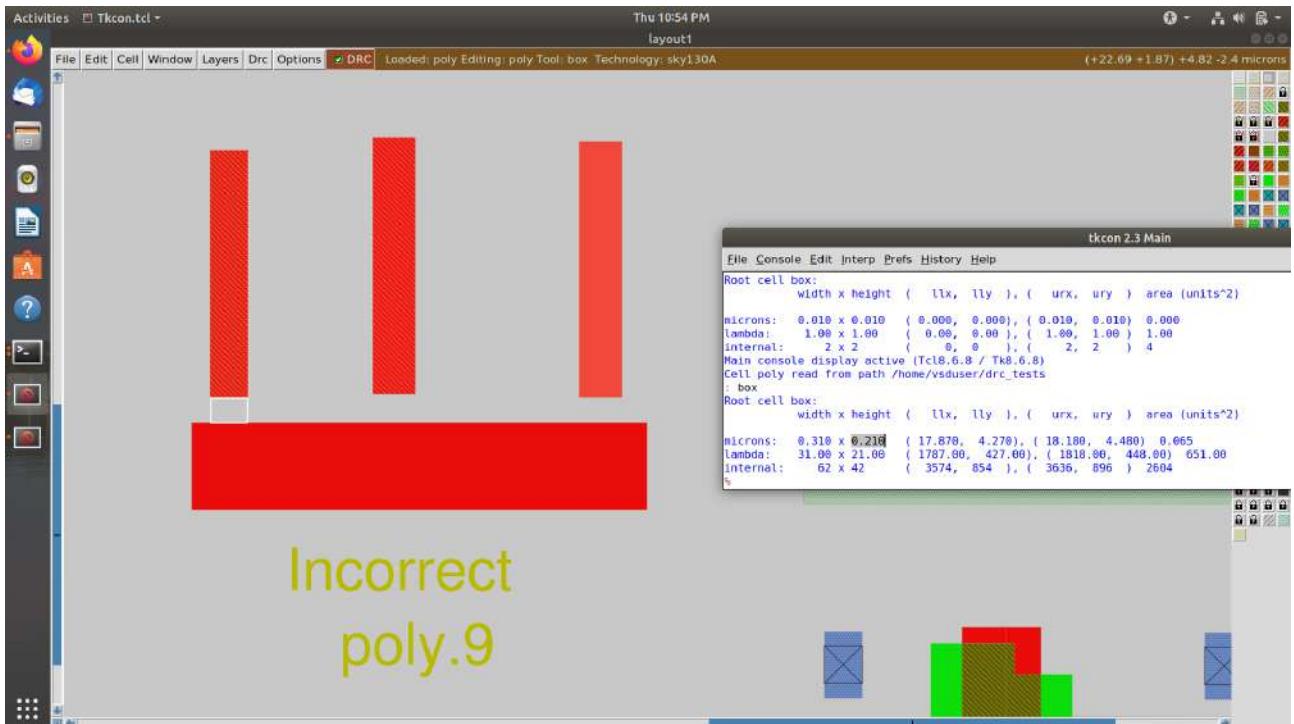
Incorrectly implemented poly.9 simple rule correction

Screenshot of poly rules



			Search	
SkyWater SKY130 PDK	(poly.1a)	Width of poly	0.150	μm
Versioning Information	(poly.1b)	Min channel length (poly width) for peft overlapping lvtn (exempt rule for dummy_poly in cells listed on Table H3)	0.350	μm
Current Status	(poly.2)	Spacing of poly to poly except for poly.c2 and poly.c3. Exempt cell: sr_bld_eq where it is same as poly.c2	0.210	μm
Known Issues	(poly.3)	Min poly resistor width	0.330	μm
Design Rules	(poly.4)	Spacing of poly on field to diff (parallel edges only)	P	0.075
PDK Contents	(poly.5)	Spacing of poly on field to tap	P	0.055
Analog Design	(poly.6)	Spacing of poly on diff to abutting tap (min source)	P	0.300
Digital Design	(poly.7)	Extension of diff beyond poly (min drain)	P	0.250
Simulation	(poly.8)	Extension of poly beyond diffusion (endcap)	P	0.130
Physical & Design Verification	(poly.9)	Poly resistor spacing to poly or spacing (no overlap) to diff/tap		0.480
Python API	(poly.10)	Poly can't overlap inner corners of diff		
Previous Nomenclature	(poly.11)	No 90 deg turns of poly on diff		
Glossary	(poly.12)	(Poly NOT (inwell NOT hv)) may not overlap tap: Rule exempted for cell name "g8tge_n_fq2" and gated_rgn and inside UHVL.	P	
How to Contribute	(poly.13)	Poly must not overlap diff/rs		
Partners	(poly.14)			
References	(poly.15)			

Incorrectly implemented poly.9 rule no drc violation even though spacing < 0.48μ



New commands inserted in sky130A.tech file to update drc

Activities M GVim Thu 11:58 PM
sky130A.tech (~/.drc_tests) - GVIM

```

4803
4804 variants *
4805
4806 #-----
4807 # POLY
4808 #-----
4809
4810 width allpoly 150 "poly.width < %d (poly.1a)"
4811 spacing allpoly allpoly 210 touching_ok "poly.spacing < %d (poly.2)"
4812 spacing allpolynonfet alldiffvnonfet 75 corner_ok allfets \
    "poly.spacing to Diffusion < %d (poly.4a)"
4813 spacing npres alldiff 480 touching_illegal \
    "poly.resistor spacing to alldiff < %d (poly.9)"
4814 spacing npres allpolynonres 480 touching_illegal \
    "poly.resistor spacing to allpolynonres < %d (poly.9)"
4815 overhang *ndiff,rndiff nfet,scnfet,npd,npass 250 "N-Diffusion overhang of nmos < %d (poly.7)"
4816 overhang *mvndiff,mvrndiff mvnfet,mvnnfet 250 \
    "N-Diffusion overhang of nmos < %d (poly.7)"
4817 overhang *pdifff,rdifff pfet,scpfet,ppu 250 "P-Diffusion overhang of pmos < %d (poly.7)"
4818 overhang *mvpdiff,mvrpdifff mvpfet 250 "P-Diffusion overhang of pmos < %d (poly.7)"
4819 overhang *poly allfets 130 "poly.overhang of transistor < %d (poly.8)"
4820 rect_only allfets "No bends in transistors (poly.11)"
4821 rect_only xhrpoly,uhrpoly "No bends in poly resistors (poly.11)"
4822 extend xpc/a xhrpoly,uhrpoly 2160 \
    "poly.contact extends poly resistor by < %d (lcon.1c + li.5)"
4823
4824 -- VISUAL --
4817,56-63 81%

```

Activities M GVim Thu 11:09 PM
sky130A.tech (~/.drc_tests) - GVIM

```

5168 # xhrpoly (P+ poly resistor)
5169 #-----
5170
5171 width xhrpoly 350 "xhrpoly resistor width < %d (P+ poly.1a)"
5172 # NOTE: xhrpoly resistor requires choice of discrete widths 0.35, 0.69, ... up to 1.27.
5173
5174 #-----
5175 # uhrpoly (P+ poly resistor, 2kOhm/sq)
5176 #-----
5177
5178 width uhrpoly 350 "uhrpoly resistor width < %d"
5179 spacing xhrpoly,uhrpoly,xpc alldiff 480 touching_illegal \
    "xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
5180 spacing xhrpoly,uhrpoly,xpc allpolynonres 480 touching_illegal \
    "xhrpoly/uhrpoly resistor spacing to allpolynonres < %d (poly.9)"
5181
5182
5183
5184
5185 #-----
5186 # MOS Varactor device rules
5187 #-----
5188
5189 overhang *nsd var,varhvt 250 \
    "N-Tap overhang of Varactor < %d (var.4)"
5190
5191
5192 overhang *mvnsd mvvar 250 \
-- VISUAL --
5182,67-74 87%

```

Commands to run in tkcon window

```
# Loading updated tech file
```

```
tech load sky130A.tech
```

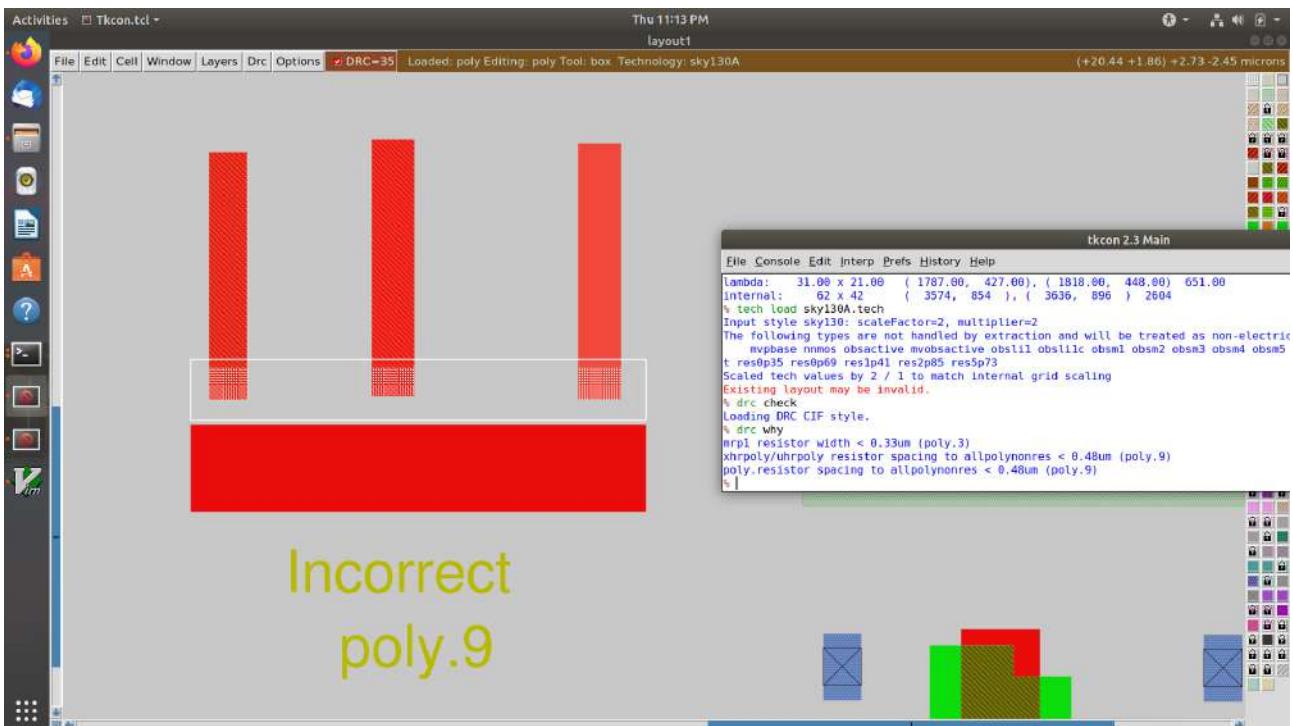
```
# Must re-run drc check to see updated drc errors
```

```
drc check
```

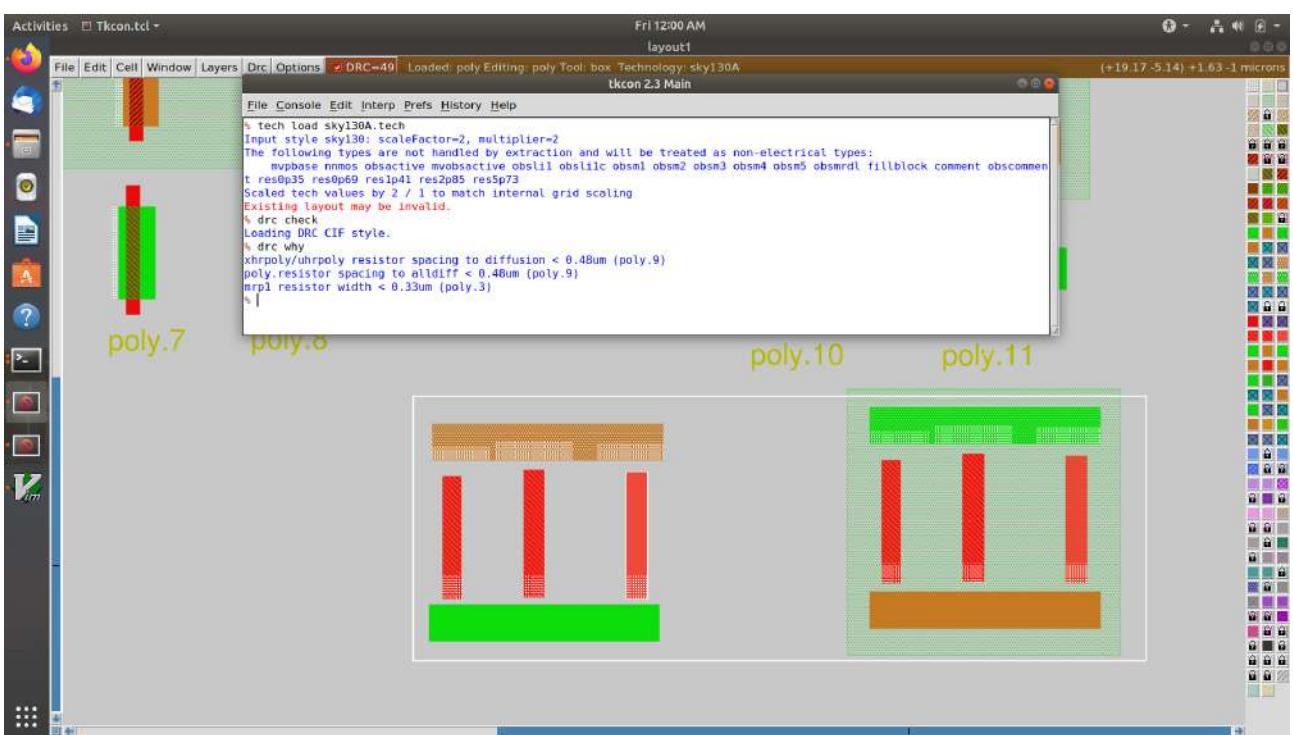
```
# Selecting region displaying the new errors and getting the error messages
```

```
drc why
```

Screenshot of magic window with rule implemented



Incorrect
poly.9



Incorrectly implemented difftap.2 simple rule correction

Screenshot of difftap rules

Activities Firefox Web Browser Fri 12:14 AM

Editing soc-design-and... yosys-tcl-ui-report/RE... nickson-jose/vsdstdce... Online Clipboard Periphery Rules — Sky... Magic VLSI

<https://skywater-pdk.readthedocs.io/en/main/rules/periphery.html#difftap>

Periphery Rules Search google@skywater-pdk

SkyWater SKY130 PDK

Versioning Information Current Status Known Issues Design Rules PDK Contents Analog Design Digital Design Simulation Physical & Design Verification Python API Previous Nomenclature Glossary How to Contribute Partners References

Name Description Flags Value Unit

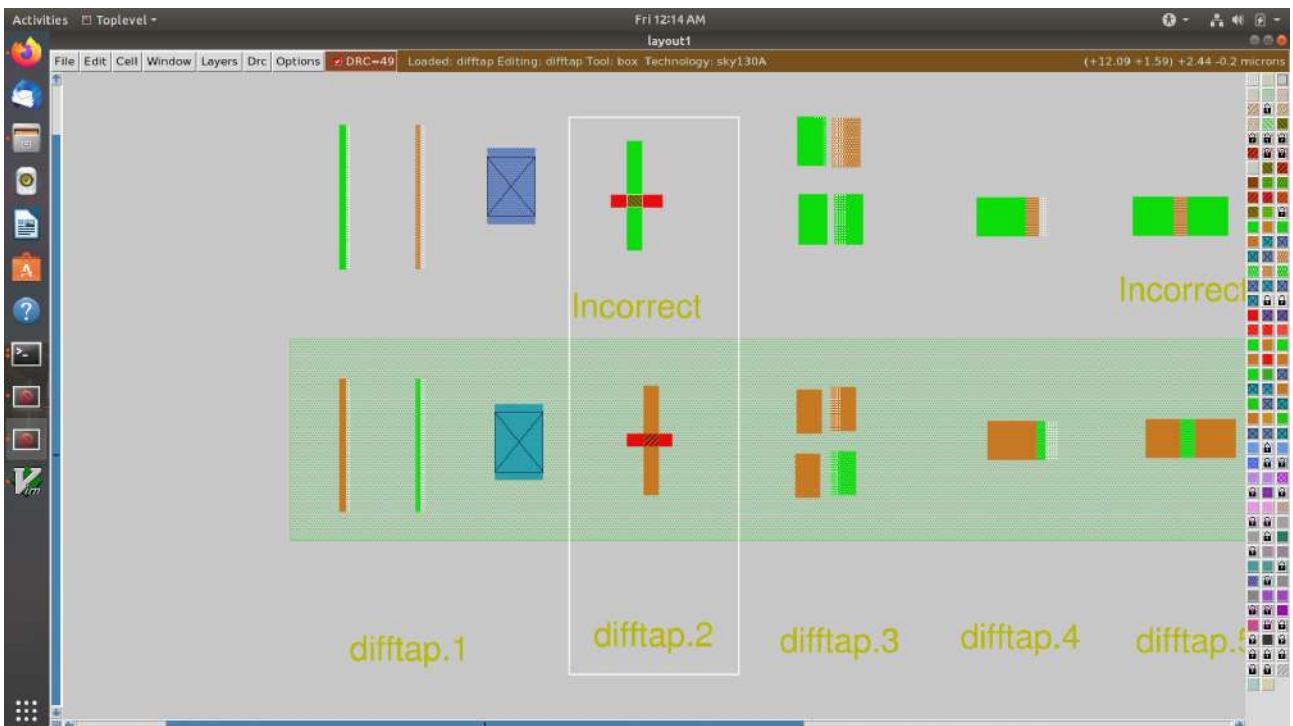
Table 38 Function: Defines active regions and contacts to substrate

Name	Description	Flags	Value	Unit
(difftap.1)	Width of diff or tap	P	0.150	μm
(difftap.2)	Minimum channel width (Diff And Poly) except for FETs inside areaid.sc: Rule exempted in the SP8* flows only, for the cells listed in rule difftap.2a	P	0.420	μm
(difftap.2a)	Minimum channel width (Diff And Poly) for cell names "s8cell_ee_plus_ssein_a", "s8cell_ee_plus_ssein_b", "s8cell_ee_plus_sseip_a", "s8cell_ee_plus_sseip_b", "s8lpls_pl8", "s8lpls_rdrv4", "s8lpls_rdrv4f" and "s8lpls_rdrv8"	P, NA	NA	μm
(difftap.2b)	Minimum channel width (Diff And Poly) for FETs inside areaid.sc	P	0.360	μm
(difftap.3)	Spacing of diff to diff, tap to tap, or non-abutting diff to tap		0.270	μm
(difftap.4)	Min tap bound by one diffusion		0.290	
(difftap.5)	Min tap bound by two diffusions	P	0.400	
(difftap.6)	Diff and tap are not allowed to extend beyond their abutting edge			
(difftap.7)	Spacing of difftap abutting edge to a non-conciding diff or tap edge	NE	0.130	μm
(difftap.8)	Enclosure of (p+) diffusion by N-well. Rule exempted inside UHVI.	DE NE P	0.180	μm
(difftap.9)	Spacing of (n+) diffusion to N-well outside UHVI	DE NE P	0.340	μm
(difftap.10)	Enclosure of (n+) tap by N-well. Rule exempted inside UHVI.	NE P	0.180	μm
(difftap.11)	Creation of resistors in N-well. Only recommended inside UHVI	NE P	0.190	μm

Contents

- Periphery Rules (x,-) (dnwell,-) (nwell,-) (pwell,-) (pudem,-) (hvtp,-) (hvtr,-) (lvtn,-) (ncm,-) (difftap,-) (tunn,-) (poly,-) (rpm,-) (varac,-) (photo,-) (npc,-) (n/ psd,-) (licon,-) (li,-) (ct,-) (capm,-) (vpp,-) /m1 -

Incorrectly implemented difftap.2 rule no drc violation even though spacing < 0.42μ



New commands inserted in sky130A.tech file to update drc

```
5178 width uhrpoly 350 "uhrpoly resistor width < %d"
5179 spacing xhrpoly,uhrpoly,xpc alldiff 480 touching_illegal \
      "xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
5180 spacing xhrpoly,uhrpoly,xpc allpolynonres 480 touching_illegal \
      "xhrpoly/uhrpoly resistor spacing to allpolynonres < %d (poly.9)"
5181
5182
5183
5184
5185 #-----
5186 # MOS Varactor device rules
5187 #-----
5188
5189 width pmos 420 \
      "mos transistor formed should have minimum width of < %d (difftap.2)"
5190 width nmos 420 \
      "mos transistor formed should have minimum width of < %d (difftap.2)"
5191
5192
5193 overhang *nsd var,varhvt 250 \
      "N-Tap overhang of Varactor < %d (var.4)"
5194
5195 overhang *mvnsd mvvar 250 \
      "N-Tap overhang of Varactor < %d (var.4)"
5196
5197 width var,varhvt,mvvar 180 "Varactor length < %d (var.1)"
5198 extend var,varhvt,mvvar *poly 1000 "Varactor width < %d (var.2)"
5199
5200
5201
5202
```

-- VISUAL -- 5192, 71 88%

Commands to run in tkcon window

```
# Loading updated tech file
```

```
tech load sky130A.tech
```

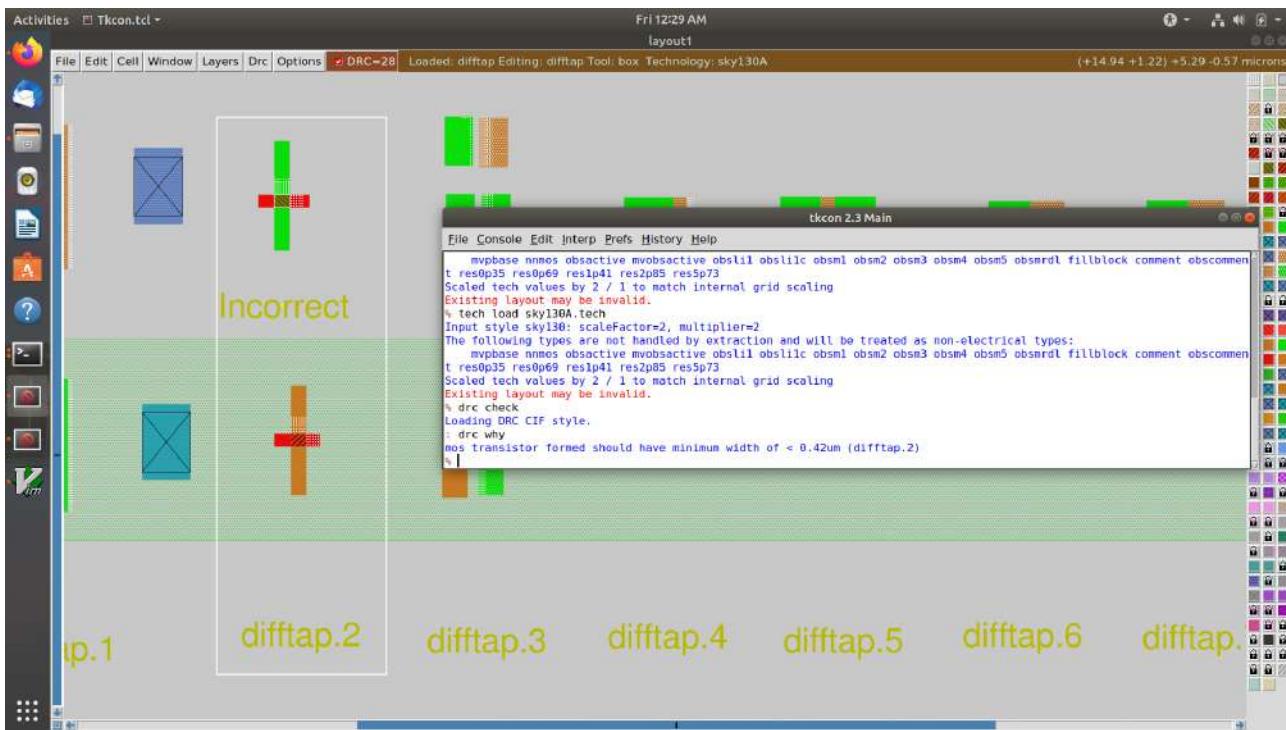
```
# Must re-run drc check to see updated drc errors
```

```
drc check
```

```
# Selecting region displaying the new errors and getting the error messages
```

```
drc why
```

Screenshot of magic window with rule implemented

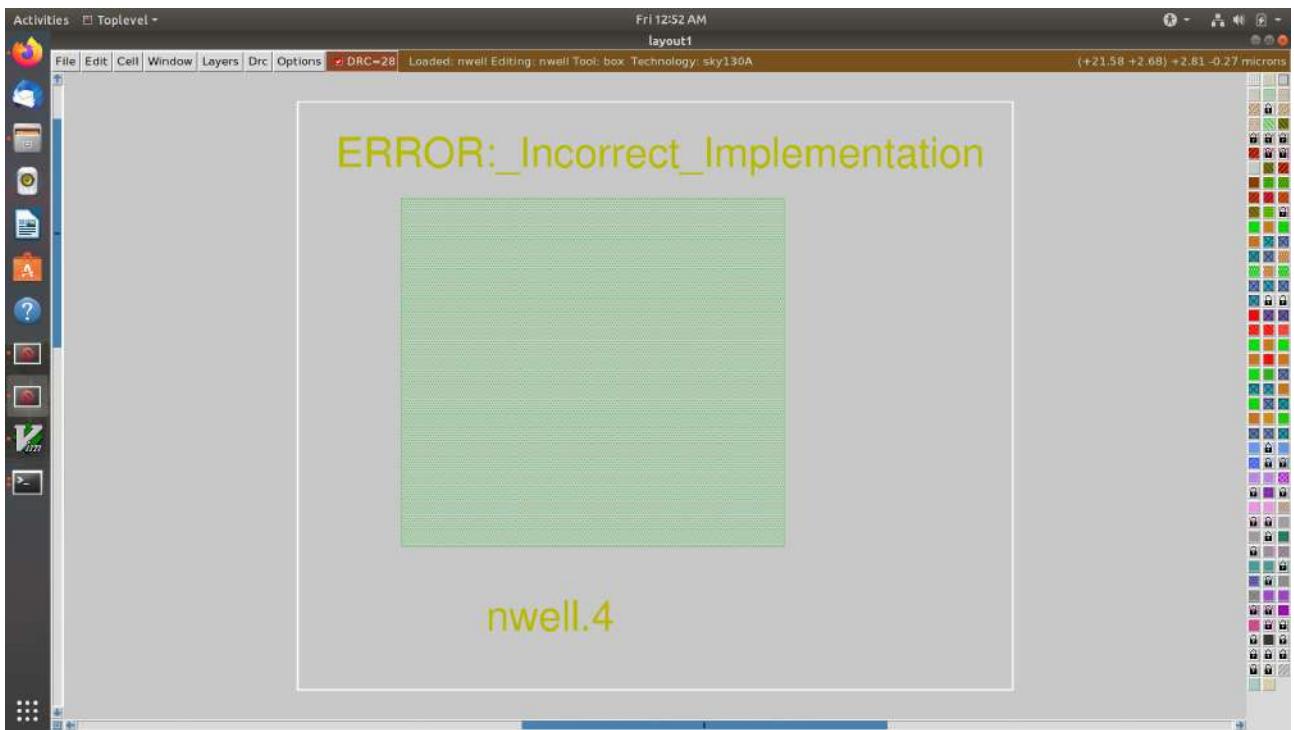


Incorrectly implemented nwell.4 complex rule correction

Screenshot of nwell rules

Table 31 Function: Define nwell implant regions.					
	Name	Description	Flags	Value	Unit
	(nwell.1)	Width of nwell		0.840	μm
	(nwell.2a)	Spacing between two n-wells		1.270	μm
	(nwell.2b)	Manual merge wells if less than minimum			
	(nwell.4)	All n-wells will contain metal-contacted tap (rule checks only for icon on top) . Rule exempted from high voltage cells inside UHVI			
	(nwell.5)	Deep nwell must be enclosed by nwell by atleast... Exempted inside UHVI or areaid, lw Nwells can merge over deep nwell if spacing too small (as in rule nwell.2)	TC	0.400	μm
	(nwell.5a)	min enclosure of nwell by dnwell inside UHVI		N/A	N/A
	(nwell.5b)	nwell inside UHVI must not be on the same net as nwell outside UHVI		N/A	N/A
	(nwell.6)	Min enclosure of nwell hole by deep nwell outside UHVI	TC	1.030	μm
	(nwell.7)	Min spacing between nwell and deep nwell on separate nets Spacing between nwell and deep nwell on the same net is set by the sum of the rules nwell.2 and nwell.5. By default, DRC run on a cell checks for the separate-net spacing, when nwell and deep nwell nets are separate within the cell hierarchy and are joined in the upper hierarchy. To allow net names to be joined and make the same-net rule applicable in this case, the "joinNets" switch should be turned on. waffle_chip	TC	4.500	μm

Incorrectly implemented nwell.4 rule no drc violation even though no tap present in nwell



New commands inserted in sky130A.tech file to update drc

Activities M GVim

Fri 1:03 AM
sky130A.tech (~/.drc_tests) - GVIM

```
File Edit Tools Syntax Buffers Window Help
1230 options calma-permissive-labels
1231
1232 # Ensure nwell overlaps dnwell at least 0.4um outside and 1.03um inside
1233 templayer dnwell_shrink dnwell
1234 shrink 1030
1235
1236 templayer nwell_missing dnwell
1237 grow 400
1238 and-not dnwell_shrink
1239 and-not nwell
1240
1241 templayer nwell_tapped
1242 bloat-all nsc nwell
1243
1244 templayer nwell_untapped nwell
1245 and-not nwell_tapped
1246
1247 # SONOS nFET devices must be in deep nwell
1248 templayer dnwell_missing nsonos
1249 and-not dnwell
1250
1251 # Define MiM cap bottom plate for spacing rule
1252 templayer mim_bottom
1253 bloat-all *mimcap *metal3
1254
-- VISUAL --
```

1245, 22 20%

Activities M GVIM

Fri 1:04 AM
sky130A.tech (~/.drc_tests) - GVIM

```
File Edit Tools Syntax Buffers Window Help
4721 spacing dnwell dnwell 6300 touching_ok "Deep N-well spacing < %d (dnwell.3)"
4722 spacing dnwell allnwell 4500 surround_ok \
4723 "Deep N-well spacing to N-well < %d (nwell.7)"
4724 cifmaxwidth nwell_missing 0 bend_illegal \
4725 "N-well overlap of Deep N-well < 0.4um outside, 1.03um inside (nwell.5a, 7)"
4726 cifmaxwidth dnwell_missing 0 bend_illegal \
4727 "SONOS nFET must be in Deep N-well (tunm.6a)"
4728
4729 #-----
4730 # NWELL
4731 #-----
4732
4733 width allnwell 840 "N-well width < %d (nwell.1)"
4734 spacing allnwell allnwell 1270 touching_ok "N-well spacing < %d (nwell.2a)"
4735
4736 variants (full)
4737 cifmaxwidth nwell_untapped 0 bend_illegal \
4738 "Nwell missing tap (nwell.4)"
4739 variants *
4740
4741 #-----
4742 # DIFF
4743 #-----
@ -- VISUAL --
```

4739, 11 80%

Commands to run in tkcon window

```
# Loading updated tech file
```

```
tech load sky130A.tech
```

Change drc style to drc full

drc style drc(full)

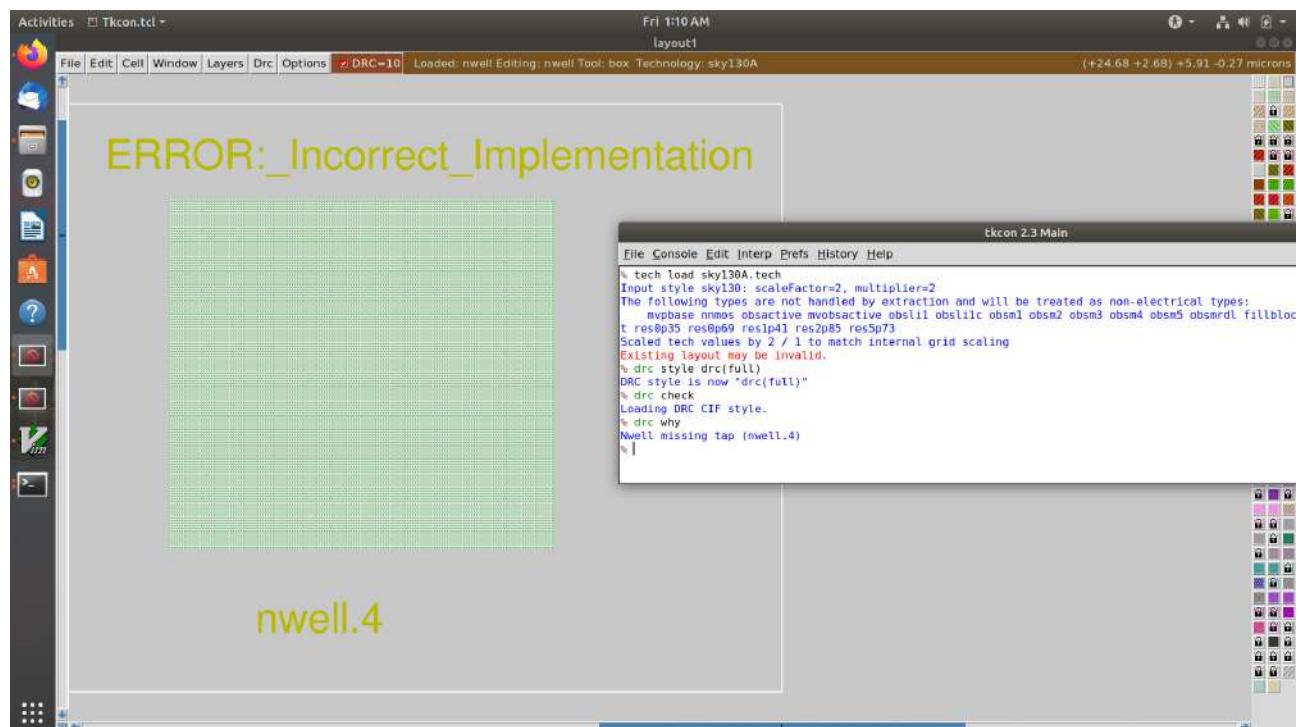
```
# Must re-run drc check to see updated drc errors
```

drc check

Selecting region displaying the new errors and getting the error messages

drc why

Screenshot of magic window with rule implemented



Section 4 - Pre-layout timing analysis and importance of good clock tree (22/03/2024 - 24/03/2024)

Theory

Implementation

- Section 4 tasks:-
 12. Fix up small DRC errors and verify the design is ready to be inserted into our flow.
 13. Save the finalized layout with custom name and open it.
 14. Generate lef from the layout.
 15. Copy the newly generated lef and associated required lib files to 'picorv32a' design 'src' directory.
 16. Edit 'config.tcl' to change lib file and add the new extra lef into the openlane flow.
 17. Run openlane flow synthesis with newly inserted custom inverter cell.
 18. Remove/reduce the newly introduced violations with the introduction of custom inverter cell by modifying design parameters.
 19. Once synthesis has accepted our custom inverter we can now run floorplan and placement and verify the cell is accepted in PnR flow.
 20. Do Post-Synthesis timing analysis with OpenSTA tool.
 21. Make timing ECO fixes to remove all violations.

22. Replace the old netlist with the new netlist generated after timing ECO fix and implement the floorplan, placement and cts.
23. Post-CTS OpenROAD timing analysis.
24. Explore post-CTS OpenROAD timing analysis by removing 'sky130_fd_sc_hd_clkbuf_1' cell from clock buffer list variable 'CTS_CLK_BUFFER_LIST'.
 - Section 4 - Tasks 1 to 4 files, reports and logs can be found in the following folder:

Section 4 - Tasks 1 to 4 (vsdstdcelldesign)

- Section 4 - Task 4 files, reports and logs can be found in the following folder:

Section 4 - Task 4 (src)

- Section 4 - Task 5 files, reports and logs can be found in the following folder:

Section 4 - Task 5 (picorv32a)

- Section 4 - Tasks 6 to 8 & 11 to 13 logs, reports and results can be found in following run folder:

Section 4 - Tasks 6 to 8 & 11 to 13 Run (24-03_10-03)

- Section 4 - Tasks 9 to 11 logs, reports and results can be found in following run folder:

Section 4 - Tasks 9 to 11 Run (25-03_18-52)

1. Fix up small DRC errors and verify the design is ready to be inserted into our flow.

Conditions to be verified before moving forward with custom designed cell layout:

- Condition 1: The input and output ports of the standard cell should lie on the intersection of the vertical and horizontal tracks.
- Condition 2: Width of the standard cell should be odd multiples of the horizontal track pitch.
- Condition 3: Height of the standard cell should be even multiples of the vertical track pitch.

Commands to open the custom inverter layout

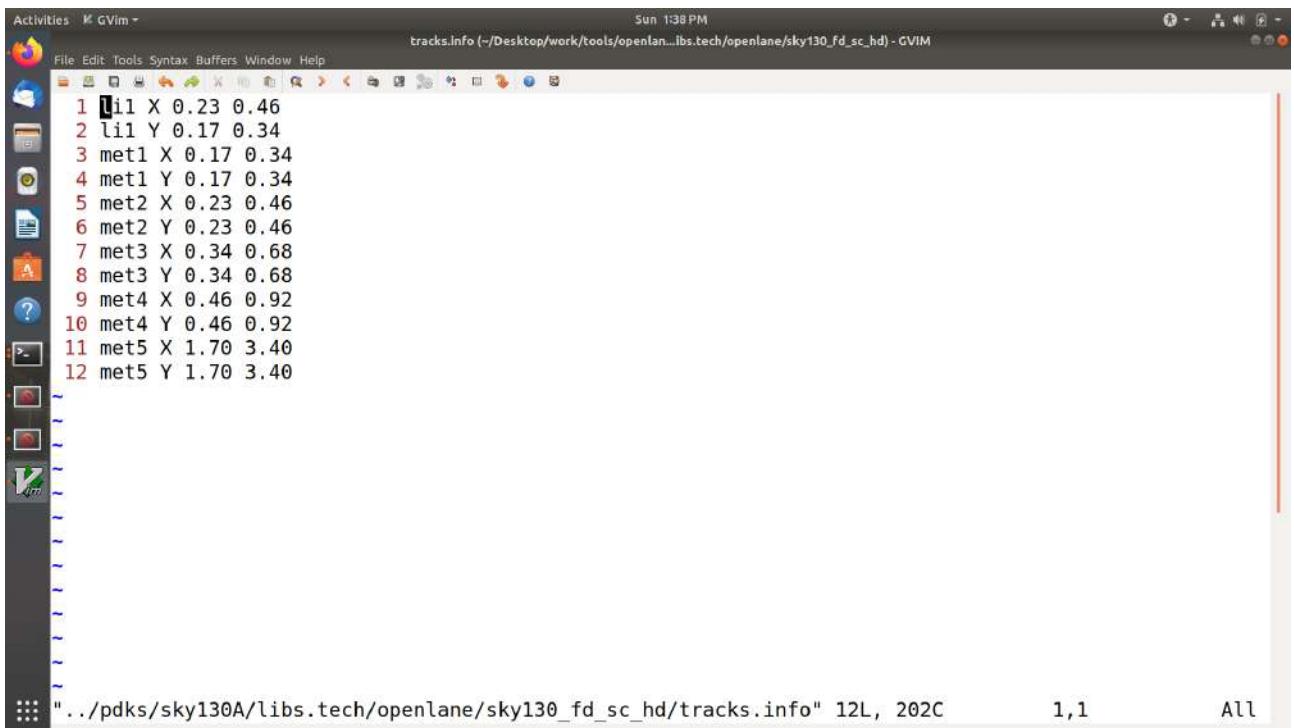
```
# Change directory to vsdstdcelldesign
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
```

```
# Command to open custom inverter layout in magic
```

```
magic -T sky130A.tech sky130_inv.mag &
```

Screenshot of tracks.info of sky130_fd_sc_hd



A screenshot of the GVIM text editor window. The title bar reads "activities K. GVIM" and "tracks.info (~/Desktop/work/tools/openlane/libs.tech/openlane/sky130_fd_sc_hd) - GVIM". The status bar shows "Sun 1:38 PM" and "1,1 All". The main pane displays a list of track coordinates:

```
1 l1l X 0.23 0.46
2 l1l Y 0.17 0.34
3 met1 X 0.17 0.34
4 met1 Y 0.17 0.34
5 met2 X 0.23 0.46
6 met2 Y 0.23 0.46
7 met3 X 0.34 0.68
8 met3 Y 0.34 0.68
9 met4 X 0.46 0.92
10 met4 Y 0.46 0.92
11 met5 X 1.70 3.40
12 met5 Y 1.70 3.40
```

Commands for tkcon window to set grid as tracks of locali layer

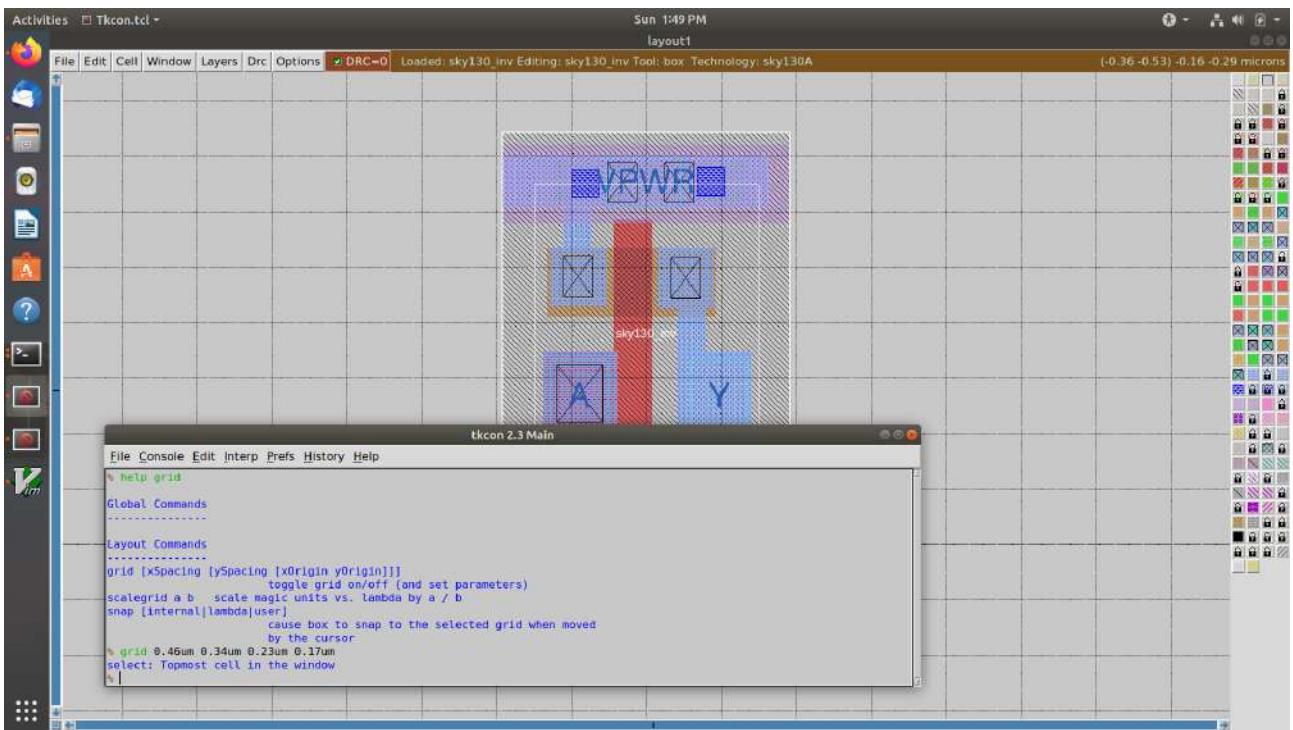
```
# Get syntax for grid command
```

```
help grid
```

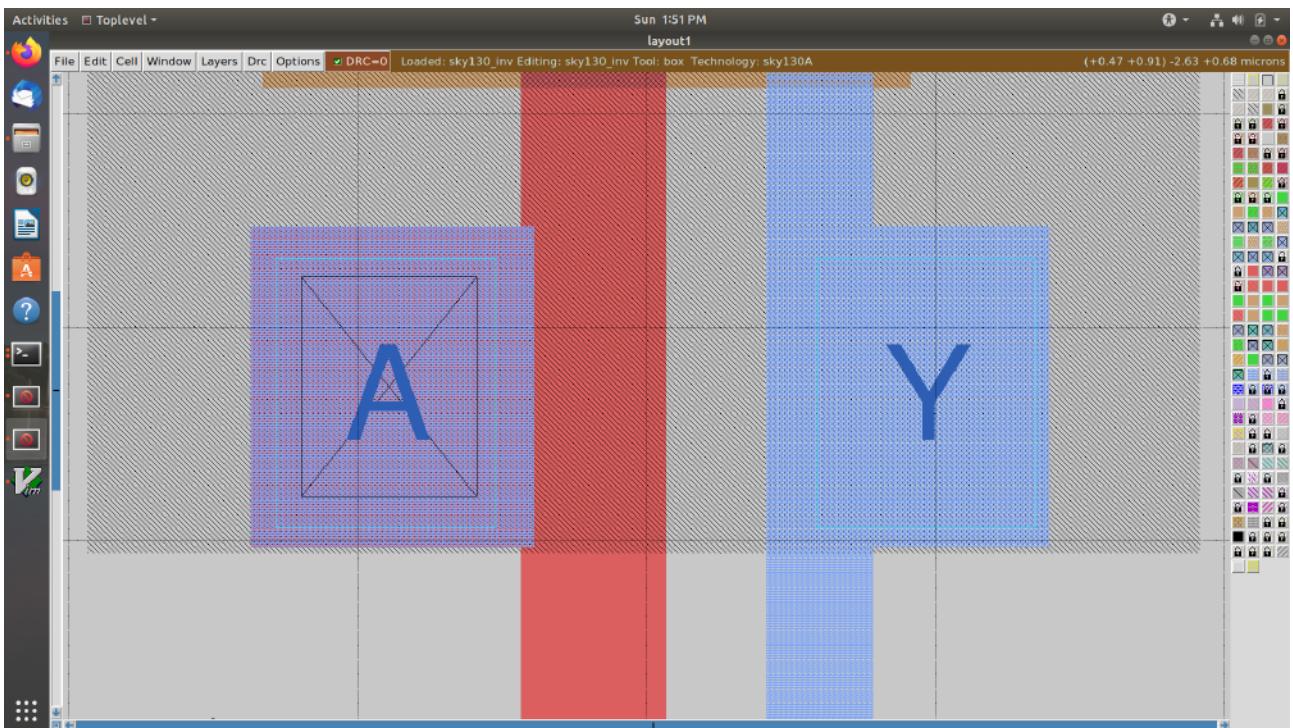
```
# Set grid values accordingly
```

```
grid 0.46um 0.34um 0.23um 0.17um
```

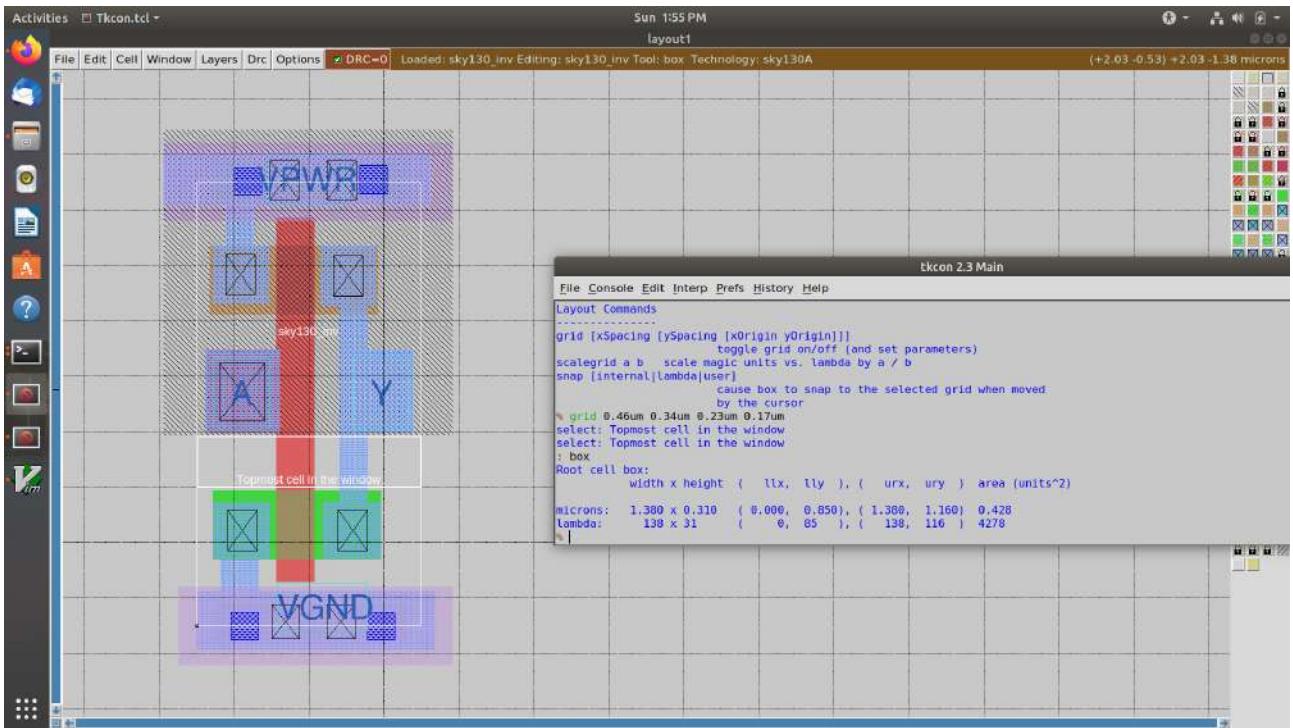
Screenshot of commands run



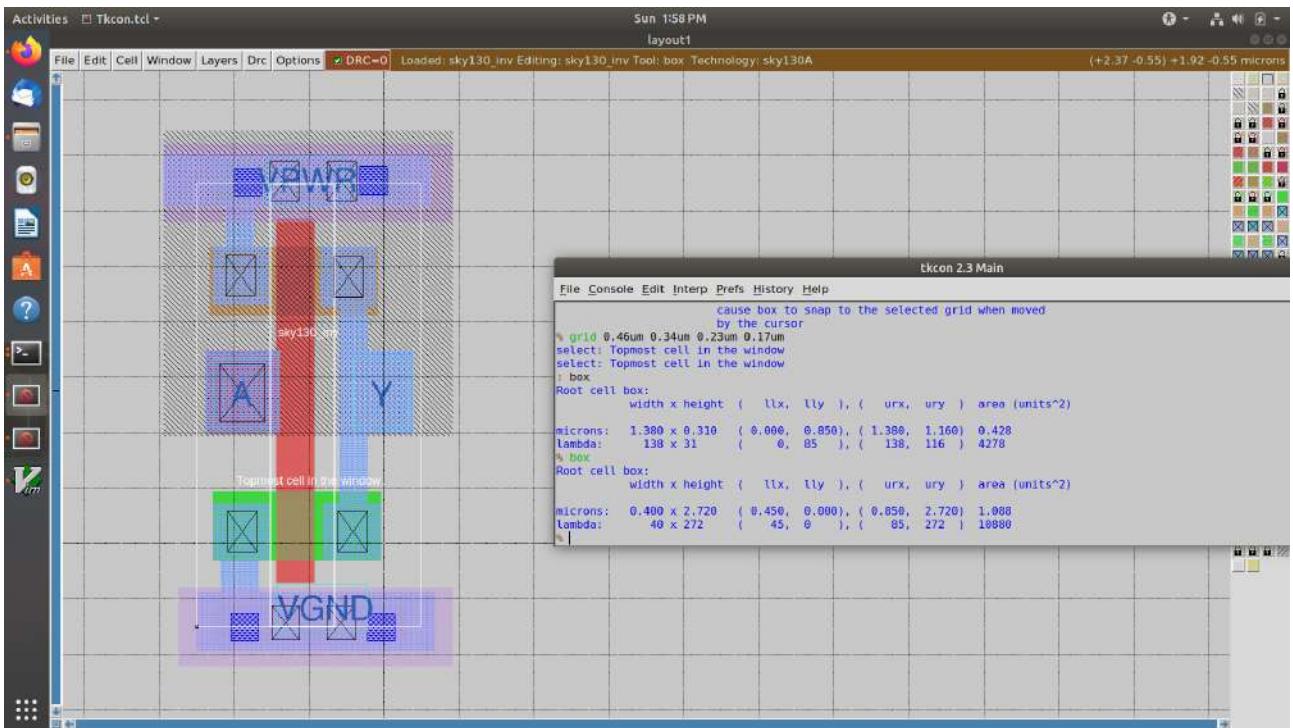
Condition 1 verified



Condition 2 verified



Condition 3 verified



2. Save the finalized layout with custom name and open it.

Command for tkcon window to save the layout with custom name

```
# Command to save as
```

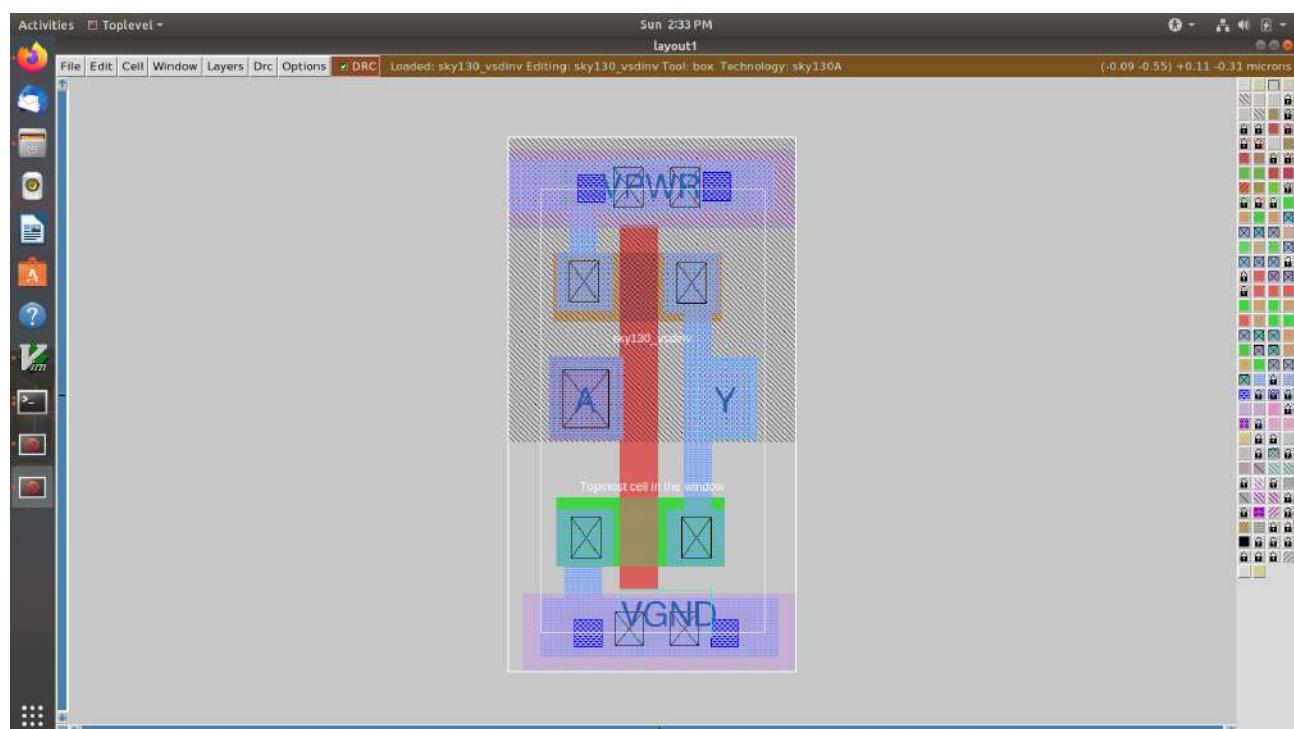
```
save sky130_vsdinv.mag
```

Command to open the newly saved layout

```
# Command to open custom inverter layout in magic
```

```
magic -T sky130A.tech sky130_vsdinv.mag &
```

Screenshot of newly saved layout



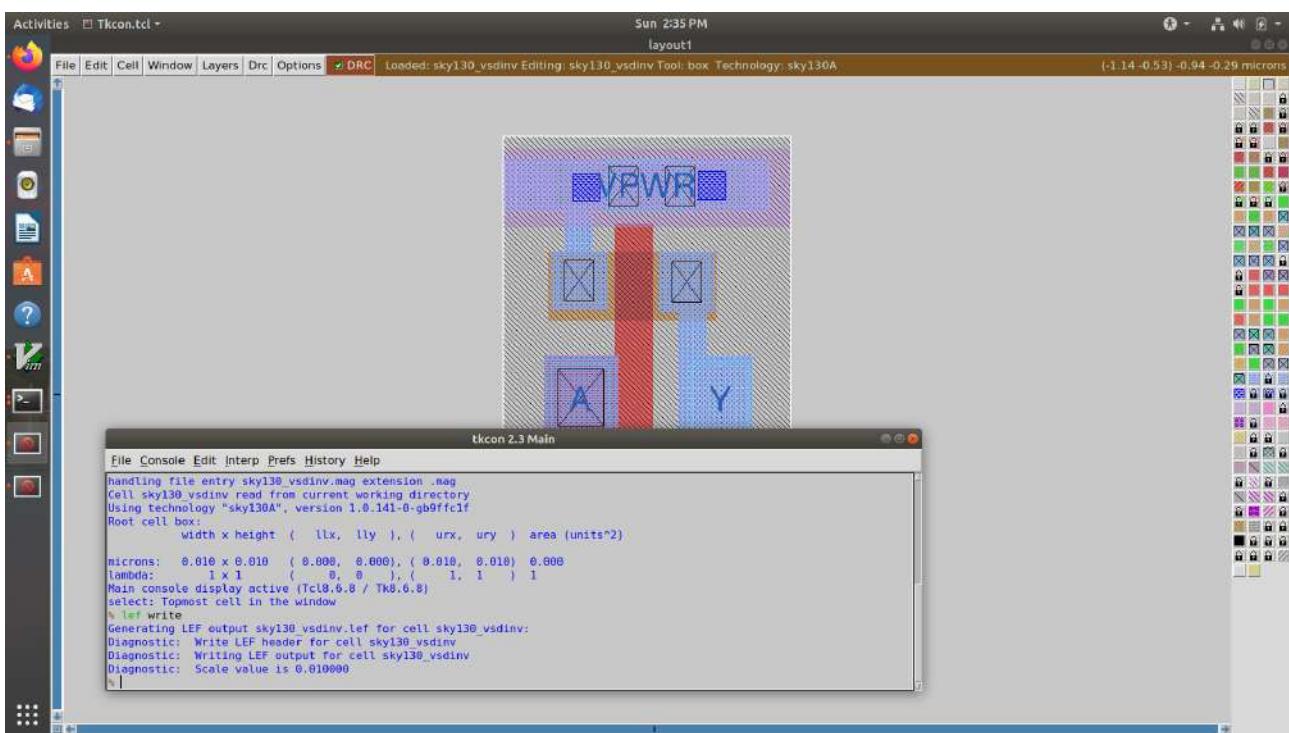
3. Generate lef from the layout.

Command for tkcon window to write lef

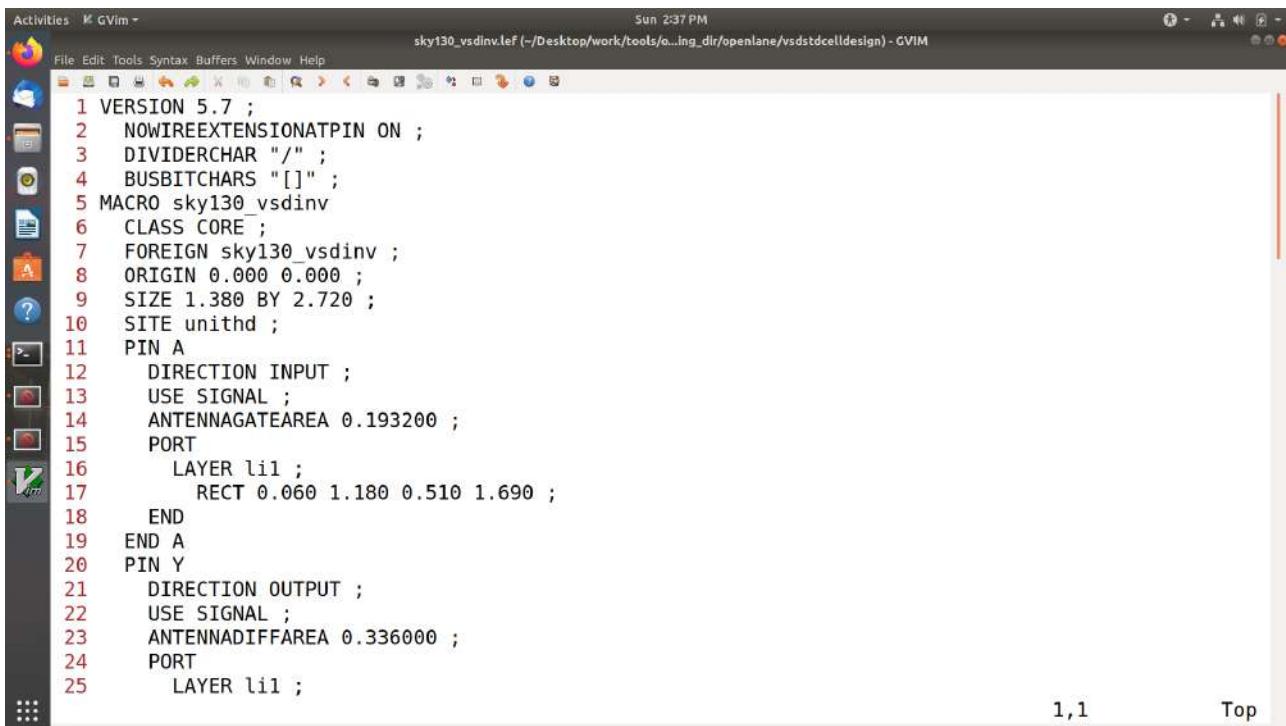
```
# lef command
```

```
lef write
```

Screenshot of command run



Screenshot of newly created lef file



A screenshot of the GVIM text editor window. The title bar reads "Activities K. GVim" and "sky130_vsdinv.lef (~/Desktop/work/tools/openlane/designs/sky130_vsdinv.lef) - GVIM". The status bar shows "Sun 2:37 PM" and "1,1 Top". The main pane displays a LEF (Liberty Cell Format) file with the following content:

```
1 VERSION 5.7 ;
2 NOWIREEXTENSIONATPIN ON ;
3 DIVIDERCHAR "/" ;
4 BUSBITCHARS "[]" ;
5 MACRO sky130_vsdinv
6 CLASS CORE ;
7 FOREIGN sky130_vsdinv ;
8 ORIGIN 0.000 0.000 ;
9 SIZE 1.380 BY 2.720 ;
10 SITE unithd ;
11 PIN A
12     DIRECTION INPUT ;
13     USE SIGNAL ;
14     ANTENNAGATEAREA 0.193200 ;
15     PORT
16         LAYER li1 ;
17         RECT 0.060 1.180 0.510 1.690 ;
18     END
19 END A
20 PIN Y
21     DIRECTION OUTPUT ;
22     USE SIGNAL ;
23     ANTENNADIFFAREA 0.336000 ;
24     PORT
25         LAYER li1 ;
```

4. Copy the newly generated lef and associated required lib files to 'picorv32a' design 'src' directory.

Commands to copy necessary files to 'picorv32a' design 'src' directory

```
# Copy lef file
```

```
cp sky130_vsdinv.lef ~/Desktop/work/tools/openlane_working_dir/openlane/designs/
picorv32a/src/
```

```
# List and check whether it's copied
```

```
ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
```

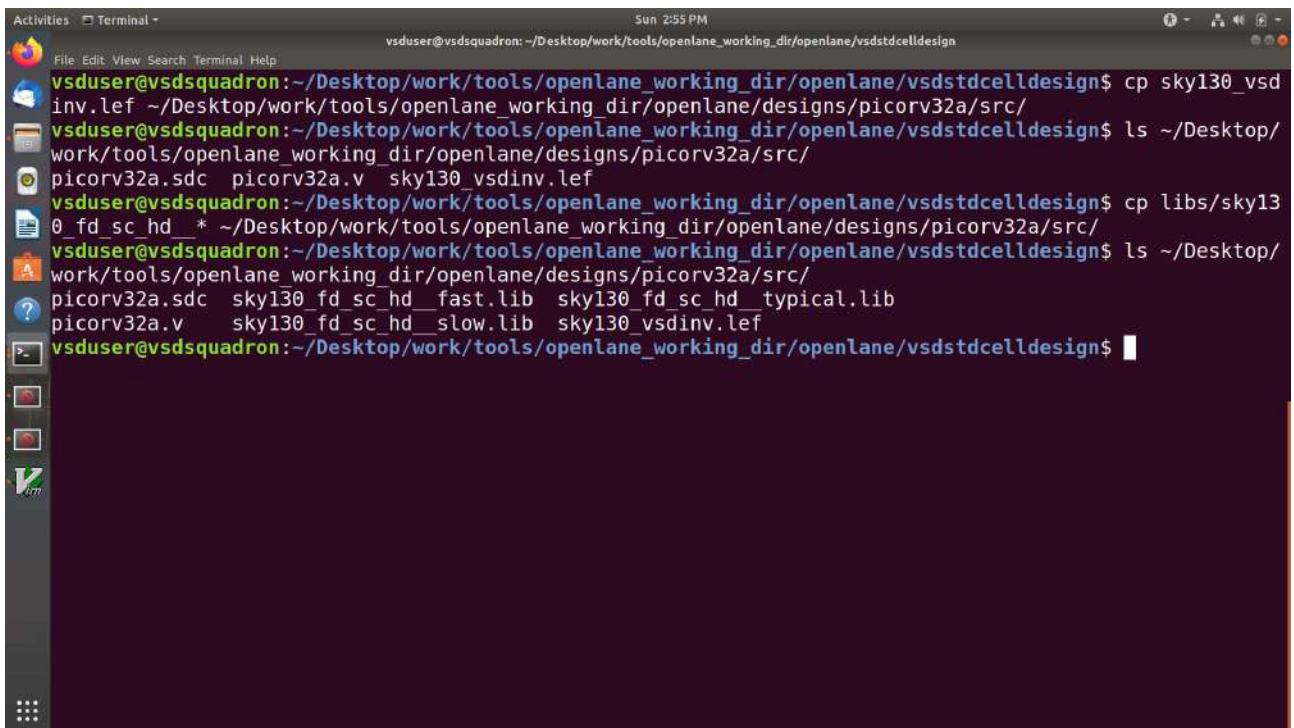
```
# Copy lib files
```

```
cp libs/sky130_fd_sc_hd_* ~/Desktop/work/tools/openlane_working_dir/openlane/designs/
picorv32a/src/
```

```
# List and check whether it's copied
```

```
ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
```

Screenshot of commands run



```
Activities Terminal Sun 2:55 PM vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cp sky130_vsdinv.lef ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
picorv32a.sdc picorv32a.v sky130_vsdinv.lef
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cp libs/sky130_fd_sc_hd_* ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
picorv32a.sdc sky130_fd_sc_hd_fast.lib sky130_fd_sc_hd_typical.lib
picorv32a.v sky130_fd_sc_hd_slow.lib sky130_vsdinv.lef
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```

5. Edit 'config.tcl' to change lib file and add the new extra lef into the openlane flow.

Commands to be added to config.tcl to include our custom cell in the openlane flow

```
set ::env(LIB_SYNTH) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/
sky130_fd_sc_hd_typical.lib"

set ::env(LIB_FASTEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/
sky130_fd_sc_hd_fast.lib"

set ::env(LIB_SLOWEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/
sky130_fd_sc_hd_slow.lib"
```

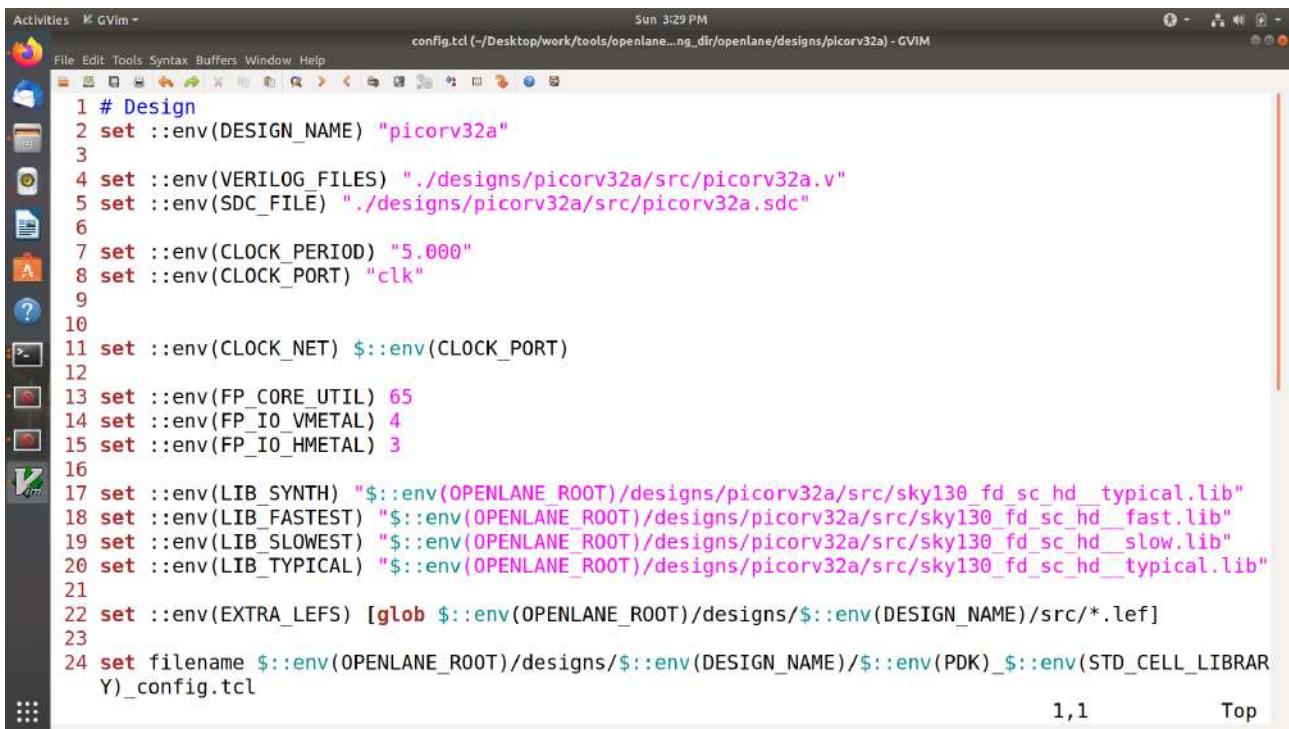
```

set ::env(LIB_TYPICAL) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/
sky130_fd_sc_hd_typical.lib"

set ::env(EXTRA_LEFS) [glob $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/
src/*.lef]

```

Edited config.tcl to include the added lef and change library to ones we added in src directory



```

Activities  M GVIM - Sun 3:29 PM config.tcl (-/Desktop/work/tools/openlane...ng_dir/openlane/designs/picorv32a) - GVIM
File Edit Tools Syntax Buffers Window Help
1 # Design
2 set ::env(DESIGN_NAME) "picorv32a"
3
4 set ::env(VERILOG_FILES) "./designs/picorv32a/src/picorv32a.v"
5 set ::env(SDC_FILE) "./designs/picorv32a/src/picorv32a.sdc"
6
7 set ::env(CLOCK_PERIOD) "5.000"
8 set ::env(CLOCK_PORT) "clk"
9
10
11 set ::env(CLOCK_NET) $::env(CLOCK_PORT)
12
13 set ::env(FP_CORE_UTIL) 65
14 set ::env(FP_IO_VMETAL) 4
15 set ::env(FP_IO_HMETAL) 3
16
17 set ::env(LIB_SYNTH) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib"
18 set ::env(LIB_FASTEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib"
19 set ::env(LIB_SLOWEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib"
20 set ::env(LIB_TYPICAL) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib"
21
22 set ::env(EXTRA_LEFS) [glob $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/src/*.lef]
23
24 set filename $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/$::env(PDK)_$::env(STD_CELL_LIBRARY)_config.tcl
1,1 Top

```

6. Run openlane flow synthesis with newly inserted custom inverter cell.

Commands to invoke the OpenLANE flow include new lef and perform synthesis

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:v0.21'
```

```
# Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command
```

```
docker
```

```
# Now that we have entered the OpenLANE flow contained docker sub-system we can invoke the OpenLANE flow in the Interactive mode using the following command
```

```
./flow.tcl -interactive
```

```
# Now that OpenLANE flow is open we have to input the required packages for proper functionality of the OpenLANE flow
```

```
package require openlane 0.9
```

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the design creating some necessary files and directories for running a specific design which in our case is 'picorv32a'
```

```
prep -design picorv32a
```

```
# Additional commands to include newly added lef to openlane flow
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

Now that the design is prepped and ready, we can run synthesis using following command

`run_synthesis`

Screenshots of commands run

Activities Terminal Sun 3:36 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
vsduser@vsdsquadron:~$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ docker
bash-4.2$ ./flow.tcl -interactive
[INFO]:

[INFO]: Version: v0.21
[INFO]: Running interactively
% package require openlane 0.9
% prep -design picorv32a
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
```

Activities Terminal Sun 3:37 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
? sky130_fd_sc_hd.lef: SITEs matched found: 0
? sky130_fd_sc_hd.lef: MACROs matched found: 437
? sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
? sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
? sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
? sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
? sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
? sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
```

```

Activities Terminal - Sun 3:37 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
::: % run_synthesis

```

```

Activities Terminal - Sun 3:45 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
::: %

```

7. Remove/reduce the newly introduced violations with the introduction of custom inverter cell by modifying design parameters.

Noting down current design values generated before modifying parameters to improve timing

```

Activities Terminal - Sun 4:00 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
sky130_fd_sc_hd_o31la_2 8
sky130_fd_sc_hd_o31a_2 19
sky130_fd_sc_hd_o31ai_2 1
sky130_fd_sc_hd_o32a_2 109
sky130_fd_sc_hd_o41a_2 2
sky130_fd_sc_hd_or2_2 1088
sky130_fd_sc_hd_or2b_2 25
sky130_fd_sc_hd_or3_2 68
sky130_fd_sc_hd_or3b_2 5
sky130_fd_sc_hd_or4_2 93
sky130_fd_sc_hd_or4b_2 6
sky130_fd_sc_hd_or4bb_2 2
sky130_vsdinv 1554

Chip area for module '\picorv32a': 147712.918400

29. Executing Verilog backend.
Dumping module '\picorv32a'.

Warnings: 307 unique messages, 307 total
End of script. Logfile hash: ea6f91c309, CPU: user 11.69s system 3.17s, MEM: 95.95 MB peak
Yosys 0.9+3621 (git sha1 84e9fa7, gcc 8.3.1 -fPIC -Os)
Time spent: 57% 2x abc (18 sec), 12% 33x opt_expr (4 sec), ...
[INFO]: Changing netlist from 0 to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis
/picorv32a.synthesis.v
[INFO]: Running Static Timing Analysis...
[INFO]: current step index: 2
OpenSTA 2.2.0-28b40207a8 Copyright (c) 2019, Parallever Software, Inc.

```

```

Activities Terminal - Sun 4:13 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.9460000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.9460000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
[INFO]: % 

```

Commands to view and change parameters to improve timing and run synthesis

Now once again we have to prep design so as to update variables

prep -design picorv32a -tag 24-03_10-03 -overwrite

```
# Addiitional commands to include newly added lef to openlane flow merged.lef
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to display current value of variable SYNTH_STRATEGY
```

```
echo $::env(SYNTH_STRATEGY)
```

```
# Command to set new value for SYNTH_STRATEGY
```

```
set ::env(SYNTH_STRATEGY) "DELAY 3"
```

```
# Command to display current value of variable SYNTH_BUFFERING to check whether it's  
enabled
```

```
echo $::env(SYNTH_BUFFERING)
```

```
# Command to display current value of variable SYNTH_SIZING
```

```
echo $::env(SYNTH_SIZING)
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Command to display current value of variable SYNTH_DRIVING_CELL to check whether it's the proper cell or not
```

```
echo $::env(SYNTH_DRIVING_CELL)
```

```
# Now that the design is prepped and ready, we can run synthesis using following command
```

```
run_synthesis
```

Screenshot of merged.lef in tmp directory with our custom inverter as macro

```
68236 MACRO Sky130_vsdinv
68237   CLASS CORE ;
68238   FOREIGN sky130_vsdinv ;
68239   ORIGIN 0.000 0.000 ;
68240   SIZE 1.380 BY 2.720 ;
68241   SITE unithd ;
68242   PIN A
68243     DIRECTION INPUT ;
68244     USE SIGNAL ;
68245     ANTENNAGATEAREA 0.193200 ;
68246     PORT
68247       LAYER l1l ;
68248       RECT 0.060 1.180 0.510 1.690 ;
68249     END
68250   END A
68251   PIN Y
68252     DIRECTION OUTPUT ;
68253     USE SIGNAL ;
68254     ANTENNADIFFAREA 0.336000 ;
68255     PORT
68256       LAYER l1l ;
68257       RECT 0.760 1.960 1.100 2.330 ;
68258       RECT 0.880 1.690 1.050 1.960 ;
68259       RECT 0.880 1.180 1.330 1.690 ;
68260       RECT 0.880 0.760 1.050 1.180 ;
```

Screenshots of commands run

```
Activities Terminal Sun 5:09 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% prep -design picorv32a -tag 24-03_10-03 -overwrite
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[WARNING]: Removing existing run /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
::: mergeLef.py : Merging LEFs
::: mergeLef.py : Merging LEFs
```

```
Activities Terminal Sun 5:09 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add lefs -src $lefs
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% echo $::env(SYNTH_STRATEGY)
AREA 0
% set ::env(SYNTH_STRATEGY) "DELAY 3"
DELAY 3
% echo $::env(SYNTH_BUFFERING)
1
% echo $::env(SYNTH_SIZING)
0
% set ::env(SYNTH_SIZING) 1
1
% echo $::env(SYNTH_DRIVING_CELL)
sky130_fd_sc_hd_inv_8
::: % run_synthesis
```

```
Activities Terminal - Sun 5:10 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
::: %
```

Comparing to previously noted run values area has increased and worst negative slack has become 0

```

Activities Terminal - Sun 5:11 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
sky130_fd_sc_hd_o32a_2 9
sky130_fd_sc_hd_o32ai_2 3
sky130_fd_sc_hd_o41ai_2 18
sky130_fd_sc_hd_or2_2 80
sky130_fd_sc_hd_or2b_2 264
sky130_fd_sc_hd_or3_2 6
sky130_fd_sc_hd_or3b_2 5
sky130_fd_sc_hd_or4_2 68
sky130_fd_sc_hd_or4b_2 4
sky130_fd_sc_hd_xnor2_2 700
sky130_fd_sc_hd_xor2_2 1164
sky130_vsdinv 1434

Chip area for module '\picorv32a': 181730.544000

29. Executing Verilog backend.
Dumping module '\picorv32a'.

Warnings: 307 unique messages, 307 total
End of script. Logfile hash: befd735e75, CPU: user 12.56s system 2.87s, MEM: 97.45 MB peak
Yosys 0.9+3621 (git sha1 84e9fa7, gcc 8.3.1 -fPIC -Os)
Time spent: 64% 2x abc (26 sec), 10% 33x opt_expr (4 sec), ...
[INFO]: Changing netlist from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis.v to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis.v
[INFO]: Running Static Timing Analysis...
[INFO]: current step index: 11
OpenSTA 2.2.0-28b10207a8 Copyright (c) 2019, Parallever Software, Inc.

```

```

Activities Terminal - Sun 5:11 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk $all_inputs_wo_clk

# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
[INFO]: % 

```

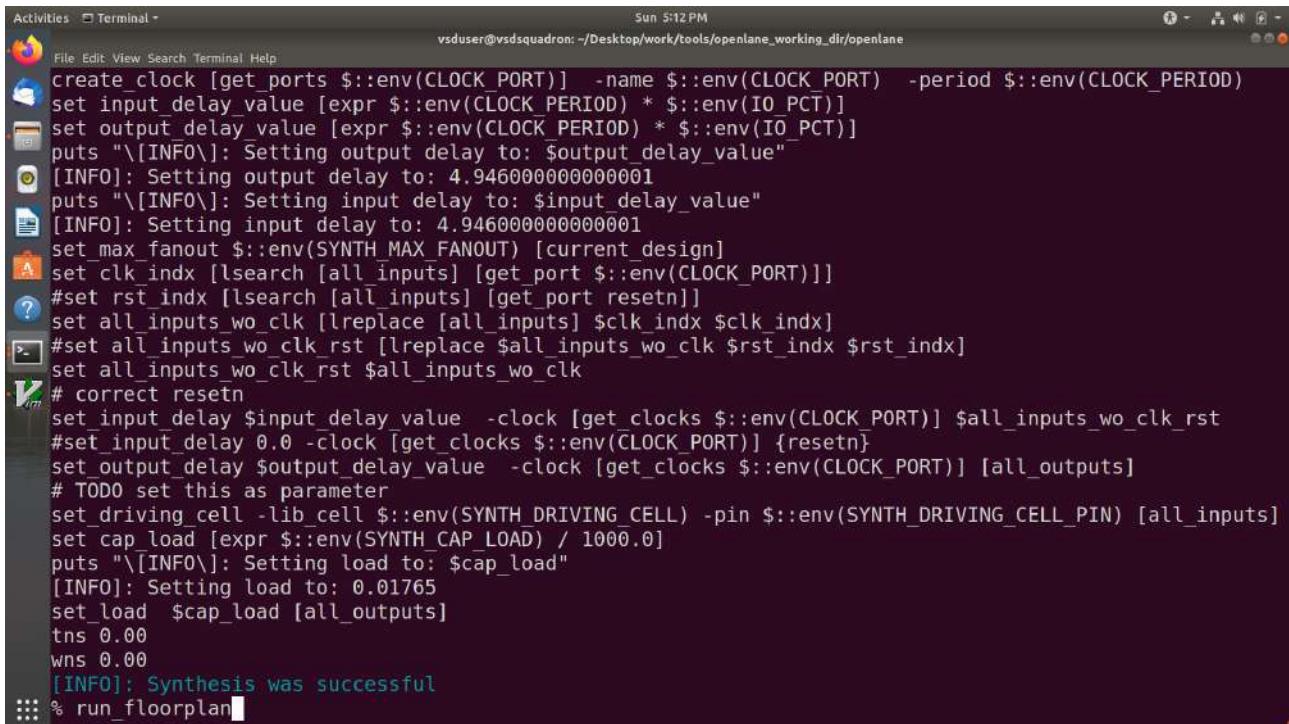
8. Once synthesis has accepted our custom inverter we can now run floorplan and placement and verify the cell is accepted in PnR flow.

Now that our custom inverter is properly accepted in synthesis we can now run floorplan using following command

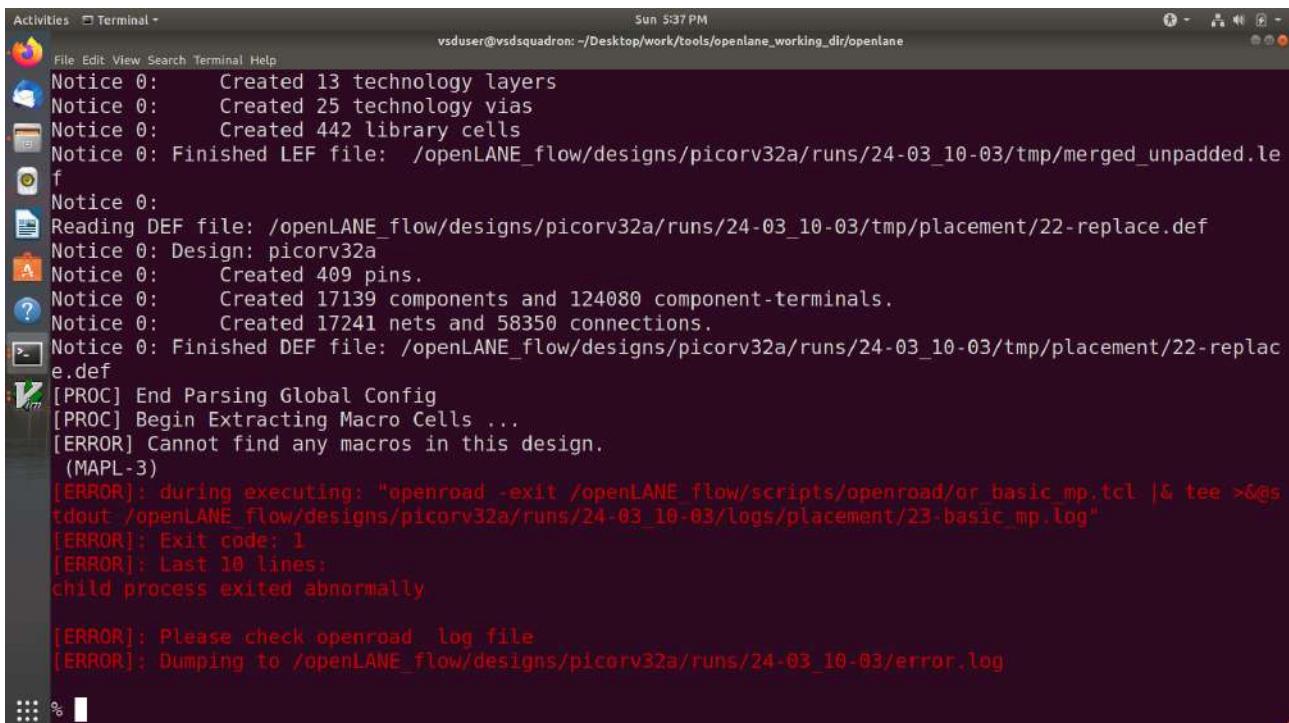
Now we can run floorplan

run_floorplan

Screenshots of command run



```
Activities Terminal Sun 5:12 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
:: % run_floorplan
```



```
Activities Terminal Sun 5:37 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/22-replace.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/22-replace.def
[PROC] End Parsing Global Config
[PROC] Begin Extracting Macro Cells ...
[ERROR] Cannot find any macros in this design.
(MAPL-3)
[ERROR]: during executing: "openroad -exit /openLANE_flow/scripts/openroad/or_basic_mp.tcl |& tee >& stdout /openLANE_flow/designs/picorv32a/runs/24-03_10-03/logs/placement/23-basic_mp.log"
[ERROR]: Exit code: 1
[ERROR]: Last 10 lines:
child process exited abnormally

[ERROR]: Please check openroad log file
[ERROR]: Dumping to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/error.log
:: %
```

Since we are facing unexpected un-explainable error while using run_floorplan command, we can instead use the following set of commands available based on information from Desktop/work/tools/openlane_working_dir/openlane/scripts/tcl_commands/floorplan.tcl and also based on Floorplan Commands section in Desktop/work/tools/openlane_working_dir/openlane/docs/source/OpenLANE_commands.md

Following commands are altogether sourced in "run_floorplan" command

init_floorplan

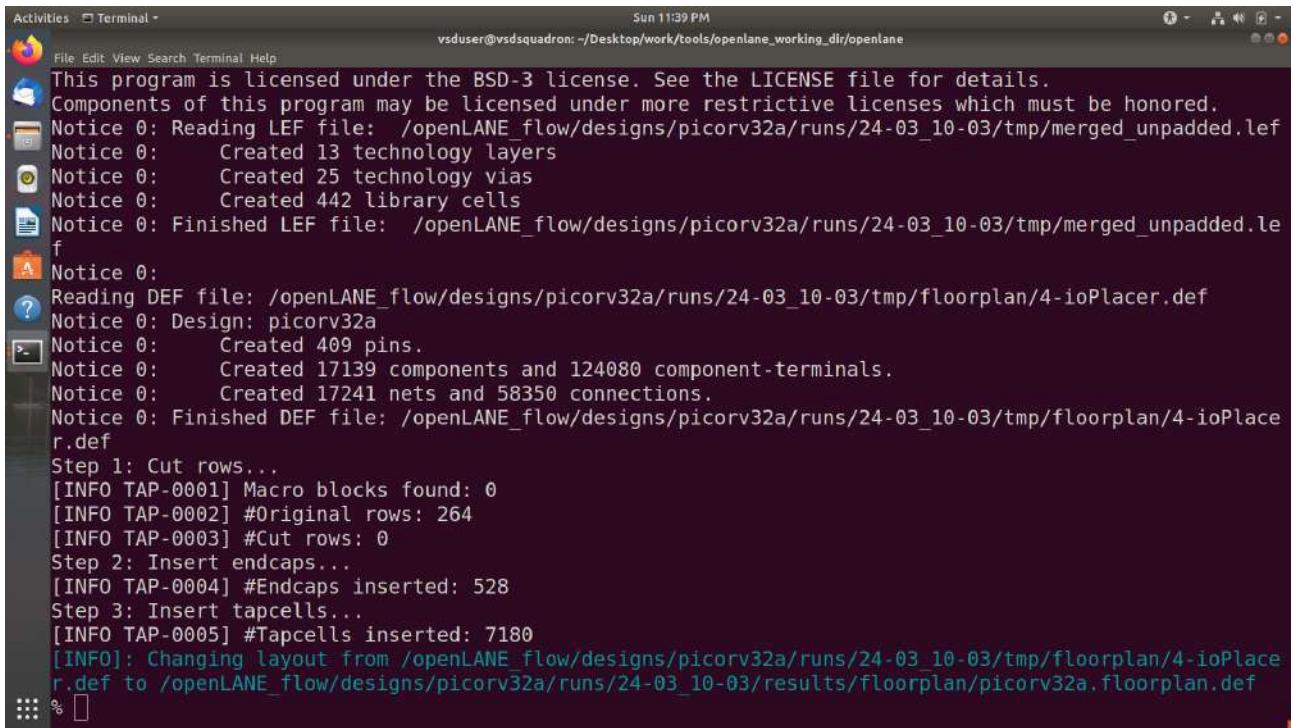
place_io

tap_decap_or

Screenshots of commands run

```
Activities Terminal Sun 11:38 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
% init_floorplan
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 3
OpenROAD 0.9.0 1415572a73
A This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
[INFO IFP-0001] Added 264 rows of 1566 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 731.615 742.335 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/3-verilog2def.die_area.rpt.
[INFO] Floorplanned on a core area of 5.52 10.88 725.88 728.96 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/3-verilog2def.core_area.rpt.
[INFO]: Core area width: 720.36
[INFO]: Core area height: 718.08
[INFO]: Changing layout from 0 to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def
::: % place_io
```

```
Activities Terminal Sun 11:38 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% place_io
[INFO]: Running IO Placement...
[INFO]: current step index: 4
OpenROAD 0.9.0 1415572a73
A This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def
#Macro blocks found: 0
Using 5u default boundaries offset
Random pin placement
RandomMode Even
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
::: % tap_decap_or
```



```
Sun 11:39 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 17139 components and 124080 component-terminals.
Notice 0:     Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Step 1: Cut rows...
[INFO TAP-0001] Macro blocks found: 0
[INFO TAP-0002] #Original rows: 264
[INFO TAP-0003] #Cut rows: 0
Step 2: Insert endcaps...
[INFO TAP-0004] #Endcaps inserted: 528
Step 3: Insert tapcells...
[INFO TAP-0005] #Tapcells inserted: 7180
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/floorplan/picorv32a.floorplan.def
```

Now that floorplan is done we can do placement using following command

Now we are ready to run placement

run_placement

Screenshots of command run

```

Activities Terminal Sun 11:49 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 17139 components and 124080 component-terminals.
Notice 0:     Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Step 1: Cut rows...
[INFO TAP-0001] Macro blocks found: 0
[INFO TAP-0002] #Original rows: 264
[INFO TAP-0003] #Cut rows: 0
Step 2: Insert endcaps...
[INFO TAP-0004] #Endcaps inserted: 528
Step 3: Insert tapcells...
[INFO TAP-0005] #Tapcells inserted: 7180
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/floorplan/picorv32a.floorplan.def
::: % run_placement

```

```

Activities Terminal Sun 11:51 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
legalized HPWL      910806.5 u
delta HPWL           2 %
[INFO DPL-0020] Mirrored 6650 instances
[INFO DPL-0021] HPWL before          910806.5 u
[INFO DPL-0022] HPWL after           895297.0 u
[INFO DPL-0023] HPWL delta           -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/6-resizer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 10
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
::: %

```

Commands to load placement def in magic in another terminal

Change directory to path containing generated placement def

```

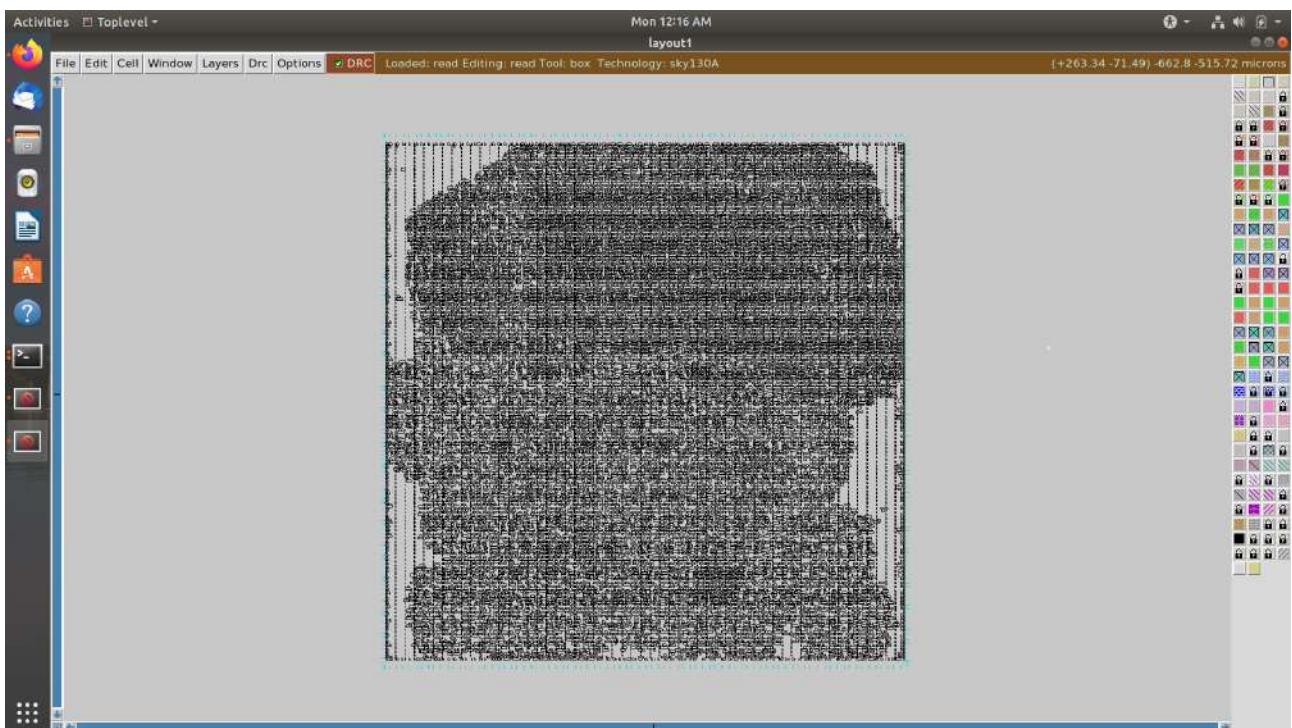
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
24-03_10-03/results/placement/

```

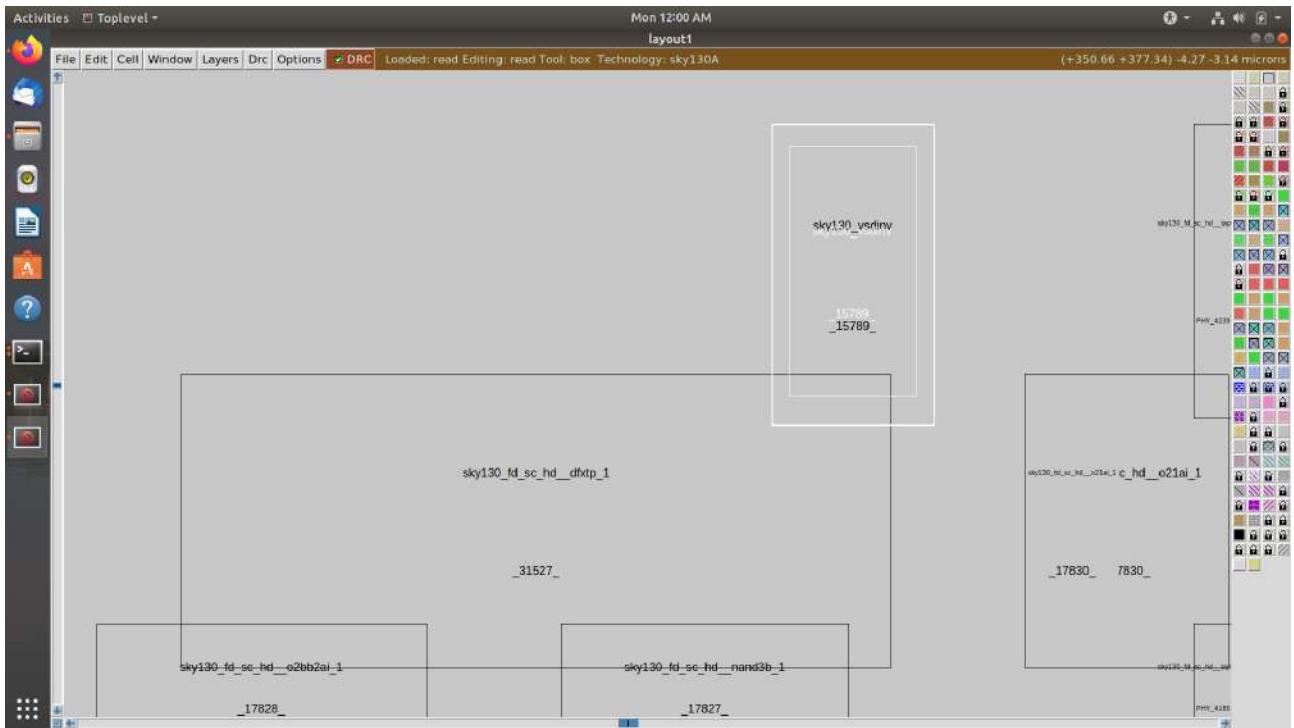
```
# Command to load the placement def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def  
&
```

Screenshot of placement def in magic



Screenshot of custom inverter inserted in placement def with proper abutment

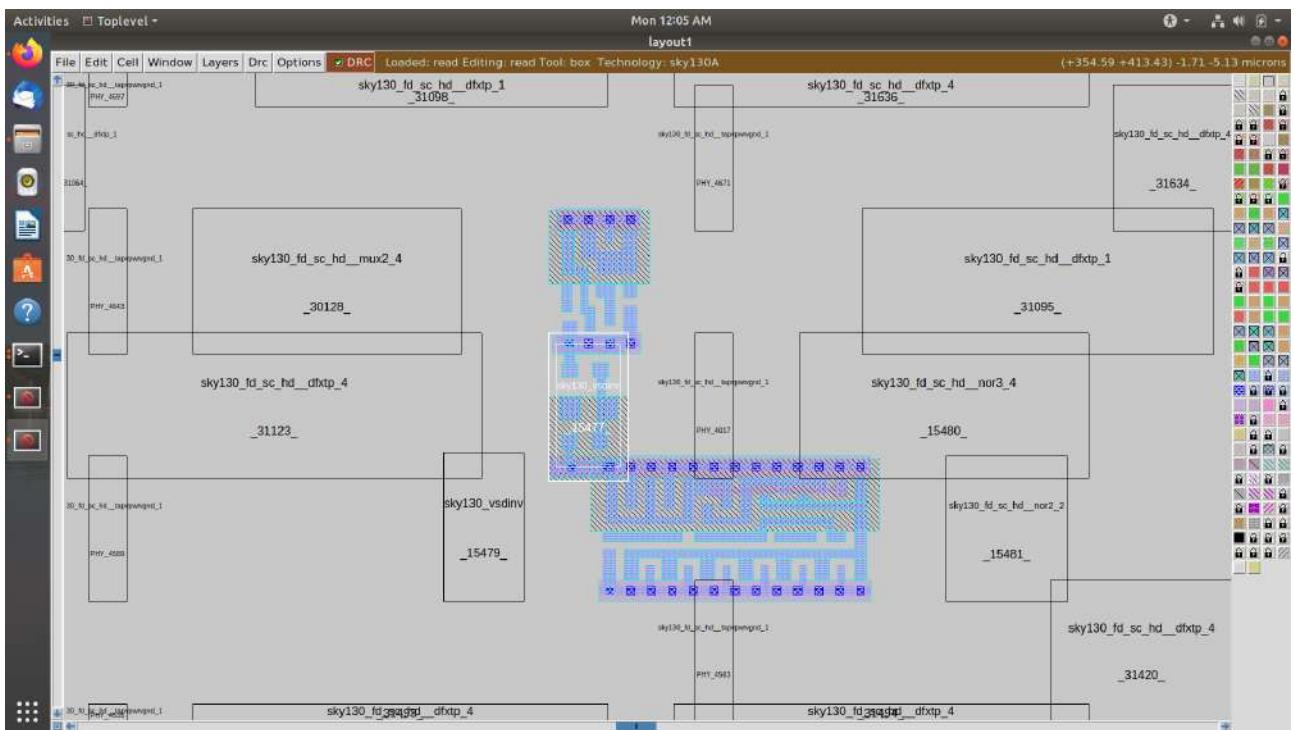
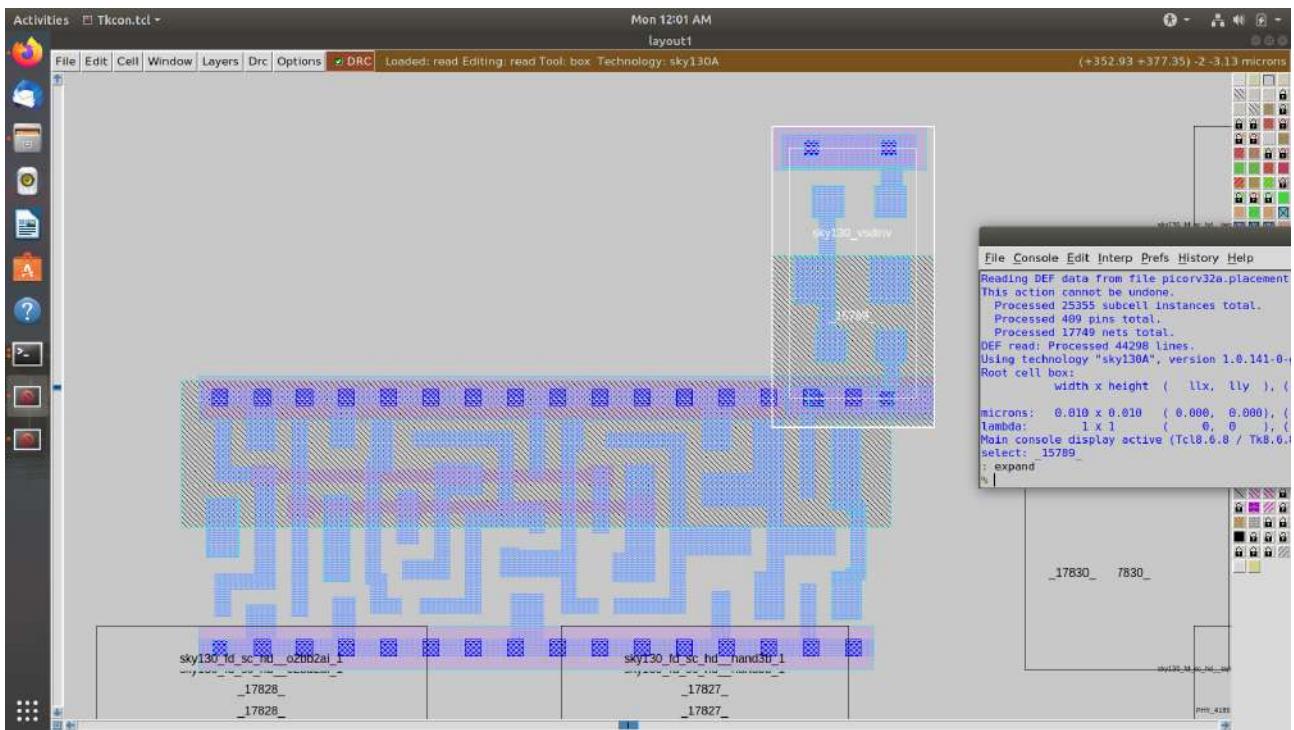


Command for tkcon window to view internal layers of cells

```
# Command to view internal connectivity layers
```

```
expand
```

Abutment of power pins with other cell from library clearly visible



9. Do Post-Synthesis timing analysis with OpenSTA tool.

Since we are having own after improved timing run we are going to do timing analysis on initial run of synthesis which has lots of violations and no parameters were added to improve timing

Commands to invoke the OpenLANE flow include new lef and perform synthesis

Change directory to openlane flow directory

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:vo.21'
```

Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command

```
docker
```

Now that we have entered the OpenLANE flow contained docker sub-system we can invoke the OpenLANE flow in the Interactive mode using the following command

```
./flow.tcl -interactive
```

Now that OpenLANE flow is open we have to input the required packages for proper functionality of the OpenLANE flow

```
package require openlane 0.9
```

Now the OpenLANE flow is ready to run any design and initially we have to prep the design creating some necessary files and directories for running a specific design which in our case is 'picorv32a'

```
prep -design picorv32a
```

```
# Additional commands to include newly added lef to openlane flow
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Now that the design is prepped and ready, we can run synthesis using following command
```

```
run_synthesis
```

Commands run final screenshot

```
Activities Terminal Tue 5:52 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
```

Newly created pre_sta.conf for STA analysis in openlane directory

Newly created `my_base.sdc` for STA analysis in `openlane/designs/picorv32a/src` directory based on the file `openlane/scripts/base.sdc`

```
Activities  M GVim - Tue 5:55 AM my_base.sdc (~Desktop/work/tools/openlane/r/openlane/designs/picorv32a/src) - GVIM1
File Edit Tools Syntax Buffers Window Help
1 set ::env(CLOCK_PORT) cLK
2 set ::env(CLOCK_PERIOD) 24.73
3 #set ::env(SYNTH_DRIVING_CELL) sky130_vsdinv
4 set ::env(SYNTH_DRIVING_CELL) sky130_fd_sc_hd_inv_8
5 set ::env(SYNTH_DRIVING_CELL_PIN) Y
6 set ::env(SYNTH_CAP_LOAD) 17.653
7 set ::env(IO_PCT) 0.2
8 set ::env(SYNTH_MAX_FANOUT) 6
9
10 create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
11 set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
12 set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
13 puts "\[INFO\]: Setting output delay to: $output_delay_value"
14 puts "\[INFO\]: Setting input delay to: $input_delay_value"
15
16 set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
17
18 set clk_idx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
19 #set rst_idx [lsearch [all_inputs] [get_port resetn]]
20 set all_inputs_wo_clk [lreplace [all_inputs] $clk_idx $clk_idx]
21 #set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_idx $rst_idx]
22 set all_inputs_wo_clk_rst $all_inputs_wo_clk
23
24 # correct resetn
```

24,16

Top

```
Activities  M GVim - Tue 5:55 AM my_base.sdc (~Desktop/work/tools/openlane/r/openlane/designs/picorv32a/src) - GVIM1
File Edit Tools Syntax Buffers Window Help
24 # correct resetn
25 set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
26 #set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
27 set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
28
29 # TODO set this as parameter
30 set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
31 set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
32 puts "\[INFO\]: Setting load to: $cap_load"
33 set_load $cap_load [all_outputs]
```

25,16

Bot

Commands to run STA in another terminal

```
# Change directory to openlane
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# Command to invoke OpenSTA tool with script
```

```
sta pre_sta.conf
```

Screenshots of commands run

```
Activities Terminal Tue 6:04 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ sta pre_sta.conf
OpenSTA 2.4.0 ac3479bc24 Copyright (c) 2021, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type `show copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type `show warranty'.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib line 24, default_fanout_load is 0.0.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib line 23, default_fanout_load is 0.0.
[INFO]: Setting output delay to: 4.946000000000001
[INFO]: Setting input delay to: 4.946000000000001
[INFO]: Setting load to: 0.017653
Startpoint: _26669_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _26669_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _26669/_0 (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.00  0.00  cpuregs[0][0] (net)
          0.03  0.00  0.00 ^ _15938/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _15938/_X (sky130_fd_sc_hd_buf_1)
          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _26669/_D (sky130_fd_sc_hd_dfxtp_2)
          0.02  0.00  0.23  data arrival time
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data arrival time
          -0.02 -0.02  0.00  slack (MET)
```

```
Activities Terminal Tue 6:05 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _26669/_0 (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.00  0.00  cpuregs[0][0] (net)
          0.03  0.00  0.00 ^ _15938/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _15938/_X (sky130_fd_sc_hd_buf_1)
          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _26669/_D (sky130_fd_sc_hd_dfxtp_2)
          0.02  0.00  0.23  data arrival time
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data arrival time
          -0.02 -0.02  0.00  slack (MET)
```

```

Activities Terminal - Tue 6:05 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
Startpoint: _27860_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _27762_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
-----
          0.00 0.00 0.00 clock clk (rise edge)
          0.00 0.00 0.00 clock network delay (ideal)
          0.00 0.00 0.00 ^ _27860/_CLK (sky130_fd_sc_hd_dfxtp_2)
          0.10 0.64 0.64 ^ _27860/_Q (sky130_fd_sc_hd_dfxtp_2)
          4   0.01      irq_mask[1] (net)
          0.10 0.00 0.64 ^ _13108/_A (sky130_vsdinv)
          0.13 0.15 0.79 v _13108/_Y (sky130_vsdinv)
          6   0.01      _10510_ (net)
          0.13 0.00 0.79 v _13113/_A1 (sky130_fd_sc_hd_a221o_2)
          0.08 0.65 1.44 v _13113/_X (sky130_fd_sc_hd_a221o_2)
          1   0.00      _10515_ (net)
          0.08 0.00 1.44 v _13132/_A (sky130_fd_sc_hd_or4_2)
          0.21 1.53 2.98 v _13132/_X (sky130_fd_sc_hd_or4_2)
          1   0.00      _10534_ (net)
          0.21 0.00 2.98 v _13160/_A1 (sky130_fd_sc_hd_o2111a_2)
          0.07 0.54 3.52 v _13160/_X (sky130_fd_sc_hd_o2111a_2)
          2   0.00      _10562_ (net)
          0.07 0.00 3.52 v _13161/_C (sky130_fd_sc_hd_or3_2)
          0.17 0.97 4.48 v _13161/_X (sky130_fd_sc_hd_or3_2)
          2   0.00      _10563_ (net)
          0.17 0.00 4.48 v _13164/_A (sky130_fd_sc_hd_or2_2)

```

```

Activities Terminal - Tue 6:08 AM
vsduser@vsduser: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
          0.14 0.68 47.22 v _13750/_X (sky130_fd_sc_hd_or2_2)
          3   0.01      10970_ (net)
          0.14 0.00 47.22 v _13751/_B (sky130_fd_sc_hd_or2_2)
          0.12 0.66 47.88 v _13751/_X (sky130_fd_sc_hd_or2_2)
          2   0.00      10971_ (net)
          0.12 0.00 47.88 v _13754/_B2 (sky130_fd_sc_hd_o221a_2)
          0.07 0.44 48.32 v _13754/_X (sky130_fd_sc_hd_o221a_2)
          1   0.00      03928_ (net)
          0.07 0.00 48.32 v _27762/_D (sky130_fd_sc_hd_dfxtp_2)
          48.32 data arrival time
          0.00 24.73 24.73 clock clk (rise edge)
          0.00 24.73 24.73 clock network delay (ideal)
          0.00 24.73 24.73 clock reconvergence pessimism
          24.73 ^ _27762/_CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.29 24.44 library setup time
          24.44 data required time
          24.44 data required time
          -48.32 data arrival time
          -23.89 slack (VIOLATED)

tns -711.59
wns -23.89
%
```

Since more fanout is causing more delay we can add parameter to reduce fanout and do synthesis again

Commands to include new lef and perform synthesis

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the  
design creating some necessary files and directories for running a specific design which in  
our case is 'picorv32a'
```

```
prep -design picorv32a -tag 25-03_18-52 -overwrite
```

```
# Additional commands to include newly added lef to openlane flow
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Command to set new value for SYNTH_MAX_FANOUT
```

```
set ::env(SYNTH_MAX_FANOUT) 4
```

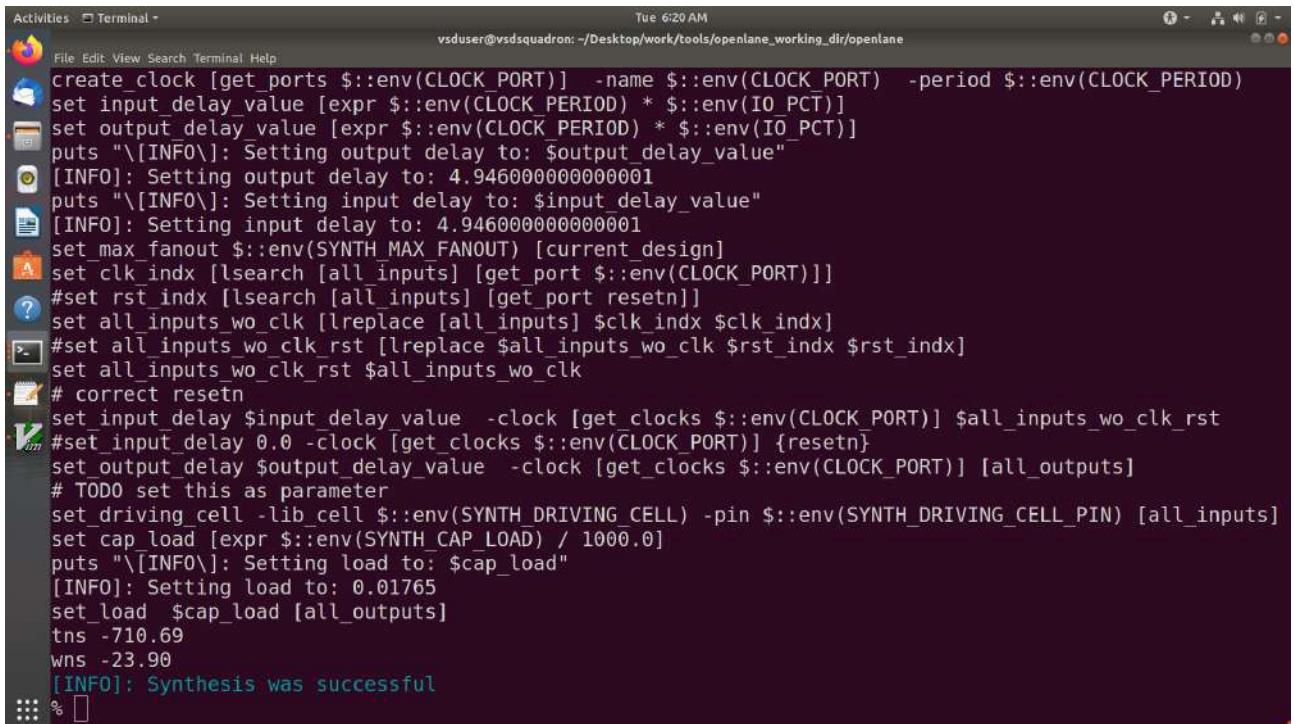
```
# Command to display current value of variable SYNTH_DRIVING_CELL to check whether  
it's the proper cell or not
```

```
echo $::env(SYNTH_DRIVING_CELL)
```

```
# Now that the design is prepped and ready, we can run synthesis using following  
command
```

run_synthesis

Commands run final screenshot



A screenshot of a terminal window titled "Terminal". The window shows a series of commands being run and their corresponding output. The commands relate to setting clock ports, input and output delays, and driving cell parameters. The output includes several "[INFO]" messages indicating the progress of the synthesis process. The terminal window has a dark background with light-colored text.

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -710.69
wns -23.90
[INFO]: Synthesis was successful
```

Commands to run STA in another terminal

```
# Change directory to openlane
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# Command to invoke OpenSTA tool with script
```

```
sta pre_sta.conf
```

Screenshots of commands run

```

Activities Terminal - Tue 6:22 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ sta pre_sta.conf
OpenSTA 2.4.0 ac3479bc24 Copyright (c) 2021, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type `show copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type `show warranty'.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_f
d_sc_hd_slow.lib line 24, default_fanout_load is 0.0.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_f
d_sc_hd_fast.lib line 23, default_fanout_load is 0.0.
[INFO]: Setting output delay to: 4.9460000000000001
[INFO]: Setting input delay to: 4.9460000000000001
[INFO]: Setting load to: 0.017653
Startpoint: _29347_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _29347_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _29347_/Q (sky130_fd_sc_hd_dfxtp_2)
          2   0.00          cpuregs[0][0] (net)
          0.02  0.00  0.10 ^ _17885/_A (sky130_fd_sc_hd_buf_1)

```

```

Activities Terminal - Tue 6:22 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _29347_/Q (sky130_fd_sc_hd_dfxtp_2)
          2   0.00          cpuregs[0][0] (net)
          0.03  0.00  0.18 ^ _17885/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _17885/_X (sky130_fd_sc_hd_buf_1)
          1   0.00          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _29347/_D (sky130_fd_sc_hd_dfxtp_2)
          0.00  0.00  0.00  data arrival time
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data required time
          -0.23 -0.23  0.00  data arrival time
          -0.24 -0.24  0.00  slack (MET)

```

Activities Terminal - Tue 6:22 AM
 vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```

Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00 ^ _29052_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.06  0.58  0.58 v _29052/_Q (sky130_fd_sc_hd_dfxtp_2)
          4   0.01           irq_pending[3] (net)
          0.06  0.00  0.58 v _14460/_A (sky130_vsdinv)
          0.19  0.17  0.75 ^ _14460/_Y (sky130_vsdinv)
          3   0.01           _11622_ (net)
          0.19  0.00  0.75 ^ _14461/_B2 (sky130_fd_sc_hd_o22ai_2)
          0.09  0.14  0.89 v _14461/_Y (sky130_fd_sc_hd_o22ai_2)
          1   0.00           _11623_ (net)
          0.09  0.00  0.89 v _14462/_C1 (sky130_fd_sc_hd_a221o_2)
          0.08  0.55  1.44 v _14462/_X (sky130_fd_sc_hd_a221o_2)
          1   0.00           _11624_ (net)
          0.08  0.00  1.44 v _14481/_A (sky130_fd_sc_hd_or4_2)
          0.21  1.53  2.97 v _14481/_X (sky130_fd_sc_hd_or4_2)
          1   0.00           _11643_ (net)
          0.21  0.00  2.97 v _14509/_A1 (sky130_fd_sc_hd_o2111a_2)
          0.07  0.54  3.51 v _14509/_X (sky130_fd_sc_hd_o2111a_2)
          2   0.00
  
```

Activities Terminal - Tue 6:23 AM
 vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```

          0.14  0.68  47.23 v _15226/_X (sky130_fd_sc_hd_or2_2)
          3   0.01           _12208_ (net)
          0.14  0.00  47.23 v _15227/_B (sky130_fd_sc_hd_or2_2)
          0.12  0.66  47.89 v _15227/_X (sky130_fd_sc_hd_or2_2)
          2   0.00           _12209_ (net)
          0.12  0.00  47.89 v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
          0.07  0.44  48.33 v _15230/_X (sky130_fd_sc_hd_o221a_2)
          1   0.00           _03928_ (net)
          0.07  0.00  48.33 v _30440/_D (sky130_fd_sc_hd_dfxtp_2)
          48.33 data arrival time
          0.00  24.73  24.73  clock clk (rise edge)
          0.00  24.73  24.73  clock network delay (ideal)
          0.00  24.73  24.73  clock reconvergence pessimism
          24.73 ^ _30440_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.29 24.44  24.44  library setup time
          24.44 24.44  24.44  data required time
          24.44 data required time
          -48.33 data arrival time
  ----- -23.90 slack (VIOLATED)

tns -710.69
wns -23.90
  
```

10. Make timing ECO fixes to remove all violations.

OR gate of drive strength 2 is driving 4 fanouts

Activities Terminal Tue 6:55 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

		0.19	0.00	0.75	^ _14461 /B2 (sky130_fd_sc_hd_o22ai_2)
1	0.00	0.09	0.14	0.89 v	_14461 /Y (sky130_fd_sc_hd_o22ai_2)
					11623 (net)
		0.09	0.00	0.89 v	_14462 /C1 (sky130_fd_sc_hd_a22lo_2)
1	0.00	0.08	0.55	1.44 v	_14462 /X (sky130_fd_sc_hd_a22lo_2)
					11624 (net)
		0.08	0.00	1.44 v	_14481 /A (sky130_fd_sc_hd_or4_2)
1	0.00	0.21	1.53	2.97 v	_14481 /X (sky130_fd_sc_hd_or4_2)
					11643 (net)
		0.21	0.00	2.97 v	_14509 /A1 (sky130_fd_sc_hd_o2111a_2)
2	0.00	0.07	0.54	3.51 v	_14509 /X (sky130_fd_sc_hd_o2111a_2)
					11671 (net)
		0.07	0.00	3.51 v	_14510 /C (sky130_fd_sc_hd_or3_2)
4	0.01	0.21	1.04	4.55 v	_14510 /X (sky130_fd_sc_hd_or3_2)
					11672 (net)
		0.21	0.00	4.55 v	_14513 /A (sky130_fd_sc_hd_or2_2)
2	0.00	0.11	0.71	5.26 v	_14513 /X (sky130_fd_sc_hd_or2_2)
					11674 (net)
		0.11	0.00	5.26 v	_14514 /C (sky130_fd_sc_hd_or3_2)
4	0.01	0.20	1.03	6.29 v	_14514 /X (sky130_fd_sc_hd_or3_2)
					11675 (net)
		0.20	0.00	6.29 v	_15166 /B (sky130_fd_sc_hd_or2_2)
2	0.00	0.11	0.67	6.96 v	_15166 /X (sky130_fd_sc_hd_or2_2)
					12148 (net)
		0.11	0.00	6.96 v	_15167 /C (sky130_fd_sc_hd_or3_2)
2	0.00	0.17	0.98	7.94 v	_15167 /X (sky130_fd_sc_hd_or3_2)
					12149 (net)
		0.17	0.00	7.94 v	_15168 /B (sky130_fd_sc_hd_or2_2)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

report_net -connections _11672_

Checking command syntax

help replace_cell

Replacing cell

replace_cell _14510_ sky130_fd_sc_hd_or3_4

Generating custom timing report

```
report_checks -fields {net cap slew input_pins} -digits 4
```

Result - slack reduced

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
----- [-23.90 slack (VIOLATED)]
tns -710.69
wns -23.90
% report_net -connections _11672_
Net _11672_
Driver pins
_14510 /X output (sky130_fd_sc_hd_or3_2)
Load pins
_14513 /A input (sky130_fd_sc_hd_or2_2)
_15505 /B input (sky130_fd_sc_hd_or2_2)
_18231 /A input (sky130_fd_sc_hd_buf_1)
_18326 /B input (sky130_fd_sc_hd_nand2_2)

% help replace_cell
replace_cell instance lib_cell
% replace_cell _14510_ sky130_fd_sc_hd_or3_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Fanout Cap Slew Delay Time Description
```

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Fanout Cap Slew Delay Time Description
-----
```

Fanout	Cap	Slew	Delay	Time	Description
		0.0000	0.0000	0.0000	clock clk (rise edge)
		0.0000	0.0000	0.0000	clock network delay (ideal)
		0.0000	0.0000	0.0000 ^	_29052_ /CLK (sky130_fd_sc_hd_dfxtp_2)
		0.0572	0.5830	0.5830 v	_29052_ /Q (sky130_fd_sc_hd_dfxtp_2)
					irq_pending[3] (net)
4	0.0067	0.0572	0.0000	0.5830 v	_14460_ /A (sky130_vsdinv)
		0.1856	0.1667	0.7497 ^	_14460_ /Y (sky130_vsdinv)
					11622 (net)
3	0.0138	0.1856	0.0000	0.7497 ^	_14461_ /B2 (sky130_fd_sc_hd_o22ai_2)
		0.0878	0.1436	0.8933 v	_14461_ /Y (sky130_fd_sc_hd_o22ai_2)
1	0.0021	0.0878	0.0000	0.8933 v	_14462_ /C1 (sky130_fd_sc_hd_a221o_2)
		0.0784	0.5469	1.4402 v	_14462_ /X (sky130_fd_sc_hd_a221o_2)
1	0.0013	0.0784	0.0000	1.4402 v	
		0.2106	1.5344	2.9746 v	_14481_ /A (sky130_fd_sc_hd_or4_2)
1	0.0024	0.2106	0.0000	2.9746 v	_14481_ /X (sky130_fd_sc_hd_or4_2)
		0.0792	0.5466	3.5212 v	_11643_ (net)
2	0.0044				_14509_ /A1 (sky130_fd_sc_hd_o2111a_2)
					14509 /X (sky130_fd_sc_hd_o2111a_2)
					11671 (net)

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

Tue 9:42 AM

3	0.0138	0.1856	0.0000	0.7497	^ _11622_ (net)
		0.0878	0.1436	0.8933	v _14461/_B2 (sky130_fd_sc_hd_o22ai_2)
1	0.0021	0.0878	0.0000	0.8933	v _14461/_Y (sky130_fd_sc_hd_o22ai_2)
		0.0784	0.5469	1.4402	v _11623_ (net)
1	0.0013	0.0784	0.0000	1.4402	v _14462/_C1 (sky130_fd_sc_hd_a221o_2)
		0.2106	1.5344	2.9746	v _14462/_X (sky130_fd_sc_hd_a221o_2)
1	0.0024	0.2106	0.0000	2.9746	v _11624_ (net)
		0.0792	0.5466	3.5212	v _14481/_A (sky130_fd_sc_hd_or4_2)
2	0.0044	0.0792	0.0000	3.5212	v _14481/_X (sky130_fd_sc_hd_or4_2)
		0.1349	0.6755	4.1967	v _11643_ (net)
4	0.0089	0.1349	0.0000	4.1967	v _14509/_A1 (sky130_fd_sc_hd_o2111a_2)
		0.1121	0.6770	4.8737	v _14509/_X (sky130_fd_sc_hd_o2111a_2)
2	0.0025	0.1121	0.0000	4.8737	v _11671_ (net)
		0.1967	1.0321	5.9057	v _14514/_C (sky130_fd_sc_hd_or3_2)
4	0.0070	0.1967	0.0000	5.9057	v _14514/_X (sky130_fd_sc_hd_or3_2)
		0.1148	0.6684	6.5742	v _11675_ (net)
2	0.0032	0.1148	0.0000	6.5742	v _15166/_B (sky130_fd_sc_hd_or2_2)
		0.1692	0.9831	7.5573	v _15166/_X (sky130_fd_sc_hd_or2_2)
2	0.0025	0.0000	0.0000	7.5573	v _12148_ (net)
		0.0000	0.0000	7.5573	v _15167/_C (sky130_fd_sc_hd_or3_2)
		0.0000	0.0000	7.5573	v _15167/_X (sky130_fd_sc_hd_or3_2)
		0.0000	0.0000	7.5573	v _12149_ (net)

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

Tue 7:07 AM

2	0.0035	0.1162	0.0000	46.1648	v _12207_ (net)
		0.1421	0.6813	46.8462	v _15226/_B (sky130_fd_sc_hd_or2_2)
3	0.0079	0.1421	0.0000	46.8462	v _15226/_X (sky130_fd_sc_hd_or2_2)
		0.1228	0.6610	47.5072	v _12208_ (net)
2	0.0044	0.1228	0.0000	47.5072	v _15227/_B (sky130_fd_sc_hd_or2_2)
		0.0713	0.4381	47.9453	v _15227/_X (sky130_fd_sc_hd_or2_2)
1	0.0016	0.0713	0.0000	47.9453	v _12209_ (net)
		0.0000	24.7300	24.7300	v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
		0.0000	24.7300	24.7300	v _15230/_X (sky130_fd_sc_hd_o221a_2)
		0.0000	24.7300	24.7300	v _03928_ (net)
		0.0000	24.7300	24.7300	v _30440/_D (sky130_fd_sc_hd_dfxtip_2)
		0.0000	24.7300	24.7300	v data arrival time
		0.0000	24.7300	24.7300	v clock clk (rise edge)
		0.0000	24.7300	24.7300	v clock network delay (ideal)
		0.0000	24.7300	24.7300	v clock reconvergence pessimism
		24.7300	24.7300	24.7300	v ^ _30440/_CLK (sky130_fd_sc_hd_dfxtip_2)
		-0.2939	24.4361	24.4361	v library setup time
		-0.2939	24.4361	24.4361	v data required time
		24.4361	24.4361	24.4361	v data arrival time
		24.4361	24.4361	24.4361	v slack (VIOLATED)
		-47.9453	-47.9453	-47.9453	v -23.5092 slack (VIOLATED)

OR gate of drive strength 2 is driving 4 fanouts

Activities Terminal Tue 9:46 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

		0.2106	1.5344	2.9746 v	_14481/_X (sky130_fd_sc_hd_or4_2)
1	0.0024				11643 (net)
		0.2106	0.0000	2.9746 v	_14509/_A1 (sky130_fd_sc_hd_o2111a_2)
		0.0792	0.5466	3.5212 v	_14509/_X (sky130_fd_sc_hd_o2111a_2)
2	0.0044				11671 (net)
		0.0792	0.0000	3.5212 v	_14510/_C (sky130_fd_sc_hd_or3_4)
		0.1349	0.6755	4.1967 v	_14510/_X (sky130_fd_sc_hd_or3_4)
4	0.0089				11672 (net)
		0.1349	0.0000	4.1967 v	_14513/_A (sky130_fd_sc_hd_or2_2)
		0.1121	0.6770	4.8737 v	_14513/_X (sky130_fd_sc_hd_or2_2)
2	0.0025				11674 (net)
		0.1121	0.0000	4.8737 v	_14514/_C (sky130_fd_sc_hd_or3_2)
		0.1967	1.0321	5.9057 v	_14514/_X (sky130_fd_sc_hd_or3_2)
4	0.0070				11675 (net)
		0.1967	0.0000	5.9057 v	_15166/_B (sky130_fd_sc_hd_or2_2)
		0.1148	0.6684	6.5742 v	_15166/_X (sky130_fd_sc_hd_or2_2)
2	0.0032				12148 (net)
		0.1148	0.0000	6.5742 v	_15167/_C (sky130_fd_sc_hd_or3_2)
		0.1692	0.9831	7.5573 v	_15167/_X (sky130_fd_sc_hd_or3_2)
2	0.0035				12149 (net)
		0.1692	0.0000	7.5573 v	_15168/_B (sky130_fd_sc_hd_or2_2)
		0.1422	0.7026	8.2599 v	_15168/_X (sky130_fd_sc_hd_or2_2)
3	0.0079				12150 (net)
		0.1422	0.0000	8.2599 v	_15169/_B (sky130_fd_sc_hd_or2_2)
		0.1162	0.6492	8.9091 v	_15169/_X (sky130_fd_sc_hd_or2_2)
2	0.0035				12151 (net)
		0.1162	0.0000	8.9091 v	_15170/_B (sky130_fd_sc_hd_or2_2)
		0.1422	0.6817	9.5904 v	_15170/_X (sky130_fd_sc_hd_or2_2)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

```
# Reports all the connections to a net
```

```
report_net -connections _11675_
```

```
# Replacing cell
```

```
replace_cell _14514_ sky130_fd_sc_hd_or3_4
```

```
# Generating custom timing report
```

```
report_checks -fields {net cap slew input_pins} -digits 4
```

Result - slack reduced

```

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Tue 9:49 AM
-47.9453  data arrival time
-----
-23.5092  slack (VIOLATED)

% report_net -connections _11675_
Net _11675_
Driver pins
_14514/_X output (sky130_fd_sc_hd_or3_2)
Load pins
_14515/_A input (sky130_vsdinv)
_14521/_B2 input (sky130_fd_sc_hd_o221a_2)
_14662/_B input (sky130_fd_sc_hd_or2_2)
_15166/_B input (sky130_fd_sc_hd_or2_2)

% replace_cell _14514_ sky130_fd_sc_hd_or3_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout      Cap      Slew      Delay      Time      Description
-----      -----      -----      -----      -----      -----
          0.0000  0.0000  0.0000  clock clk (rise edge)
          0.0000  0.0000  slack network delay (ideal)

```

Tue 9:50 AM						
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane						
Fanout	Cap	Slew	Delay	Time	Description	
1	0.0013				11624_ (net)	
		0.0784	0.0000	1.4402	v 14481/_A (sky130_fd_sc_hd_or4_2)	
		0.2106	1.5344	2.9746	v 14481/_X (sky130_fd_sc_hd_or4_2)	
1	0.0024				11643_ (net)	
		0.2106	0.0000	2.9746	v 14509/_A1 (sky130_fd_sc_hd_o2111a_2)	
		0.0792	0.5466	3.5212	v 14509/_X (sky130_fd_sc_hd_o2111a_2)	
2	0.0044				11671_ (net)	
		0.0792	0.0000	3.5212	v 14510/_C (sky130_fd_sc_hd_or3_4)	
		0.1349	0.6755	4.1967	v 14510/_X (sky130_fd_sc_hd_or3_4)	
4	0.0089				11672_ (net)	
		0.1349	0.0000	4.1967	v 14513/_A (sky130_fd_sc_hd_or2_2)	
		0.1182	0.6880	4.8847	v 14513/_X (sky130_fd_sc_hd_or2_2)	
2	0.0034				11674_ (net)	
		0.1182	0.0000	4.8847	v 14514/_C (sky130_fd_sc_hd_or3_4)	
		0.1290	0.6794	5.5641	v 14514/_X (sky130_fd_sc_hd_or3_4)	
4	0.0070				11675_ (net)	
		0.1290	0.0000	5.5641	v 15166/_B (sky130_fd_sc_hd_or2_2)	
		0.1148	0.6414	6.2055	v 15166/_X (sky130_fd_sc_hd_or2_2)	
2	0.0032				12148_ (net)	
		0.1148	0.0000	6.2055	v 15167/_C (sky130_fd_sc_hd_or3_2)	
		0.1692	0.9831	7.1886	v 15167/_X (sky130_fd_sc_hd_or3_2)	
2	0.0035				12149_ (net)	
		0.1692	0.0000	7.1886	v 15168/_B (sky130_fd_sc_hd_or2_2)	
		0.1422	0.7026	7.8912	v 15168/_X (sky130_fd_sc_hd_or2_2)	
3	0.0079				12150_ (net)	
		0.1422	0.0000	7.8912	v 15169/_B (sky130_fd_sc_hd_or2_2)	
		0.1162	0.6492	8.5404	v 15169/_X (sky130_fd_sc_hd_or2_2)	
2	0.0025				12151_ (net)	

```

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
2 0.0035
    0.1162 0.0000 45.7962 v _12207_(net)
    0.1421 0.6813 46.4775 v _15226/_B(sky130_fd_sc_hd_or2_2)
    0.1421 0.0000 46.4775 v _15226/_X(sky130_fd_sc_hd_or2_2)
    0.1228 0.6610 47.1385 v _12208_(net)
    0.1228 0.0000 47.1385 v _15227/_B(sky130_fd_sc_hd_or2_2)
    0.0713 0.4381 47.5766 v _15227/_X(sky130_fd_sc_hd_o221a_2)
    0.0713 0.0000 47.5766 v _03928_(net)
    0.0713 0.0000 47.5766 v _30440/_D(sky130_fd_sc_hd_dfxtpl_2)
                                         data arrival time
                                         0.0000 24.7300 24.7300 clock clk (rise edge)
                                         0.0000 24.7300 24.7300 clock network delay (ideal)
                                         0.0000 24.7300 24.7300 clock reconvergence pessimism
                                         24.7300 ^ _30440/_CLK(sky130_fd_sc_hd_dfxtpl_2)
                                         -0.2939 24.4361 library setup time
                                         24.4361 data required time
                                         24.4361 24.4361 data arrival time
                                         -----
                                         24.4361 data required time
                                         -47.5766 data arrival time
                                         -----
                                         -23.1405 slack (VIOLATED)

```

OR gate of drive strength 2 driving OA gate has more delay

```

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Fanout Cap Slew Delay Time Description
-----+
                                         0.0000 0.0000 0.0000 clock clk (rise edge)
                                         0.0000 0.0000 0.0000 clock network delay (ideal)
                                         0.0572 0.5830 0.5830 v _29052/_Q(sky130_fd_sc_hd_dfxtpl_2)
                                         0.0572 0.0000 ^ _29052/_CLK(sky130_fd_sc_hd_dfxtpl_2)
                                         0.1856 0.1667 0.7497 ^ _14460/_Y(sky130_vsdinv)
                                         0.1856 0.0000 0.7497 ^ _14461/_B2(sky130_fd_sc_hd_o22ai_2)
                                         0.0878 0.1436 0.8933 v _14461/_Y(sky130_fd_sc_hd_o22ai_2)
                                         0.0878 0.0000 0.8933 v _14462/_C1(sky130_fd_sc_hd_a221o_2)
                                         0.0784 0.5469 1.4402 v _14462/_X(sky130_fd_sc_hd_a221o_2)
                                         0.0784 0.0000 1.4402 v _14481/_A(sky130_fd_sc_hd_or4_2)
                                         0.2106 1.5344 2.9746 v _14481/_X(sky130_fd_sc_hd_or4_2)
                                         0.2106 0.0000 2.9746 v _11643_(net)
                                         0.0792 0.5466 3.5212 v _14509/_A1(sky130_fd_sc_hd_o2111a_2)
                                         0.0792 0.0000 3.5212 v _14509/_X(sky130_fd_sc_hd_o2111a_2)
                                         0.1349 0.6755 4.1967 v _11671_(net)
                                         0.1349 0.0000 4.1967 v _14510/_C(sky130_fd_sc_hd_or3_4)
                                         0.1182 0.6880 4.8847 v _14510/_X(sky130_fd_sc_hd_or3_4)
                                         0.1182 0.0000 4.8847 v _11672_(net)
                                         0.1349 0.0000 4.1967 v _14513/_A(sky130_fd_sc_hd_or2_2)
                                         0.1182 0.0000 4.8847 v _14513/_X(sky130_fd_sc_hd_or2_2)
                                         0.1182 0.0000 4.8847 v _11674_(net)

```

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

```
report_net -connections _11643_
```

```
# Replacing cell
```

```
replace_cell _14481_ sky130_fd_sc_hd__or4_4
```

```
# Generating custom timing report
```

```
report_checks -fields {net cap slew input_pins} -digits 4
```

Result - slack reduced

```

Activities Terminal - Tue 10:29 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
-47.5766 data arrival time
-----  

-23.1405 slack (VIOLATED)

% report_net -connections _11643_
Net _11643_
Driver pins
_14481 /X output (sky130_fd_sc_hd_or4_2)
Load pins
_14509 /A1 input (sky130_fd_sc_hd_o2111a_2)

% replace_cell _14481_ sky130_fd_sc_hd_or4_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29043_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
-----  

          0.0000 0.0000 0.0000 clock clk (rise edge)
          0.0000 0.0000 0.0000 clock network delay (ideal)
          0.0000 0.0000 0.0000 ^ _29043/_CLK (sky130_fd_sc_hd_dfxtp_2)
          0.0581 0.5838 0.5838 v _29043/_Q (sky130_fd_sc_hd_dfxtp_2)
          1 0.0060
-----  


```

```

Activities Terminal - Tue 10:29 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
2 0.0035
          0.1162 0.0000 45.7918 v _12207_(net)
          0.1421 0.6813 46.4731 v _15226/_B (sky130_fd_sc_hd_or2_2)
          0.1421 0.0000 46.4731 v _15226/_X (sky130_fd_sc_hd_or2_2)
          0.1228 0.6610 47.1341 v _12208_(net)
          0.1228 0.0000 47.1341 v _15227/_B (sky130_fd_sc_hd_or2_2)
          0.1228 0.0000 47.1341 v _15227/_X (sky130_fd_sc_hd_or2_2)
          0.0713 0.4381 47.5723 v _12209_(net)
          0.0713 0.0000 47.5723 v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
          0.0713 0.0000 47.5723 v _15230/_X (sky130_fd_sc_hd_o221a_2)
          0.0713 0.0000 47.5723 v _03928_(net)
          0.0713 0.0000 47.5723 v _30440/_D (sky130_fd_sc_hd_dfxtp_2)
          0.0713 0.0000 47.5723 v data arrival time
-----  

          0.0000 24.7300 24.7300 clock clk (rise edge)
          0.0000 24.7300 24.7300 clock network delay (ideal)
          0.0000 24.7300 24.7300 clock reconvergence pessimism
          24.7300 ^ _30440/_CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.2939 24.4361 library setup time
          24.4361 data required time
          24.4361 data arrival time
-----  

          -23.1362 slack (VIOLATED)
-----  


```

OR gate of drive strength 2 driving OA gate has more delay

Activities Terminal Tue 10:32 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

				irq_pending[12] (net)
4	0.0069	0.0581	0.0000	0.5838 v _14484 /A (sky130_vsdinv)
		0.1864	0.1676	0.7515 ^ _14484 /Y (sky130_vsdinv)
3	0.0139	0.1864	0.0000	11646 (net)
		0.0878	0.1674	0.7515 ^ _14486 /A2 (sky130_fd_sc_hd_o22ai_2)
1	0.0021	0.0878	0.0000	0.9189 v _14486 /Y (sky130_fd_sc_hd_o22ai_2)
		0.0784	0.5469	11648 (net)
1	0.0013	0.0784	0.0000	1.4658 v _14487 /C1 (sky130_fd_sc_hd_a22lo_2)
		0.2092	1.5317	11649 (net)
1	0.0023	0.2092	0.0000	2.9975 v _14506 /A (sky130_fd_sc_hd_or4_2)
		0.0792	0.5193	11668 (net)
2	0.0044	0.0792	0.0000	3.5168 v _14509 /A2 (sky130_fd_sc_hd_o2111a_2)
		0.1349	0.6755	11671 (net)
4	0.0089	0.1349	0.0000	3.5168 v _14510 /C (sky130_fd_sc_hd_or3_4)
		0.1182	0.6880	4.1923 v _14510 /X (sky130_fd_sc_hd_or3_4)
2	0.0034	0.1182	0.0000	11672 (net)
		0.1290	0.6794	4.8803 v _14513 /A (sky130_fd_sc_hd_or2_2)
4	0.0070	0.1290	0.0000	4.8803 v _14513 /X (sky130_fd_sc_hd_or2_2)
		0.1148	0.6414	11674 (net)
2	0.0022	0.1148	0.0000	5.5597 v _14514 /C (sky130_fd_sc_hd_or3_4)
		0.1290	0.6794	5.5597 v _14514 /X (sky130_fd_sc_hd_or3_4)
4	0.0070	0.1290	0.0000	11675 (net)
		0.1148	0.6414	6.2011 v _15166 /B (sky130_fd_sc_hd_or2_2)
2	0.0022	0.1148	0.0000	6.2011 v _15166 /X (sky130_fd_sc_hd_or2_2)
		0.1290	0.6794	11676 (net)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

report_net -connections _11668_

Replacing cell

replace_cell _14506_ sky130_fd_sc_hd_or4_4

Generating custom timing report

report_checks -fields {net cap slew input_pins} -digits 4

Result - slack reduced

```

Activities Terminal - Tue 10:36 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
-47.5723  data arrival time
-----  

-23.1362  slack (VIOLATED)

% report_net -connections _11668_
Net _11668
Driver pins
_14506 /X output (sky130_fd_sc_hd_or4_2)
Load pins
_14509 /A2 input (sky130_fd_sc_hd_o2111a_2)

% replace_cell _14506_ sky130_fd_sc_hd_or4_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout      Cap      Slew      Delay      Time      Description
-----  

          0.0000  0.0000  0.0000  clock clk (rise edge)
          0.0000  0.0000  0.0000  clock network delay (ideal)
          0.0000  0.0000  0.0000 ^ _29052 /CLK (sky130_fd_sc_hd_dfxtp_2)
          0.0572  0.5830  0.5830 v _29052 /Q (sky130_fd_sc_hd_dfxtp_2)
           0.0067  


```

```

Activities Terminal - Tue 10:37 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
2  0.0035
          0.1162  0.0000  45.2729 v _12207_ (net)
          0.1421  0.6813  45.9542 v _15226 /B (sky130_fd_sc_hd_or2_2)
          0.1421  0.0000  45.9542 v _15226 /X (sky130_fd_sc_hd_or2_2)
          0.1228  0.6610  46.6153 v _12208_ (net)
          0.1228  0.0000  46.6153 v _15227 /B (sky130_fd_sc_hd_or2_2)
          0.1228  0.0000  46.6153 v _15227 /X (sky130_fd_sc_hd_or2_2)
          0.0713  0.4381  47.0534 v _12209_ (net)
          0.0713  0.0000  47.0534 v _15230 /B2 (sky130_fd_sc_hd_o221a_2)
          0.0713  0.0000  47.0534 v _15230 /X (sky130_fd_sc_hd_o221a_2)
          0.0713  0.0000  47.0534 v _03928_ (net)
          0.0713  0.0000  47.0534 v _30440 /D (sky130_fd_sc_hd_dfxtp_2)
          0.0713  0.0000  47.0534 data arrival time
          0.0000  24.7300  24.7300  clock clk (rise edge)
          0.0000  24.7300  24.7300  clock network delay (ideal)
          0.0000  24.7300  24.7300  clock reconvergence pessimism
          0.0000  24.7300 ^ _30440 /CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.2939  24.4361  library setup time
          24.4361  data required time
          24.4361  data arrival time
-----  

-22.6173  slack (VIOLATED)

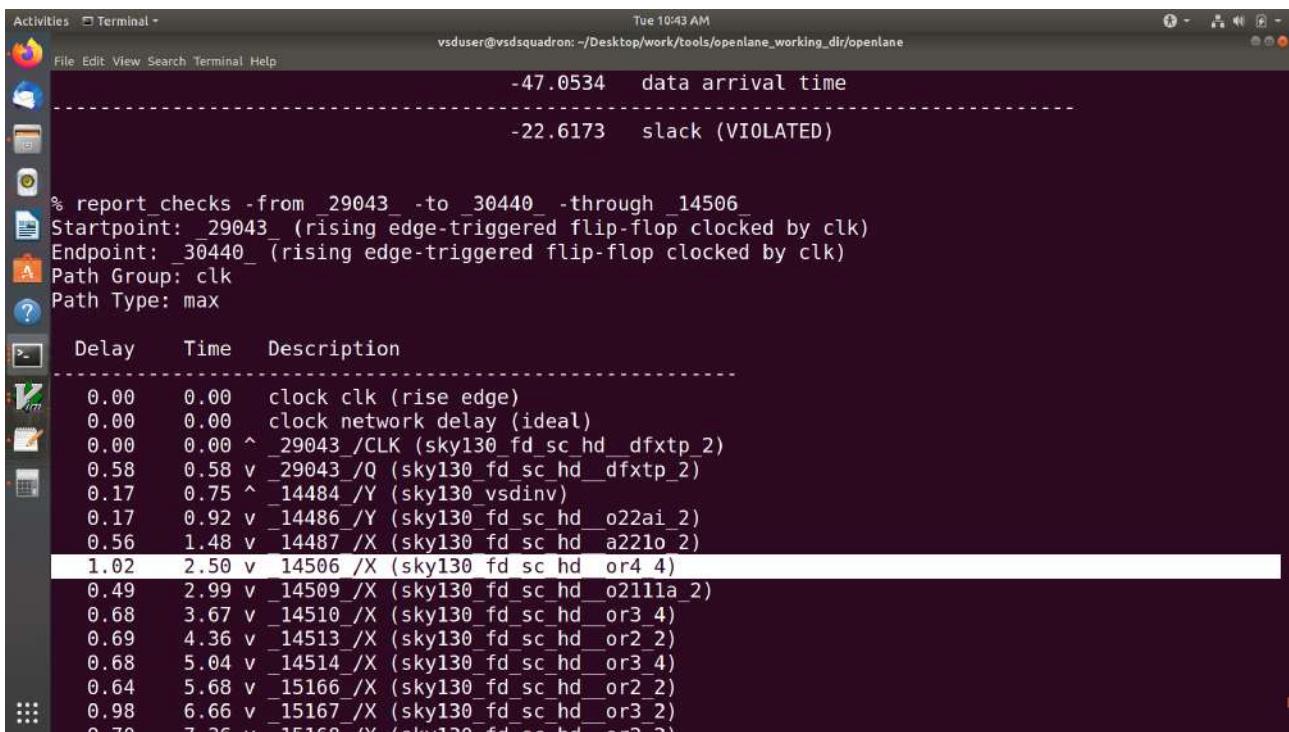
```

Commands to verify instance _14506_ is replaced with sky130_fd_sc_hd_or4_4

Generating custom timing report

report_checks -from _29043_ -to _30440_ -through _14506_

Screenshot of replaced instance



The screenshot shows a terminal window with the following output:

```
Tue 10:43 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
-47.0534  data arrival time
-----
-22.6173  slack (VIOLATED)

% report_checks -from 29043 -to 30440 -through 14506
Startpoint: 29043 (rising edge-triggered flip-flop clocked by clk)
Endpoint: 30440 (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Delay      Time      Description
-----
0.00      0.00      clock clk (rise edge)
0.00      0.00      clock network delay (ideal)
0.00      0.00 ^ 29043 /CLK (sky130_fd_sc_hd_dfxtpl_2)
0.58      0.58 v 29043 /Q (sky130_fd_sc_hd_dfxtpl_2)
0.17      0.75 ^ 14484 /Y (sky130_vsdinv)
0.17      0.92 v 14486 /Y (sky130_fd_sc_hd_o22ai_2)
0.56      1.48 v 14487 /X (sky130_fd_sc_hd_a22lo_2)
1.02      2.50 v 14506 /X (sky130_fd_sc_hd_or4_4)
0.49      2.99 v 14509 /X (sky130_fd_sc_hd_o2111a_2)
0.68      3.67 v 14510 /X (sky130_fd_sc_hd_or3_4)
0.69      4.36 v 14513 /X (sky130_fd_sc_hd_or2_2)
0.68      5.04 v 14514 /X (sky130_fd_sc_hd_or3_4)
0.64      5.68 v 15166 /X (sky130_fd_sc_hd_or2_2)
0.98      6.66 v 15167 /X (sky130_fd_sc_hd_or3_2)
0.70      7.26 v 15168 /X (sky130_fd_sc_hd_or2_2)
```

We started ECO fixes at wns -23.9000 and now we stand at wns -22.6173 we reduced around 1.2827 ns of violation

11. Replace the old netlist with the new netlist generated after timing ECO fix and implement the floorplan, placement and cts.

Now to insert this updated netlist to PnR flow and we can use write_verilog and overwrite the synthesis netlist but before that we are going to make a copy of the old old netlist

Commands to make copy of netlist

```
# Change from home directory to synthesis results directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
25-03_18-52/results/synthesis/
```

```
# List contents of the directory
```

```
ls
```

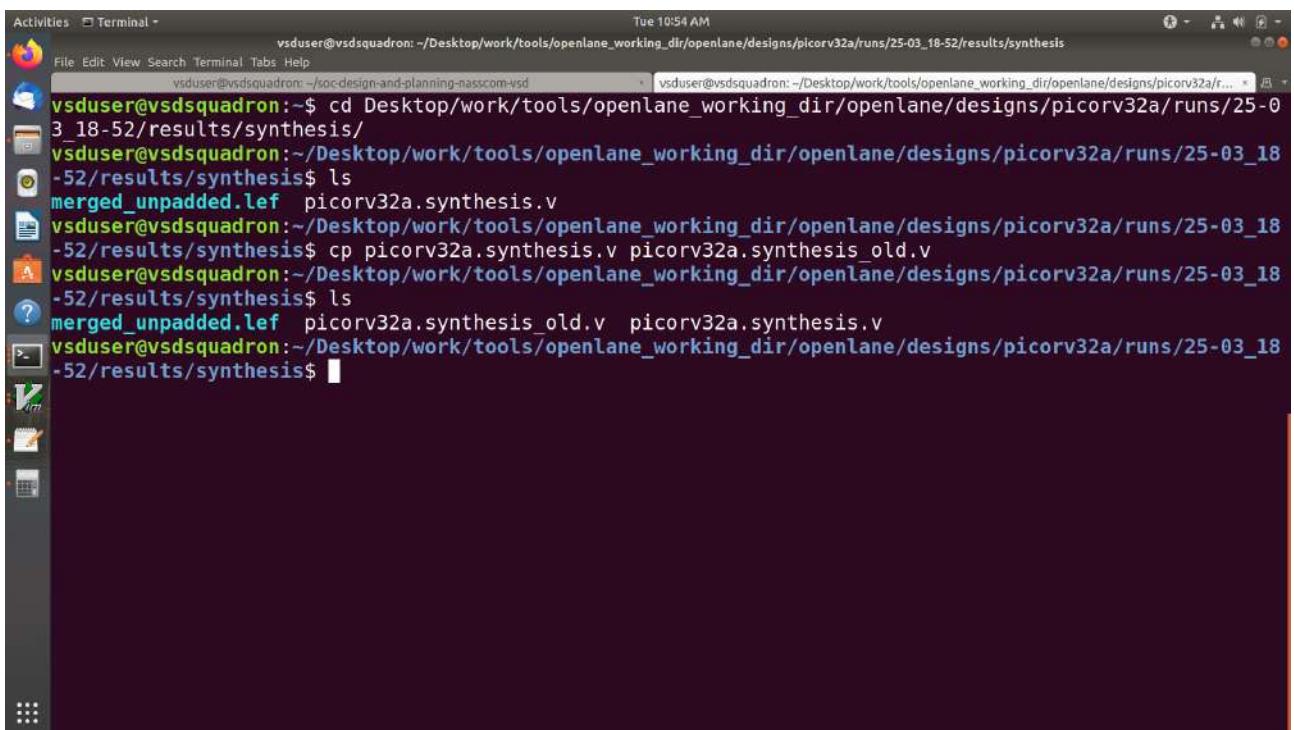
```
# Copy and rename the netlist
```

```
cp picorv32a.synthesis.v picorv32a.synthesis_old.v
```

```
# List contents of the directory
```

```
ls
```

Screenshot of commands run



The screenshot shows a terminal window titled "Terminal" with a dark theme. The window title bar includes the text "Activities Terminal" and the date "Tue 10:54 AM". The terminal window displays a command-line session:

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$ ls
merged_unpadded.lef picorv32a.synthesis.v
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$ cp picorv32a.synthesis.v picorv32a.synthesis_old.v
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$ ls
merged_unpadded.lef picorv32a.synthesis_old.v picorv32a.synthesis.v
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$
```

Commands to write verilog

```
# Check syntax
```

```
help write_verilog
```

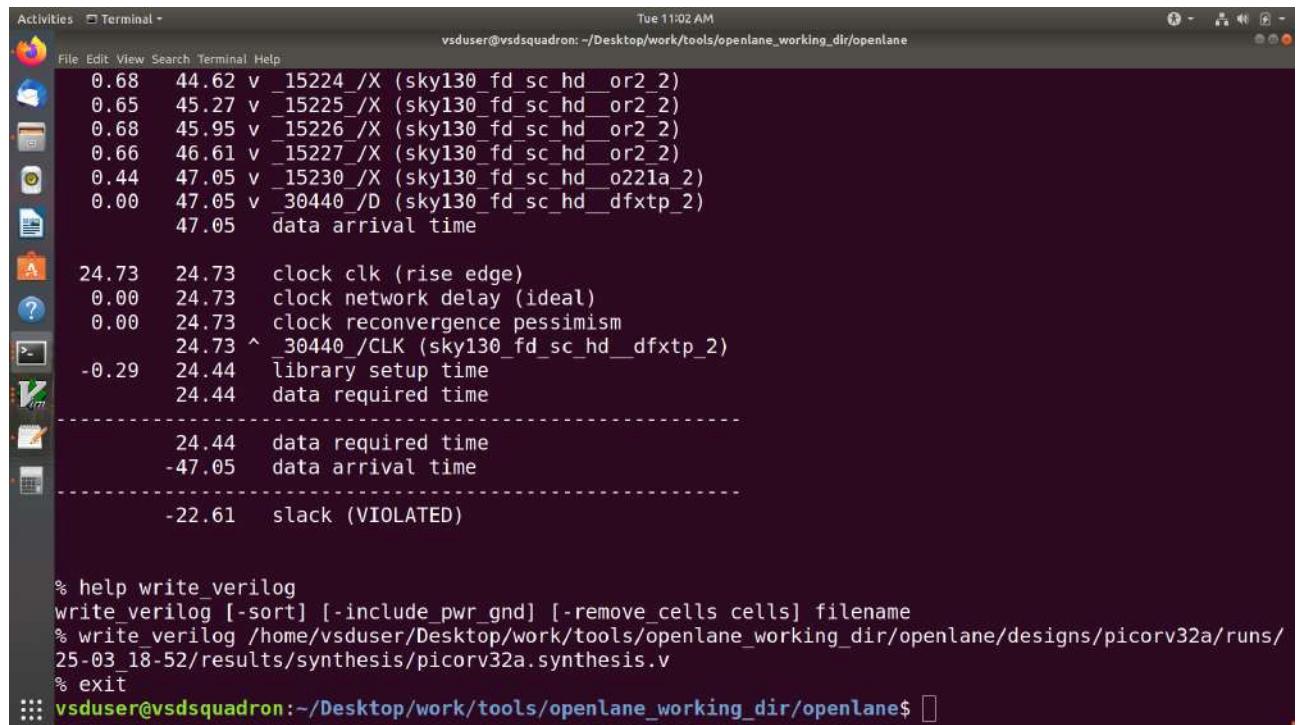
```
# Overwriting current synthesis netlist
```

```
write_verilog /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis/picorv32a.synthesis.v
```

```
# Exit from OpenSTA since timing analysis is done
```

```
exit
```

Screenshot of commands run



The screenshot shows a terminal window with the following content:

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
Tue 11:02 AM
File Edit View Search Terminal Help
0.68 44.62 v _15224_X (sky130_fd_sc_hd_or2_2)
0.65 45.27 v _15225_X (sky130_fd_sc_hd_or2_2)
0.68 45.95 v _15226_X (sky130_fd_sc_hd_or2_2)
0.66 46.61 v _15227_X (sky130_fd_sc_hd_or2_2)
0.44 47.05 v _15230_X (sky130_fd_sc_hd_o221a_2)
0.00 47.05 v _30440_D (sky130_fd_sc_hd_dfxtp_2)
47.05 data arrival time

24.73 24.73 clock clk (rise edge)
0.00 24.73 clock network delay (ideal)
0.00 24.73 clock reconvergence pessimism
24.73 ^ _30440_CLK (sky130_fd_sc_hd_dfxtp_2)
-0.29 24.44 library setup time
24.44 data required time
-----
24.44 data required time
-47.05 data arrival time
-----
-22.61 slack (VIOLATED)

% help write_verilog
write_verilog [-sort] [-include_pwr_gnd] [-remove_cells cells] filename
% write_verilog /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis/picorv32a.synthesis.v
% exit
::: vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$
```

Verified that the netlist is overwritten by checking that instance `_14506_` is replaced with `sky130_fd_sc_hd_or4_4`

```

Activities  M. GVim -
Tue 11:01 AM
picorv32a.synthesis.v (~-/Desktop/work/too...ns/25-03_18-52/results/synthesis) - GVIM2
File Edit Tools Syntax Buffers Window Help
16359     .Y(_11665_));
16360   sky130_fd_sc_hd_o22ai_2 _14504_ (.A1(\irq_mask[21]),
16361     .A2(_11664),
16362     .B1(\irq_mask[23]),
16363     .B2(_11665),
16364     .Y(_11666));
16365   sky130_fd_sc_hd_a221o_2 _14505_ (.A1(_11662),
16366     .A2(\irq_pending[20]),
16367     .B1(_11663),
16368     .B2(\irq_pending[22]),
16369     .C1(_11666),
16370     .X(_11667));
16371   sky130_fd_sc_hd_or4_4 _14506_ (.A(_11649),
16372     .B(_11655),
16373     .C(_11661),
16374     .D(_11667),
16375     .X(_11668));
16376   sky130_vsdinv _14507_ (.A(irq_active),
16377     .Y(_11669));
16378   sky130_vsdinv _14508_ (.A(irq_delay),
16379     .Y(_11670));
16380   sky130_fd_sc_hd_o2111a_2 _14509_ (.A1(_11643),
16381     .A2(_11668),
16382     .B1(_11669),
16383     .C1(_11670),
hlsearch
16371,25      21%

```

Since we confirmed that netlist is replaced and will be loaded in PnR but since we want to follow up on the earlier o violation design we are continuing with the clean design to further stages

Commands load the design and run necessary stages

```
# Now once again we have to prep design so as to update variables
```

```
prep -design picorv32a -tag 24-03_10-03 -overwrite
```

```
# Additional commands to include newly added lef to openlane flow merged.lef
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_STRATEGY
```

```
set ::env(SYNTH_STRATEGY) "DELAY 3"

# Command to set new value for SYNTH_SIZING

set ::env(SYNTH_SIZING) 1

# Now that the design is prepped and ready, we can run synthesis using following
# command

run_synthesis

# Following commands are altogether sourced in "run_floorplan" command

init_floorplan

place_io

tap_decap_or

# Now we are ready to run placement

run_placement

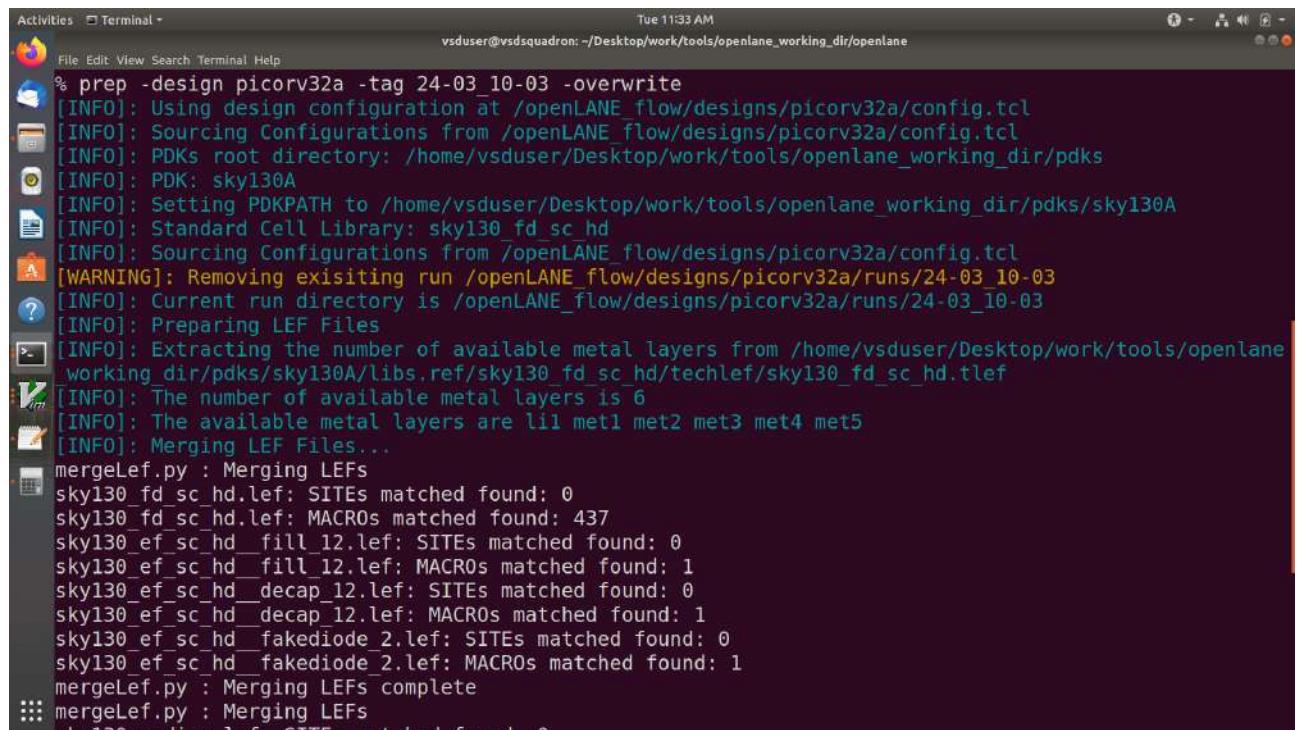
# Incase getting error

unset ::env(LIB_CTS)
```

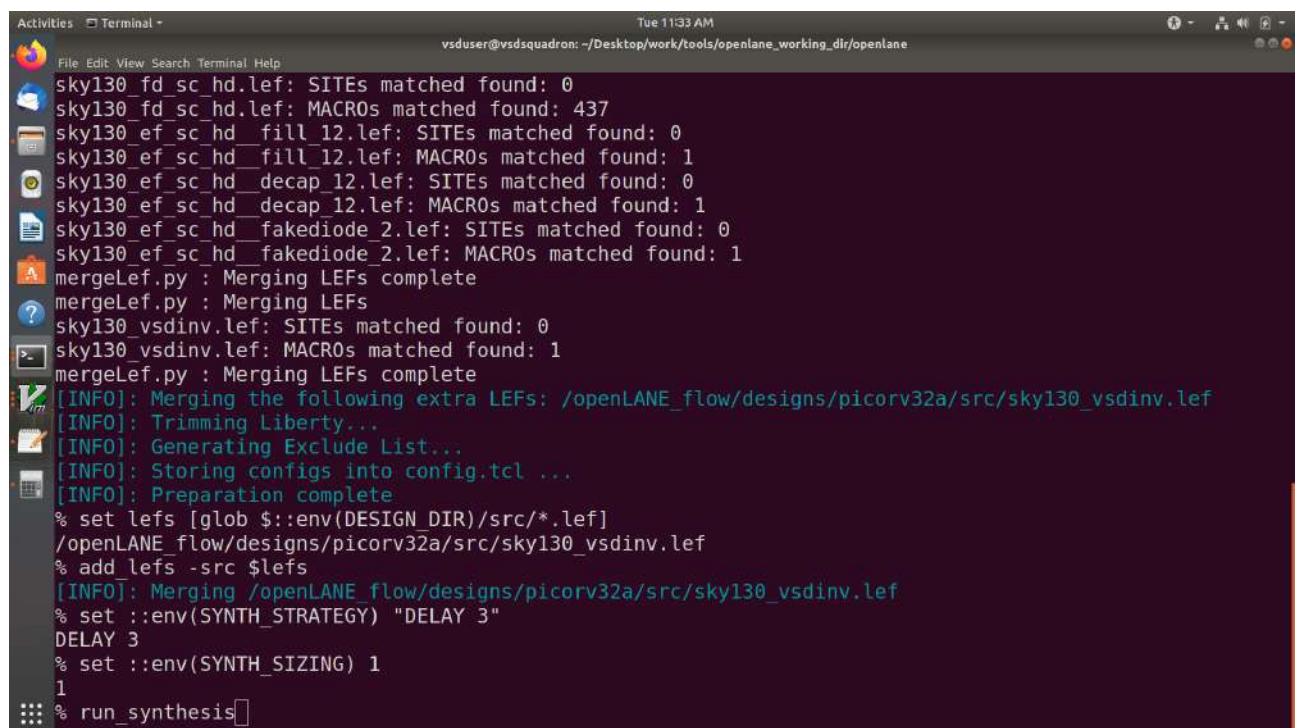
```
# With placement done we are now ready to run CTS
```

```
run_cts
```

Screenshots of commands run



```
Activities Terminal Tue 11:33 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% prep -design picorv32a -tag 24-03_10-03 -overwrite
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130 fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[WARNING]: Removing existing run /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.tlef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1l met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
::: mergeLef.py : Merging LEFs
    120 SITEs and 15 MACROs
```



```
Activities Terminal Tue 11:33 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% set ::env(SYNTH_STRATEGY) "DELAY 3"
DELAY 3
% set ::env(SYNTH_SIZING) 1
1
::: % run_synthesis
```

```
Activities Terminal - Tue 11:35 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
::: % init_floorplan
```

```
Activities Terminal - Tue 11:36 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
% init_floorplan
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 8
OpenROAD 0.9.0 1415572a73
A This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
[INFO IFP-0001] Added 264 rows of 1566 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 731.615 742.335 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/8-verilog2def.die_area.rpt.
[INFO] Floorplanned on a core area of 5.52 10.88 725.88 728.96 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/8-verilog2def.core_area.rpt.
[INFO]: Core area width: 720.36
[INFO]: Core area height: 718.08
[INFO]: Changing layout from 0 to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def
::: % place_io
```

```
Activities Terminal - Tue 11:37 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% place_io
[INFO]: Running IO Placement...
[INFO]: current step index: 9
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def
#Macro blocks found: 0
Using 5u default boundaries offset
Random pin placement
RandomMode Even
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def
::: % tap_decap_or
```

```
Activities Terminal - Tue 11:38 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% place_io
[INFO]: Running IO Placement...
[INFO]: current step index: 9
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def
Step 1: Cut rows...
[INFO TAP-0001] Macro blocks found: 0
[INFO TAP-0002] #Original rows: 264
[INFO TAP-0003] #Cut rows: 0
Step 2: Insert endcaps...
[INFO TAP-0004] #Endcaps inserted: 528
Step 3: Insert tapcells...
[INFO TAP-0005] #Tapcells inserted: 7180
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/floorplan/picorv32a.floorplan.def
::: % run_placement
```

```
Activities Terminal - Tue 11:39 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
legalized HPWL      910806.5 u
delta HPWL          2 %

[INFO DPL-0020] Mirrored 6650 instances
[INFO DPL-0021] HPWL before      910806.5 u
[INFO DPL-0022] HPWL after       895297.0 u
[INFO DPL-0023] HPWL delta      -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/11-resize.r.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 15
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
% run_cts
```

```
Activities Terminal - Tue 12:00 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 25690 components and 145610 component-terminals.
Notice 0:     Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
[INFO]: Changing netlist from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis_optimized.v to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis_cts.v
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 19
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def.png'
Done
[INFO]: Screenshot taken.
% 
```

12. Post-CTS OpenROAD timing analysis.

Commands to be run in OpenLANE flow to do OpenROAD timing analysis with integrated OpenSTA in OpenROAD

```
# Command to run OpenROAD tool
```

```
openroad
```

```
# Reading lef file
```

```
read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
```

```
# Reading def file
```

```
read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
```

```
# Creating an OpenROAD database to work with
```

```
write_db pico_cts.db
```

```
# Loading the created database in OpenROAD
```

```
read_db pico_cts.db
```

```
# Read netlist post CTS
```

```
read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/  
picorv32a.synthesis_cts.v
```

```
# Read library for design
```

```
read_liberty $::env(LIB_SYNTH_COMPLETE)
```

```
# Link design and library

link_design picorv32a

# Read in the custom sdc we created

read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc

# Setting all cloks as propagated clocks

set_propagated_clock [all_clocks]

# Check syntax of 'report_checks' command

help report_checks

# Generating custom timing report

report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format
full_clock_expanded -digits 4

# Exit to OpenLANE flow

exit
```

Screenshots of commands run and timing report generated

```
Activities Terminal - Tue 12:55 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% openroad
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
% read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
% read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 25690 components and 145610 component-terminals.
Notice 0:     Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
% write_db pico_cts.db
% read_db pico_cts.db
% read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis
_cts.v
% read_liberty $::env(LIB_SYNTH_COMPLETE)
1
% link_design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_tapvpwrvgnd_1 has no liberty cell.
```

```
Activities Terminal - Tue 12:57 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

% read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
[INFO]: Setting output delay to: 4.9460000000000001
[INFO]: Setting input delay to: 4.9460000000000001
[INFO]: Setting load to: 0.017653
[INFO]: Setting propagated_clock [all_clocks]
% help report_checks
report_checks
report_checks [-from from_list|-rise_from from_list|-fall_from from_list] [-through through_list|-rise_through through_list|-fall_through through_list] [-to to_list|-rise_to to_list|-fall_to to_list] [-unconstrained] [-path_delay min|min_rise|min_fall|max|max_rise|max_fall|min_max] [-corner corner_name] [-group_count path_count] [-endpoint_count path_count] [-unique_paths_to_endpoint] [-slack_max slack_max] [-slack_min slack_min] [-sort_by_slack] [-path_group group_name] [-format full|full_clock|full_clock_expanded|short|end|summary] [-fields [capacitance|slew|input_pin|net]] [-digits digits] [-no_line_splits] [> filename] [>> filename]
% report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
Startpoint: _30990_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30955_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----.
                               0.0000 0.0000 clock clk (rise edge)
                               0.0000 0.0000 clock source latency
                               0.0225 0.0100 ^ clk (in)
                               0.0079 0.0000 ^ clk (net)
1 0.0079 0.0000 0.0100 ^ clk (in) 0.0100 ^ clk (net)
```

```

Activities Terminal - Tue 12:58 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
11 0.0206
    0.0650  0.0000  1.6203 ^ _30955/_CLK (sky130_fd_sc_hd_dfxtp_2)
    0.0000  1.6203  clock reconvergence pessimism
   -0.0263  1.5941  library hold time
    1.5941  data required time
-----
    1.5941  data required time
   -1.8059  data arrival time
-----
    0.2119  slack (MET)

Startpoint: resetn (input port clocked by clk)
Endpoint: mem_la_read (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
----- 0.0000 0.0000 0.0000 0.0000 clock clk (rise edge)
          0.0000 0.0000 4.9460 4.9460 ^ input external delay
          0.0172 0.0055 4.9515 ^ resetn (in)
          0.0042 0.0172 0.0000 4.9515 ^ input101/A (sky130_fd_sc_hd_clkbuf_8)
          0.0582 0.1265 5.0780 ^ input101/X (sky130_fd_sc_hd_clkbuf_8)
          0.0234 0.0582 0.0000 5.0780 ^ net101 (net)

```

```

Activities Terminal - Tue 11:09 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
6 0.0270
    0.0947  0.0000  5.2526 ^ 12638_(net)
    0.1284  0.1277  5.3802 v 17093/_C (sky130_fd_sc_hd_nand3_4)
          0.1284  0.0000  5.3802 v 17093/_Y (sky130_fd_sc_hd_nand3_4)
          0.0799  0.1239  5.5041 ^ 13857_(net)
          0.0023 0.0799 0.0000 5.5041 ^ 18867/_B1 (sky130_fd_sc_hd_a21oi_4)
          0.0799  0.0000 5.5041 ^ 18867/_Y (sky130_fd_sc_hd_a21oi_4)
          0.0177 0.1052 0.1596 5.6637 ^ net199_(net)
          0.1052 0.0000 5.6637 ^ output199/A (sky130_fd_sc_hd_clkbuf_2)
          0.1052 0.0000 5.6637 ^ output199/X (sky130_fd_sc_hd_clkbuf_2)
          0.0000 0.0000 24.7300 24.7300 clock clk (rise edge)
          0.0000 0.0000 24.7300 24.7300 clock network delay (propagated)
          0.0000 0.0000 24.7300 24.7300 clock reconvergence pessimism
         -4.9460 19.7840 19.7840 output external delay
         19.7840 19.7840 data required time
         -5.6637 14.1203 14.1203 data arrival time
-----
         19.7840 14.1203 slack (MET)

% exit
%
```

**13. Explore post-CTS OpenROAD timing analysis by removing
'sky130_fd_sc_hd_clkbuf_1' cell from clock buffer list variable
'CTS_CLK_BUFFER_LIST'.**

**Commands to be run in OpenLANE flow to do OpenROAD timing analysis after
changing CTS_CLK_BUFFER_LIST**

```
# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)

# Removing 'sky130_fd_sc_hd_clkbuf_1' from the list

set ::env(CTS_CLK_BUFFER_LIST) [lreplace $::env(CTS_CLK_BUFFER_LIST) 0 0]

# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)

# Checking current value of 'CURRENT_DEF'

echo $::env(CURRENT_DEF)

# Setting def as placement def

set ::env(CURRENT_DEF) /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/
placement/picorv32a.placement.def

# Run CTS again

run_cts

# Checking current value of 'CTS_CLK_BUFFER_LIST'
```

```
echo $::env(CTS_CLK_BUFFER_LIST)

# Command to run OpenROAD tool

openroad

# Reading lef file

read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef

# Reading def file

read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def

# Creating an OpenROAD database to work with

write_db pico_cts1.db

# Loading the created database in OpenROAD

read_db pico_cts.db

# Read netlist post CTS

read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/
picorv32a.synthesis_cts.v
```

```
# Read library for design

read_liberty $::env(LIB_SYNTH_COMPLETE)

# Link design and library

link_design picorv32a

# Read in the custom sdc we created

read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc

# Setting all cloks as propagated clocks

set_propagated_clock [all_clocks]

# Generating custom timing report

report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format
full_clock_expanded -digits 4

# Report hold skew

report_clock_skew -hold
```

```
# Report setup skew

report_clock_skew -setup

# Exit to OpenLANE flow

exit

# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)

# Inserting 'sky130_fd_sc_hd__clkbuf_1' to first index of list

set ::env(CTS_CLK_BUFFER_LIST) [linsert $::env(CTS_CLK_BUFFER_LIST) 0
sky130_fd_sc_hd__clkbuf_1]

# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)
```

Screenshots of commands run and timing report generated

```
Activities Terminal - Tue 1:42 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_
8
% set ::env(CTS_CLK_BUFFER_LIST) [lreplace $::env(CTS_CLK_BUFFER_LIST) 0 0]
sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
% set ::env(CURRENT_DEF) /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
% run_cts
[INFO]: Running TritonCTS...
[INFO]: current step index: 20
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Done
```

```
Activities Terminal - Tue 1:45 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def.png'
Done
[INFO]: Screenshot taken.
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% openroad
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
% read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
% read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 25690 components and 145610 component-terminals.
Notice 0: Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
% write_db pico_cts1.db
% read_db pico_cts.db
```

```

Activities Terminal - Tue 1:48 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% write_db pico_cts1.db
% read_db pico_cts.db
% read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis
_cts.v
% read_liberty $::env(LIB_SYNTH_COMPLETE)
1
% link_design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_tapvpwrvgnd_1 has no liberty cell.
% read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
[INFO]: Setting output delay to: 4.946000000000001
[INFO]: Setting input delay to: 4.946000000000001
[INFO]: Setting load to: 0.017653
% set_propagated_clock [all_clocks]
% report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
Startpoint: _30990_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30955_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----  

1 0.0079 0.0225 0.0000 0.0100 ^ clkbuf_0_clk/A (sky130_fd_sc_hd_clkbuf_16)  

0.0225 0.0000 0.0100 ^ clkbuf_0_clk/X (sky130_fd_sc_hd_clkbuf_16)

```

```

Activities Terminal - Tue 1:48 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% report_checks -path_delay max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
0.0520 0.0000 1.2459 ^ _30955/_CLK (sky130_fd_sc_hd_dfxtpl_2)
0.0000 1.2459 clock reconvergence pessimism
-0.0280 1.2179 library hold time
1.2179 data required time
-----  

1.2179 data required time
-1.5305 data arrival time
-----  

0.3125 slack (MET)

Startpoint: resetn (input port clocked by clk)
Endpoint: mem_la_read (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
-----  

1 0.0042 0.0172 0.0000 4.9515 ^ resetn/in
0.0000 0.0000 4.9460 ^ input external delay
0.0172 0.0055 4.9515 ^ resetn/net
0.0172 0.0000 4.9515 ^ input101/A (sky130_fd_sc_hd_clkbuf_8)
1 0.0234 0.0582 0.1265 5.0780 ^ input101/X (sky130_fd_sc_hd_clkbuf_8)
0.0582 0.0000 5.0780 ^ net101/net
0.0582 0.0000 5.0780 ^ 15304/A (sky130_fd_sc_hd_clkbuf_4)
0.0042 0.0000 5.2526 ^ 15304/X (sky130_fd_sc_hd_clkbuf_4)

```

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      Tue 1:50 PM
          -4.9460  19.7840  output external delay
          19.7840  data required time
          19.7840  data required time
          -5.6637  data arrival time
          14.1203  slack (MET)

% report_clock_skew -hold
Clock clk
Latency CRPR Skew
_31226 /CLK ^
    1.36
_32416 /CLK ^
    0.94    0.00    0.42

% report_clock_skew -setup
Clock clk
Latency CRPR Skew
_31226 /CLK ^
    1.36
_32416 /CLK ^
    0.94    0.00    0.42

% exit
%
```

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      Tue 1:53 PM
          % echo $::env(CTS_CLK_BUFFER_LIST)
          sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
          % set ::env(CTS_CLK_BUFFER_LIST) [linsert $::env(CTS_CLK_BUFFER_LIST) 0 sky130_fd_sc_hd_clkbuf_1]
          sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_
          8
          % echo $::env(CTS_CLK_BUFFER_LIST)
          sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_
          8
%
```

Section 5 - Final steps for RTL2GDS using tritonRoute and openSTA (25/03/2024 - 26/03/2024)

Theory

Implementation

- **Section 5 tasks:-**
25. Perform generation of Power Distribution Network (PDN) and explore the PDN layout.
 26. Perform detailed routing using TritonRoute.
 27. Post-Route parasitic extraction using SPEF extractor.
 28. Post-Route OpenSTA timing analysis with the extracted parasitics of the route.
- All section 5 logs, reports and results can be found in following run folder:

Section 5 Run - 26-03_08-45

1. Perform generation of Power Distribution Network (PDN) and explore the PDN layout.

Commands to perform all necessary stages up until now

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:vo.21'
```

```
# Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command
```

```
docker
```

```
# Now that we have entered the OpenLANE flow contained docker sub-system we can  
invoke the OpenLANE flow in the Interactive mode using the following command
```

```
./flow.tcl -interactive
```

```
# Now that OpenLANE flow is open we have to input the required packages for proper  
functionality of the OpenLANE flow
```

```
package require openlane 0.9
```

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the  
design creating some necessary files and directories for running a specific design which in  
our case is 'picorv32a'
```

```
prep -design picorv32a
```

```
# Additional commands to include newly added lef to openlane flow merged.lef
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_STRATEGY
```

```
set ::env(SYNTH_STRATEGY) "DELAY 3"
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Now that the design is prepped and ready, we can run synthesis using following command
```

```
run_synthesis
```

```
# Following commands are altogether sourced in "run_floorplan" command
```

```
init_floorplan
```

```
place_io
```

```
tap_decap_or
```

```
# Now we are ready to run placement
```

```
run_placement
```

```
# Incase getting error
```

```
unset ::env(LIB_CTS)
```

```
# With placement done we are now ready to run CTS
```

```
run_cts
```

Now that CTS is done we can do power distribution network

gen_pdn

Screenshots of power distribution network run

```
Activities Terminal Tue 2:22 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: Screenshot taken.
% gen pdn
[INFO]: Generating PDN...
[INFO]: current step index: 14
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 25690 components and 145610 component-terminals.
Notice 0:     Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/cts/picorv32a.cts.def
[INFO] [PDNG-0016] Power Delivery Network Generator: Generating PDN
[INFO] [PDNG-0016] config: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdkss/sky130A/libs.tech/openlane/common_pdn.tcl
[INFO] [PDNG-0008] Design Name is picorv32a
[INFO] [PDNG-0009] Reading technology data
[INFO] [PDNG-0011] ***** INFO *****
Tunne: stdcell -mid
```

```
Activities Terminal Tue 2:22 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[WARNING PSM-0030] Vsrc location at (705.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
[WARNING PSM-0030] Vsrc location at (425.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 563.420um).
[WARNING PSM-0030] Vsrc location at (705.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 710.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 716.600um).
[WARNING PSM-0030] Vsrc location at (705.520um, 710.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 716.600um).
[INFO PSM-0031] Number of nodes on net VGND = 24383.
[INFO PSM-0037] G matrix created successfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/cts/picorv32a.cts.def to /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
% 
```

Commands to load PDN def in magic in another terminal

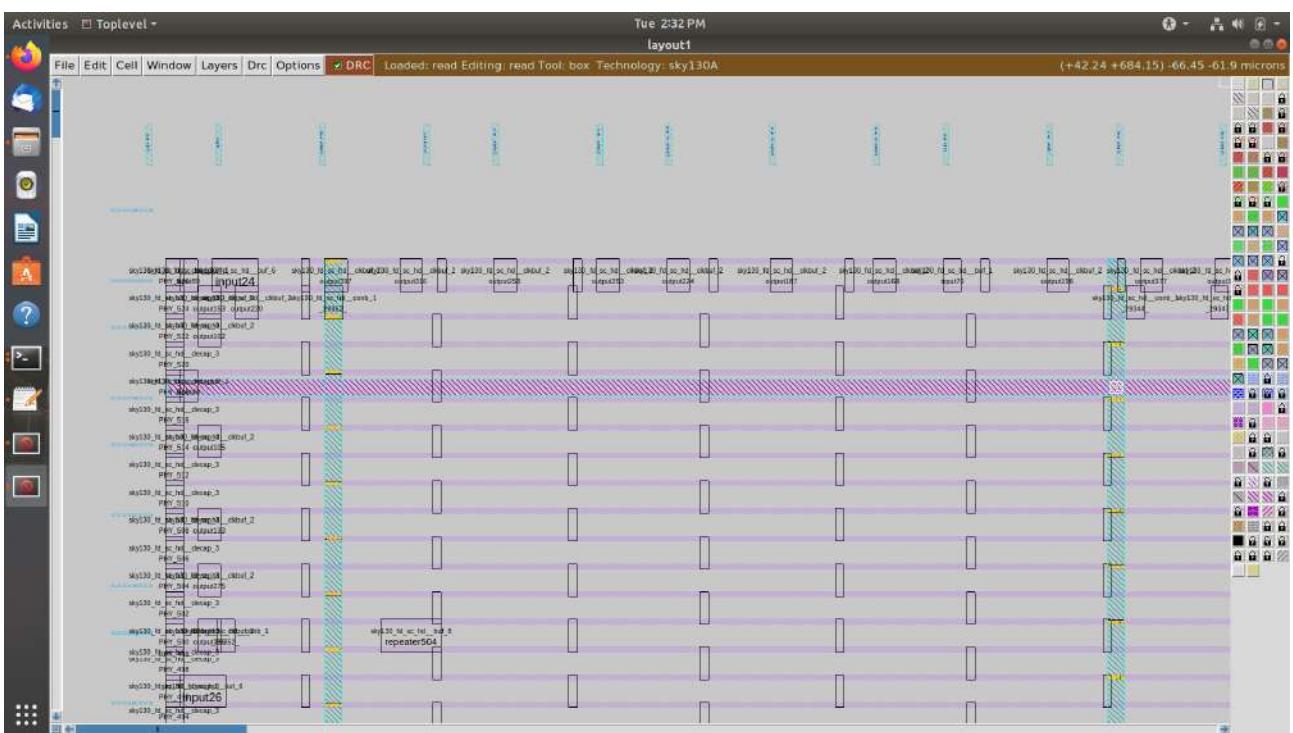
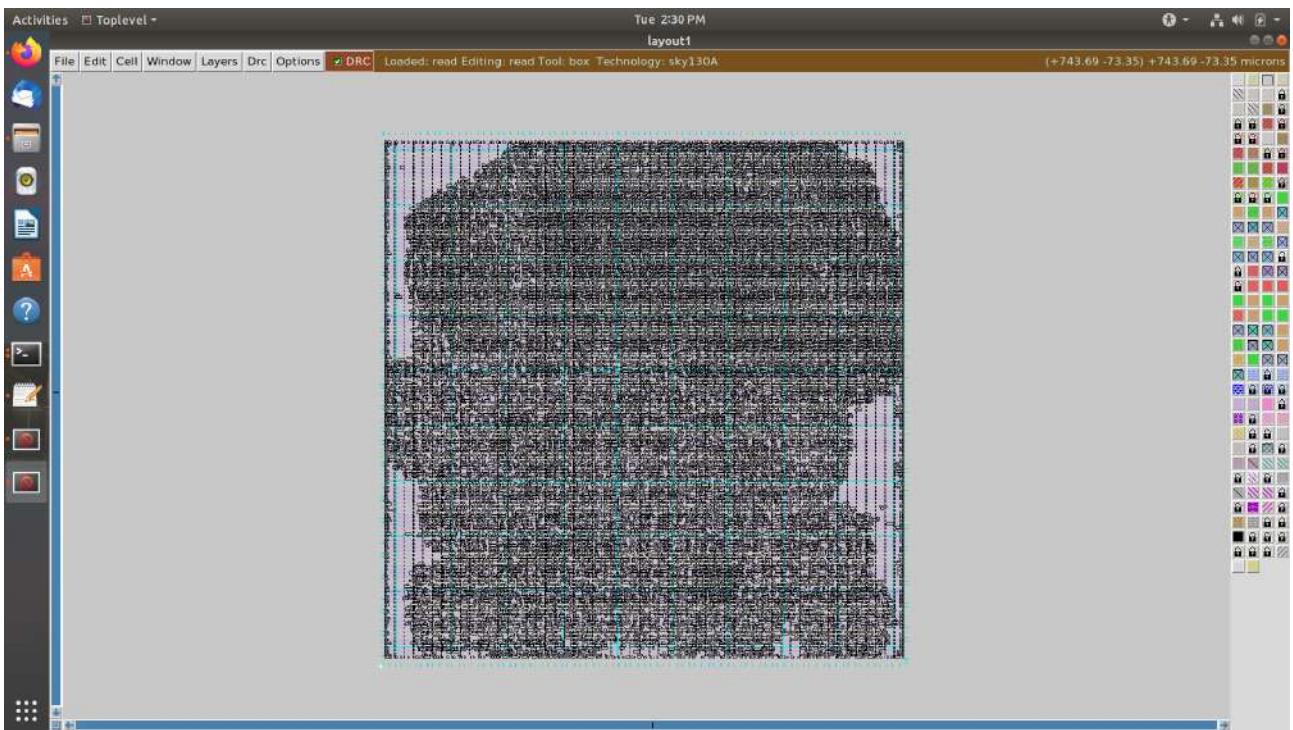
```
# Change directory to path containing generated PDN def
```

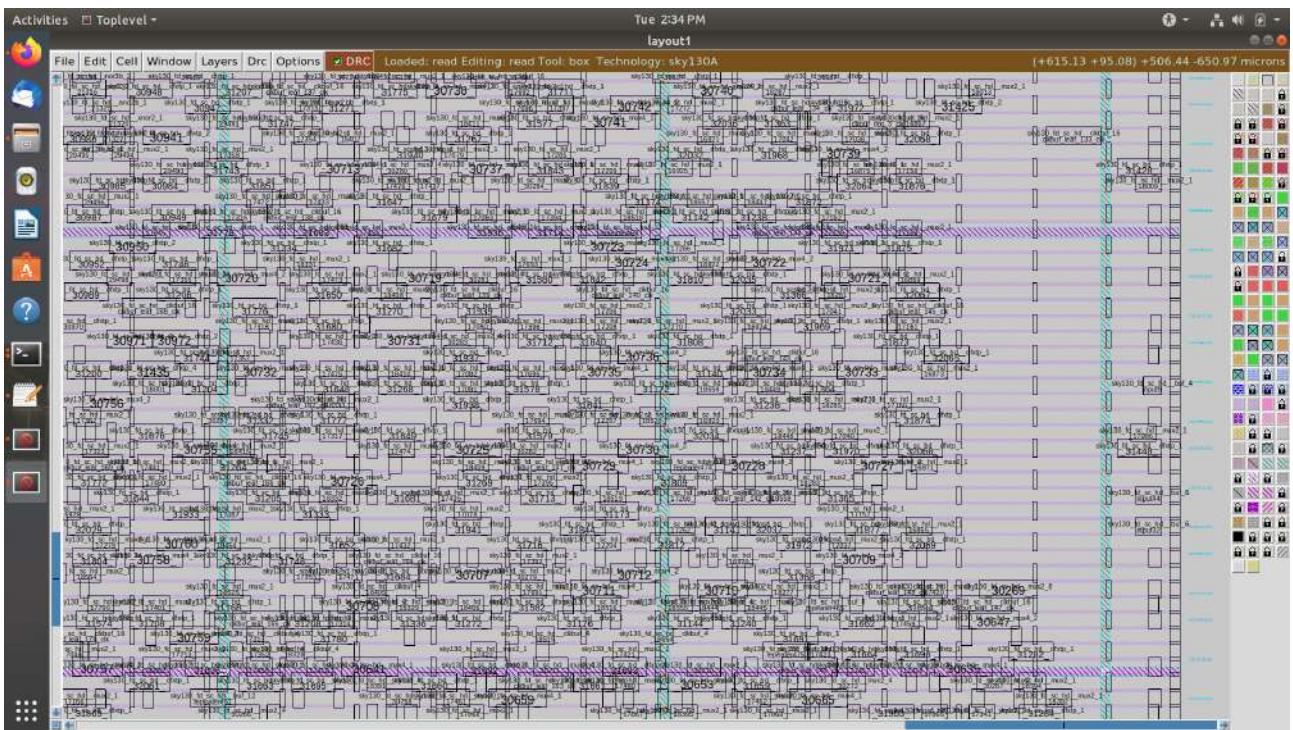
```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/  
26-03_08-45/tmp/floorplan/
```

```
# Command to load the PDN def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read 14-pdn.def &
```

Screenshots of PDN def





2. Perform detailed routing using TritonRoute and explore the routed layout.

Command to perform routing

```
# Check value of 'CURRENT_DEF'
```

```
echo $::env(CURRENT_DEF)
```

```
# Check value of 'ROUTING_STRATEGY'
```

```
echo $::env(ROUTING_STRATEGY)
```

```
# Command for detailed route using TritonRoute
```

```
run_routing
```

Screenshots of routing run

```
Activities Terminal - Tue 2:48 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
% echo $::env(ROUTING_STRATEGY)
can't read "::env(ROUTING_STRATEGY)": no such variable
% run_routing
[INFO]: Routing...
[INFO]: Running Global Routing...
[INFO]: current step index: 15
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
Notice 0: Design: picorv32a
Notice 0: Created 411 pins.
Notice 0: Created 25690 components and 145610 component-terminals.
Notice 0: Created 2 special nets and 0 connections.
Notice 0: Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
Min routing layer: 2
Max routing layer: 6
```

```
Activities Terminal - Tue 3:38 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
elapsed time = 00:00:08, memory = 782.73 (MB)
completing 60% with 0 violations
elapsed time = 00:00:10, memory = 782.73 (MB)
completing 70% with 0 violations
elapsed time = 00:00:12, memory = 782.73 (MB)
completing 80% with 0 violations
elapsed time = 00:00:14, memory = 782.73 (MB)
completing 90% with 0 violations
elapsed time = 00:00:15, memory = 782.73 (MB)
completing 100% with 0 violations
elapsed time = 00:00:17, memory = 782.73 (MB)
number of violations = 0
cpu time = 00:00:16, elapsed time = 00:00:17, memory = 782.73 (MB), peak = 854.19 (MB)
total wire length = 1103187 um
total wire length on LAYER l1l = 2639 um
total wire length on LAYER met1 = 483058 um
total wire length on LAYER met2 = 482317 um
total wire length on LAYER met3 = 122196 um
total wire length on LAYER met4 = 12976 um
total wire length on LAYER met5 = 0 um
total number of vias = 145509
up-via summary (total 145509):

-----
FR_MASTERSLICE      0
      l1l    60472
      met1   78129
      met2   6540
```

```

Activities Terminal - Tue 3:29 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Calculating Runtime From the Start...
[INFO]: Routing completed for picorv32a/26-03_08-45 in 1h7m11s
::: %

```

Commands to load routed def in magic in another terminal

Change directory to path containing routed def

```

cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
26-03_08-45/results/routing/

```

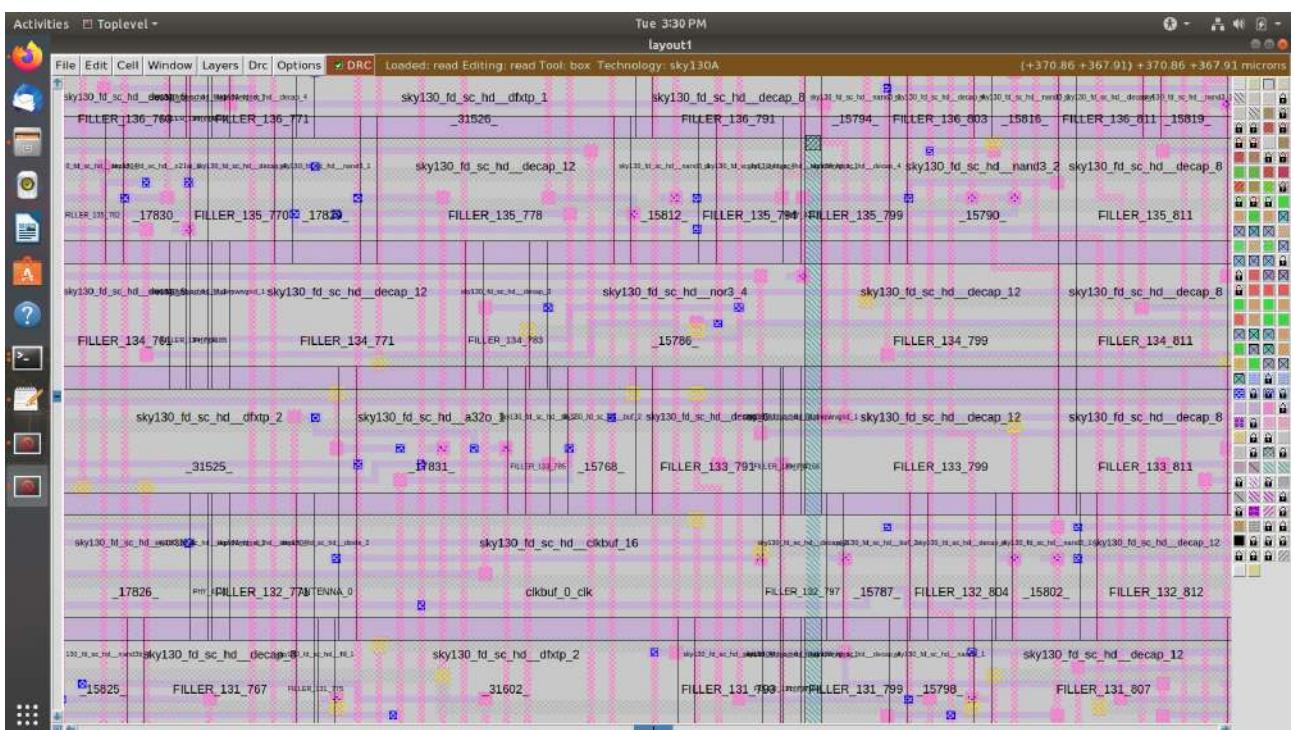
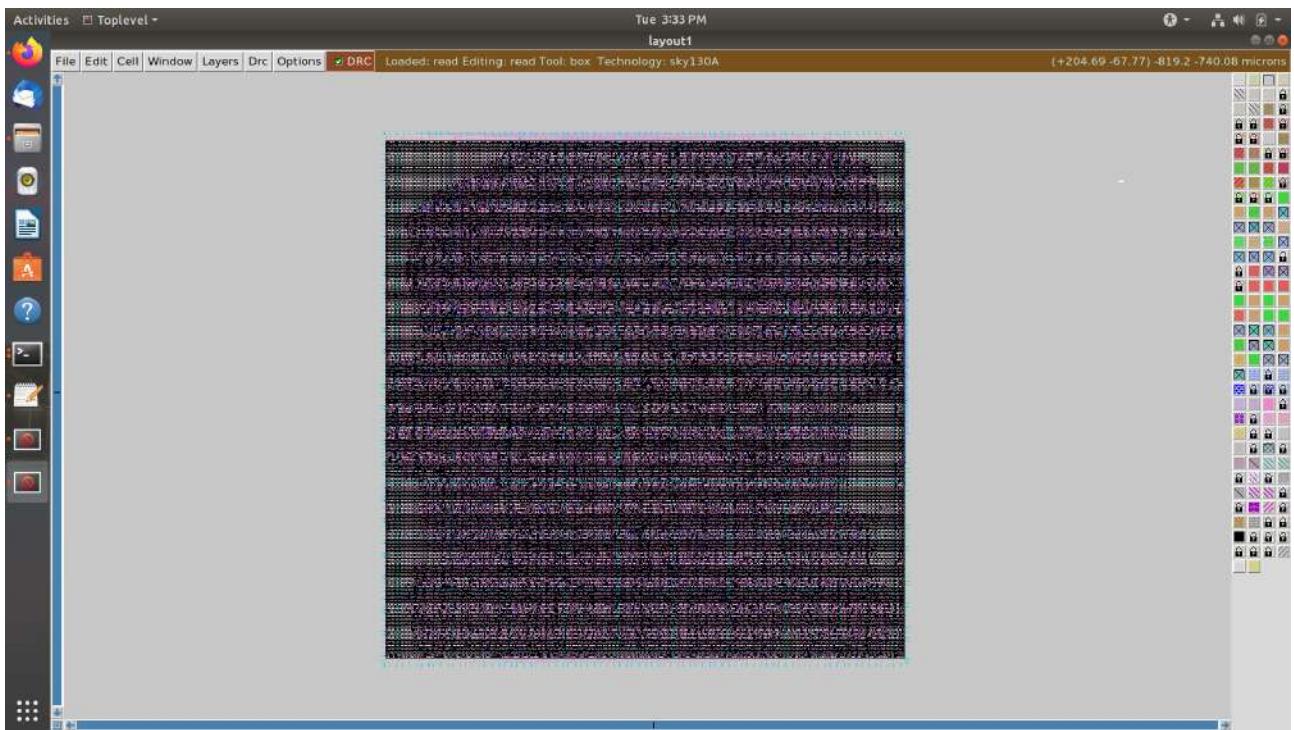
Command to load the routed def in magic tool

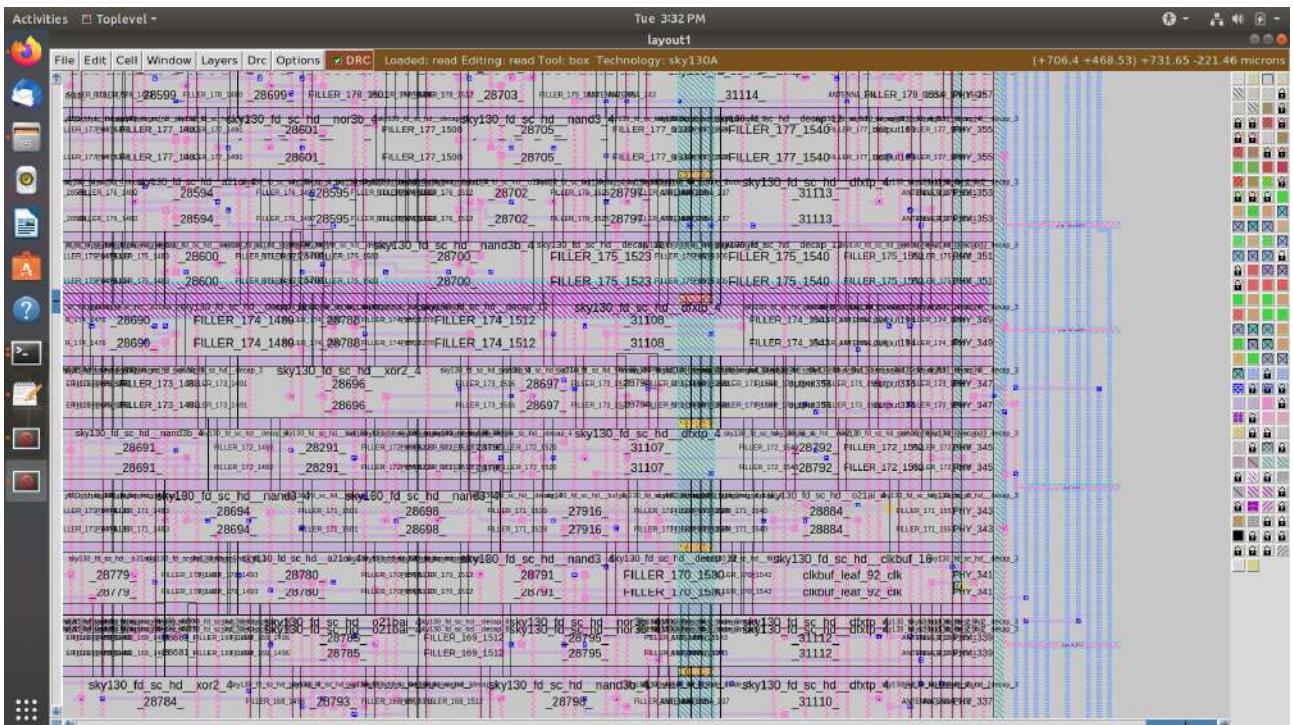
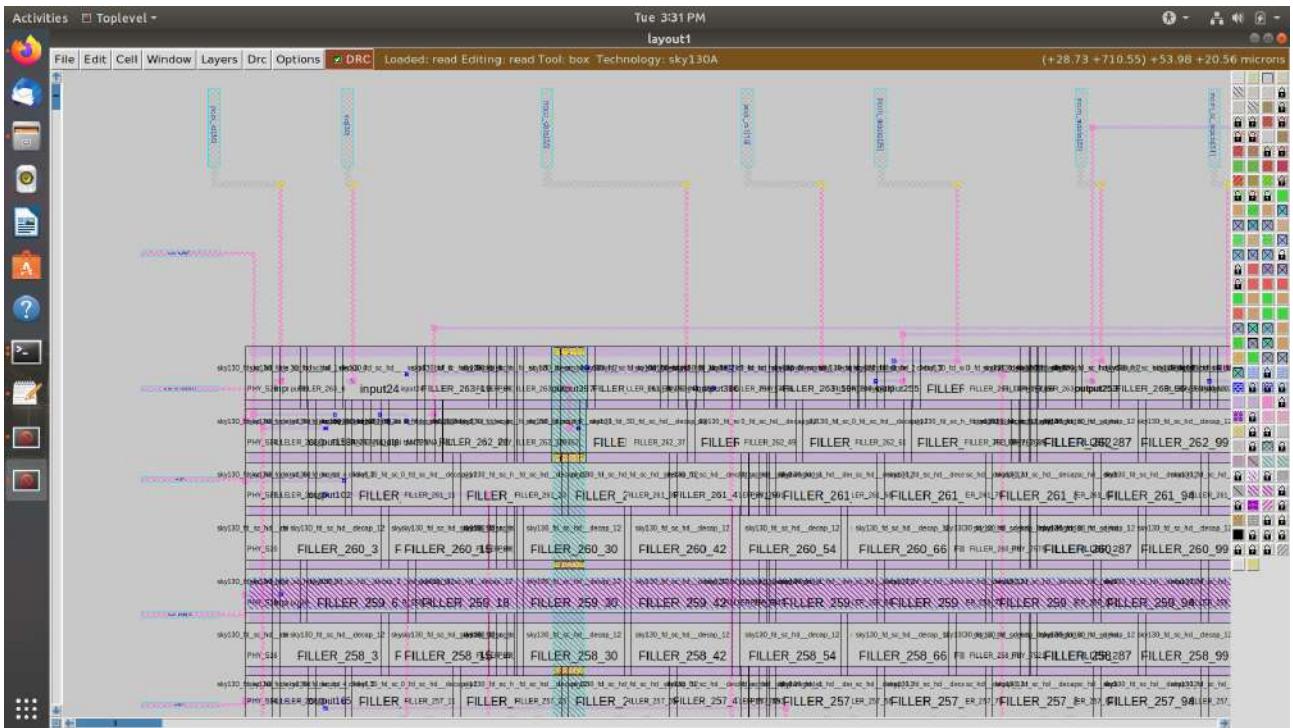
```

magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.def &

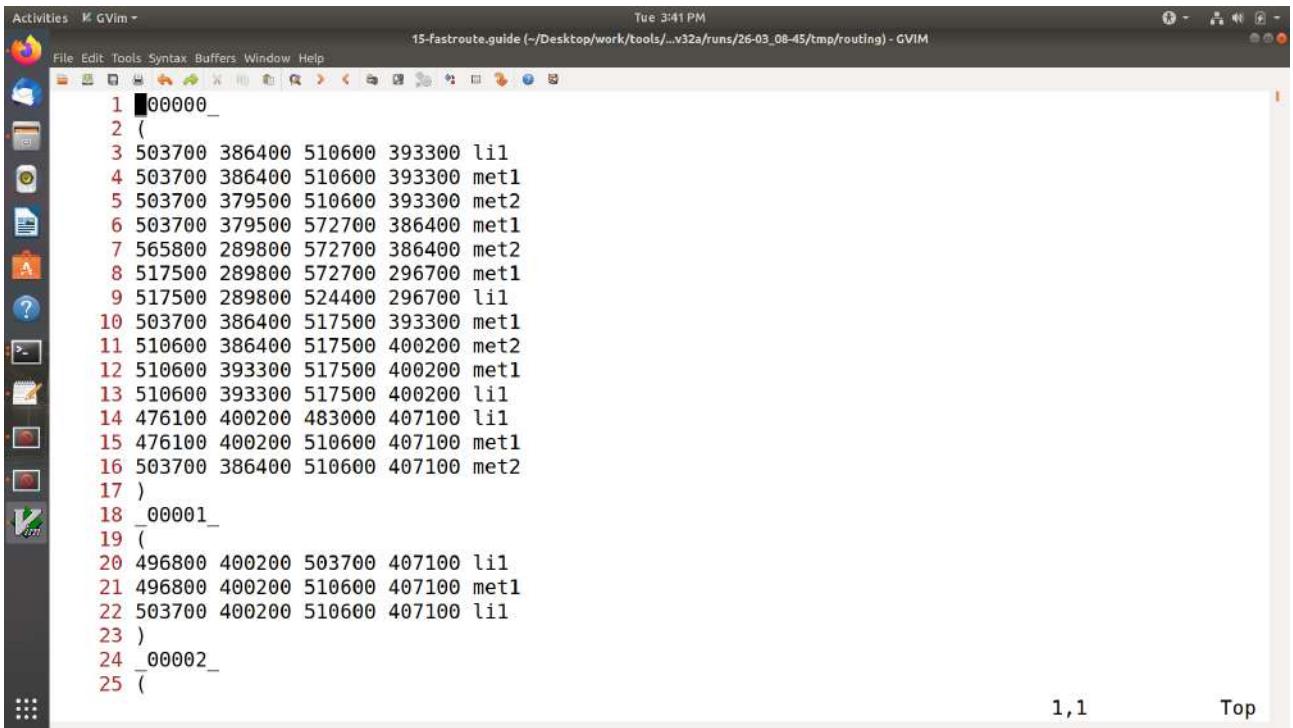
```

Screenshots of routed def





Screenshot of fast route guide present in openlane/designs/picorv32a/runs/26-03_08-45/tmp/routing directory



The screenshot shows a terminal window titled "Activities" with "GVim" selected. The title bar displays "15-fastroute.guide (~/Desktop/work/tools/...v32a/runs/26-03_08-45/tmp/routing) - GVIM" and the date "Tue 3:41 PM". The GVim interface includes a toolbar with icons for file operations like Open, Save, and Print, and a menu bar with File, Edit, Tools, Syntax, Buffers, Window, and Help. The main editor area contains the following text:

```
1 _00000_
2 (
3 503700 386400 510600 393300 l1l
4 503700 386400 510600 393300 met1
5 503700 379500 510600 393300 met2
6 503700 379500 572700 386400 met1
7 565800 289800 572700 386400 met2
8 517500 289800 572700 296700 met1
9 517500 289800 524400 296700 l1l
10 503700 386400 517500 393300 met1
11 510600 386400 517500 400200 met2
12 510600 393300 517500 400200 met1
13 510600 393300 517500 400200 l1l
14 476100 400200 483000 407100 l1l
15 476100 400200 510600 407100 met1
16 503700 386400 510600 407100 met2
17 )
18 _00001_
19 (
20 496800 400200 503700 407100 l1l
21 496800 400200 510600 407100 met1
22 503700 400200 510600 407100 l1l
23 )
24 _00002_
25 )
```

The status bar at the bottom right shows "1,1" and "Top".

3. Post-Route parasitic extraction using SPEF extractor.

Commands for SPEF extraction using external tool

```
# Change directory
```

```
cd Desktop/work/tools/SPEF_EXTRACTOR
```

```
# Command extract spef
```

```
python3 main.py /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/
designs/picorv32a/runs/26-03_08-45/tmp/merged.lef /home/vsduser/Desktop/work/tools/
openlane_working_dir/openlane/designs/picorv32a/runs/26-03_08-45/results/routing/
picorv32a.def
```

4. Post-Route OpenSTA timing analysis with the extracted parasitics of the route.

Commands to be run in OpenLANE flow to do OpenROAD timing analysis with integrated OpenSTA in OpenROAD

```
# Command to run OpenROAD tool
```

```
openroad
```

```
# Reading lef file
```

```
read_lef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
```

```
# Reading def file
```

```
read_def /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/  
picorv32a.def
```

```
# Creating an OpenROAD database to work with
```

```
write_db pico_route.db
```

```
# Loading the created database in OpenROAD
```

```
read_db pico_route.db
```

```
# Read netlist post CTS
```

```
read_verilog /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/synthesis/  
picorv32a.synthesis_preroute.v
```

```
# Read library for design

read_liberty $::env(LIB_SYNTH_COMPLETE)

# Link design and library

link_design picorv32a

# Read in the custom sdc we created

read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc

# Setting all cloks as propagated clocks

set_propagated_clock [all_clocks]

# Read SPEF

read_spef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/
picorv32a.spef

# Generating custom timing report

report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format
full_clock_expanded -digits 4
```

```
# Exit to OpenLANE flow
```

```
exit
```

Screenshots of commands run and timing report generated

```

Activities Terminal - Tue 11:16 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% openroad
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
% read_lef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
% read_def /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.def
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.def
Notice 0: Design: picorv32a
Notice 0: Created 429 pins.
Notice 0: Created 65617 components and 305814 component-terminals.
Notice 0: Created 2 special nets and 0 connections.
Notice 0: Created 18084 nets and 60532 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.def
% write_db pico_route.db
% read_db pico_route.db
% read_verilog /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/synthesis/picorv32a.synthesis_preroute.v
% read_liberty /openLANE_flow/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib
1
::: % link design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_fill_1 has no liberty cell.

```

```

Activities Terminal - Tue 11:17 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% link_design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_fill_1 has no liberty cell.
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_fill_2 has no liberty cell.
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_tapvpwrvrnd_1 has no liberty cell.
% read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
[INFO]: Setting output delay to: 4.9460000000000001
[INFO]: Setting input delay to: 4.9460000000000001
[INFO]: Setting load to: 0.017653
% set_propagated_clock [all_clocks]
% read_spef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.spef
1
% report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
Startpoint: _30900_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30910_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----
                           0.0000  0.0000  clock clk (rise edge)
                           0.0000  0.0000  clock source latency
                           0.0897  0.0624  0.0624 ^ clk (in)
                           0.0563          clk (net)
                           0.0900  0.0000  0.0624 ^ clkbuf_0_clk/A (sky130_fd_sc_hd_clkbuff_16)
                           0.0371  0.1366  0.1990 ^ clkbuf_0_clk/X (sky130_fd_sc_hd_clkbuff_16)
                           2     0.0143          clknet_0_clk (net)

```

```

Activities Terminal - Tue 11:17 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      5  0.0099
      0.0596  0.0002  2.3273 ^ clknet_leaf_220_clk (net)
      0.0000  2.3273  clock reconvergence pessimism
      -0.0274  2.2998  library hold time
      2.2998  data required time
      2.2998  data required time
      -1.9092  data arrival time
      -0.3907  slack (VIOLATED)

Startpoint: resetn (input port clocked by clk)
Endpoint: mem_la_read (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout   Cap     Slew     Delay    Time   Description
-----+-----+-----+-----+-----+
          0.0000  0.0000  clock clk (rise edge)
          0.0000  0.0000  clock network delay (propagated)
          4.9460  4.9460 ^ input external delay
          0.0172  0.0055  4.9515 ^ resetn (in)
          1  0.0042   resetn (net)
          0.0172  0.0000  4.9515 ^ input101/A (sky130_fd_sc_hd_clkbuf_8)
          0.0662  0.1329  5.0843 ^ input101/X (sky130_fd_sc_hd_clkbuf_8)
          7  0.0299   net101 (net)

```

```

Activities Terminal - Tue 11:17 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      6  0.0211
      0.0760  0.0002  5.2498 ^ 12638_(net)
      0.0933  0.0927  5.3425 v 17093/_C (sky130_fd_sc_hd_nand3_4)
      4  0.0143
      0.0933  0.0001  5.3426 v 17093/_Y (sky130_fd_sc_hd_nand3_4)
      0.4344  0.3758  5.7184 ^ 13857_(net)
      2  0.0603
      0.4349  0.0115  5.7299 ^ 18867/_B1 (sky130_fd_sc_hd_a21oi_4)
      0.1189  0.2493  5.9793 ^ 18867/_Y (sky130_fd_sc_hd_a21oi_4)
      1  0.0177
      0.1189  0.0002  5.9795 ^ net199 (net)
      0.1189  0.0002  5.9795 ^ mem_la_read (net)
      24.7300  24.7300  clock clk (rise edge)
      0.0000  24.7300  clock network delay (propagated)
      0.0000  24.7300  clock reconvergence pessimism
      -4.9460  19.7840  output external delay
      19.7840  data required time
      -5.9795  data arrival time
      13.8045  slack (MET)

% exit
%
```

About

2 Week digital VLSI SoC design and planning workshop with complete RTL2GDSII flow organised by VSD in collaboration with NASSCOM (Advanced Physical Design using OpenLANE/Sky130)

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Folders and files

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History

--	--	--

Desktop/work/tools/ openlane working dir	Add files via upload	
--	--	--

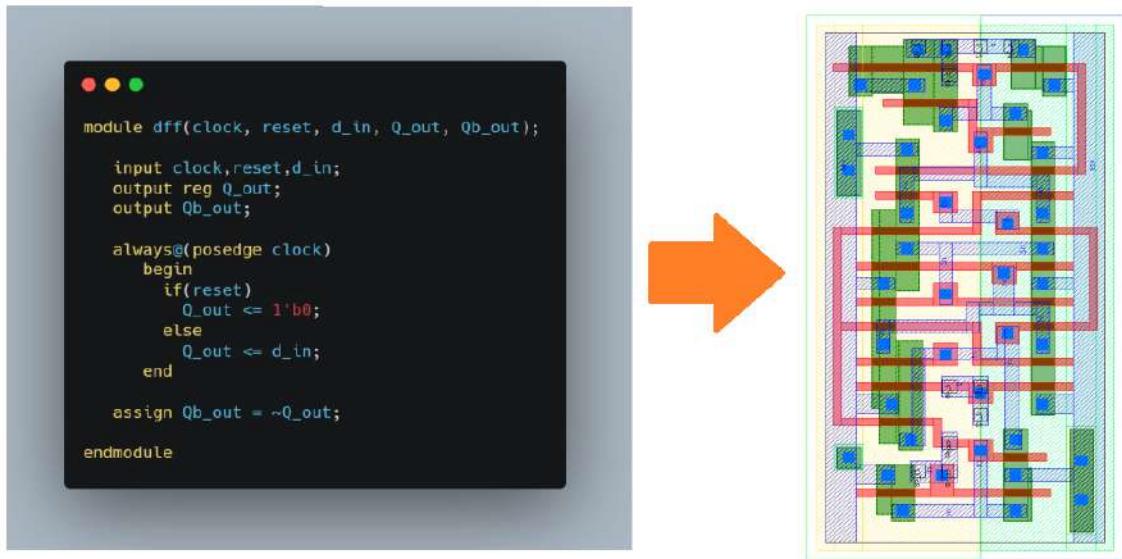
drc test	Add files via upload	
--------------------------	--	--

README.m d	Update README.md	
--------------------------------	--------------------------------------	--

drc tests.tg z	Add files via upload	
------------------------------------	--	--

Repository files navigation

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Digital VLSI SoC Design & Planning (RTL2GDSII Flow)

Digital VLSI SoC Design and Planning

OS linux

EDA Tools OpenLANE-Flow, Yosys, abc, OpenROAD, TritonRoute, OpenSTA, magic, netgen, GUNA

languages verilog, bash, TCL last commit last wednesday languages 12

verilog 96.2% repo size 179 MB code size 32.9 MB files 4

2 Week digital VLSI SoC design and planning workshop with complete RTL2GDSII flow organised by VSD in collaboration with NASSCOM

Section 1 - Inception of open-source EDA, OpenLANE and Sky130 PDK (14/03/2024 - 15/03/2024)

Theory

Expand or Collapse

Implementation

Section 1 tasks:-

1. Run 'picorv32a' design synthesis using OpenLANE flow and generate necessary outputs.
2. Calculate the flop ratio.

- All section 1 logs, reports and results can be found in following run folder:

Section 1 Run - 15-03_15-51

1. Run 'picorv32a' design synthesis using OpenLANE flow and generate necessary outputs.

Commands to invoke the OpenLANE flow and perform synthesis

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:vo.21'
```

```
# Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command
```

```
docker
```

```
# Now that we have entered the OpenLANE flow contained docker sub-system we can  
invoke the OpenLANE flow in the Interactive mode using the following command
```

```
./flow.tcl -interactive
```

```
# Now that OpenLANE flow is open we have to input the required packages for proper  
functionality of the OpenLANE flow
```

```
package require openlane 0.9
```

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the  
design creating some necessary files and directories for running a specific design which in  
our case is 'picorv32a'
```

```
prep -design picorv32a
```

```
# Now that the design is prepped and ready, we can run synthesis using following  
command
```

```
run_synthesis
```

```
# Exit from OpenLANE flow
```

```
exit
```

```
# Exit from OpenLANE flow docker sub-system
```

`exit`

Screenshots of running each commands

Activities Terminal Fri 9:23 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
vsduser@vsdsquadron:~$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ docker
bash-4.2$ ./flow.tcl -interactive
[INFO]:
[INFO]: Version: v0.21
[INFO]: Running interactively
% package require openlane 0.9
0.9
% prep -design picorv32a
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/15-03_15-51
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane
```

Activities Terminal Fri 9:24 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/15-03_15-51
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.tlef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1l met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
[INFO]: % run_synthesis[]
```

```
Activities Terminal Fri 9:29 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -759.46
wns -24.89
[INFO]: Synthesis was successful
::: %
```

2. Calculate the flop ratio.

Screenshots of synthesis statistics report file with required values highlighted

Activities M GVim Fri 10:02 PM

File Edit Tools Syntax Buffers Window Help

```

1 28. Printing statistics.
2
3 === picorv32a ===
4
5     Number of wires:          14596
6     Number of wire bits:      14978
7     Number of public wires:   1565
8     Number of public wire bits: 1947
9
10    Number of memories:       0
11    Number of memory bits:    0
12    Number of processes:      0
13    Number of cells:          14876
14        sky130_fd_sc_hd_a2111o_2      1
15        sky130_fd_sc_hd_a211o_2      35
16        sky130_fd_sc_hd_a211oi_2     60
17        sky130_fd_sc_hd_a21bo_2      149
18        sky130_fd_sc_hd_a21boi_2     8
19        sky130_fd_sc_hd_a21o_2       57
20        sky130_fd_sc_hd_a21oi_2      244
21        sky130_fd_sc_hd_a221o_2      86
22        sky130_fd_sc_hd_a22o_2       1013
23        sky130_fd_sc_hd_a2bb2o_2     1748
24        sky130_fd_sc_hd_a2bb2oi_2    81
25        sky130_fd_sc_hd_a311o_2      2

```

hlsearch 25, 38 Top

Activities M GVIM Fri 10:03 PM

File Edit Tools Syntax Buffers Window Help

```

25    sky130_fd_sc_hd_a311o_2      2
26    sky130_fd_sc_hd_a31o_2       49
27    sky130_fd_sc_hd_a31oi_2      7
28    sky130_fd_sc_hd_a32o_2       46
29    sky130_fd_sc_hd_a41o_2       1
30    sky130_fd_sc_hd_and2_2       157
31    sky130_fd_sc_hd_and3_2       58
32    sky130_fd_sc_hd_and4_2       345
33    sky130_fd_sc_hd_and4b_2      1
34    sky130_fd_sc_hd_buf_1        1656
35    sky130_fd_sc_hd_buf_2        8
36    sky130_fd_sc_hd_conb_1       42
37    sky130_fd_sc_hd_dfxtp_2      1613
38    sky130_fd_sc_hd_inv_2        1615
39    sky130_fd_sc_hd_mux2_1       1224
40    sky130_fd_sc_hd_mux2_2       2
41    sky130_fd_sc_hd_mux4_1       221
42    sky130_fd_sc_hd_nand2_2      78
43    sky130_fd_sc_hd_nor2_2       524
44    sky130_fd_sc_hd_nor2b_2      1
45    sky130_fd_sc_hd_nor3_2       42
46    sky130_fd_sc_hd_nor4_2       1
47    sky130_fd_sc_hd_o2111a_2     2
48    sky130_fd_sc_hd_o211a_2      69
49    sky130_fd_sc_hd_o211ai_2     6

```

search hit BOTTOM, continuing at TOP 49, 38 48%

Calculation of Flop Ratio and DFF % from synthesis statistics report file

Section 2 - Good floorplan vs bad floorplan and introduction to library cells (16/03/2024 - 17/03/2024)

Theory

Implementation

Section 2 tasks:-

1. Run 'picorv32a' design floorplan using OpenLANE flow and generate necessary outputs.
 2. Calculate the die area in microns from the values in floorplan def.
 3. Load generated floorplan def in magic tool and explore the floorplan.
 4. Run 'picorv32a' design congestion aware placement using OpenLANE flow and generate necessary outputs.
 5. Load generated placement def in magic tool and explore the placement.
-
- All section 2 logs, reports and results can be found in following run folder:

Section 2 Run - 17-03_12-06

1. Run 'picorv32a' design floorplan using OpenLANE flow and generate necessary outputs.

Commands to invoke the OpenLANE flow and perform floorplan

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:v0.21'
```

Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command

```
docker
```

Now that we have entered the OpenLANE flow contained docker sub-system we can invoke the OpenLANE flow in the interactive mode using the following command

```
./flow.tcl -interactive
```

Now that OpenLANE flow is open we have to input the required packages for proper functionality of the OpenLANE flow

```
package require openlane 0.9
```

Now the OpenLANE flow is ready to run any design and initially we have to prep the design creating some necessary files and directories for running a specific design which in our case is 'picorv32a'

```
prep -design picorv32a
```

Now that the design is prepped and ready, we can run synthesis using following command

```
run_synthesis
```

```
# Now we can run floorplan
```

```
run_floorplan
```

Screenshot of floorplan run

```
Activities Terminal - Sun 6:06 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: Synthesis was successful
% run_floorplan
[INFO]: Running Floorplanning...
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 3
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/l
ib/sky130_fd_sc_hd_tt_025C_lv80.lib line 31, default_operating_condition tt_025C_lv80 not found.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/merged_unpadded.le
f
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 440 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/merged_unpadded.le
f
[INFO IFP-0001] Added 238 rows of 1412 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 660.685 671.405 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/reports/floorplan/3-verilog2def.die_area.rpt.
[INFO] Floorplanned on a core area of 5.52 10.88 655.04 658.24 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/reports/floorplan/3-verilog2def.core_area.rpt.
[INFO]: Core area width: 649.52
[INFO]: Core area height: 647.36
[INFO]: Changing layout from 0 to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/floorplan/3-ve
rilog2def_openroad.def
[INFO]: Running IO Placement...
[INFO]: success! step index: 3
```

```
Activities Terminal - Sun 6:06 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
er stripe. Moving to closest stripe at (567.000um, 103.880um).
[WARNING PSM-0030] Vsrc location at (565.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 257.060um).
[WARNING PSM-0030] Vsrc location at (5.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (145.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
[WARNING PSM-0030] Vsrc location at (425.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 563.420um).
[INFO PSM-0031] Number of nodes on net VGND = 19223.
[INFO PSM-0037] G matrix created sucessfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/floorplan/picorv32a.floorplan.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/floorplan/7-pdn.def
1
% [ ]
```

2. Calculate the die area in microns from the values in floorplan def.

Screenshot of contents of floorplan def

```

1 VERSION 5.8 ;
2 DIVIDERCHAR "/";
3 BUSBITCHARS "[]";
4 DESIGN picorv32a ;
5 UNITS DISTANCE MICRONS 1000 ;
6 DIEAREA ( 0 0 ) ( 660685 671405 ) ;
7 ROW ROW_0 unithd 5520 10880 FS DO 1412 BY 1 STEP 460 0 ;
8 ROW ROW_1 unithd 5520 13600 N DO 1412 BY 1 STEP 460 0 ;
9 ROW ROW_2 unithd 5520 16320 FS DO 1412 BY 1 STEP 460 0 ;
10 ROW ROW_3 unithd 5520 19040 N DO 1412 BY 1 STEP 460 0 ;
11 ROW ROW_4 unithd 5520 21760 FS DO 1412 BY 1 STEP 460 0 ;
12 ROW ROW_5 unithd 5520 24480 N DO 1412 BY 1 STEP 460 0 ;
13 ROW ROW_6 unithd 5520 27200 FS DO 1412 BY 1 STEP 460 0 ;
14 ROW ROW_7 unithd 5520 29920 N DO 1412 BY 1 STEP 460 0 ;
15 ROW ROW_8 unithd 5520 32640 FS DO 1412 BY 1 STEP 460 0 ;
16 ROW ROW_9 unithd 5520 35360 N DO 1412 BY 1 STEP 460 0 ;
17 ROW ROW_10 unithd 5520 38080 FS DO 1412 BY 1 STEP 460 0 ;
18 ROW ROW_11 unithd 5520 40800 N DO 1412 BY 1 STEP 460 0 ;
19 ROW ROW_12 unithd 5520 43520 FS DO 1412 BY 1 STEP 460 0 ;
20 ROW ROW_13 unithd 5520 46240 N DO 1412 BY 1 STEP 460 0 ;
21 ROW ROW_14 unithd 5520 48960 FS DO 1412 BY 1 STEP 460 0 ;
22 ROW ROW_15 unithd 5520 51680 N DO 1412 BY 1 STEP 460 0 ;
23 ROW ROW_16 unithd 5520 54400 FS DO 1412 BY 1 STEP 460 0 ;
24 ROW ROW_17 unithd 5520 57120 N DO 1412 BY 1 STEP 460 0 ;
25 ROW ROW_18 unithd 5520 59840 FS DO 1412 BY 1 STEP 460 0 ;

```

According to floorplan def

3. Load generated floorplan def in magic tool and explore the floorplan.

Commands to load floorplan def in magic in another terminal

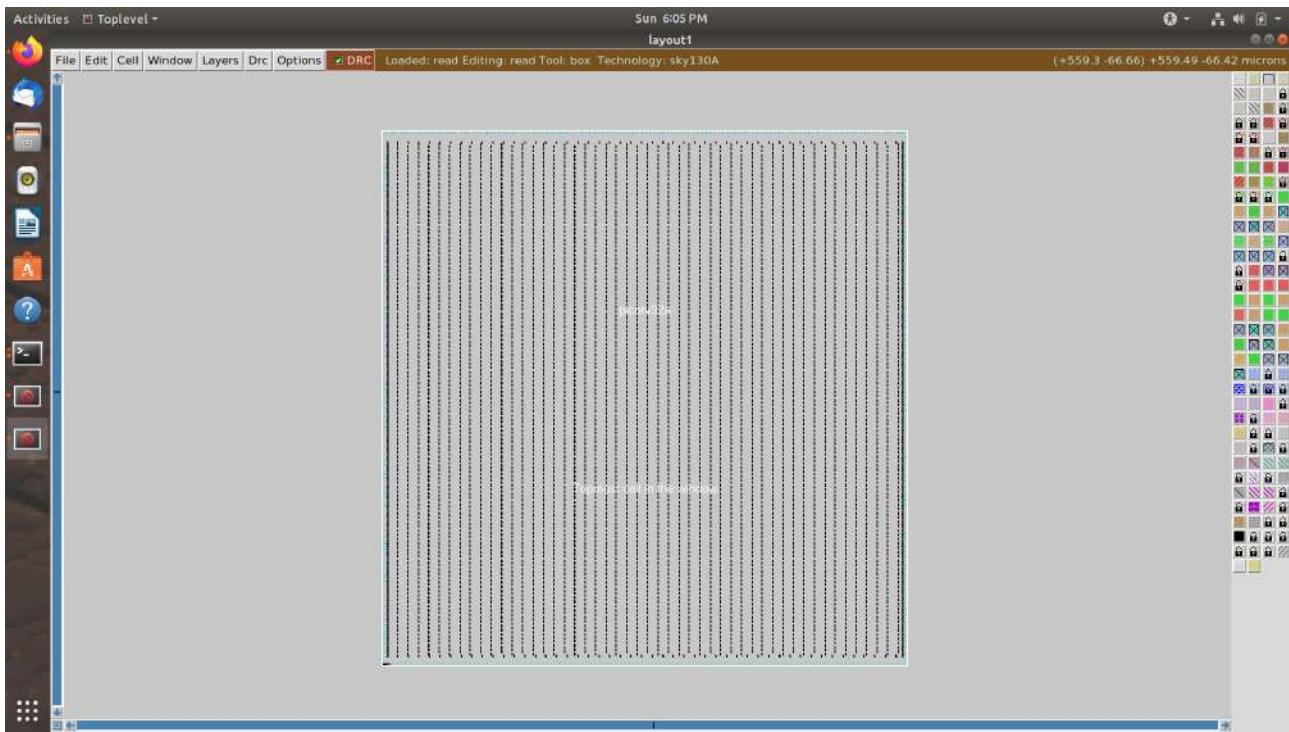
```
# Change directory to path containing generated floorplan def
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
17-03_12-06/results/floorplan/
```

```
# Command to load the floorplan def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.floorplan.def &
```

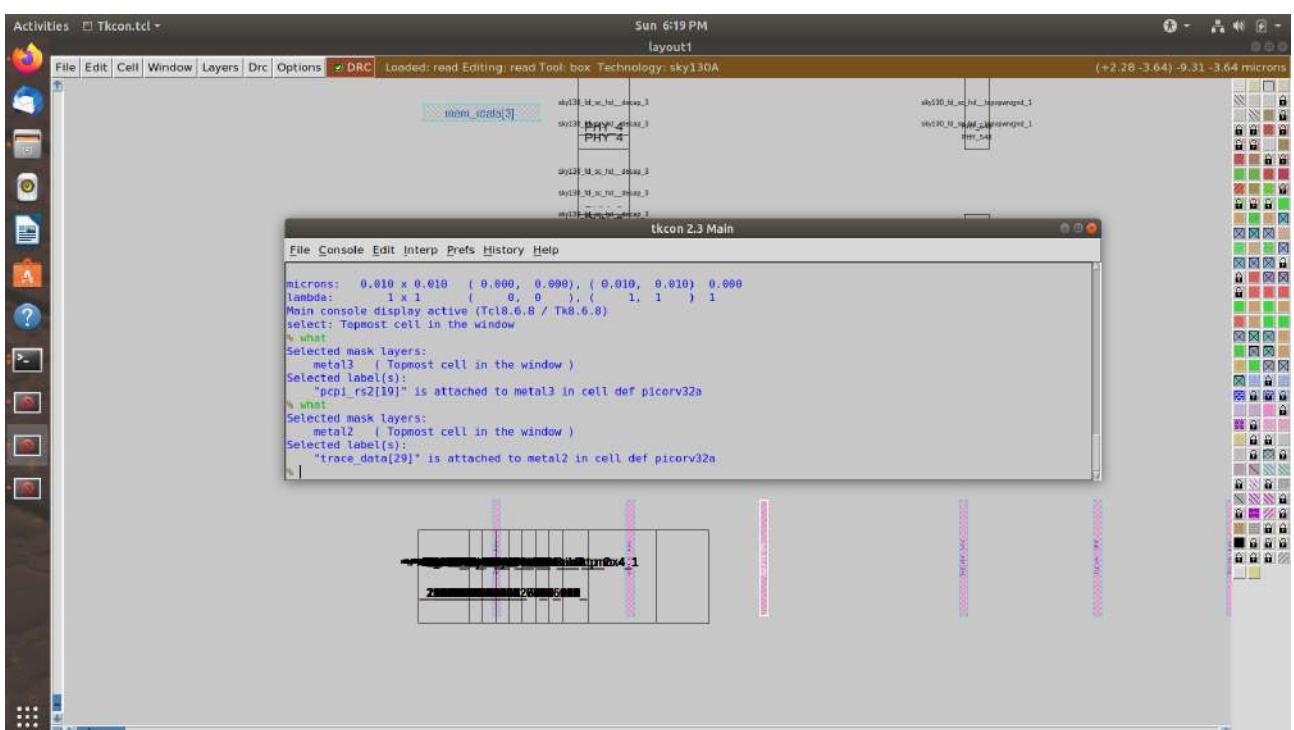
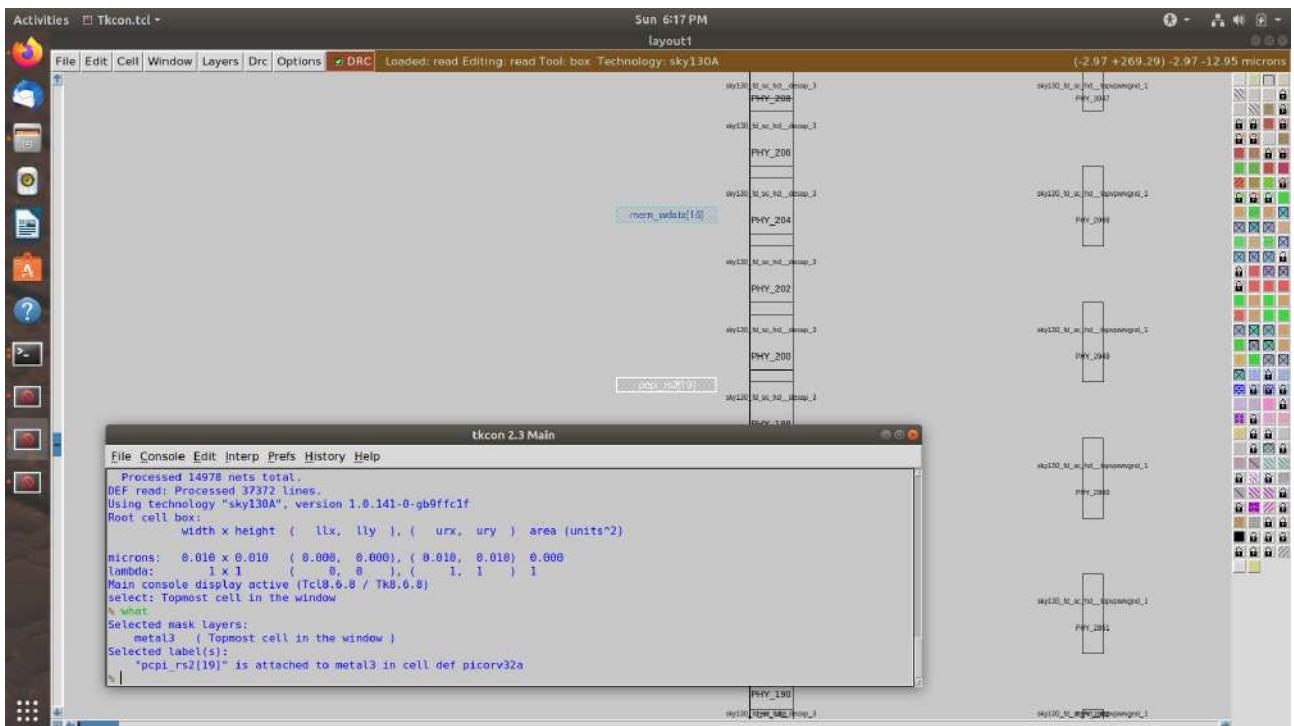
Screenshots of floorplan def in magic



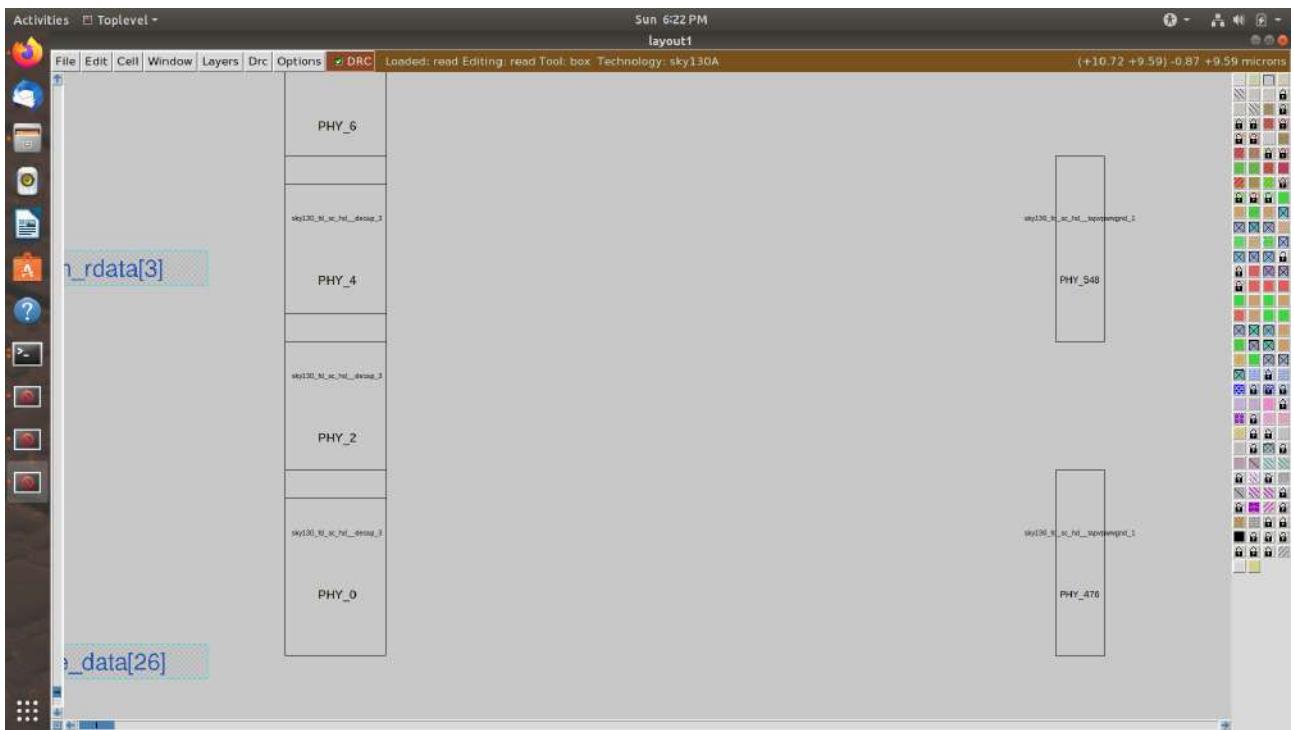
Equidistant placement of ports



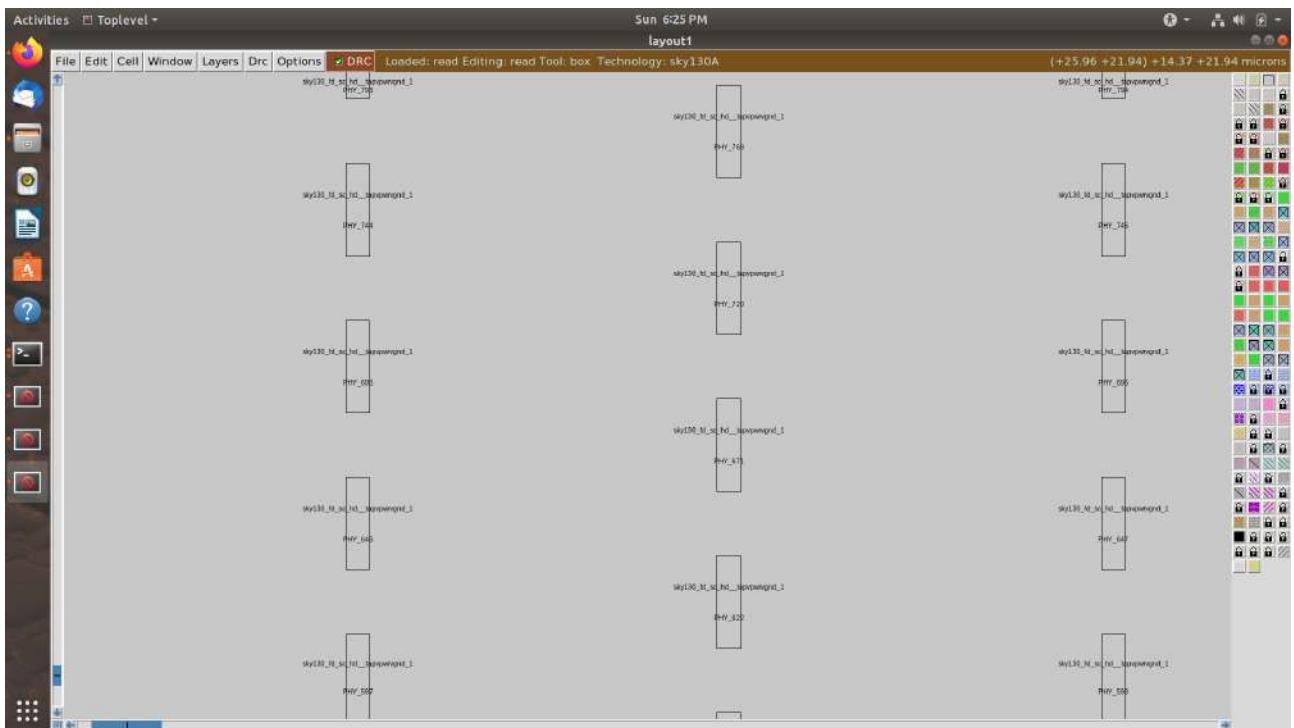
Port layer as set through config.tcl



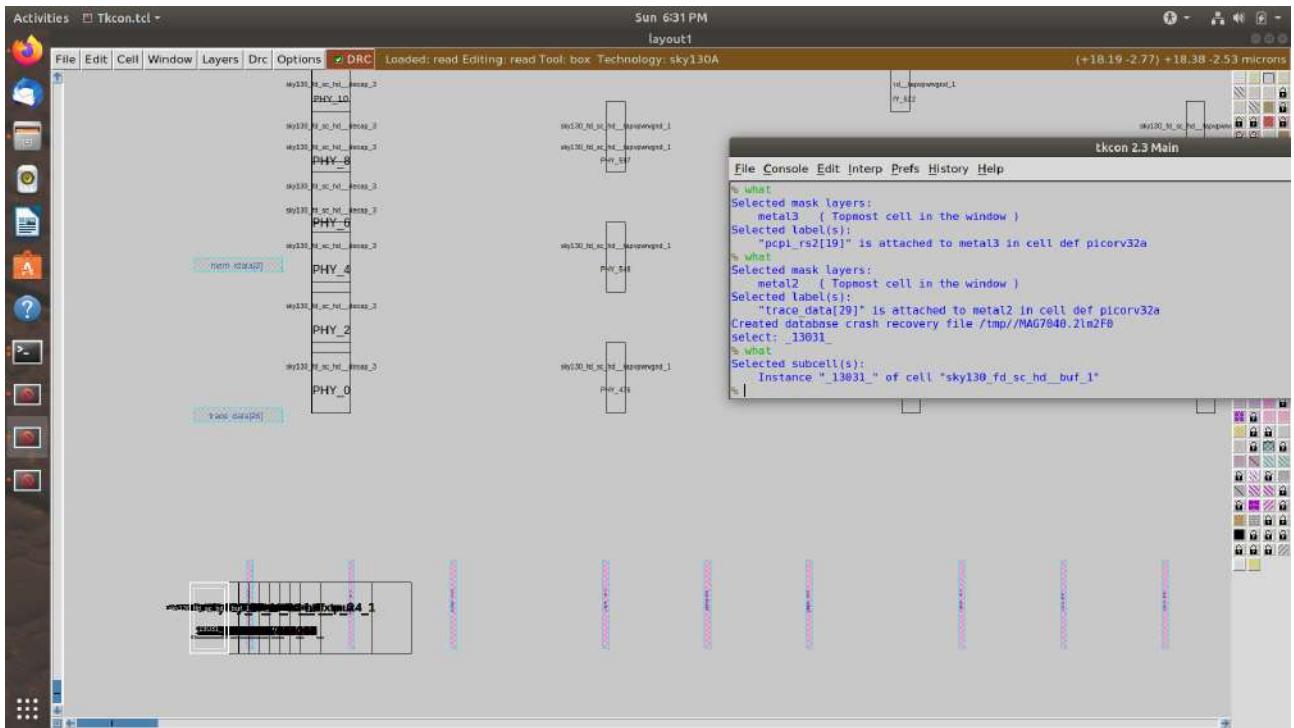
Decap Cells and Tap Cells



Diagonally equidistant Tap cells



Unplaced standard cells at the origin



4. Run 'picorv32a' design congestion aware placement using OpenLANE flow and generate necessary outputs.

Command to run placement

```
# Congestion aware placement by default
```

```
run_placement
```

Screenshots of placement run

```
Activities Terminal - Sun 10:44 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
er stripe. Moving to closest stripe at (567.000um, 103.880um).
[WARNING PSM-0030] Vsrc location at (565.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 257.060um).
[WARNING PSM-0030] Vsrc location at (5.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (145.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
[WARNING PSM-0030] Vsrc location at (425.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 563.420um).
[INFO PSM-0031] Number of nodes on net VGND = 19223.
[INFO PSM-0037] G matrix created sucessfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/floorplan/picorv32a.floorplan.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/floorplan/7-pdn.def
1
::: % run_placement
```

```
Activities Terminal - Sun 10:46 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
legalized HPWL      779196.5 u
delta HPWL          2 %

[INFO DPL-0020] Mirrored 6193 instances
[INFO DPL-0021] HPWL before      779196.5 u
[INFO DPL-0022] HPWL after       766080.0 u
[INFO DPL-0023] HPWL delta      -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/tmp/placement/8-resizer.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 12
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/17-03_12-06/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
::: %
```

5. Load generated placement def in magic tool and explore the placement.

Commands to load placement def in magic in another terminal

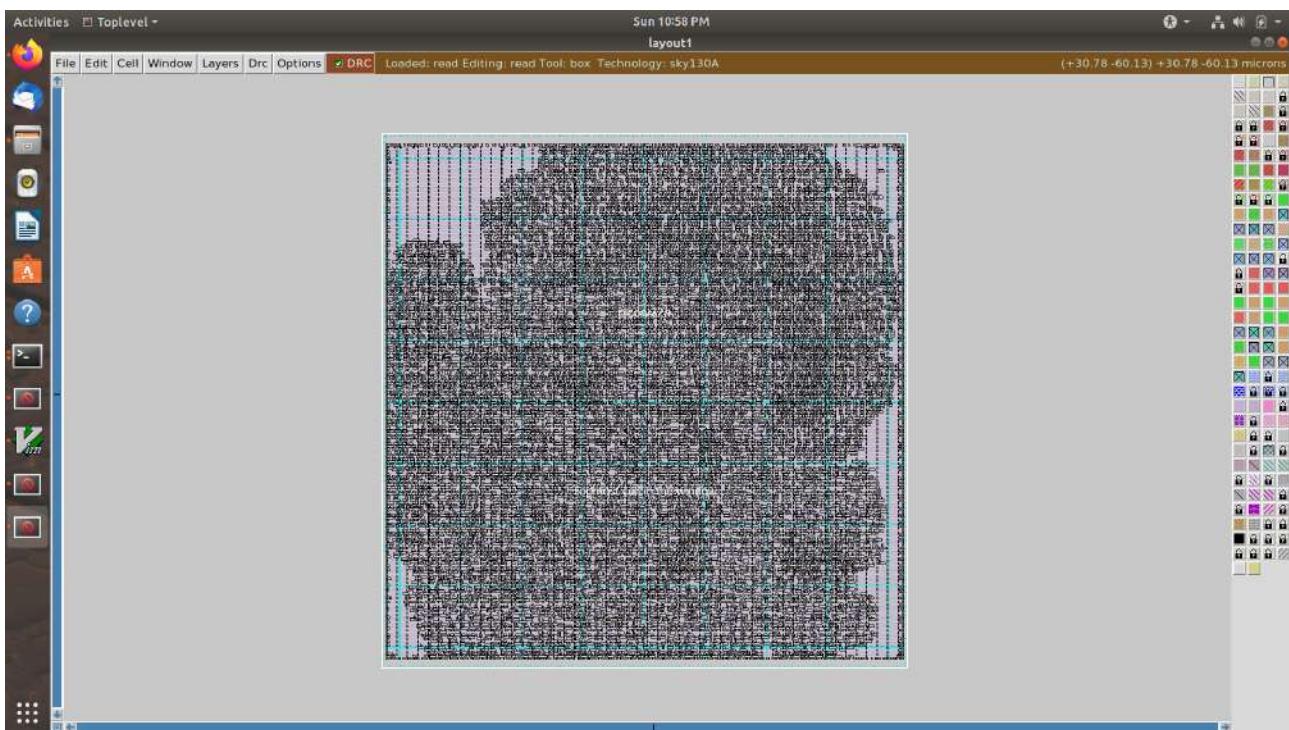
```
# Change directory to path containing generated placement def
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/  
17-03_12-06/results/placement/
```

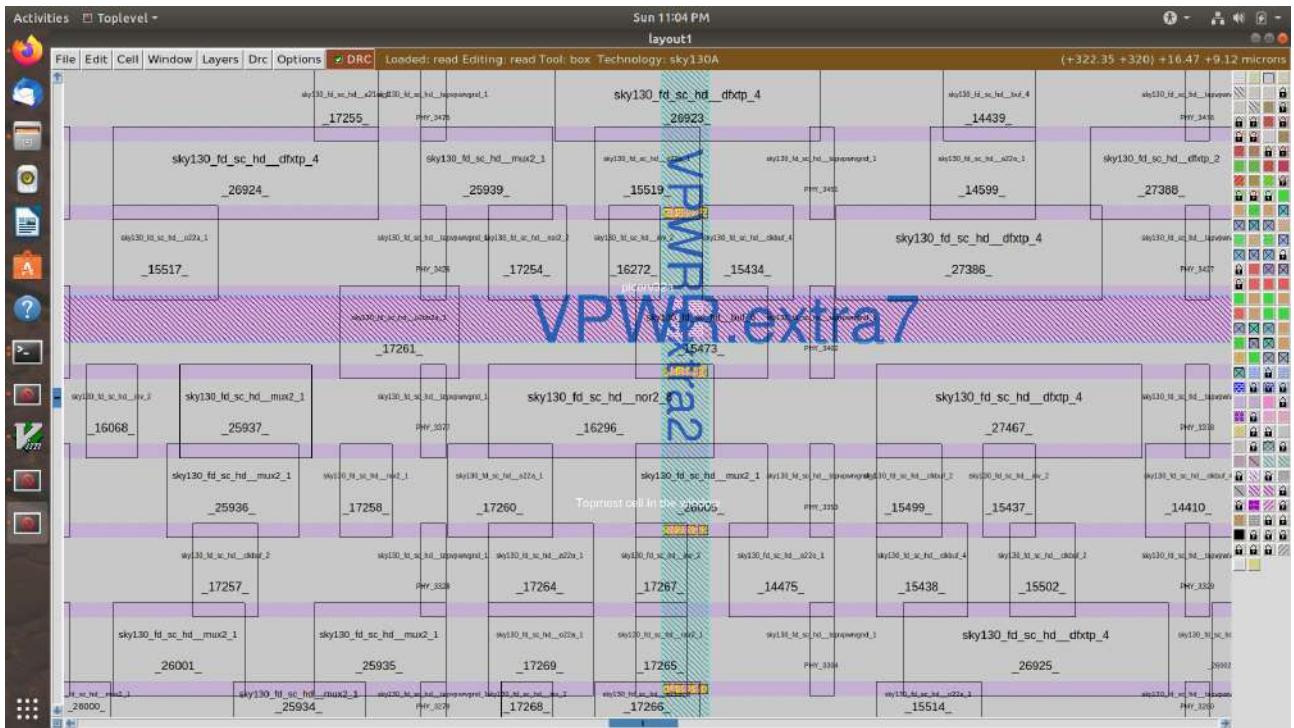
```
# Command to load the placement def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def  
&
```

Screenshots of floorplan def in magic



Standard cells legally placed



Commands to exit from current run

```
# Exit from OpenLANE flow
```

```
exit
```

```
# Exit from OpenLANE flow docker sub-system
```

```
exit
```

Section 3 - Design library cell using Magic Layout and ngspice characterization (18/03/2024 - 21/03/2024)

Theory

Implementation

- **Section 3 tasks:-**
- 6. Clone custom inverter standard cell design from github repository: [Standard cell design and characterization using OpenLANE flow.](#)
- 7. Load the custom inverter layout in magic and explore.
- 8. Spice extraction of inverter in magic.
- 9. Editing the spice model file for analysis through simulation.
- 10. Post-layout ngspice simulations.
- 11. Find problem in the DRC section of the old magic tech file for the skywater process and fix them.
- Section 3 - Tasks 1 to 5 files, reports and logs can be found in the following folder:

[Section 3 - Tasks 1 to 5 \(vsdstdcelldesign\)](#)

- Section 3 - Task 6 files, reports and logs can be found in the following folder:

[Section 3 - Task 6 \(drc_tests\)](#)

1. Clone custom inverter standard cell design from github repository

```
# Change directory to openlane
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# Clone the repository with custom inverter design
```

```
git clone https://github.com/nickson-jose/vsdstdcelldesign
```

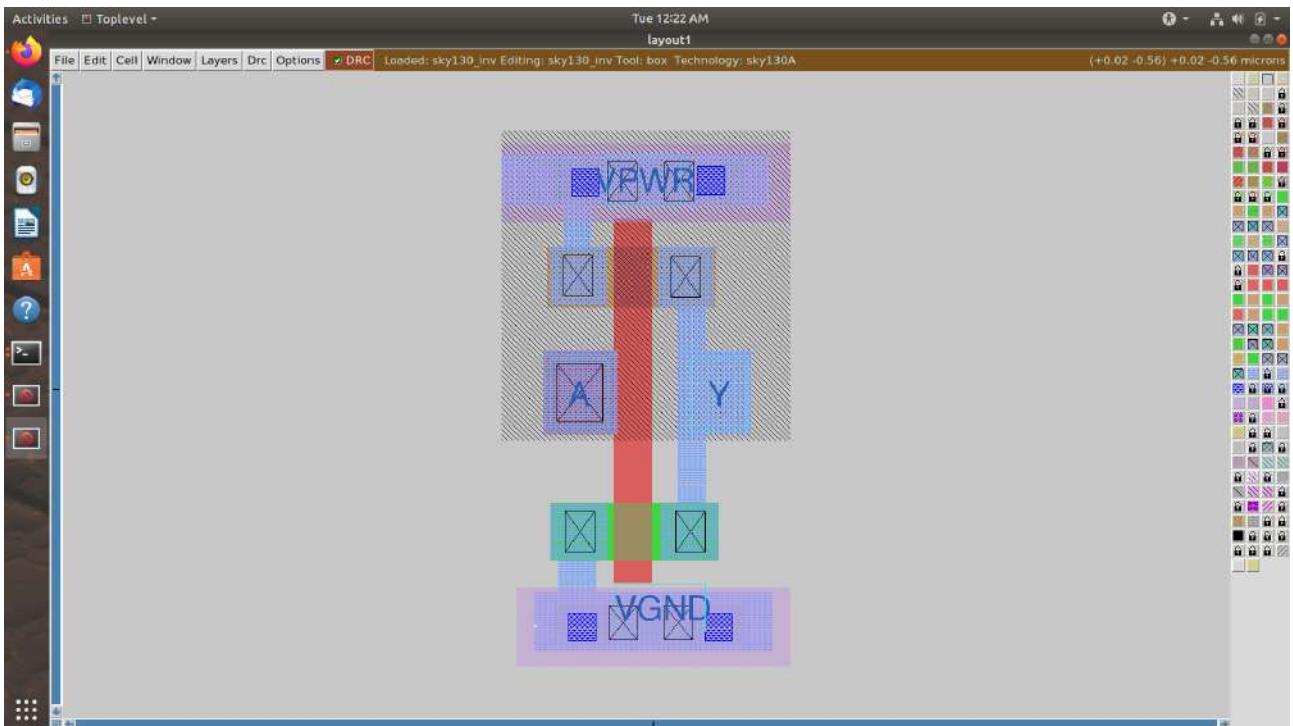
```
# Change into repository directory  
  
cd vsdstdcelldesign  
  
# Copy magic tech file to the repo directory for easy access  
  
cp /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/  
magic/sky130A.tech .  
  
# Check contents whether everything is present  
  
ls  
  
# Command to open custom inverter layout in magic  
  
magic -T sky130A.tech sky130_inv.mag &
```

Screenshot of commands run

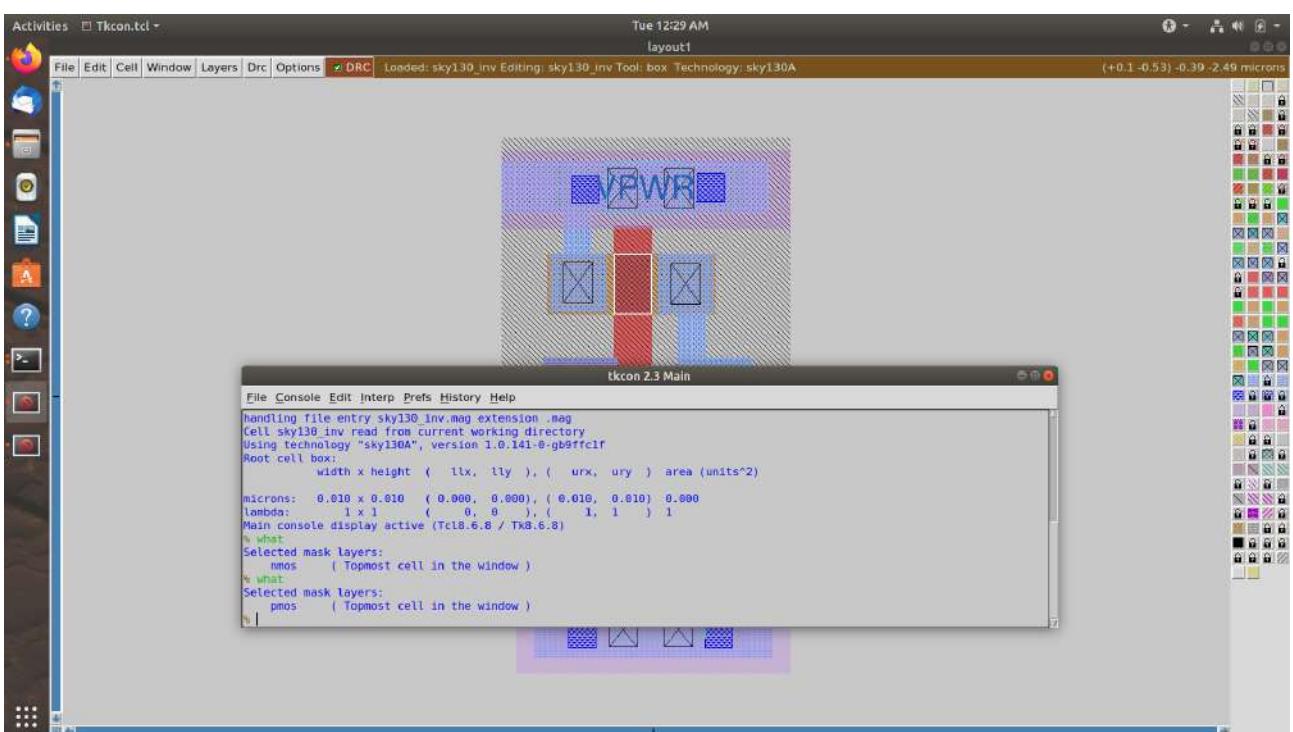
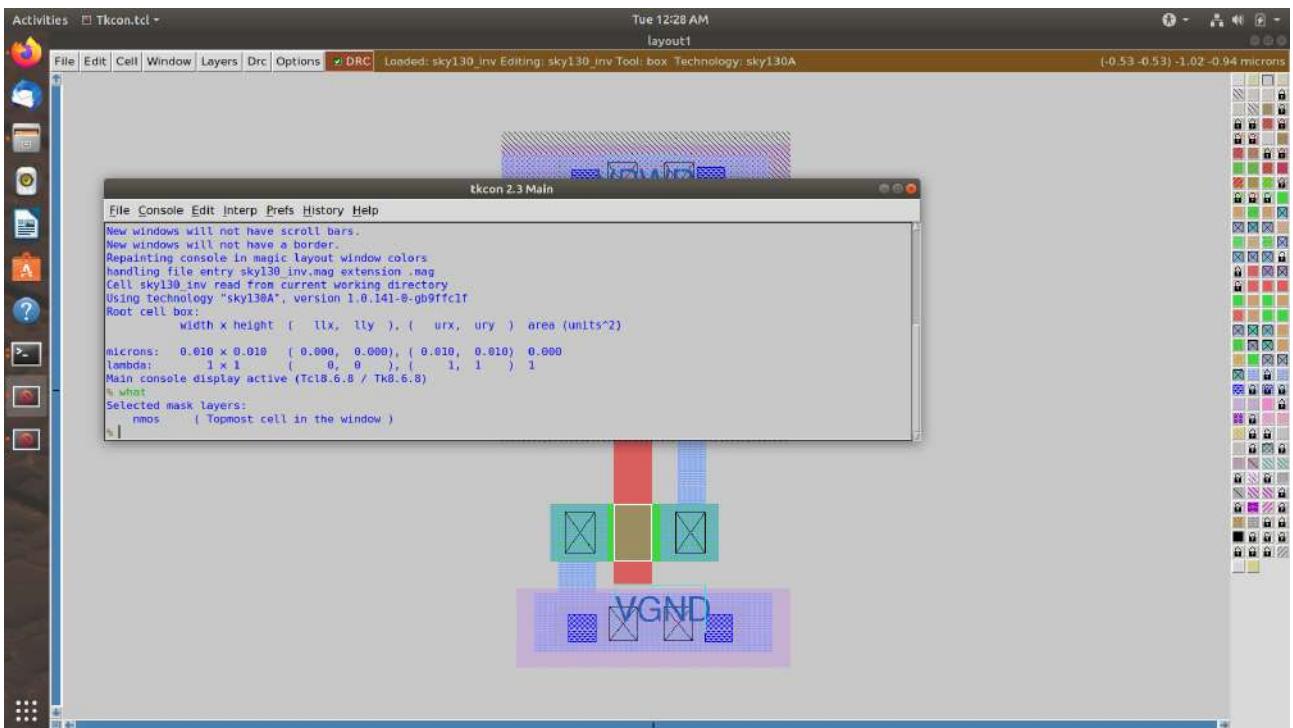
```
Activities Terminal Tue 12:22 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ git clone https://github.com/nickson-jose/vsdstdcelldesign
Cloning into 'vsdstdcelldesign'...
remote: Enumerating objects: 492, done.
remote: Counting objects: 100% (18/18), done.
remote: Compressing objects: 100% (18/18), done.
remote: Total 492 (delta 7), reused 0 (delta 0), pack-reused 474
Receiving objects: 100% (492/492), 24.08 MiB | 480.00 KiB/s, done.
Resolving deltas: 100% (210/210), done.
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd vsdstdcelldesign
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cp /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/magic/sky130A.tech .
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls
extras Images libs LICENSE README.md sky130A.tech sky130_inv.mag
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ magic -T sky130A.tech sky130_inv.mag &
[1] 4495
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```

2. Load the custom inverter layout in magic and explore.

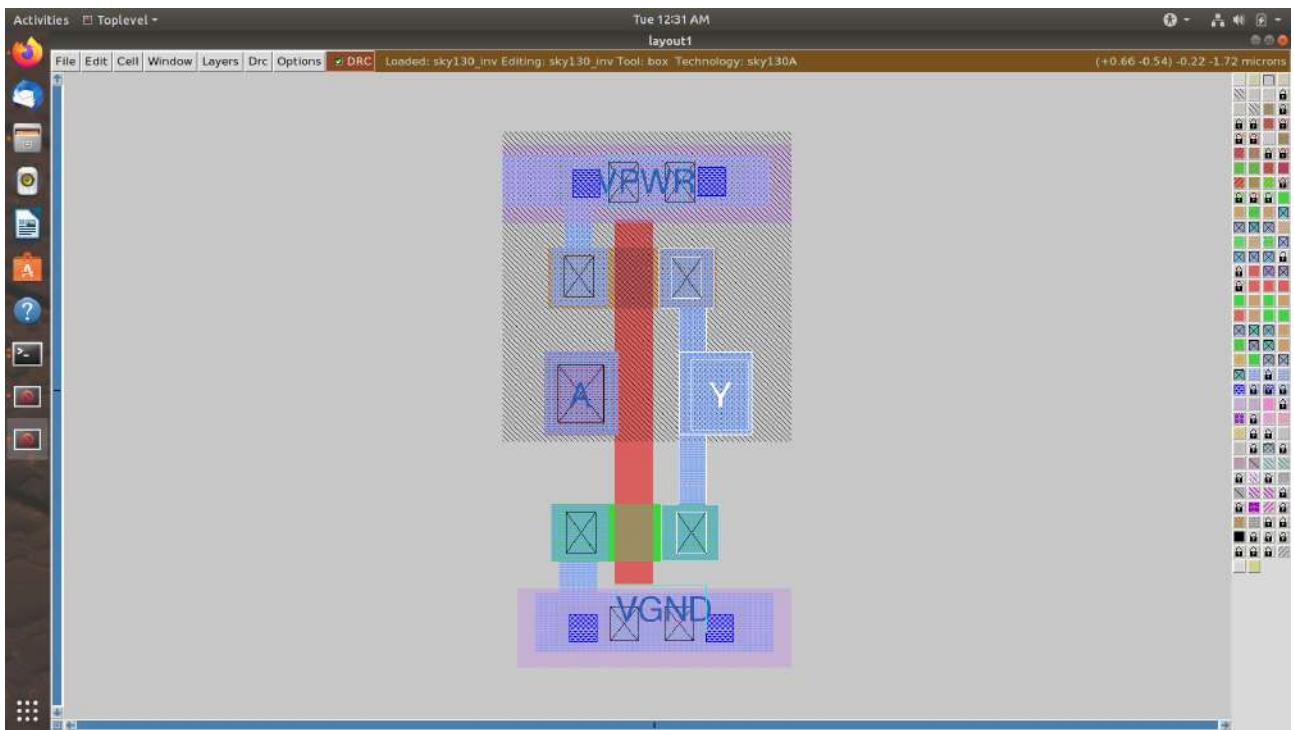
Screenshot of custom inverter layout in magic



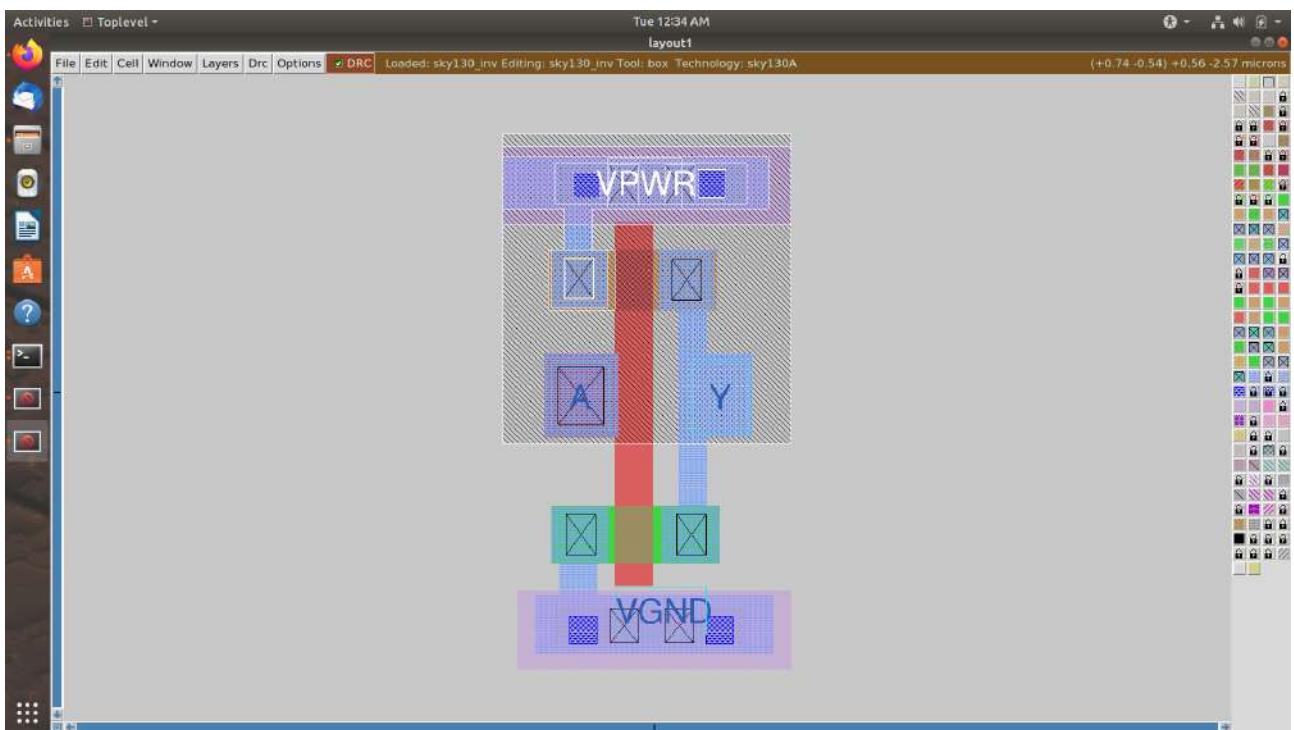
NMOS and PMOS identified



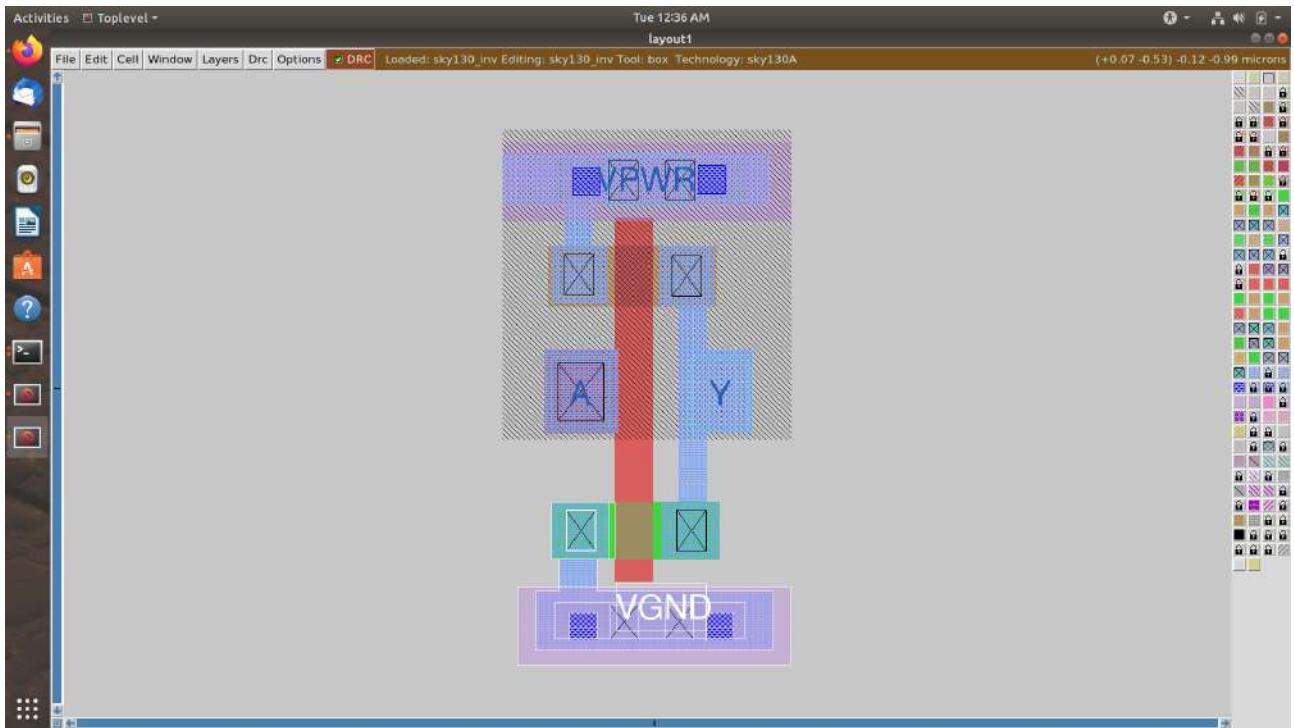
Output Y connectivity to PMOS and NMOS drain verified



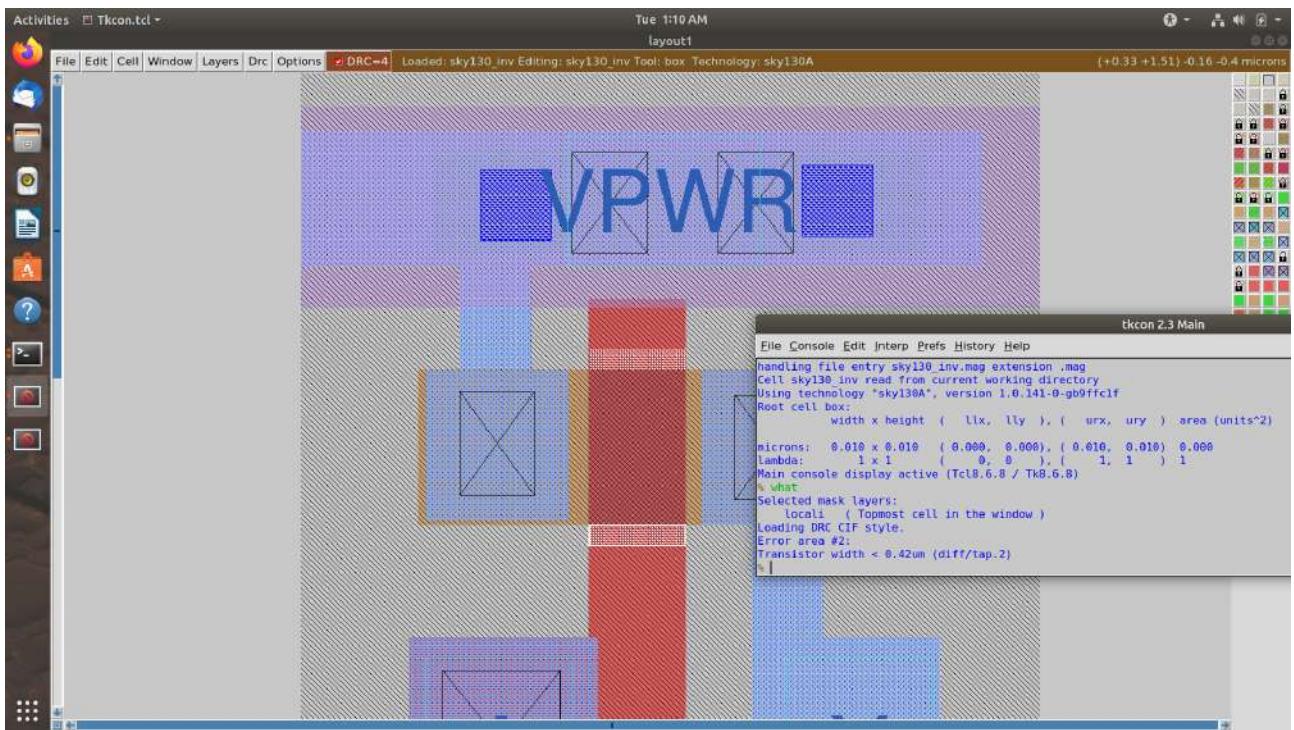
PMOS source connectivity to VDD (here VPWR) verified



NMOS source connectivity to VSS (here VGND) verified



Deleting necessary layout part to see DRC error



3. Spice extraction of inverter in magic.

Commands for spice extraction of the custom inverter layout to be used in tkcon window of magic

```
# Check current directory
```

pwd

```
# Extraction command to extract to .ext format
```

extract all

Before converting ext to spice this command enable the parasitic extraction also

`ext2splice cthresh 0 rthresh 0`

Converting to ext to spice

ext2spice

Screenshot of tkcon window after running above commands

```
Activities □ Tkcon.tcl - Tue 1:24 AM
tkcon 2.3 Main

File Console Edit Interp Prefs History Help
loading history file ... 16 events added
Use openmwrapper to create a new GUI-based layout window
Use closerwrapper to remove a new GUI-based layout window

Magic 8.3 revision 400 - Compiled on Mon May 22 20:58:24 IST 2023.
Starting magic under Tcl Interpreter
Using Tk console window
Using TrueColor, VisualID 0x21 depth 24
Input style sky130(): scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
    nmos obsactive mvobsactive obsl1l obsml obsm2 obsm3 obsm4 obsm5 obsnndl ubm fillblock comment obscomment res8p35 res8p69 reslp41 res2p85 res5p73
Processing system .magicrc file
New windows will not have a title caption.
New windows will not have scroll bars.
New windows will not have a border.
Repainting console in magic layout window colors
handling file entry sky130_inv.mag extension .mag
Cell sky130_inv read from current working directory
Using technology "sky130A", version 1.0.141-0-gb9fffc1f
Root cell box:
    width x height ( llx, lly ),( urx, ury ) area (units^2)
microns: 0.010 x 0.010 ( 0.000, 0.000), ( 0.010, 0.010) 0.000
lambda: 1 x 1 ( 0, 0 ), ( 1, 1 ) 1
Main console display active (Tcl8.6.8 / Tk8.6.8)
    ped
/home/vsdsuser/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
    extract all
Extracting sky130_inv into sky130_inv.ext:
% ext2spice cthresh 0 rthresh 0
% ext2spice
ext2spice finished.
%
```

Screenshot of created spice file

Activities ▾ GVim -

Tue 1:27 AM

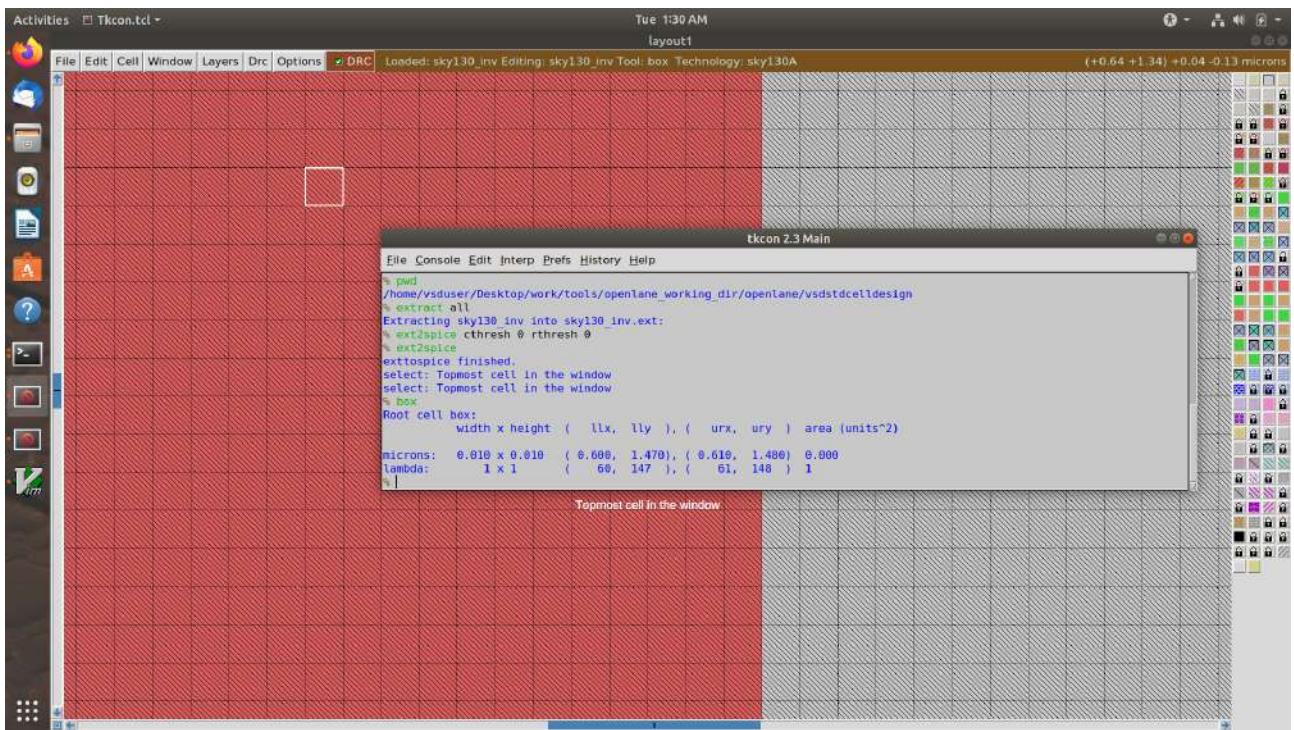
sky130_inv.spice (~/Desktop/work/tools/op...ing_dlr/openlane/vsdstdcelldesign) - GVIM

File Edit Tools Syntax Buffers Window Help

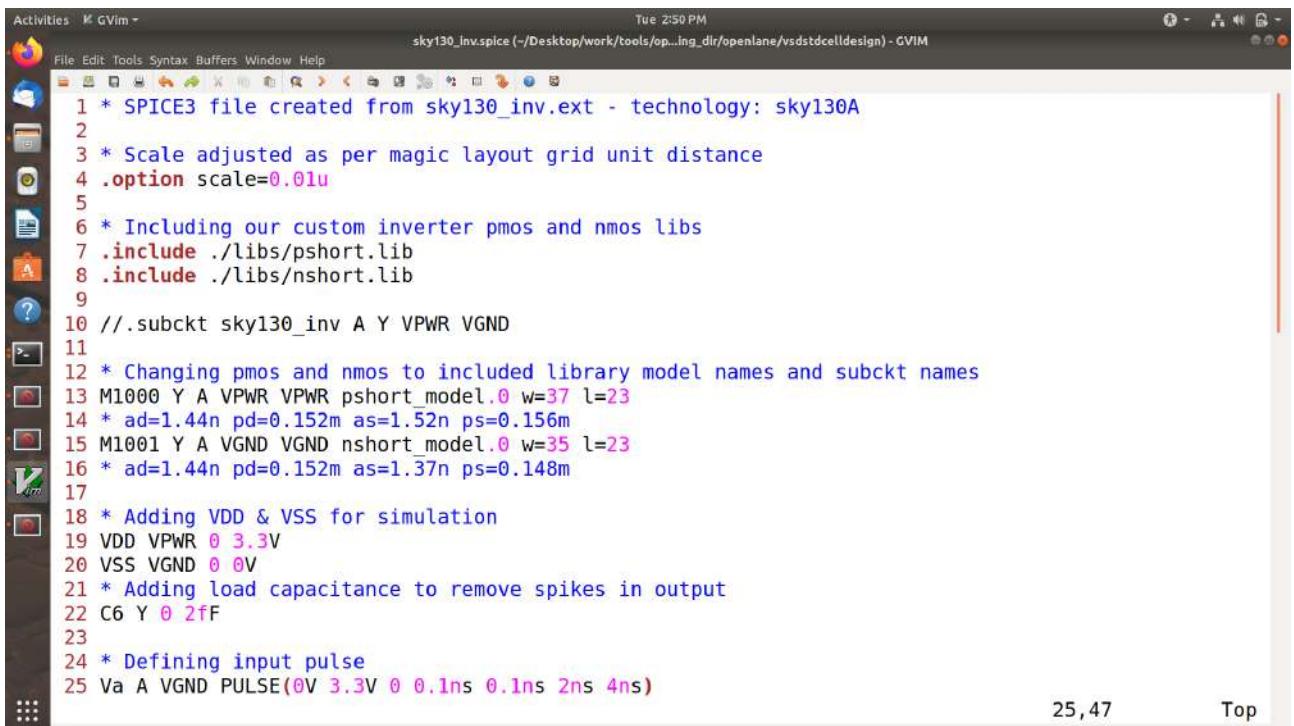
```
1 * SPICE3 file created from sky130_inv.ext - technology: sky130A
2
3 .option scale=10m
4
5 .subckt sky130_inv A Y VPWR VGND
6 X0 Y A VGND VGND sky130_fd_pr_nfet_01v8 ad=1.44n pd=0.152m as=1.37n ps=0.148m w=35 l=23
7 X1 Y A VPWR VPWR sky130_fd_pr_pfet_01v8 ad=1.44n pd=0.152m as=1.52n ps=0.156m w=37 l=23
8 C0 A VPWR 0.0774f
9 C1 Y VPWR 0.117f
10 C2 A Y 0.0754f
11 C3 Y VGND 0.279f
12 C4 A VGND 0.45f
13 C5 VPWR VGND 0.781f
14 .ends
```

4. Editing the spice model file for analysis through simulation.

Measuring unit distance in layout grid



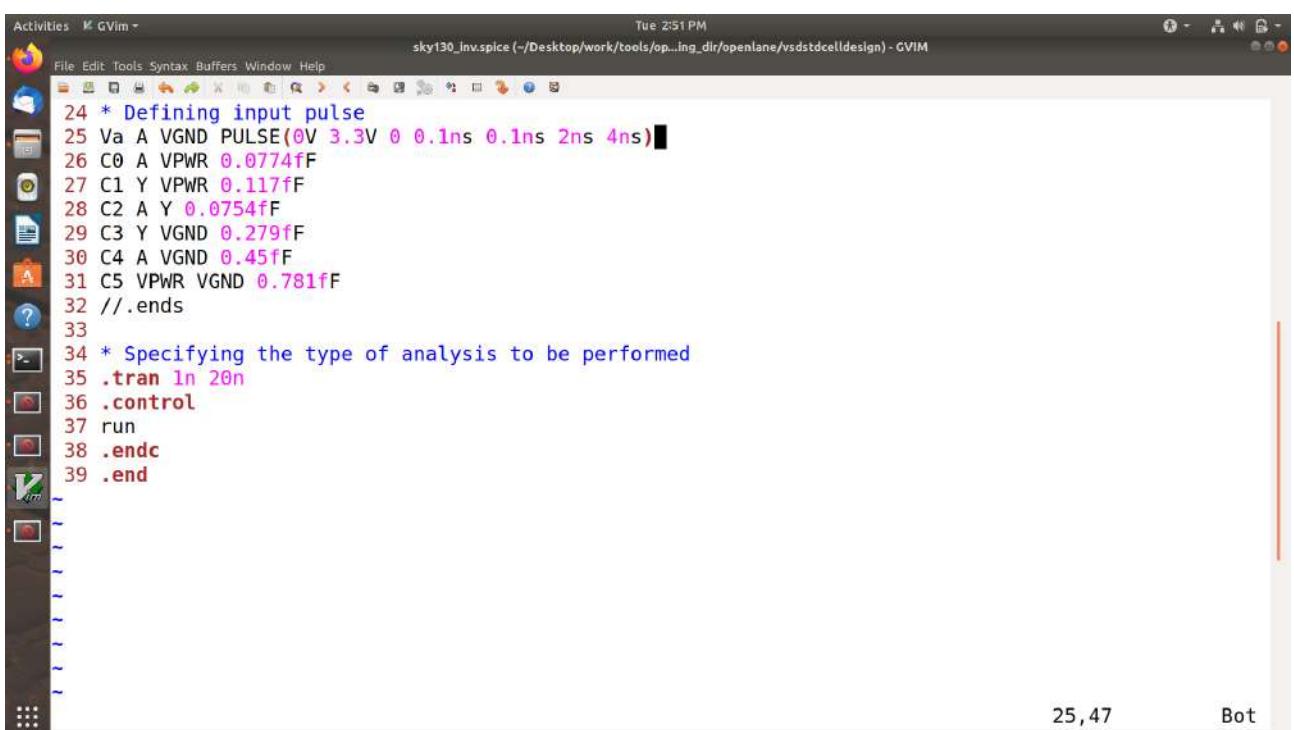
Final edited spice file ready for ngspice simulation



```
Activities  M GVim - Tue 2:50 PM
sky130_inv.spice (~/Desktop/work/tools/op...ing_dir/openlane/vsdstdcelldesign) - GVIM
File Edit Tools Syntax Buffers Window Help
1 * SPICE3 file created from sky130_inv.ext - technology: sky130A
2
3 * Scale adjusted as per magic layout grid unit distance
4 .option scale=0.01u
5
6 * Including our custom inverter pmos and nmos libs
7 .include ./libs/pshort.lib
8 .include ./libs/nshort.lib
9
10 // .subckt sky130_inv A Y VPWR VGND
11
12 * Changing pmos and nmos to included library model names and subckt names
13 M1000 Y A VPWR VPWR pshort_model.0 w=37 l=23
14 * ad=1.44n pd=0.152m as=1.52n ps=0.156m
15 M1001 Y A VGND VGND nshort_model.0 w=35 l=23
16 * ad=1.44n pd=0.152m as=1.37n ps=0.148m
17
18 * Adding VDD & VSS for simulation
19 VDD VPWR 0 3.3V
20 VSS VGND 0 0V
21 * Adding load capacitance to remove spikes in output
22 C6 Y 0 2fF
23
24 * Defining input pulse
25 Va A VGND PULSE(0V 3.3V 0 0.1ns 0.1ns 2ns 4ns)
26
27
28
29
30
31
32 // .ends
33
34 * Specifying the type of analysis to be performed
35 .tran 1n 20n
36 .control
37 run
38 .endc
39 .end
```

25,47

Top



```
Activities  M GVim - Tue 2:51 PM
sky130_inv.spice (~/Desktop/work/tools/op...ing_dir/openlane/vsdstdcelldesign) - GVIM
File Edit Tools Syntax Buffers Window Help
24 * Defining input pulse
25 Va A VGND PULSE(0V 3.3V 0 0.1ns 0.1ns 2ns 4ns)■
26 C0 A VPWR 0.0774fF
27 C1 Y VPWR 0.117fF
28 C2 A Y 0.0754fF
29 C3 Y VGND 0.279fF
30 C4 A VGND 0.45fF
31 C5 VPWR VGND 0.781fF
32 // .ends
33
34 * Specifying the type of analysis to be performed
35 .tran 1n 20n
36 .control
37 run
38 .endc
39 .end
```

25,47

Bot

5. Post-layout ngspice simulations.

Commands for ngspice simulation

```
# Command to directly load spice file for simulation to ngspice
```

```
ngspice sky130_inv.spice
```

```
# Now that we have entered ngspice with the simulation spice file loaded we just have to  
load the plot
```

```
plot y vs time a
```

Screenshots of ngspice run

```

Activities Terminal - vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ngspice sky130_inv.spice
*****
** ngspice-27 : Circuit level simulation program
** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California.
** Please get your ngspice manual from http://ngspice.sourceforge.net/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Tue Dec 26 17:10:20 UTC 2017
*****
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node Voltage
-----
y 3.3
a 0
vpwr 3.3
vgnd 0
va#branch 0

```

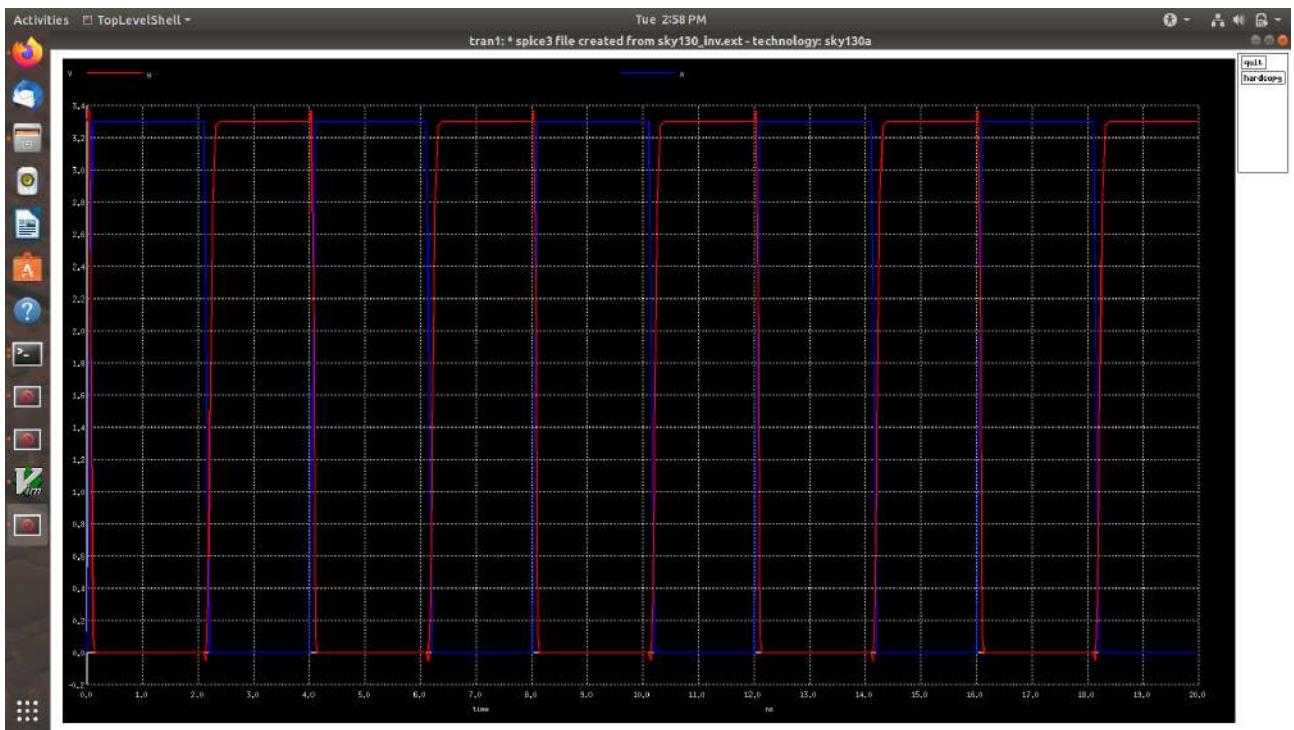
```

Activities TopLevelShell - vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ 
*****
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node Voltage
-----
y 3.3
a 0
vpwr 3.3
vgnd 0
va#branch 0
vss#branch 3.32351e-12
vdd#branch -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
::: ngspice 1 -> 

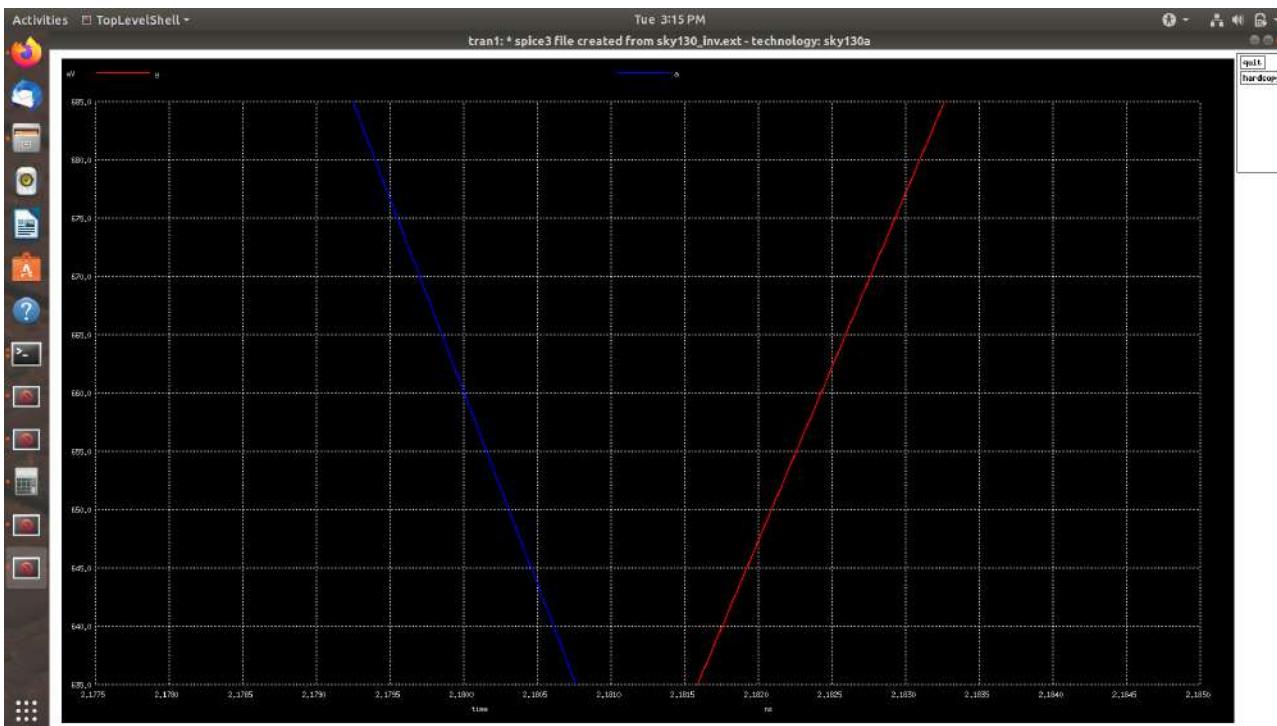
```

Screenshot of generated plot



Rise transition time calculation

20% Screenshots



Activities Terminal -

Tue 3:20 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign

```

File Edit View Search Terminal Help
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a

Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

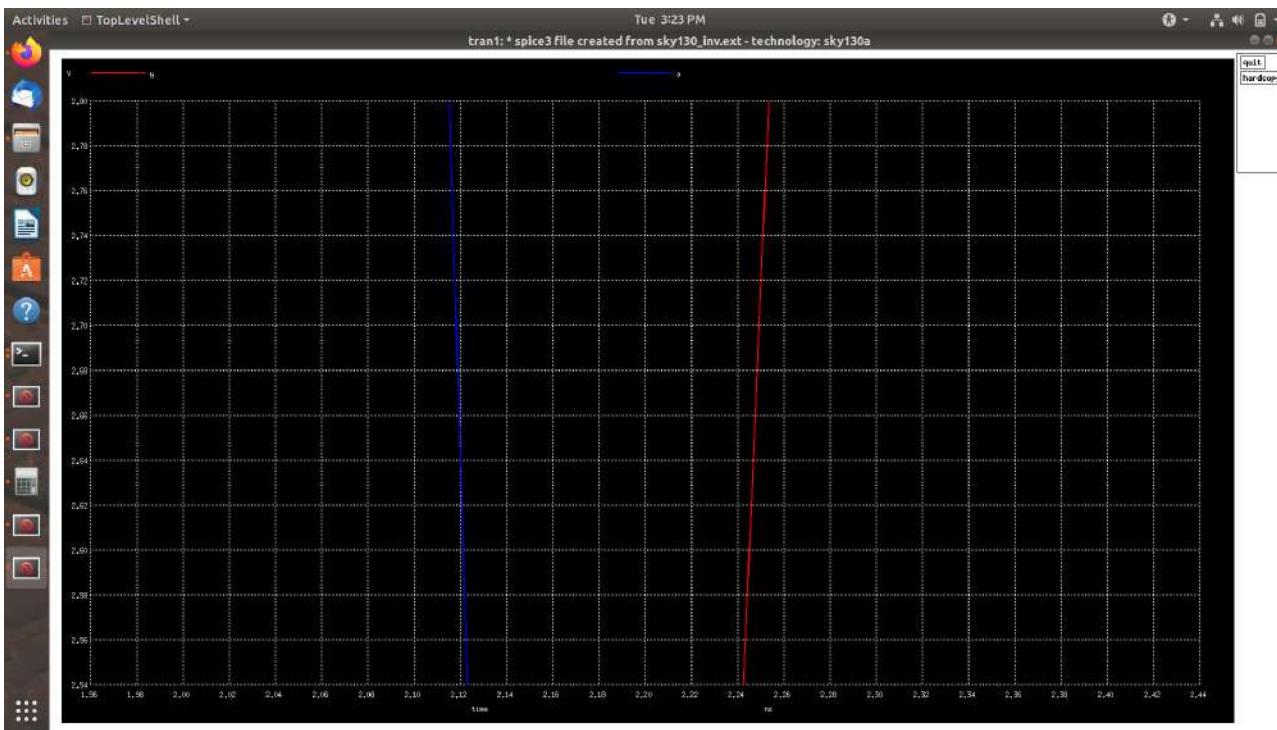
Warning: va: no DC value, transient time 0 value used

Initial Transient Solution
-----
Node          Voltage
---- 
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043

```

80% Screenshots



Activities Terminal -

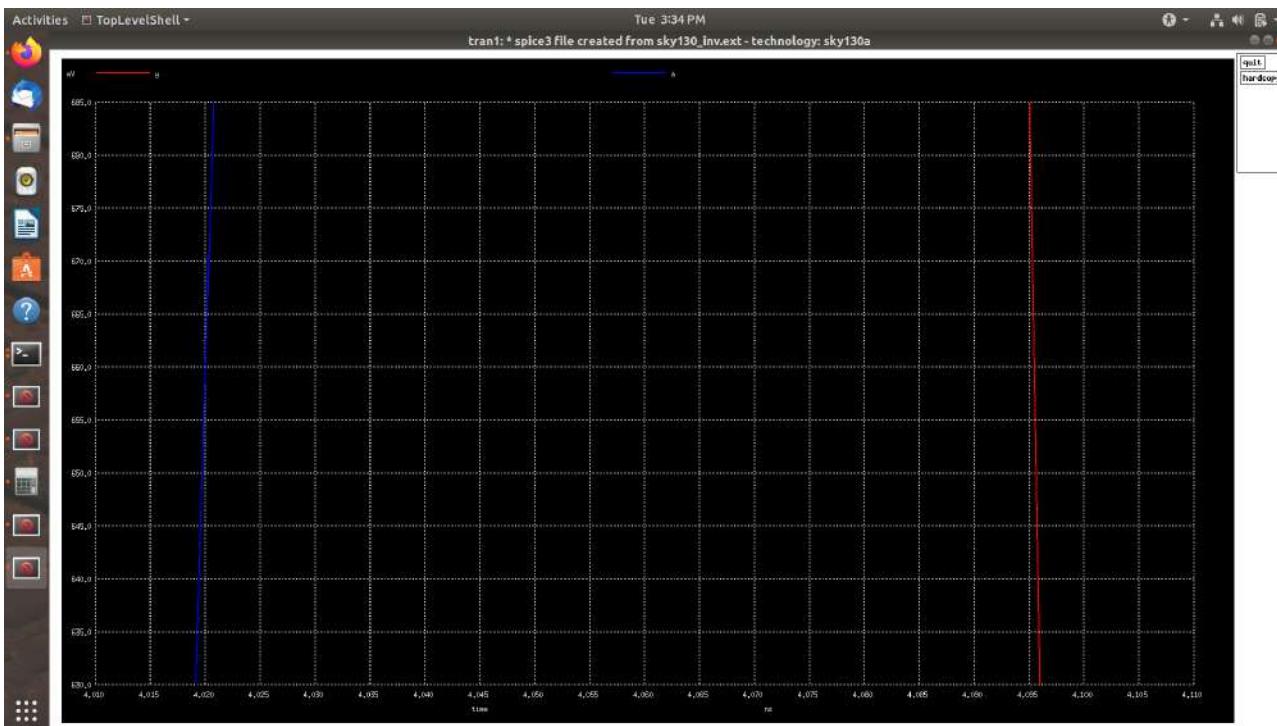
Tue 3:24 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```
File Edit View Search Terminal Help
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node          Voltage
-----
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
```

Fall transition time calculation

20% Screenshots



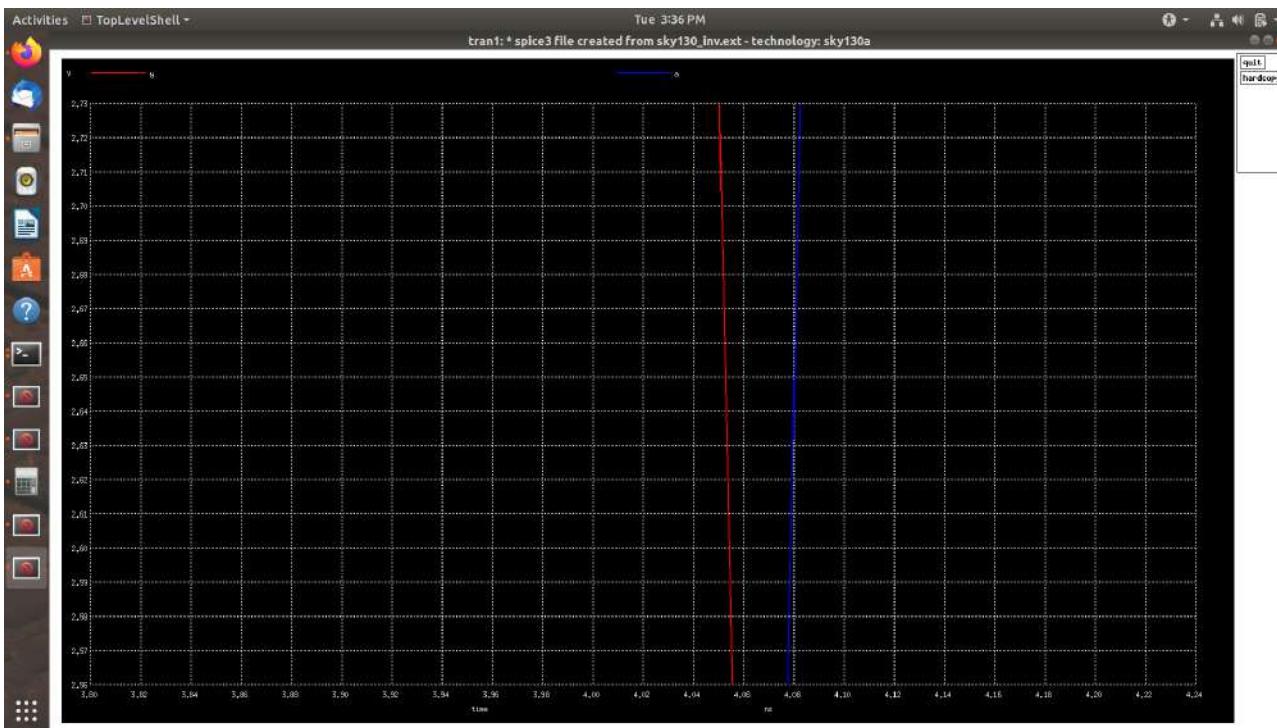
Activities Terminal

Tue 3:34 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```
Warning: va: no DC value, transient time 0 value used
Initial Transient Solution
-----
Node          Voltage
-----
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
x0 = 4.09555e-09, y0 = 0.660127
```

80% Screenshots



Activities Terminal -

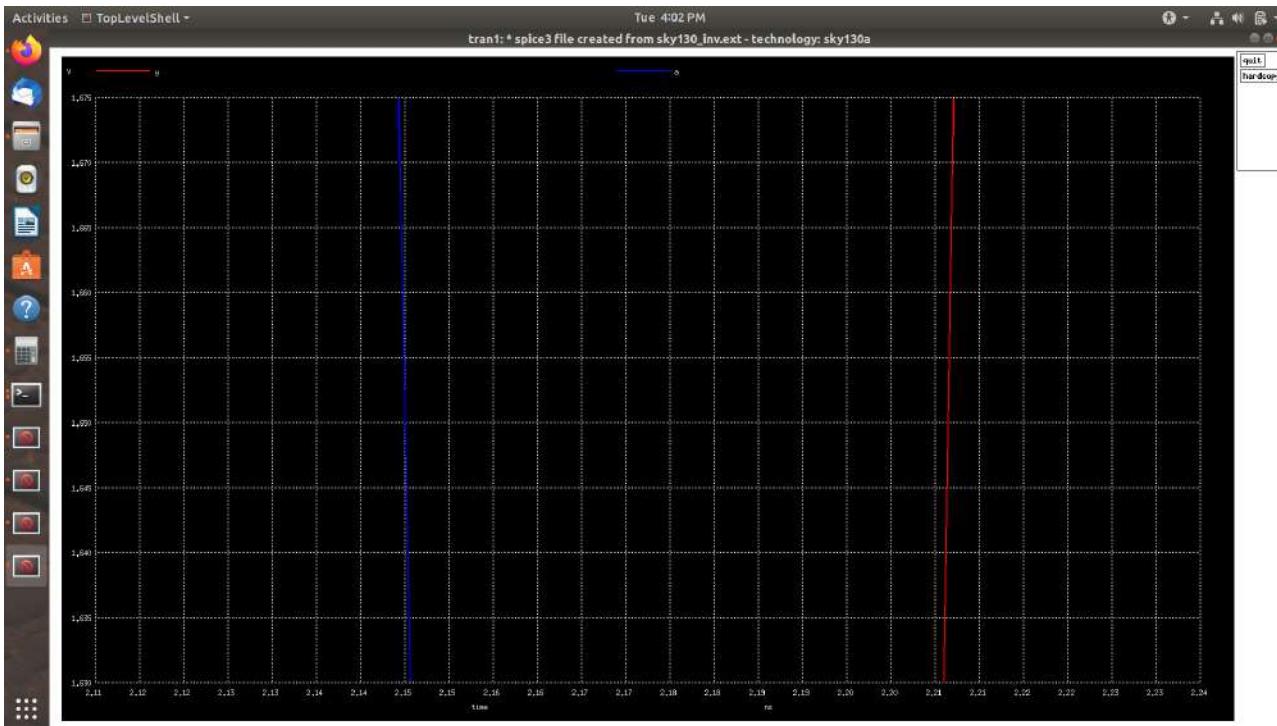
Tue 3:36 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```
Initial Transient Solution
-----
Node          Voltage
-----
y            3.3
a            0
vpwr         3.3
vgnd         0
va#branch    0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
x0 = 4.09555e-09, y0 = 0.660127
x0 = 4.0536e-09, y0 = 2.64
```

Rise Cell Delay Calculation

50% Screenshots



Activities Terminal

Tue 4:03 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign

```

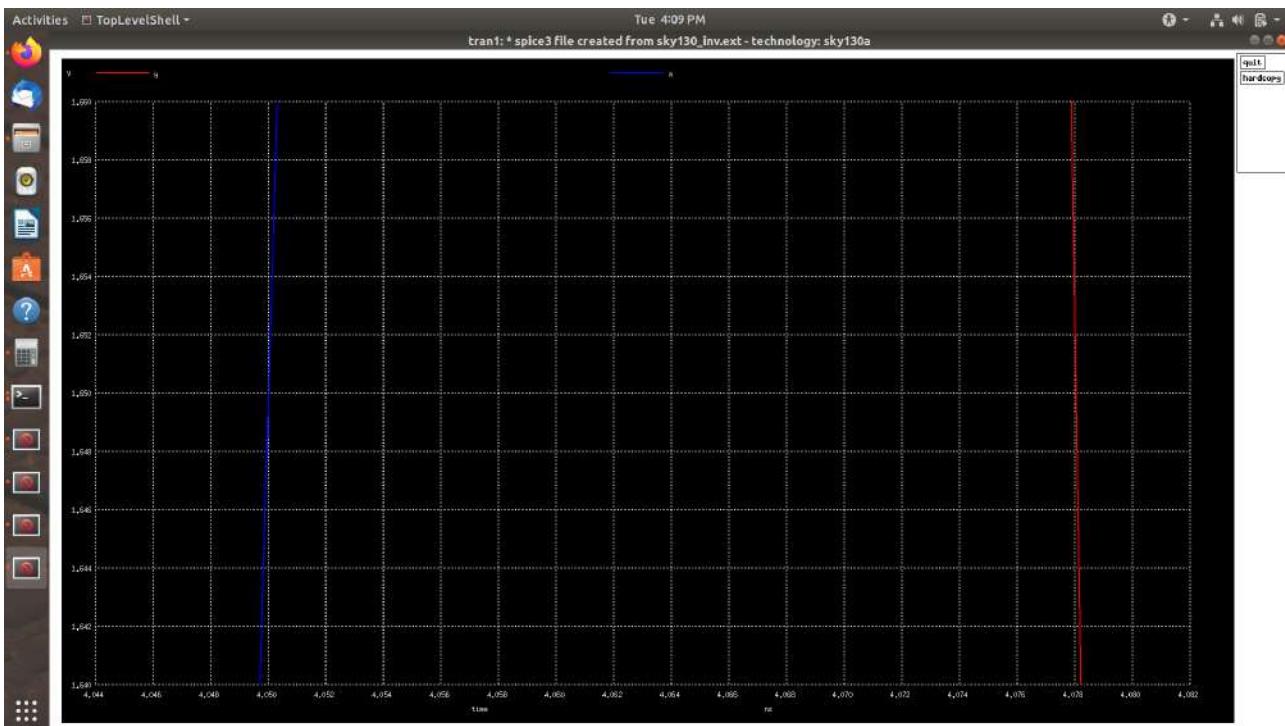
File Edit View Search Terminal Help
Node          Voltage
-----
y             3.3
a             0
vpwr          3.3
vgnd          0
va#branch     0
vss#branch    3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
x0 = 2.24638e-09, y0 = 2.6403
x0 = 4.09555e-09, y0 = 0.660127
x0 = 4.0536e-09, y0 = 2.64
x0 = 2.21144e-09, y0 = 1.65
x0 = 2.15008e-09, y0 = 1.6501

```

Fall Cell Delay Calculation

50% Screenshots



Activities Terminal Tue 4:10 PM

vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdceldesign

```

File Edit View Search Terminal Help
vpwr          3.3
vgnd          0
va#branch     0
vss#branch   3.32351e-12
vdd#branch   -3.32355e-12

No. of Data Rows : 160
ngspice 1 -> plot y vs time a
ngspice 1 ->
x0 = 2.18242e-09, y0 = 0.660043
> x0 = 2.24638e-09, y0 = 2.6403
> x0 = 4.09555e-09, y0 = 0.660127
> x0 = 4.0536e-09, y0 = 2.64
> x0 = 2.21144e-09, y0 = 1.65
> x0 = 2.15008e-09, y0 = 1.6501
> x0 = 4.07807e-09, y0 = 1.65005
> x0 = 4.05e-09, y0 = 1.65002

```

6. Find problem in the DRC section of the old magic tech file for the skywater process and fix them.

Link to Sky130 Periphery rules: <https://skywater-pdk.readthedocs.io/en/main/rules/periphery.html>

Commands to download and view the corrupted skywater process magic tech file and associated files to perform drc corrections

```
# Change to home directory
```

```
cd
```

```
# Command to download the lab files
```

```
wget http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
```

```
# Since lab file is compressed command to extract it
```

```
tar xfz drc_tests.tgz
```

```
# Change directory into the lab folder
```

```
cd drc_tests
```

```
# List all files and directories present in the current directory
```

```
ls -al
```

```
# Command to view .magicrc file
```

```
gvim .magicrc
```

```
# Command to open magic tool in better graphics
```

```
magic -d XR &
```

Screenshots of commands run

Activities Terminal Thu 10:33 PM
vsduser@vsdsquadron:~/drc_tests

```
File Edit View Search Terminal Help
vsduser@vsdsquadron:~$ cd
vsduser@vsdsquadron:~$ wget http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
--2024-03-21 22:31:14-- http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
Resolving opencircuitdesign.com (opencircuitdesign.com)... 69.251.37.208
Connecting to opencircuitdesign.com (opencircuitdesign.com)|69.251.37.208|:80... connected.
HTTP request sent, awaiting response... 200 OK
Length: 41651 (41K) [application/x-gzip]
Saving to: 'drc_tests.tgz'

drc_tests.tgz          100%[=====] 40.67K 160KB/s in 0.3s

2024-03-21 22:31:15 (160 KB/s) - 'drc_tests.tgz' saved [41651/41651]

vsduser@vsdsquadron:~$ tar xfz drc_tests.tgz
vsduser@vsdsquadron:~$ cd drc_tests
vsduser@vsdsquadron:~/drc_tests$ ls -al
total 276
drwxrwxr-x 2 vsduser vsduser 4096 Sep 16 2020 .
drwxr-xr-x 22 vsduser vsduser 4096 Mar 21 22:31 ..
-rw-rw-r-- 1 vsduser vsduser 3178 Sep 15 2020 capm.mag
-rw-rw-r-- 1 vsduser vsduser 3610 Sep 16 2020 difftap.mag
-rw-rw-r-- 1 vsduser vsduser 1535 Sep 16 2020 dnwell.mag
-rw-rw-r-- 1 vsduser vsduser 1684 Sep 15 2020 hvtp.mag
-rw-rw-r-- 1 vsduser vsduser 897 Sep 15 2020 hvtr.mag
-rw-rw-r-- 1 vsduser vsduser 11586 Sep 15 2020 licon.mag
-rw-rw-r-- 1 vsduser vsduser 1480 Sep 15 2020 li.mag
-rw-rw-r-- 1 vsduser vsduser 4648 Sep 15 2020 lvtn.mag
-rw-rw-r-- 1 vsduser vsduser 2565 Sep 15 2020 .magicrc
```

Activities Terminal Thu 10:34 PM
vsduser@vsdsquadron:~/drc_tests

```
File Edit View Search Terminal Help
-rw-rw-r-- 1 vsduser vsduser 11586 Sep 15 2020 licon.mag
-rw-rw-r-- 1 vsduser vsduser 1480 Sep 15 2020 li.mag
-rw-rw-r-- 1 vsduser vsduser 4648 Sep 15 2020 lvtn.mag
-rw-rw-r-- 1 vsduser vsduser 2565 Sep 15 2020 .magicrc
-rw-rw-r-- 1 vsduser vsduser 1198 Sep 15 2020 mcon.mag
-rw-rw-r-- 1 vsduser vsduser 2103 Sep 15 2020 met1.mag
-rw-rw-r-- 1 vsduser vsduser 1799 Sep 15 2020 met2.mag
-rw-rw-r-- 1 vsduser vsduser 1500 Sep 16 2020 met3.mag
-rw-rw-r-- 1 vsduser vsduser 1114 Sep 16 2020 met4.mag
-rw-rw-r-- 1 vsduser vsduser 757 Sep 15 2020 met5.mag
-rw-rw-r-- 1 vsduser vsduser 1948 Sep 15 2020 npc.mag
-rw-rw-r-- 1 vsduser vsduser 2497 Sep 15 2020 nsd.mag
-rw-rw-r-- 1 vsduser vsduser 1351 Sep 16 2020 nwell.mag
-rw-rw-r-- 1 vsduser vsduser 536 Sep 15 2020 pad.mag
-rw-rw-r-- 1 vsduser vsduser 5588 Sep 16 2020 poly.mag
-rw-rw-r-- 1 vsduser vsduser 2565 Sep 15 2020 psd.mag
-rw-rw-r-- 1 vsduser vsduser 3025 Sep 15 2020 rpm.mag
-rw-rw-r-- 1 vsduser vsduser 135962 Sep 16 2020 sky130A.tech
-rw-rw-r-- 1 vsduser vsduser 2476 Sep 16 2020 tunm.mag
-rw-rw-r-- 1 vsduser vsduser 4114 Sep 16 2020 varac.mag
-rw-rw-r-- 1 vsduser vsduser 1271 Sep 15 2020 via2.mag
-rw-rw-r-- 1 vsduser vsduser 1267 Sep 15 2020 via3.mag
-rw-rw-r-- 1 vsduser vsduser 966 Sep 15 2020 via4.mag
-rw-rw-r-- 1 vsduser vsduser 955 Sep 15 2020 via.mag
vsduser@vsdsquadron:~/drc_tests$ gvim .magicrc
vsduser@vsdsquadron:~/drc_tests$ magic -d XR
```

Screenshot of .magicrc file

```

Thu 10:35 PM
.magicrc (~/.drc_tests) - GVIM

File Edit Tools Syntax Buffers Window Help
1 puts stdout "Sourcing design .magicrc for technology sky130A ..."
2
3 # Put grid on 0.005 pitch. This is important, as some commands don't
4 # rescale the grid automatically (such as lef read?).
5
6 set scalefac [tech lambda]
7 if {[lindex $scalefac 1] < 2} {
8     scalegrid 1 2
9 }
10
11 # drc off
12 drc euclidean on
13
14 # Allow override of PDK path from environment variable PDKPATH
15 if {[catch {set PDKPATH $env(PDKPATH)}]} {
16     set PDKPATH "~/cad/pdk/sky130A"
17 }
18
19 # loading technology
20 # tech load $PDKPATH/libs.tech/magic/sky130A.tech
21 tech load sky130A.tech
22
23 # load device generator
24 # source $PDKPATH/libs.tech/magic/sky130A.tcl
25

".magicrc" 74L, 2565C

```

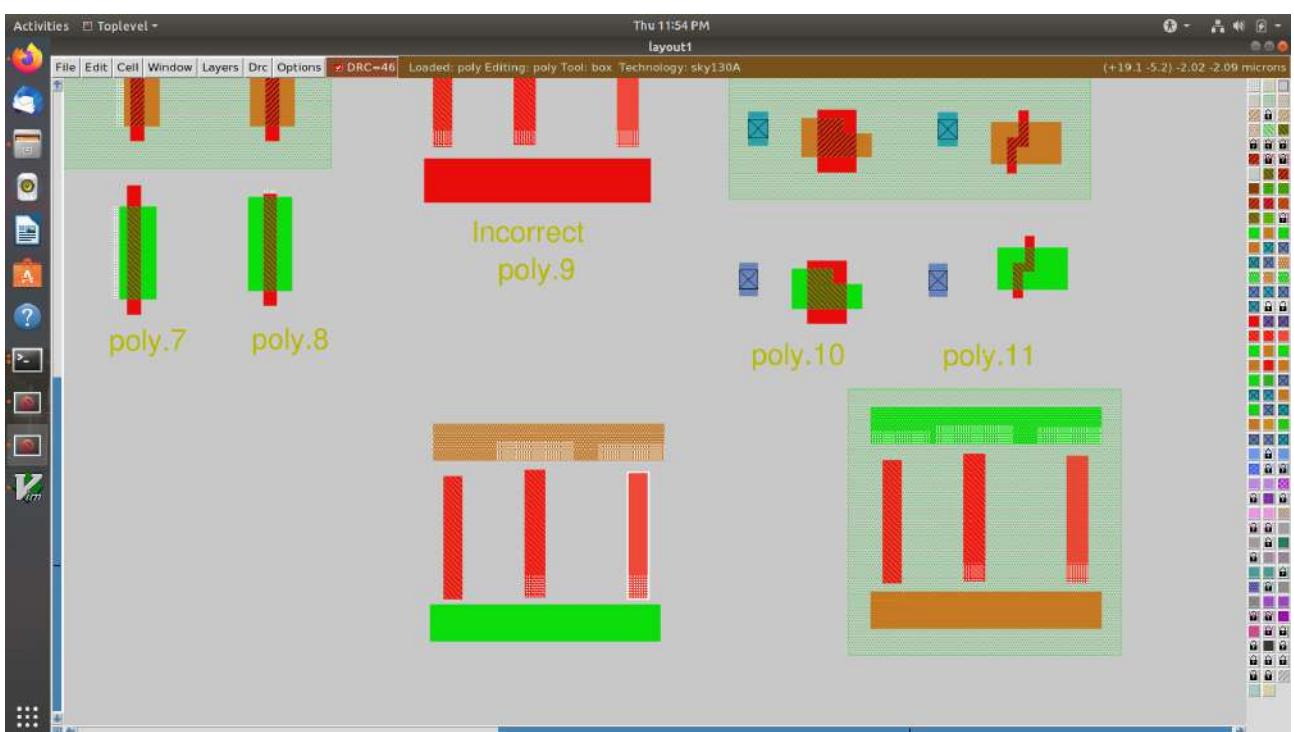
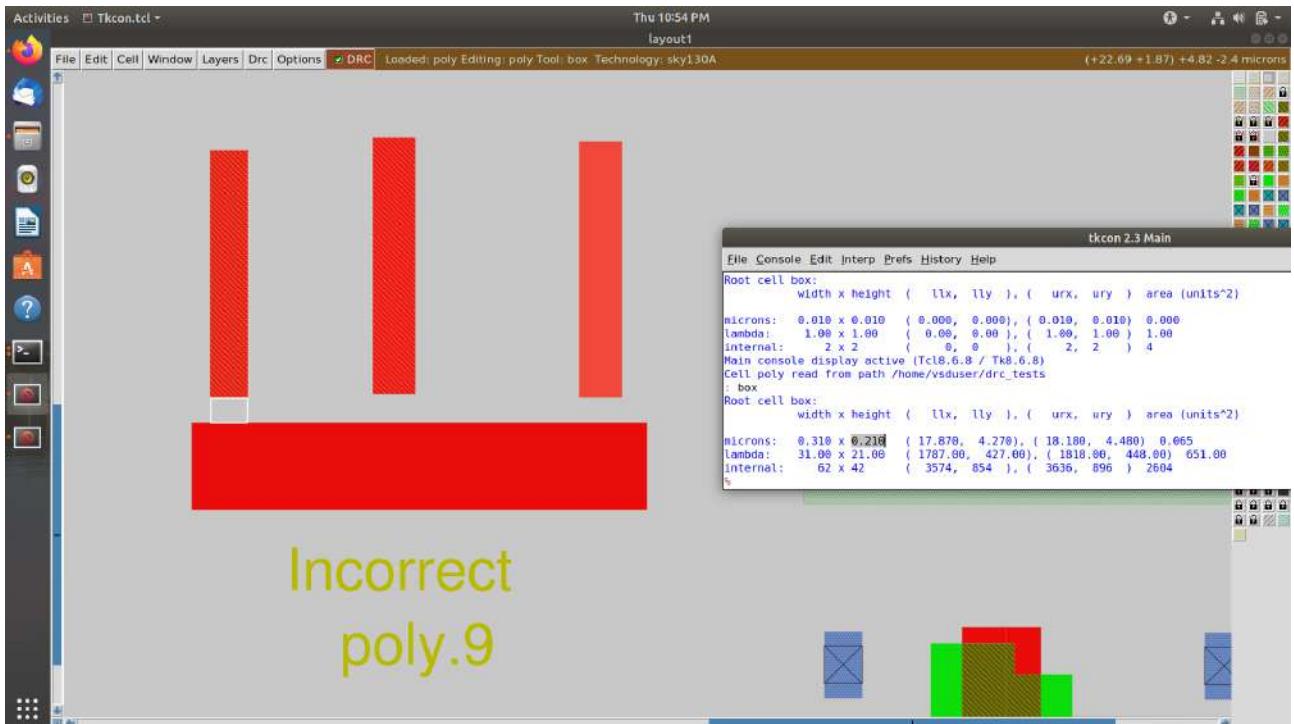
1,1 Top

Incorrectly implemented poly.9 simple rule correction

Screenshot of poly rules

Periphery Rules		Search	google/skywater-pdk
SkyWater SKY130 PDK	(poly.1a)	Width of poly	0.150 μm
Versioning Information	(poly.1b)	Min channel length (poly width) for peft overlapping lvtn (exempt rule for dummy_poly in cells listed on Table H3)	0.350 μm
Current Status	(poly.2)	Spacing of poly to poly except for poly.c2 and poly.c3. Exempt cell: sr_bld_eq where it is same as poly.c2	0.210 μm
Known Issues	(poly.3)	Min poly resistor width	0.330 μm
Design Rules	(poly.4)	Spacing of poly on field to diff (parallel edges only)	P 0.075 μm
PDK Contents	(poly.5)	Spacing of poly on field to tap	P 0.055 μm
Analog Design	(poly.6)	Spacing of poly on diff to abutting tap (min source)	P 0.300 μm
Digital Design	(poly.7)	Extension of diff beyond poly (min drain)	P 0.250
Simulation	(poly.8)	Extension of poly beyond diffusion (endcap)	P 0.130
Physical & Design Verification	(poly.9)	Poly resistor spacing to poly or spacing (no overlap) to diff/tap	0.480 μm
Python API	(poly.10)	Poly can't overlap inner corners of diff	
Previous Nomenclature	(poly.11)	No 90 deg turns of poly on diff	
Glossary	(poly.12)	(Poly NOT (inwell NOT hv)) may not overlap tap: Rule exempted for cell name "g8tge_n_fq2" and gated_rgn and inside UHVL.	P
How to Contribute	(poly.13)	Poly must not overlap diff/rs	
Partners	(poly.14)		
References	(poly.15)		

Incorrectly implemented poly.9 rule no drc violation even though spacing < 0.48μ



New commands inserted in sky130A.tech file to update drc

Activities M GVim Thu 11:58 PM
sky130A.tech (~/.drc_tests) - GVIM

```

4803
4804 variants *
4805
4806 #-----
4807 # POLY
4808 #-----
4809
4810 width allpoly 150 "poly.width < %d (poly.1a)"
4811 spacing allpoly allpoly 210 touching_ok "poly.spacing < %d (poly.2)"
4812 spacing allpolynonfet alldiffvnonfet 75 corner_ok allfets \
    "poly.spacing to Diffusion < %d (poly.4a)"
4813 spacing npres alldiff 480 touching_illegal \
    "poly.resistor spacing to alldiff < %d (poly.9)"
4814 spacing npres allpolynonres 480 touching_illegal \
    "poly.resistor spacing to allpolynonres < %d (poly.9)"
4815 overhang *ndiff,rndiff nfet,scnfet,npd,npass 250 "N-Diffusion overhang of nmos < %d (poly.7)"
4816 overhang *mvndiff,mvrndiff mvnfet,mvnnfet 250 \
    "N-Diffusion overhang of nmos < %d (poly.7)"
4817 overhang *pdifff,rdifff pfet,scpfet,ppu 250 "P-Diffusion overhang of pmos < %d (poly.7)"
4818 overhang *mvpdiff,mvrpdifff mvpfet 250 "P-Diffusion overhang of pmos < %d (poly.7)"
4819 overhang *poly allfets 130 "poly.overhang of transistor < %d (poly.8)"
4820 rect_only allfets "No bends in transistors (poly.11)"
4821 rect_only xhrpoly,uhrpoly "No bends in poly resistors (poly.11)"
4822 extend xpc/a xhrpoly,uhrpoly 2160 \
    "poly.contact extends poly resistor by < %d (lcon.1c + li.5)"
4823
4824 -- VISUAL --
4817,56-63 81%

```

Activities M GVim Thu 11:09 PM
sky130A.tech (~/.drc_tests) - GVIM

```

5168 # xhrpoly (P+ poly resistor)
5169 #-----
5170
5171 width xhrpoly 350 "xhrpoly resistor width < %d (P+ poly.1a)"
5172 # NOTE: xhrpoly resistor requires choice of discrete widths 0.35, 0.69, ... up to 1.27.
5173
5174 #-----
5175 # uhrpoly (P+ poly resistor, 2kOhm/sq)
5176 #-----
5177
5178 width uhrpoly 350 "uhrpoly resistor width < %d"
5179 spacing xhrpoly,uhrpoly,xpc alldiff 480 touching_illegal \
    "xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
5180 spacing xhrpoly,uhrpoly,xpc allpolynonres 480 touching_illegal \
    "xhrpoly/uhrpoly resistor spacing to allpolynonres < %d (poly.9)"
5181
5182
5183
5184
5185 #-----
5186 # MOS Varactor device rules
5187 #-----
5188
5189 overhang *nsd var,varhvt 250 \
    "N-Tap overhang of Varactor < %d (var.4)"
5190
5191
5192 overhang *mvnsd mvvar 250 \
-- VISUAL --
5182,67-74 87%

```

Commands to run in tkcon window

```
# Loading updated tech file
```

```
tech load sky130A.tech
```

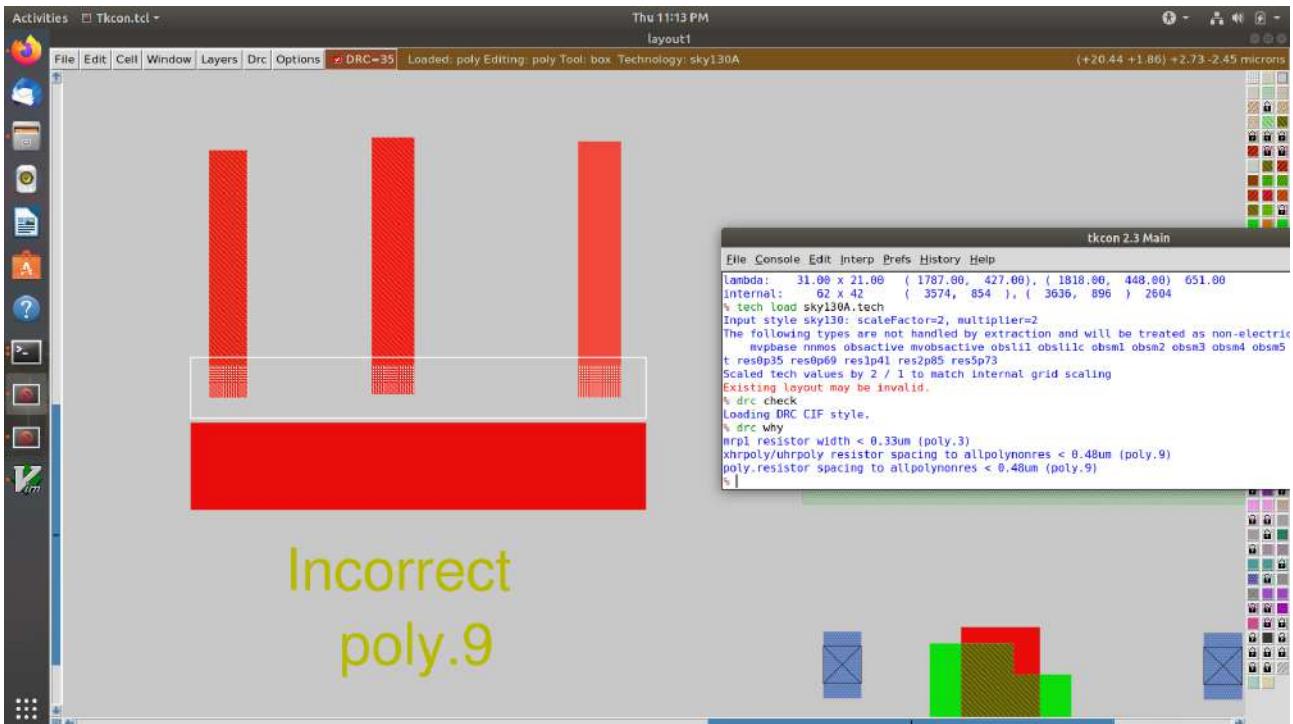
```
# Must re-run drc check to see updated drc errors
```

```
drc check
```

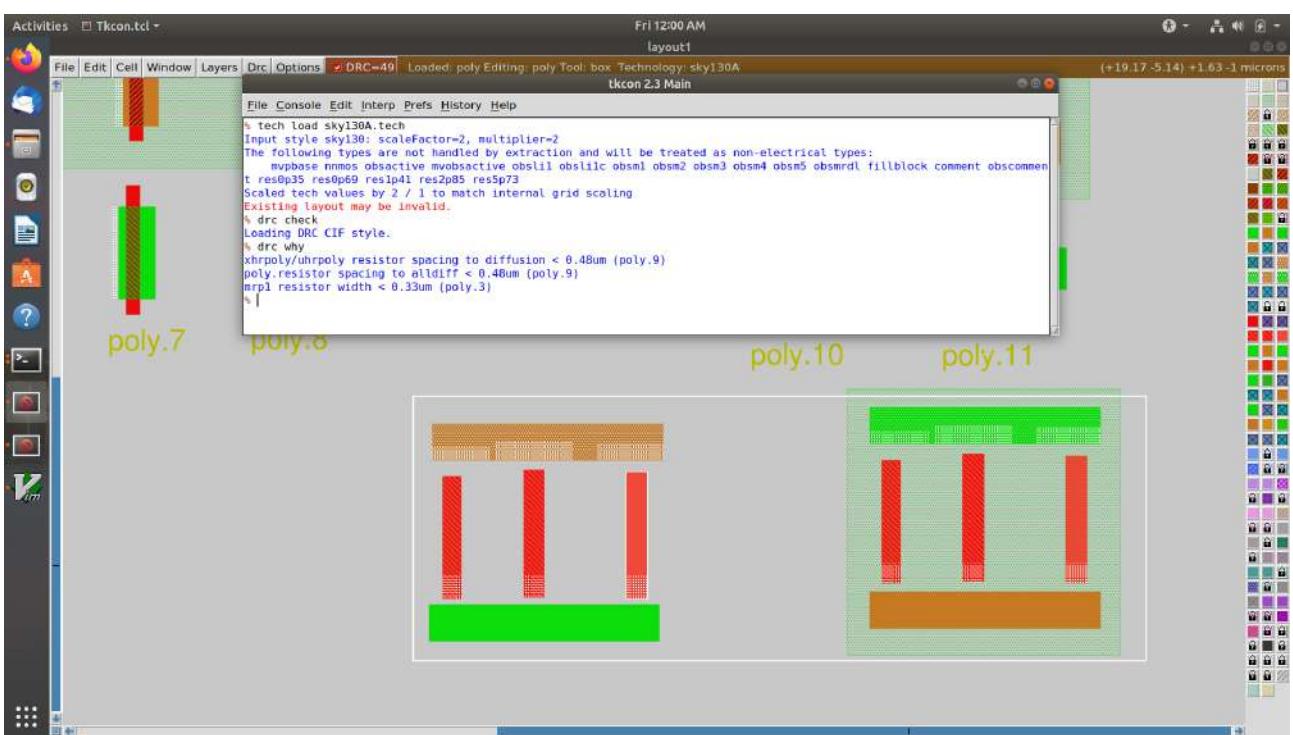
```
# Selecting region displaying the new errors and getting the error messages
```

```
drc why
```

Screenshot of magic window with rule implemented



Incorrect
poly.9



Incorrectly implemented difftap.2 simple rule correction

Screenshot of difftap rules

Activities Firefox Web Browser Fri 12:14 AM

Editing soc-design-and... yosys-tcl-ui-report/RE... nickson-jose/vsdstdce... Online Clipboard Periphery Rules — Sky... Magic VLSI

<https://skywater-pdk.readthedocs.io/en/main/rules/periphery.html#difftap>

Periphery Rules Search google@skywater-pdk

SkyWater SKY130 PDK

Versioning Information Current Status Known Issues Design Rules PDK Contents Analog Design Digital Design Simulation Physical & Design Verification Python API Previous Nomenclature Glossary How to Contribute Partners References

Name Description Flags Value Unit

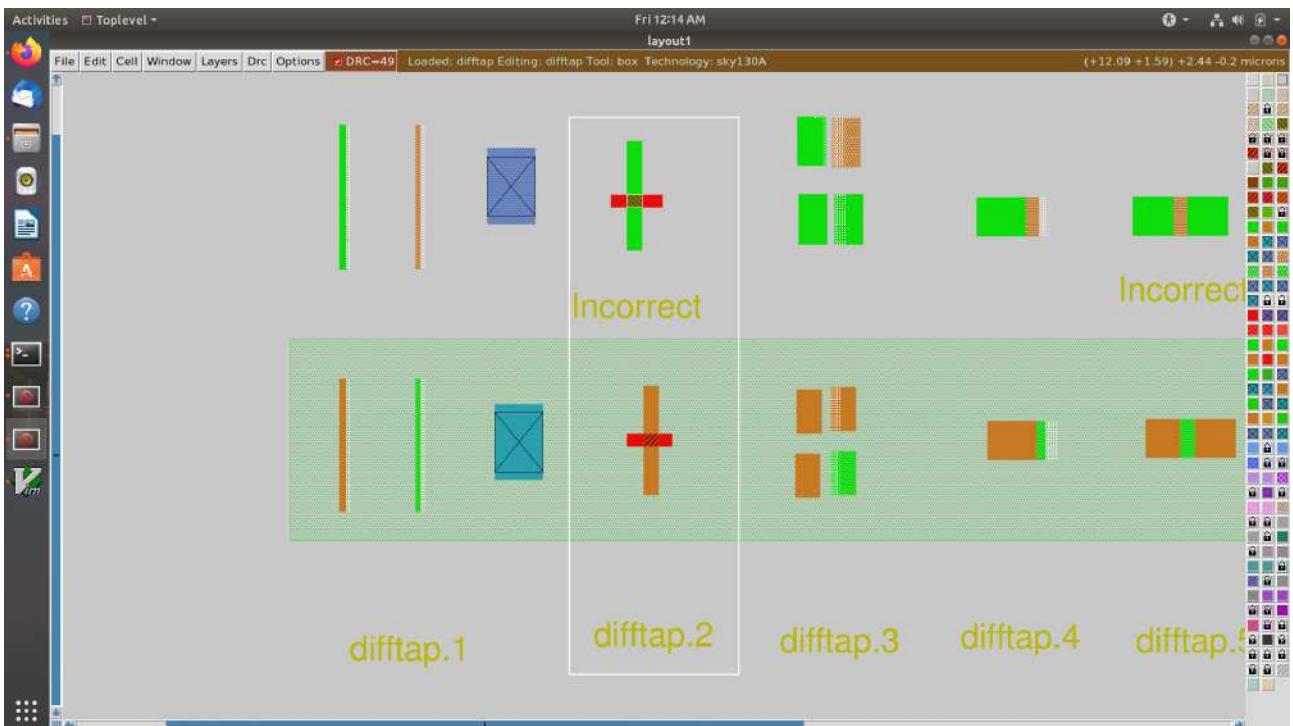
Table 38 Function: Defines active regions and contacts to substrate

Name	Description	Flags	Value	Unit
(difftap.1)	Width of diff or tap	P	0.150	μm
(difftap.2)	Minimum channel width (Diff And Poly) except for FETs inside areaid.sc: Rule exempted in the SP8* flows only, for the cells listed in rule difftap.2a	P	0.420	μm
(difftap.2a)	Minimum channel width (Diff And Poly) for cell names "s8cell_ee_plus_ssein_a", "s8cell_ee_plus_ssein_b", "s8cell_ee_plus_sseip_a", "s8cell_ee_plus_sseip_b", "s8lpls_pl8", "s8lpls_rdrv4", "s8lpls_rdrv4f" and "s8lpls_rdrv8"	P, NA	NA	μm
(difftap.2b)	Minimum channel width (Diff And Poly) for FETs inside areaid.sc	P	0.360	μm
(difftap.3)	Spacing of diff to diff, tap to tap, or non-abutting diff to tap		0.270	μm
(difftap.4)	Min tap bound by one diffusion		0.290	
(difftap.5)	Min tap bound by two diffusions	P	0.400	
(difftap.6)	Diff and tap are not allowed to extend beyond their abutting edge			
(difftap.7)	Spacing of difftap abutting edge to a non-conciding diff or tap edge	NE	0.130	μm
(difftap.8)	Enclosure of (p+) diffusion by N-well. Rule exempted inside UHVI.	DE NE P	0.180	μm
(difftap.9)	Spacing of (n+) diffusion to N-well outside UHVI	DE NE P	0.340	μm
(difftap.10)	Enclosure of (n+) tap by N-well. Rule exempted inside UHVI.	NE P	0.180	μm
Creation of resistors in N-well. Only recommended inside UHVI				
Δ 196 nm				

Contents

- Periphery Rules (x,-) (dnwell,-) (nwell,-) (pwell,-) (pudem,-) (hvtp,-) (hvtr,-) (lvtn,-) (ncm,-) (difftap,-) (tunn,-) (poly,-) (rpm,-) (varac,-) (photo,-) (npc,-) (n/ psd,-) (licon,-) (li,-) (ct,-) (capm,-) (vpp,-) /m1 -

Incorrectly implemented difftap.2 rule no drc violation even though spacing < 0.42μ



New commands inserted in sky130A.tech file to update drc

```
5178 width uhrpoly 350 "uhrpoly resistor width < %d"
5179 spacing xhrpoly,uhrpoly,xpc alldiff 480 touching_illegal \
      "xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
5180 spacing xhrpoly,uhrpoly,xpc allpolynonres 480 touching_illegal \
      "xhrpoly/uhrpoly resistor spacing to allpolynonres < %d (poly.9)"
5181
5182
5183
5184
5185 #-----
5186 # MOS Varactor device rules
5187 #-----
5188
5189 width pmos 420 \
      "mos transistor formed should have minimum width of < %d (difftap.2)"
5190 width nmos 420 \
      "mos transistor formed should have minimum width of < %d (difftap.2)"
5191
5192
5193 overhang *nsd var,varhvt 250 \
      "N-Tap overhang of Varactor < %d (var.4)"
5194
5195 overhang *mvnsd mvvar 250 \
      "N-Tap overhang of Varactor < %d (var.4)"
5196
5197 width var,varhvt,mvvar 180 "Varactor length < %d (var.1)"
5198 extend var,varhvt,mvvar *poly 1000 "Varactor width < %d (var.2)"
5199
5200
5201
5202
```

-- VISUAL --

5192, 71 88%

Commands to run in tkcon window

```
# Loading updated tech file
```

```
tech load sky130A.tech
```

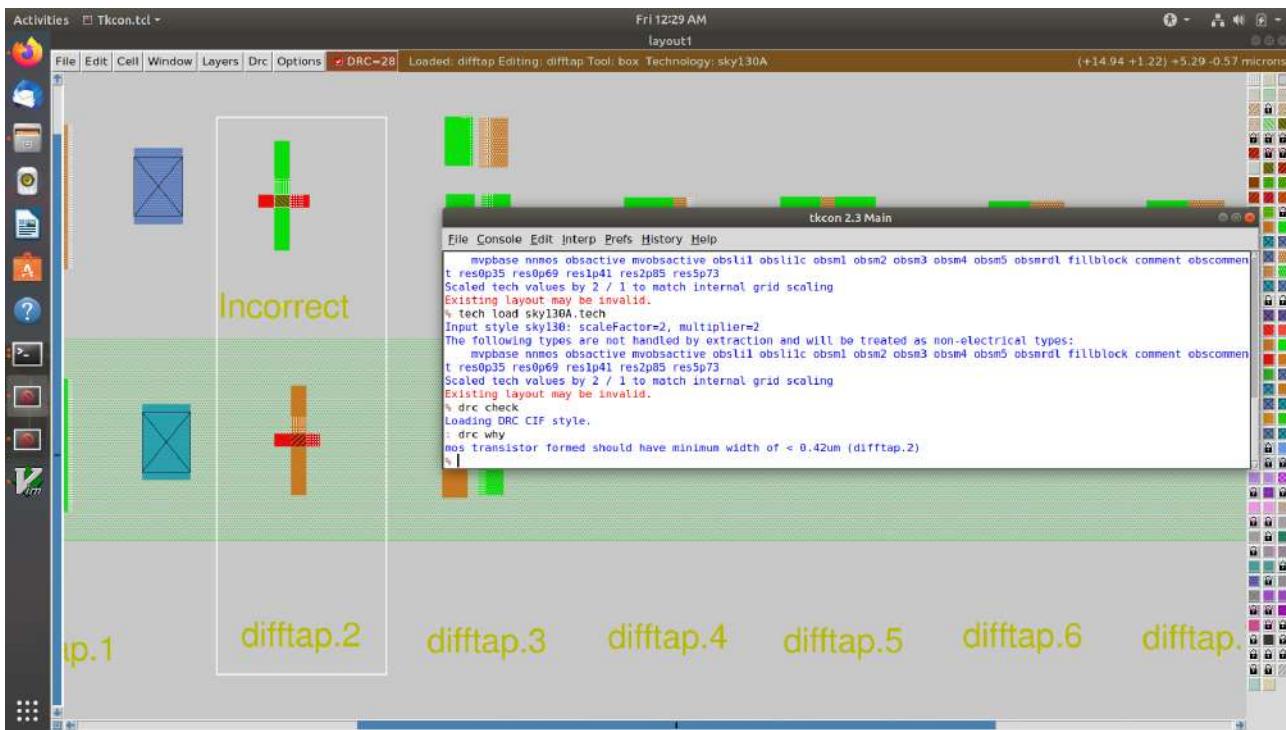
```
# Must re-run drc check to see updated drc errors
```

```
drc check
```

```
# Selecting region displaying the new errors and getting the error messages
```

```
drc why
```

Screenshot of magic window with rule implemented

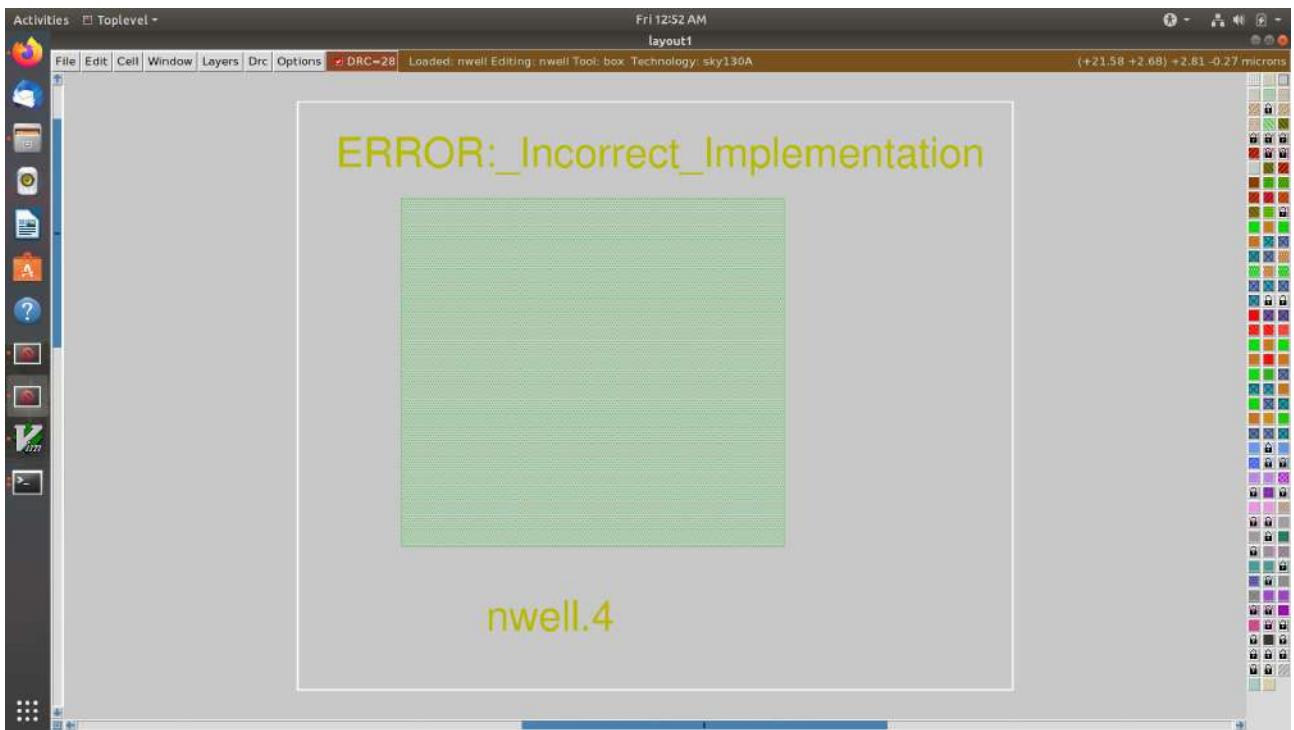


Incorrectly implemented nwell.4 complex rule correction

Screenshot of nwell rules

Table 31 Function: Define nwell implant regions.					
	Name	Description	Flags	Value	Unit
	(nwell.1)	Width of nwell		0.840	μm
	(nwell.2a)	Spacing between two n-wells		1.270	μm
	(nwell.2b)	Manual merge wells if less than minimum			
	(nwell.4)	All n-wells will contain metal-contacted tap (rule checks only for icon on top) . Rule exempted from high voltage cells inside UHVI			
	(nwell.5)	Deep nwell must be enclosed by nwell by atleast... Exempted inside UHVI or areaid, lw Nwells can merge over deep nwell if spacing too small (as in rule nwell.2)	TC	0.400	μm
	(nwell.5a)	min enclosure of nwell by dnwell inside UHVI		N/A	N/A
	(nwell.5b)	nwell inside UHVI must not be on the same net as nwell outside UHVI		N/A	N/A
	(nwell.6)	Min enclosure of nwell hole by deep nwell outside UHVI	TC	1.030	μm
	(nwell.7)	Min spacing between nwell and deep nwell on separate nets Spacing between nwell and deep nwell on the same net is set by the sum of the rules nwell.2 and nwell.5. By default, DRC run on a cell checks for the separate-net spacing, when nwell and deep nwell nets are separate within the cell hierarchy and are joined in the upper hierarchy. To allow net names to be joined and make the same-net rule applicable in this case, the "joinNets" switch should be turned on. waffle_chip	TC	4.500	μm

Incorrectly implemented nwell.4 rule no drc violation even though no tap present in nwell



New commands inserted in sky130A.tech file to update drc

Activities M GVim

Fri 1:03 AM
sky130A.tech (~/.drc_tests) - GVIM

```

1230 options calma-permissive-labels
1231
1232 # Ensure nwell overlaps dnwell at least 0.4um outside and 1.03um inside
1233 templayer dnwell_shrink dnwell
1234 shrink 1030
1235
1236 templayer nwell_missing dnwell
1237 grow 400
1238 and-not dnwell_shrink
1239 and-not nwell
1240
1241 templayer nwell_tapped
1242 bloat-all nsc nwell
1243
1244 templayer nwell_untapped nwell
1245 and-not nwell_tapped
1246
1247 # SONOS nFET devices must be in deep nwell
1248 templayer dnwell_missing nsonos
1249 and-not dnwell
1250
1251 # Define MiM cap bottom plate for spacing rule
1252 templayer mim_bottom
1253 bloat-all *mimcap *metal3
1254
-- VISUAL --

```

1245, 22 20%

Activities M GVim

Fri 1:04 AM
sky130A.tech (~/.drc_tests) - GVIM

```

4721 spacing dnwell dnwell 6300 touching_ok "Deep N-well spacing < %d (dnwell.3)"
4722 spacing dnwell allnwell 4500 surround_ok \
4723 "Deep N-well spacing to N-well < %d (nwell.7)"
4724 cifmaxwidth nwell_missing 0 bend_illegal \
4725 "N-well overlap of Deep N-well < 0.4um outside, 1.03um inside (nwell.5a, 7)"
4726 cifmaxwidth dnwell_missing 0 bend_illegal \
4727 "SONOS nFET must be in Deep N-well (tunm.6a)"
4728
4729 #-----
4730 # NWELL
4731 #-----
4732
4733 width allnwell 840 "N-well width < %d (nwell.1)"
4734 spacing allnwell allnwell 1270 touching_ok "N-well spacing < %d (nwell.2a)"
4735
4736 variants (full)
4737 cifmaxwidth nwell_untapped 0 bend_illegal \
4738 "Nwell missing tap (nwell.4)"
4739 variants *
4740
4741 #-----
4742 # DIFF
4743 #-----
@ -- VISUAL --

```

4739, 11 80%

Commands to run in tkcon window

```
# Loading updated tech file
```

```
tech load sky130A.tech
```

Change drc style to drc full

drc style drc(full)

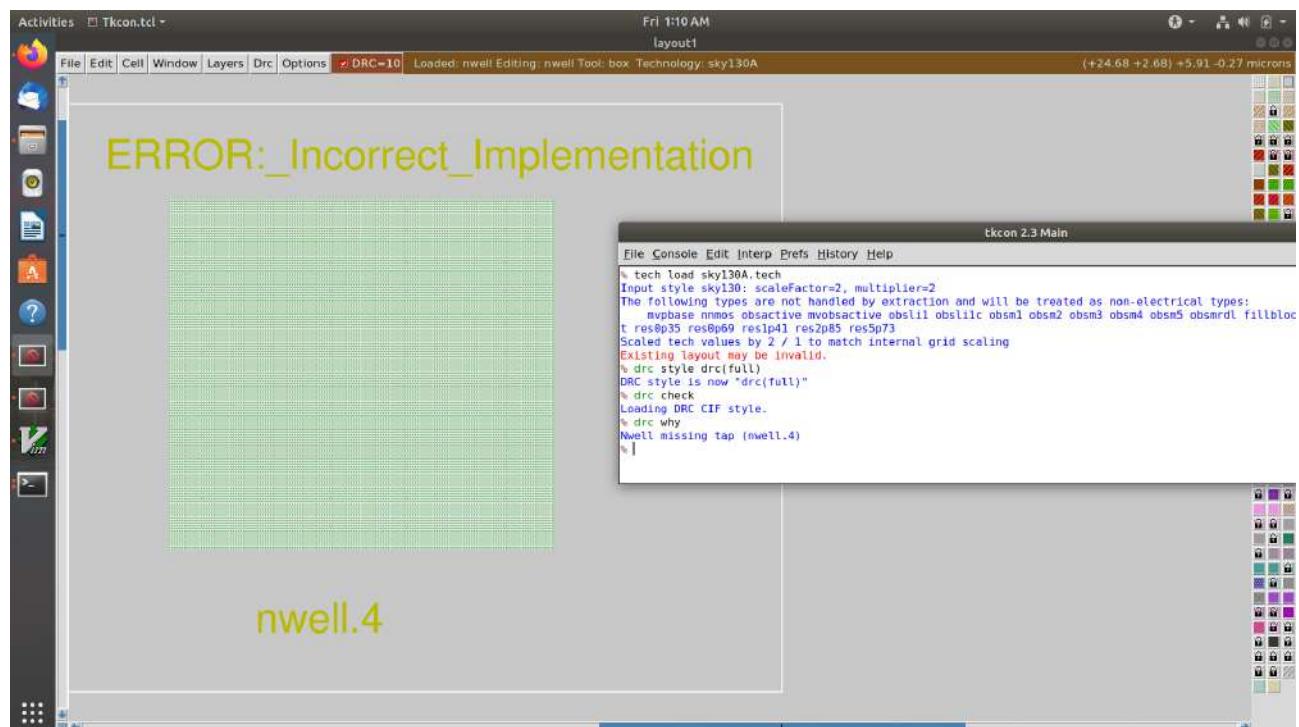
```
# Must re-run drc check to see updated drc errors
```

drc check

Selecting region displaying the new errors and getting the error messages

drc why

Screenshot of magic window with rule implemented



Section 4 - Pre-layout timing analysis and importance of good clock tree (22/03/2024 - 24/03/2024)

Theory

Implementation

- Section 4 tasks:-
 12. Fix up small DRC errors and verify the design is ready to be inserted into our flow.
 13. Save the finalized layout with custom name and open it.
 14. Generate lef from the layout.
 15. Copy the newly generated lef and associated required lib files to 'picorv32a' design 'src' directory.
 16. Edit 'config.tcl' to change lib file and add the new extra lef into the openlane flow.
 17. Run openlane flow synthesis with newly inserted custom inverter cell.
 18. Remove/reduce the newly introduced violations with the introduction of custom inverter cell by modifying design parameters.
 19. Once synthesis has accepted our custom inverter we can now run floorplan and placement and verify the cell is accepted in PnR flow.
 20. Do Post-Synthesis timing analysis with OpenSTA tool.
 21. Make timing ECO fixes to remove all violations.

22. Replace the old netlist with the new netlist generated after timing ECO fix and implement the floorplan, placement and cts.
23. Post-CTS OpenROAD timing analysis.
24. Explore post-CTS OpenROAD timing analysis by removing 'sky130_fd_sc_hd_clkbuf_1' cell from clock buffer list variable 'CTS_CLK_BUFFER_LIST'.
 - Section 4 - Tasks 1 to 4 files, reports and logs can be found in the following folder:

Section 4 - Tasks 1 to 4 (vsdstdcelldesign)

- Section 4 - Task 4 files, reports and logs can be found in the following folder:

Section 4 - Task 4 (src)

- Section 4 - Task 5 files, reports and logs can be found in the following folder:

Section 4 - Task 5 (picorv32a)

- Section 4 - Tasks 6 to 8 & 11 to 13 logs, reports and results can be found in following run folder:

Section 4 - Tasks 6 to 8 & 11 to 13 Run (24-03_10-03)

- Section 4 - Tasks 9 to 11 logs, reports and results can be found in following run folder:

Section 4 - Tasks 9 to 11 Run (25-03_18-52)

1. Fix up small DRC errors and verify the design is ready to be inserted into our flow.

Conditions to be verified before moving forward with custom designed cell layout:

- Condition 1: The input and output ports of the standard cell should lie on the intersection of the vertical and horizontal tracks.
- Condition 2: Width of the standard cell should be odd multiples of the horizontal track pitch.
- Condition 3: Height of the standard cell should be even multiples of the vertical track pitch.

Commands to open the custom inverter layout

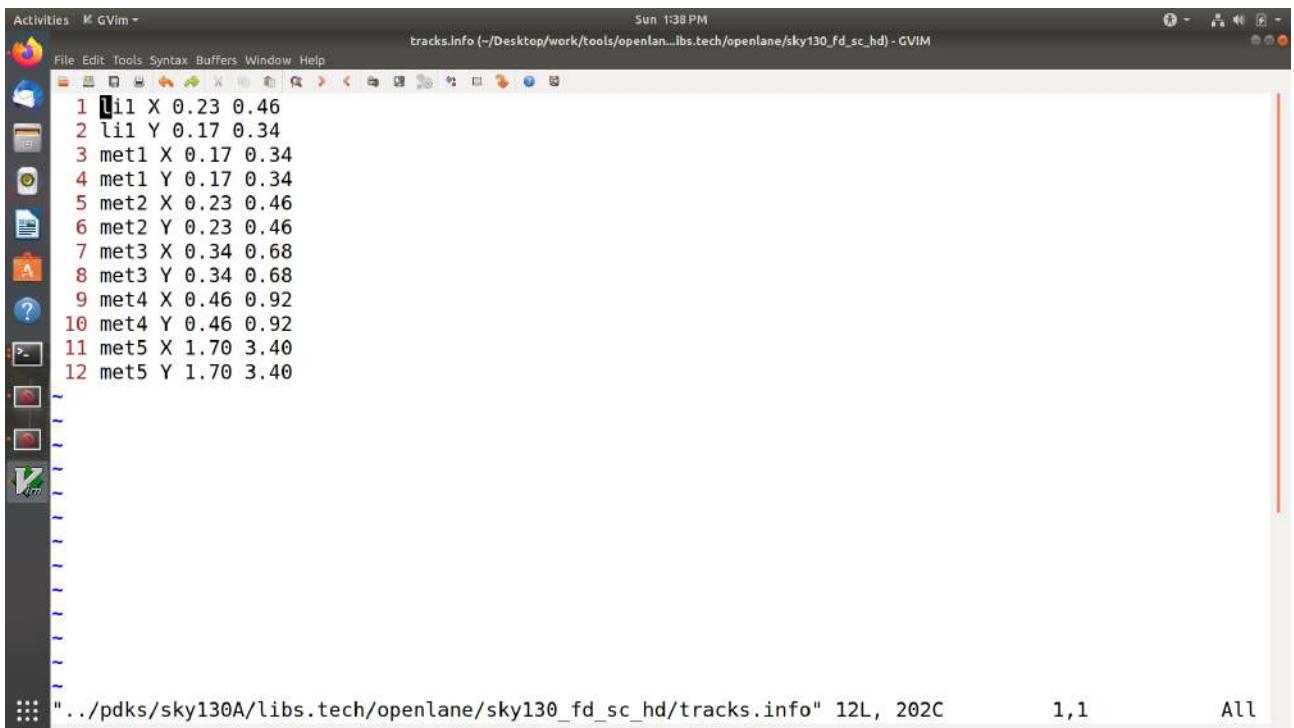
```
# Change directory to vsdstdcelldesign
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
```

```
# Command to open custom inverter layout in magic
```

```
magic -T sky130A.tech sky130_inv.mag &
```

Screenshot of tracks.info of sky130_fd_sc_hd



A screenshot of the GVIM text editor window. The title bar reads "activities K. GVIM" and "tracks.info (~/Desktop/work/tools/openlane/libs.tech/openlane/sky130_fd_sc_hd) - GVIM". The status bar shows "Sun 1:38 PM" and "1,1 All". The main pane displays a list of track coordinates:

```
1 l1l X 0.23 0.46
2 l1l Y 0.17 0.34
3 met1 X 0.17 0.34
4 met1 Y 0.17 0.34
5 met2 X 0.23 0.46
6 met2 Y 0.23 0.46
7 met3 X 0.34 0.68
8 met3 Y 0.34 0.68
9 met4 X 0.46 0.92
10 met4 Y 0.46 0.92
11 met5 X 1.70 3.40
12 met5 Y 1.70 3.40
```

Commands for tkcon window to set grid as tracks of locali layer

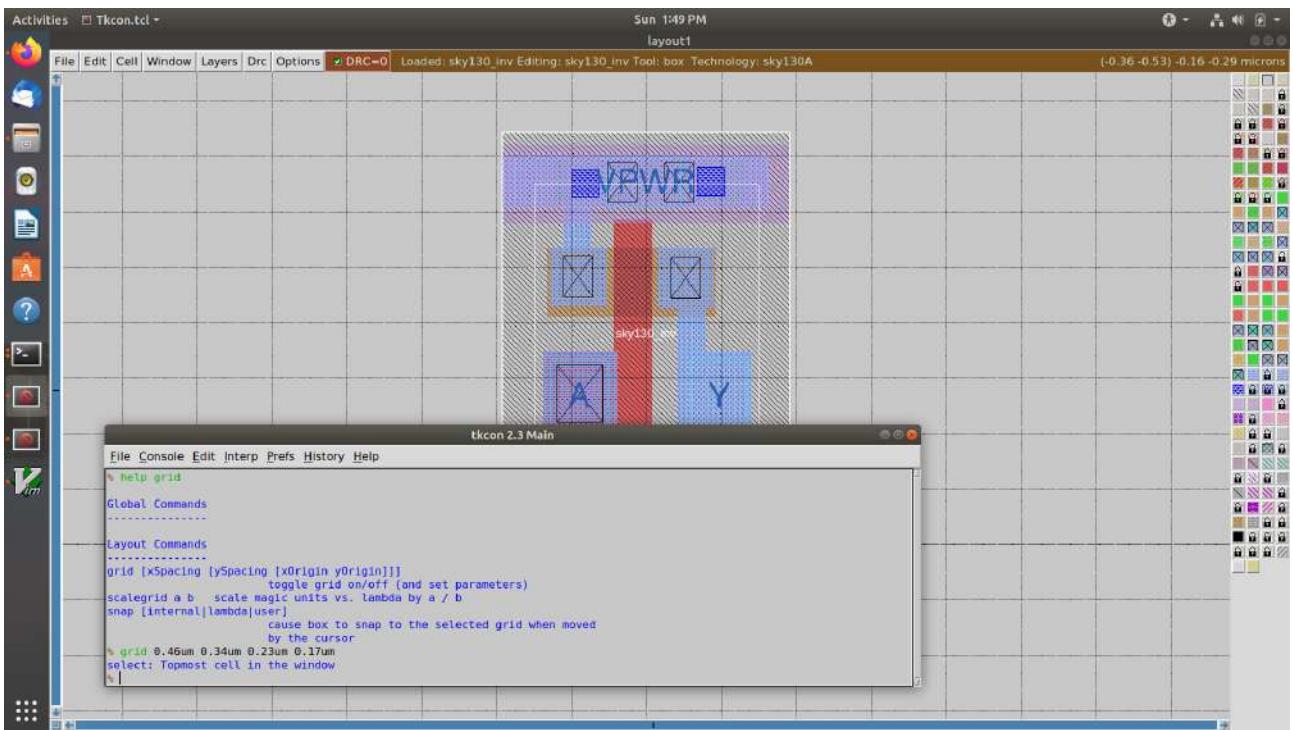
```
# Get syntax for grid command
```

```
help grid
```

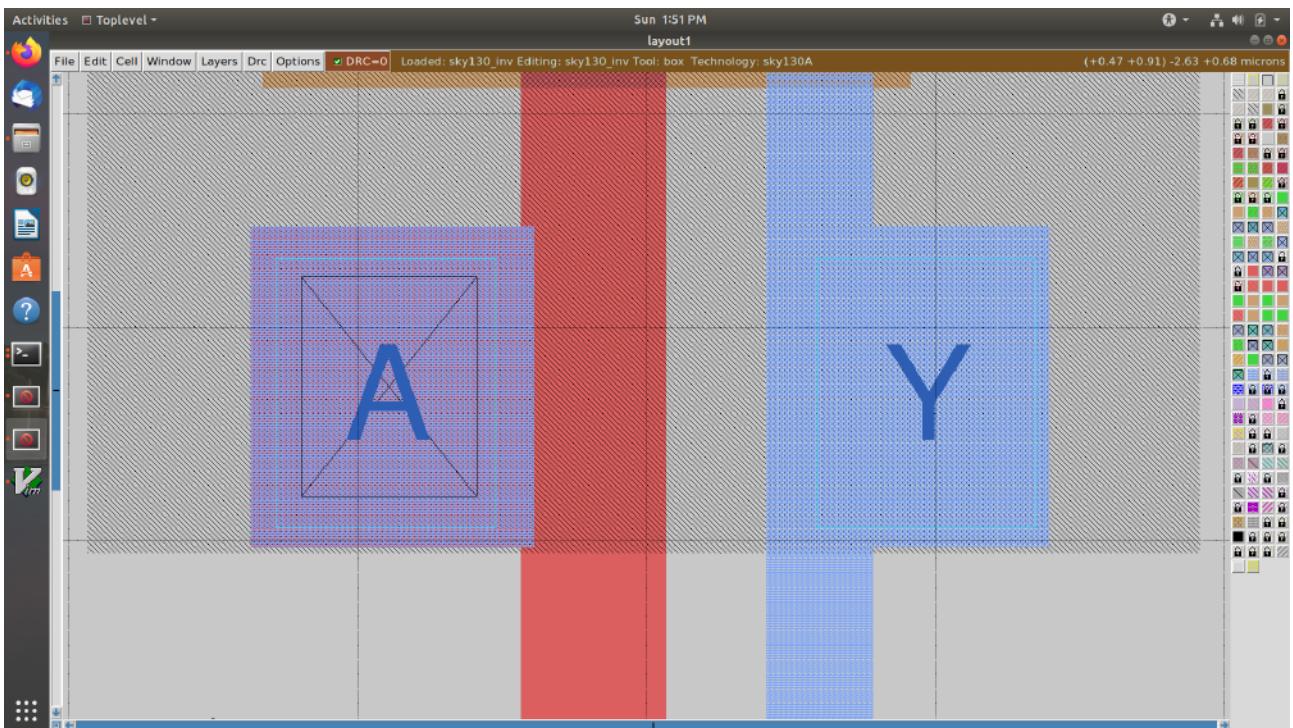
```
# Set grid values accordingly
```

```
grid 0.46um 0.34um 0.23um 0.17um
```

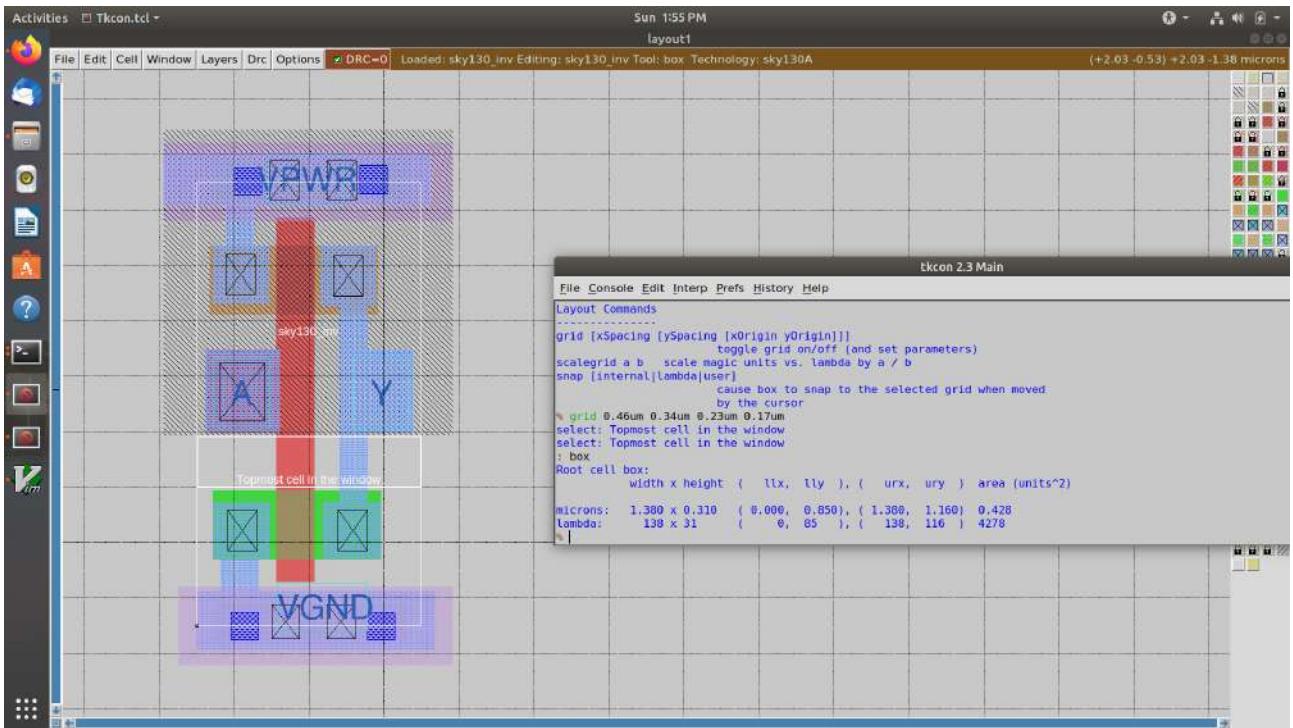
Screenshot of commands run



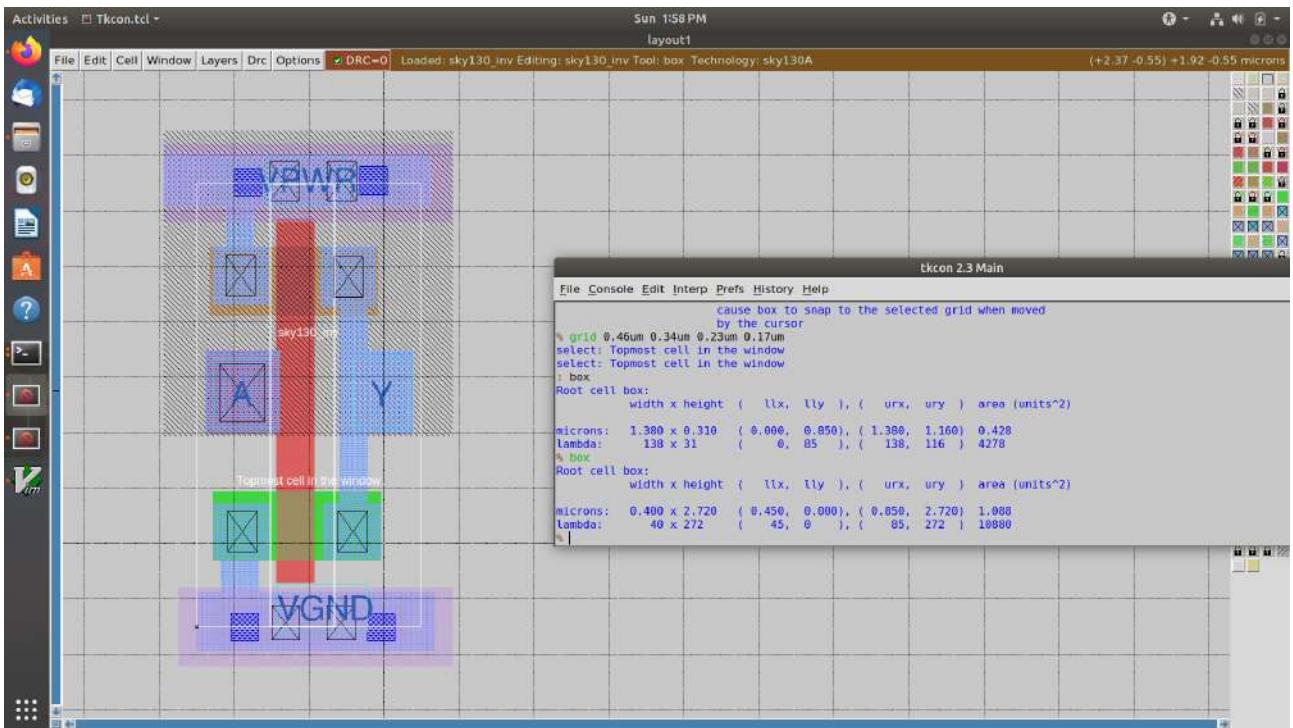
Condition 1 verified



Condition 2 verified



Condition 3 verified



2. Save the finalized layout with custom name and open it.

Command for tkcon window to save the layout with custom name

```
# Command to save as
```

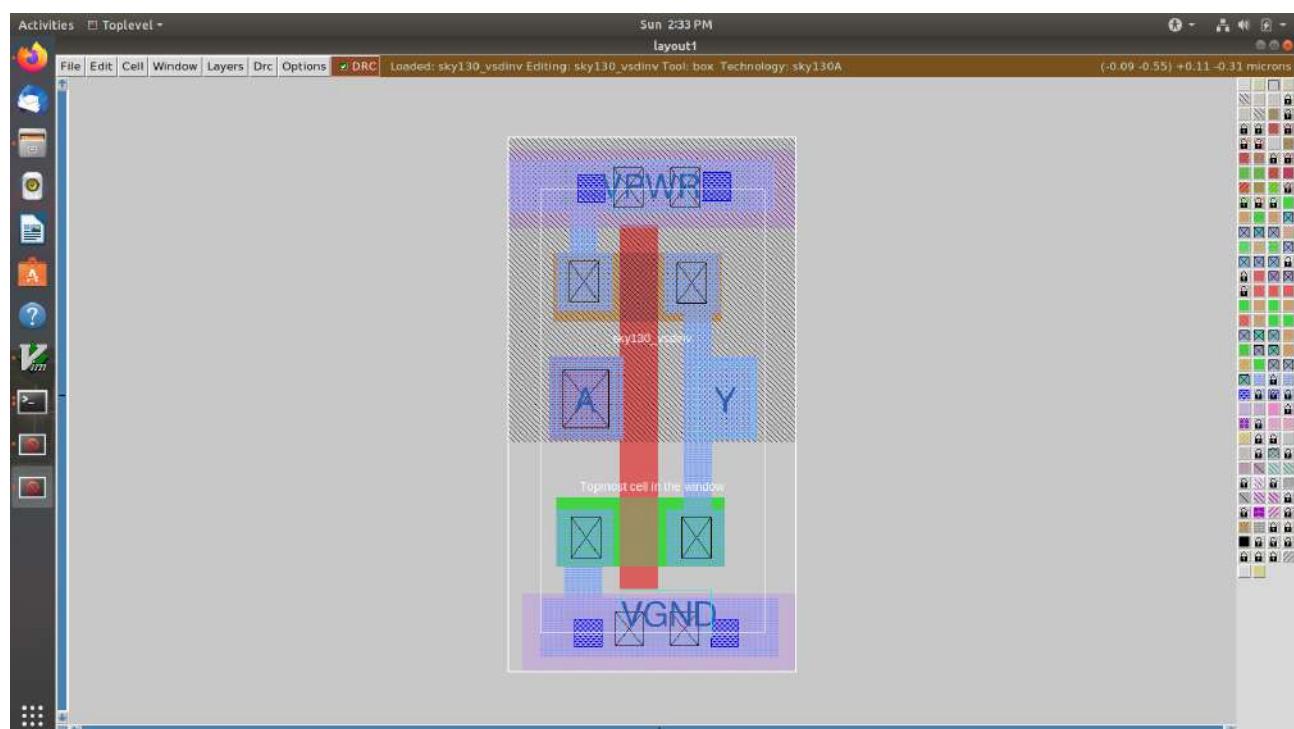
```
save sky130_vsdinv.mag
```

Command to open the newly saved layout

```
# Command to open custom inverter layout in magic
```

```
magic -T sky130A.tech sky130_vsdinv.mag &
```

Screenshot of newly saved layout



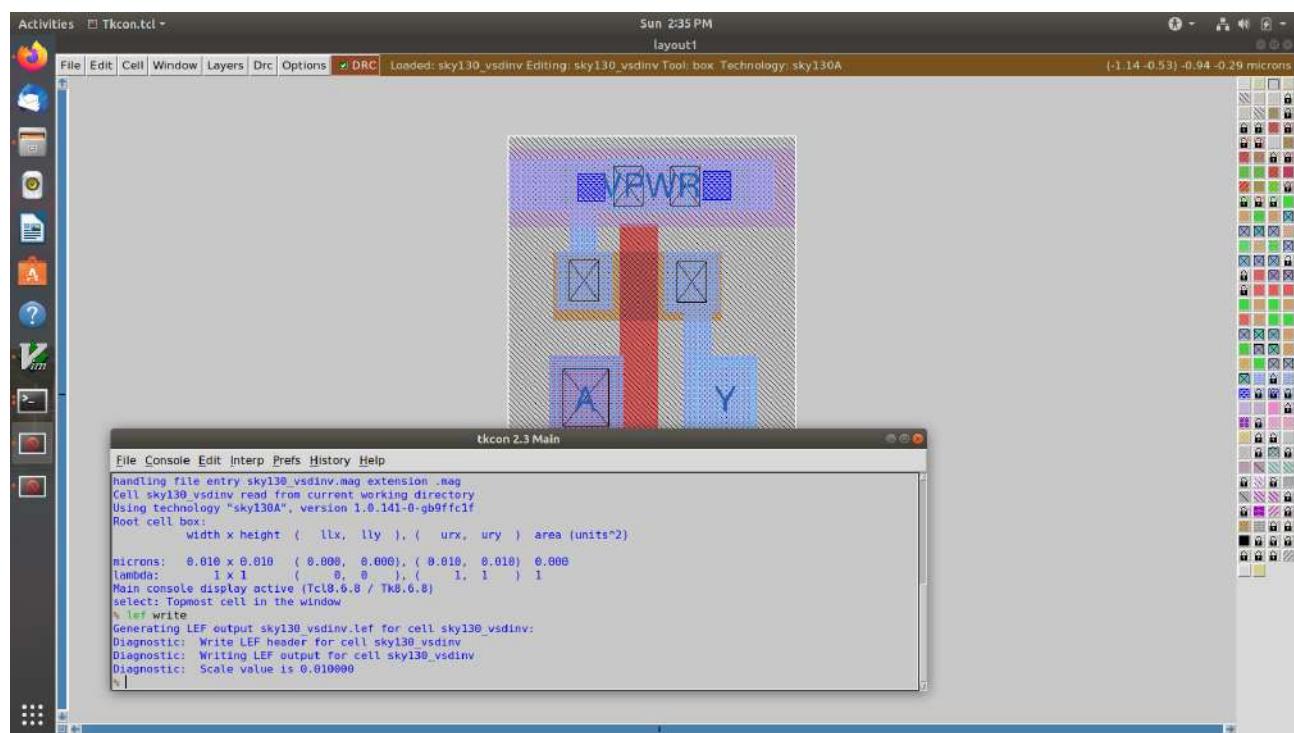
3. Generate lef from the layout.

Command for tkcon window to write lef

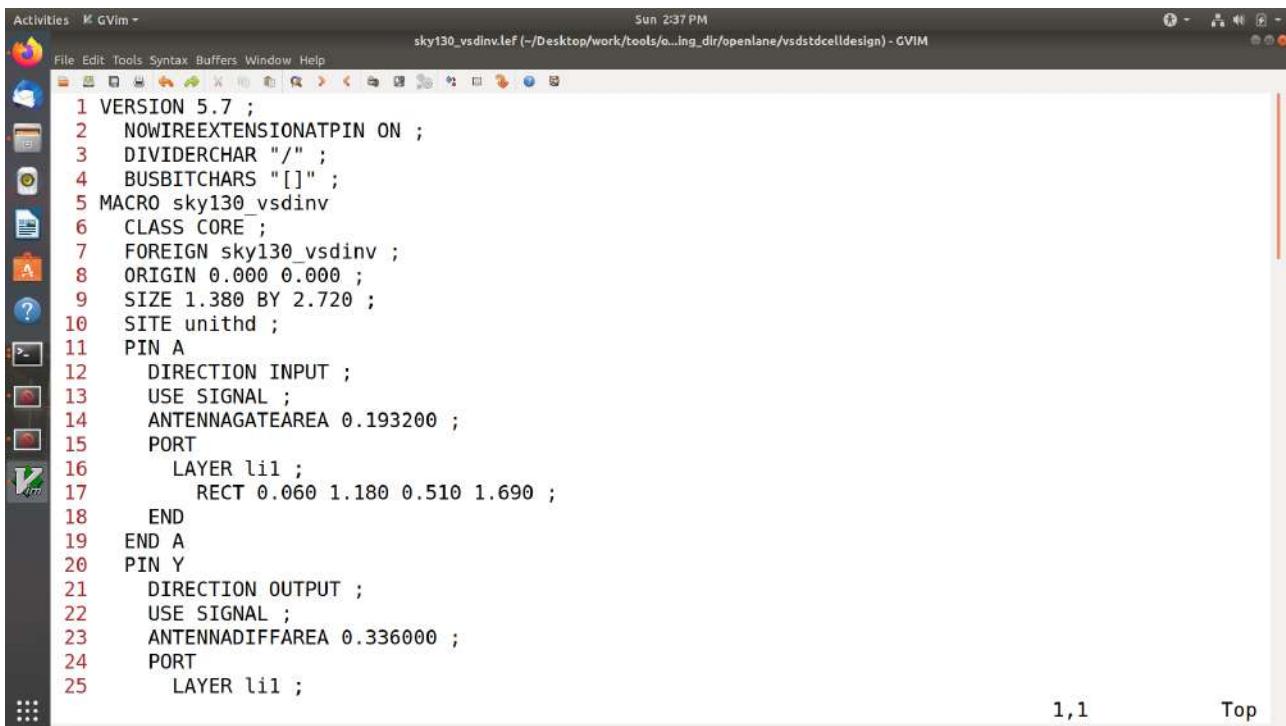
```
# lef command
```

```
lef write
```

Screenshot of command run



Screenshot of newly created lef file



A screenshot of the GVIM text editor window. The title bar reads "Activities K. GVim" and "sky130_vsdinv.lef (~/Desktop/work/tools/openlane/designs/sky130_vsdinv.lef) - GVIM". The status bar shows "Sun 2:37 PM" and "1,1 Top". The main pane displays a LEF (Liberty Cell Format) file with the following content:

```
1 VERSION 5.7 ;
2 NOWIREEXTENSIONATPIN ON ;
3 DIVIDERCHAR "/" ;
4 BUSBITCHARS "[]" ;
5 MACRO sky130_vsdinv
6 CLASS CORE ;
7 FOREIGN sky130_vsdinv ;
8 ORIGIN 0.000 0.000 ;
9 SIZE 1.380 BY 2.720 ;
10 SITE unithd ;
11 PIN A
12     DIRECTION INPUT ;
13     USE SIGNAL ;
14     ANTENNAGATEAREA 0.193200 ;
15     PORT
16         LAYER li1 ;
17         RECT 0.060 1.180 0.510 1.690 ;
18     END
19 END A
20 PIN Y
21     DIRECTION OUTPUT ;
22     USE SIGNAL ;
23     ANTENNADIFFAREA 0.336000 ;
24     PORT
25         LAYER li1 ;
```

4. Copy the newly generated lef and associated required lib files to 'picorv32a' design 'src' directory.

Commands to copy necessary files to 'picorv32a' design 'src' directory

```
# Copy lef file
```

```
cp sky130_vsdinv.lef ~/Desktop/work/tools/openlane_working_dir/openlane/designs/
picorv32a/src/
```

```
# List and check whether it's copied
```

```
ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
```

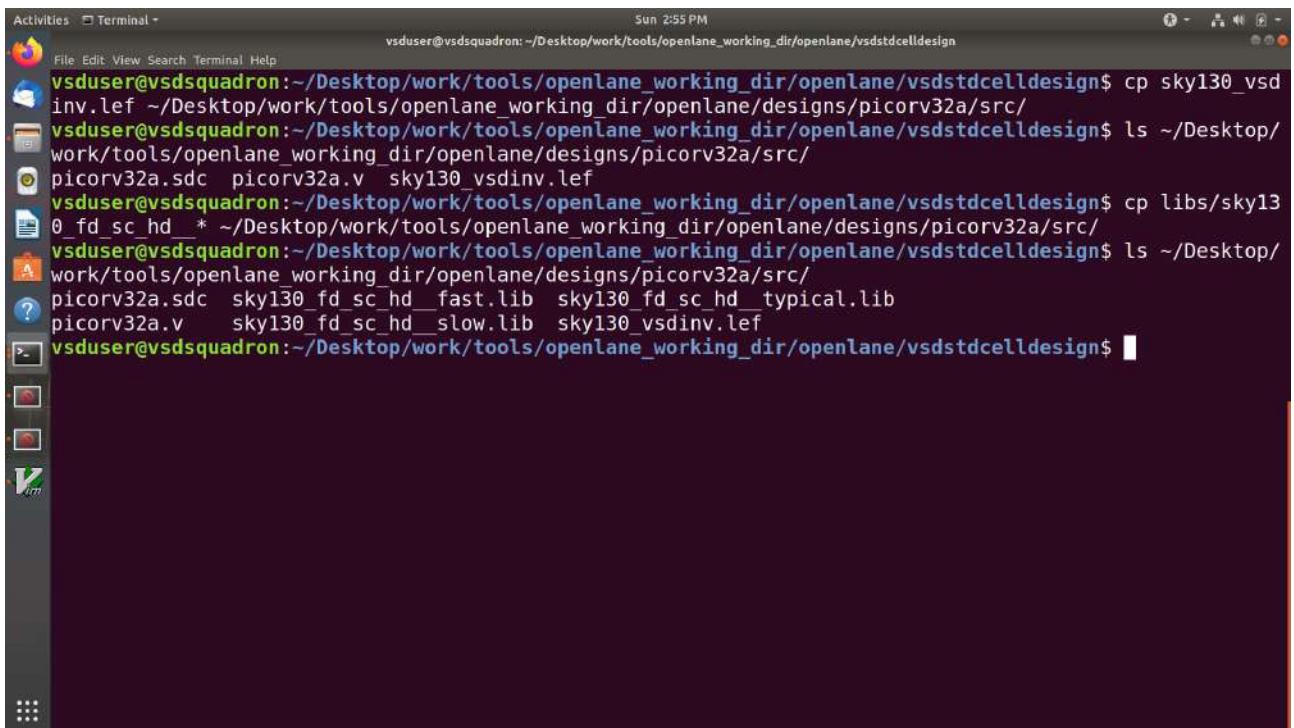
```
# Copy lib files
```

```
cp libs/sky130_fd_sc_hd_* ~/Desktop/work/tools/openlane_working_dir/openlane/designs/
picorv32a/src/
```

```
# List and check whether it's copied
```

```
ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
```

Screenshot of commands run



```
Activities Terminal Sun 2:55 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cp sky130_vsdinv.lef ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
picorv32a.sdc picorv32a.v sky130_vsdinv.lef
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cp libs/sky130_fd_sc_hd_* ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/
picorv32a.sdc sky130_fd_sc_hd_fast.lib sky130_fd_sc_hd_typical.lib
picorv32a.v sky130_fd_sc_hd_slow.lib sky130_vsdinv.lef
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```

5. Edit 'config.tcl' to change lib file and add the new extra lef into the openlane flow.

Commands to be added to config.tcl to include our custom cell in the openlane flow

```
set ::env(LIB_SYNTH) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib"

set ::env(LIB_FASTEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib"

set ::env(LIB_SLOWEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib"
```

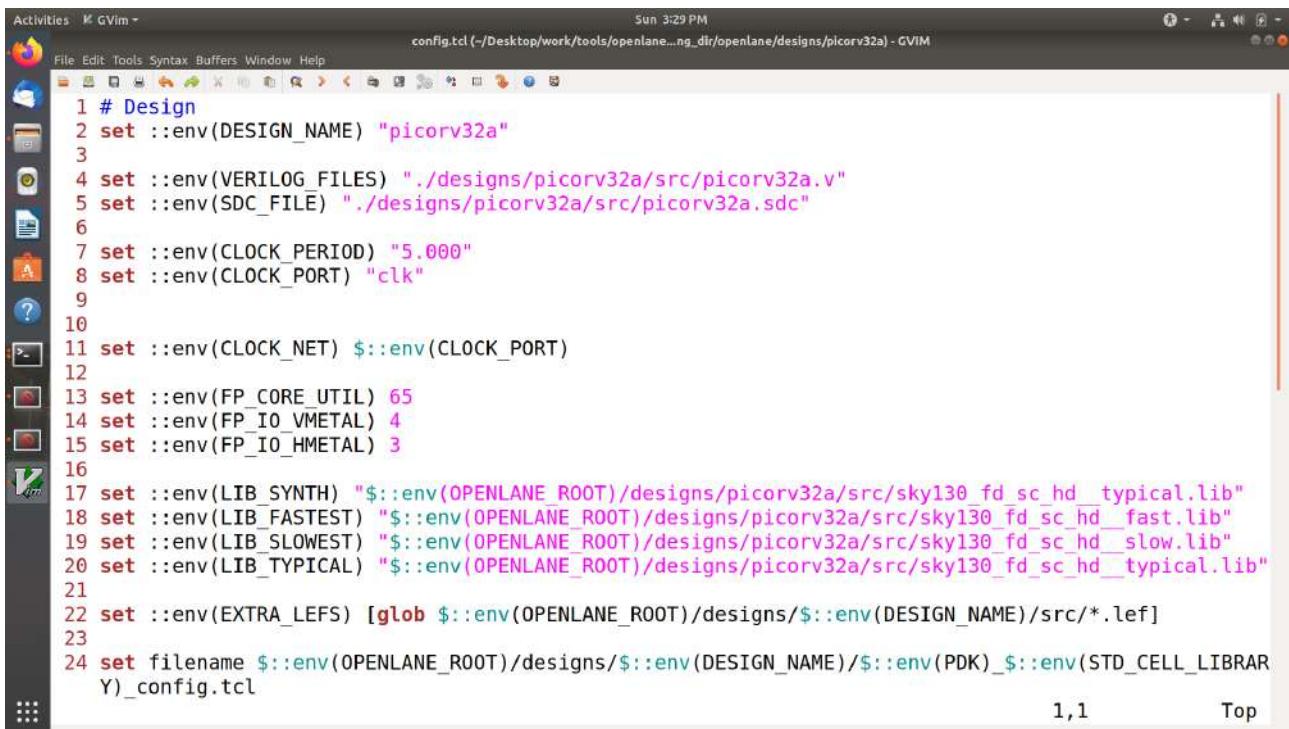
```

set ::env(LIB_TYPICAL) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/
sky130_fd_sc_hd_typical.lib"

set ::env(EXTRA_LEFS) [glob $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/
src/*.lef]

```

Edited config.tcl to include the added lef and change library to ones we added in src directory



```

Activities  M GVIM - Sun 3:29 PM config.tcl (-/Desktop/work/tools/openlane...ng_dir/openlane/designs/picorv32a) - GVIM
File Edit Tools Syntax Buffers Window Help
1 # Design
2 set ::env(DESIGN_NAME) "picorv32a"
3
4 set ::env(VERILOG_FILES) "./designs/picorv32a/src/picorv32a.v"
5 set ::env(SDC_FILE) "./designs/picorv32a/src/picorv32a.sdc"
6
7 set ::env(CLOCK_PERIOD) "5.000"
8 set ::env(CLOCK_PORT) "clk"
9
10
11 set ::env(CLOCK_NET) $::env(CLOCK_PORT)
12
13 set ::env(FP_CORE_UTIL) 65
14 set ::env(FP_IO_VMETAL) 4
15 set ::env(FP_IO_HMETAL) 3
16
17 set ::env(LIB_SYNTH) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib"
18 set ::env(LIB_FASTEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib"
19 set ::env(LIB_SLOWEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib"
20 set ::env(LIB_TYPICAL) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib"
21
22 set ::env(EXTRA_LEFS) [glob $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/src/*.lef]
23
24 set filename $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/$::env(PDK)_$::env(STD_CELL_LIBRARY)_config.tcl
1,1 Top

```

6. Run openlane flow synthesis with newly inserted custom inverter cell.

Commands to invoke the OpenLANE flow include new lef and perform synthesis

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:v0.21'
```

```
# Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command
```

```
docker
```

```
# Now that we have entered the OpenLANE flow contained docker sub-system we can invoke the OpenLANE flow in the interactive mode using the following command
```

```
./flow.tcl -interactive
```

```
# Now that OpenLANE flow is open we have to input the required packages for proper functionality of the OpenLANE flow
```

```
package require openlane 0.9
```

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the design creating some necessary files and directories for running a specific design which in our case is 'picorv32a'
```

```
prep -design picorv32a
```

```
# Additional commands to include newly added lef to openlane flow
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

Now that the design is prepped and ready, we can run synthesis using following command

`run_synthesis`

Screenshots of commands run

Activities Terminal Sun 3:36 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
vsduser@vsdsquadron:~$ cd Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ docker
bash-4.2$ ./flow.tcl -interactive
[INFO]:

[INFO]: Version: v0.21
[INFO]: Running interactively
% package require openlane 0.9
% prep -design picorv32a
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
```

Activities Terminal Sun 3:37 PM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane

```
File Edit View Search Terminal Help
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
? sky130_fd_sc_hd.lef: SITEs matched found: 0
? sky130_fd_sc_hd.lef: MACROs matched found: 437
? sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
? sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
? sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
? sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
? sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
? sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
```

```

Activities Terminal - Sun 3:37 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
::: % run_synthesis

```

```

Activities Terminal - Sun 3:45 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
::: %

```

7. Remove/reduce the newly introduced violations with the introduction of custom inverter cell by modifying design parameters.

Noting down current design values generated before modifying parameters to improve timing

```

Activities Terminal - Sun 4:00 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
sky130_fd_sc_hd_o31la_2 8
sky130_fd_sc_hd_o31a_2 19
sky130_fd_sc_hd_o31ai_2 1
sky130_fd_sc_hd_o32a_2 109
sky130_fd_sc_hd_o41a_2 2
sky130_fd_sc_hd_or2_2 1088
sky130_fd_sc_hd_or2b_2 25
sky130_fd_sc_hd_or3_2 68
sky130_fd_sc_hd_or3b_2 5
sky130_fd_sc_hd_or4_2 93
sky130_fd_sc_hd_or4b_2 6
sky130_fd_sc_hd_or4bb_2 2
sky130_vsdinv 1554

Chip area for module '\picorv32a': 147712.918400

29. Executing Verilog backend.
Dumping module '\picorv32a'.

Warnings: 307 unique messages, 307 total
End of script. Logfile hash: ea6f91c309, CPU: user 11.69s system 3.17s, MEM: 95.95 MB peak
Yosys 0.9+3621 (git sha1 84e9fa7, gcc 8.3.1 -fPIC -Os)
Time spent: 57% 2x abc (18 sec), 12% 33x opt_expr (4 sec), ...
[INFO]: Changing netlist from 0 to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis
/picorv32a.synthesis.v
[INFO]: Running Static Timing Analysis...
[INFO]: current step index: 2
OpenSTA 2.2.0-28b40207a8 Copyright (c) 2019, Parallever Software, Inc.

```

```

Activities Terminal - Sun 4:13 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.9460000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.9460000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
[INFO]: % 

```

Commands to view and change parameters to improve timing and run synthesis

Now once again we have to prep design so as to update variables

prep -design picorv32a -tag 24-03_10-03 -overwrite

```
# Addiitional commands to include newly added lef to openlane flow merged.lef
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to display current value of variable SYNTH_STRATEGY
```

```
echo $::env(SYNTH_STRATEGY)
```

```
# Command to set new value for SYNTH_STRATEGY
```

```
set ::env(SYNTH_STRATEGY) "DELAY 3"
```

```
# Command to display current value of variable SYNTH_BUFFERING to check whether it's  
enabled
```

```
echo $::env(SYNTH_BUFFERING)
```

```
# Command to display current value of variable SYNTH_SIZING
```

```
echo $::env(SYNTH_SIZING)
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Command to display current value of variable SYNTH_DRIVING_CELL to check whether it's the proper cell or not
```

```
echo $::env(SYNTH_DRIVING_CELL)
```

```
# Now that the design is prepped and ready, we can run synthesis using following command
```

```
run_synthesis
```

Screenshot of merged.lef in tmp directory with our custom inverter as macro

```
68236 MACRO Sky130_vsdinv
68237   CLASS CORE ;
68238   FOREIGN sky130_vsdinv ;
68239   ORIGIN 0.000 0.000 ;
68240   SIZE 1.380 BY 2.720 ;
68241   SITE unithd ;
68242   PIN A
68243     DIRECTION INPUT ;
68244     USE SIGNAL ;
68245     ANTENNAGATEAREA 0.193200 ;
68246     PORT
68247       LAYER l1l ;
68248       RECT 0.060 1.180 0.510 1.690 ;
68249     END
68250   END A
68251   PIN Y
68252     DIRECTION OUTPUT ;
68253     USE SIGNAL ;
68254     ANTENNADIFFAREA 0.336000 ;
68255     PORT
68256       LAYER l1l ;
68257       RECT 0.760 1.960 1.100 2.330 ;
68258       RECT 0.880 1.690 1.050 1.960 ;
68259       RECT 0.880 1.180 1.330 1.690 ;
68260       RECT 0.880 0.760 1.050 1.180 ;
```

Screenshots of commands run

```
Activities Terminal Sun 5:09 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% prep -design picorv32a -tag 24-03_10-03 -overwrite
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[WARNING]: Removing existing run /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
::: mergeLef.py : Merging LEFs
::: mergeLef.py : Merging LEFs
```

```
Activities Terminal Sun 5:09 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add lefs -src $lefs
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% echo $::env(SYNTH_STRATEGY)
AREA 0
% set ::env(SYNTH_STRATEGY) "DELAY 3"
DELAY 3
% echo $::env(SYNTH_BUFFERING)
1
% echo $::env(SYNTH_SIZING)
0
% set ::env(SYNTH_SIZING) 1
1
% echo $::env(SYNTH_DRIVING_CELL)
sky130_fd_sc_hd_inv_8
::: % run_synthesis
```

```
Activities Terminal - Sun 5:10 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
::: %
```

Comparing to previously noted run values area has increased and worst negative slack has become 0

```

Activities Terminal - Sun 5:11 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
sky130_fd_sc_hd_o32a_2 9
sky130_fd_sc_hd_o32ai_2 3
sky130_fd_sc_hd_o41ai_2 18
sky130_fd_sc_hd_or2_2 80
sky130_fd_sc_hd_or2b_2 264
sky130_fd_sc_hd_or3_2 6
sky130_fd_sc_hd_or3b_2 5
sky130_fd_sc_hd_or4_2 68
sky130_fd_sc_hd_or4b_2 4
sky130_fd_sc_hd_xnor2_2 700
sky130_fd_sc_hd_xor2_2 1164
sky130_vsdinv 1434

Chip area for module '\picorv32a': 181730.544000

29. Executing Verilog backend.
Dumping module '\picorv32a'.

Warnings: 307 unique messages, 307 total
End of script. Logfile hash: befd735e75, CPU: user 12.56s system 2.87s, MEM: 97.45 MB peak
Yosys 0.9+3621 (git sha1 84e9fa7, gcc 8.3.1 -fPIC -Os)
Time spent: 64% 2x abc (26 sec), 10% 33x opt_expr (4 sec), ...
[INFO]: Changing netlist from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis.v to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis.v
[INFO]: Running Static Timing Analysis...
[INFO]: current step index: 11
OpenSTA 2.2.0-28b10207a8 Copyright (c) 2019, Parallever Software, Inc.

```

```

Activities Terminal - Sun 5:11 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_idx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_idx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_idx $clk_idx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_idx $rst_idx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk

# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful

```

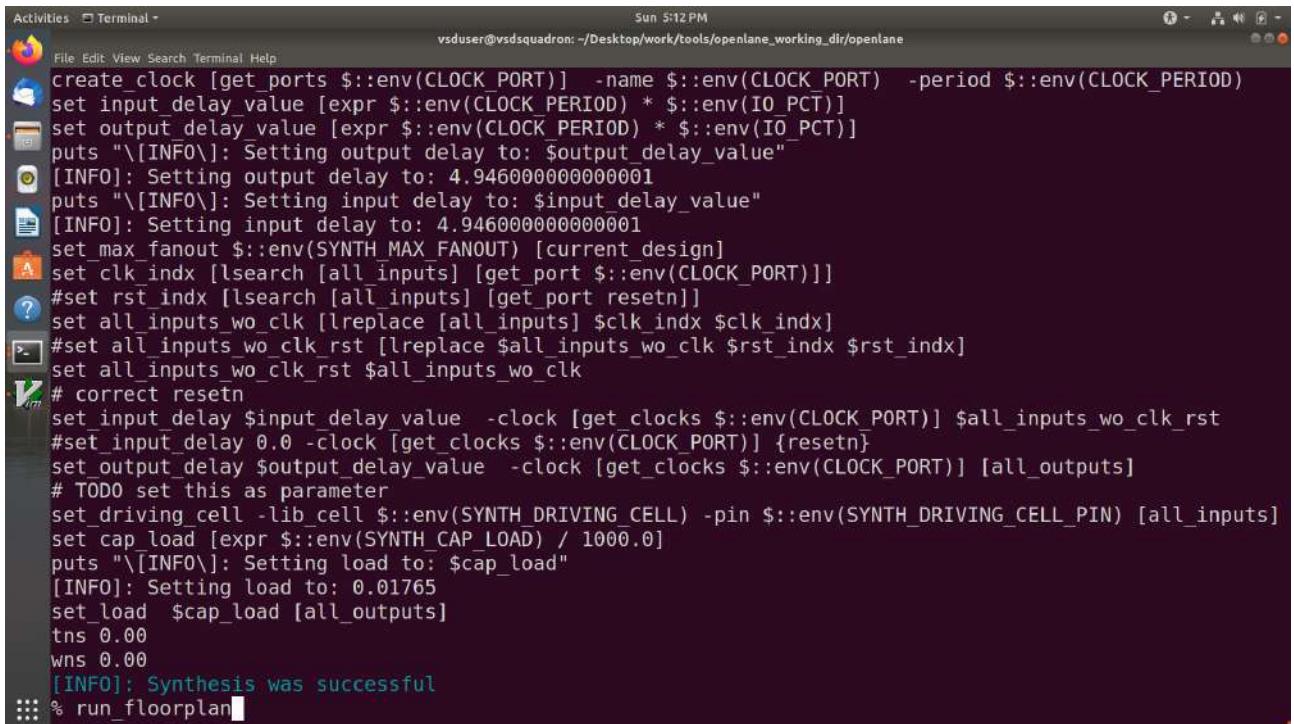
8. Once synthesis has accepted our custom inverter we can now run floorplan and placement and verify the cell is accepted in PnR flow.

Now that our custom inverter is properly accepted in synthesis we can now run floorplan using following command

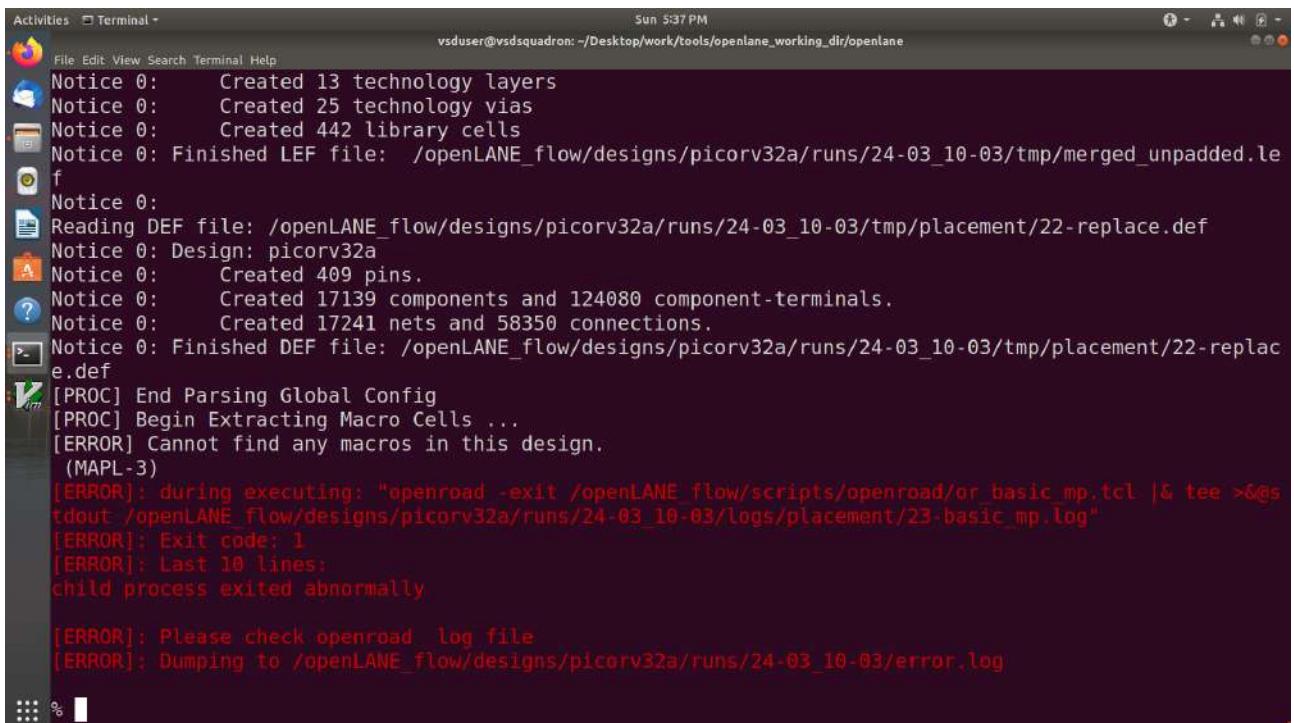
Now we can run floorplan

run_floorplan

Screenshots of command run



```
Activities Terminal Sun 5:12 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
:: % run_floorplan
```



```
Activities Terminal Sun 5:37 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/22-replace.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/22-replace.def
[PROC] End Parsing Global Config
[PROC] Begin Extracting Macro Cells ...
[ERROR] Cannot find any macros in this design.
(MAPL-3)
[ERROR]: during executing: "openroad -exit /openLANE_flow/scripts/openroad/or_basic_mp.tcl |& tee >& stdout /openLANE_flow/designs/picorv32a/runs/24-03_10-03/logs/placement/23-basic_mp.log"
[ERROR]: Exit code: 1
[ERROR]: Last 10 lines:
child process exited abnormally

[ERROR]: Please check openroad log file
[ERROR]: Dumping to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/error.log
:: %
```

Since we are facing unexpected un-explainable error while using run_floorplan command, we can instead use the following set of commands available based on information from Desktop/work/tools/openlane_working_dir/openlane/scripts/tcl_commands/floorplan.tcl and also based on Floorplan Commands section in Desktop/work/tools/openlane_working_dir/openlane/docs/source/OpenLANE_commands.md

Following commands are altogether sourced in "run_floorplan" command

init_floorplan

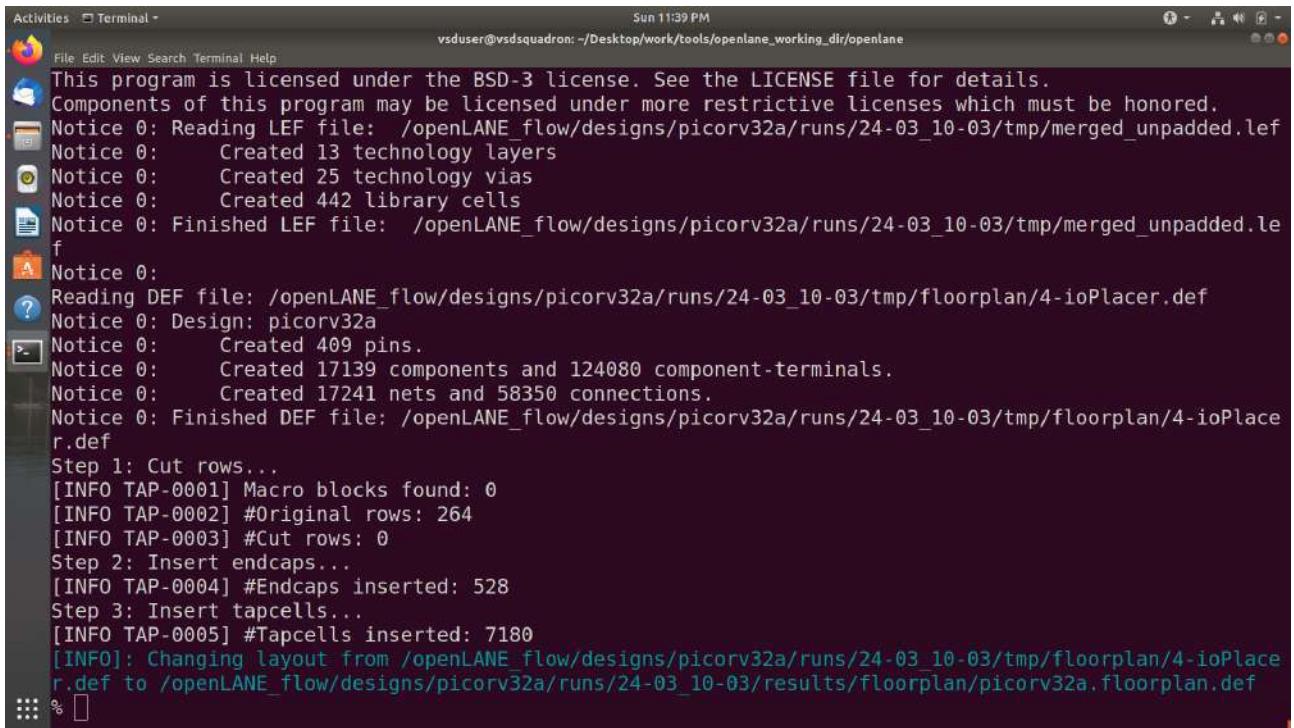
place_io

tap_decap_or

Screenshots of commands run

```
Activities Terminal Sun 11:38 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
% init_floorplan
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 3
OpenROAD 0.9.0 1415572a73
A This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
[INFO IFP-0001] Added 264 rows of 1566 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 731.615 742.335 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/3-verilog2def.die_area.rpt.
[INFO] Floorplanned on a core area of 5.52 10.88 725.88 728.96 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/3-verilog2def.core_area.rpt.
[INFO]: Core area width: 720.36
[INFO]: Core area height: 718.08
[INFO]: Changing layout from 0 to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def
::: % place_io
```

```
Activities Terminal Sun 11:38 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% place_io
[INFO]: Running IO Placement...
[INFO]: current step index: 4
OpenROAD 0.9.0 1415572a73
A This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def
#Macro blocks found: 0
Using 5u default boundaries offset
Random pin placement
RandomMode Even
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/3-verilog2def_openroad.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
::: % tap_decap_or
```



```
Sun 11:39 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 17139 components and 124080 component-terminals.
Notice 0:     Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Step 1: Cut rows...
[INFO TAP-0001] Macro blocks found: 0
[INFO TAP-0002] #Original rows: 264
[INFO TAP-0003] #Cut rows: 0
Step 2: Insert endcaps...
[INFO TAP-0004] #Endcaps inserted: 528
Step 3: Insert tapcells...
[INFO TAP-0005] #Tapcells inserted: 7180
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/floorplan/picorv32a.floorplan.def
```

Now that floorplan is done we can do placement using following command

Now we are ready to run placement

run_placement

Screenshots of command run

```

Activities Terminal Sun 11:49 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 17139 components and 124080 component-terminals.
Notice 0:     Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def
Step 1: Cut rows...
[INFO TAP-0001] Macro blocks found: 0
[INFO TAP-0002] #Original rows: 264
[INFO TAP-0003] #Cut rows: 0
Step 2: Insert endcaps...
[INFO TAP-0004] #Endcaps inserted: 528
Step 3: Insert tapcells...
[INFO TAP-0005] #Tapcells inserted: 7180
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/4-ioPlacer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/floorplan/picorv32a.floorplan.def
::: % run_placement

```

```

Activities Terminal Sun 11:51 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
legalized HPWL      910806.5 u
delta HPWL          2 %
[INFO DPL-0020] Mirrored 6650 instances
[INFO DPL-0021] HPWL before      910806.5 u
[INFO DPL-0022] HPWL after       895297.0 u
[INFO DPL-0023] HPWL delta      -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/6-resizer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 10
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
::: %

```

Commands to load placement def in magic in another terminal

Change directory to path containing generated placement def

```

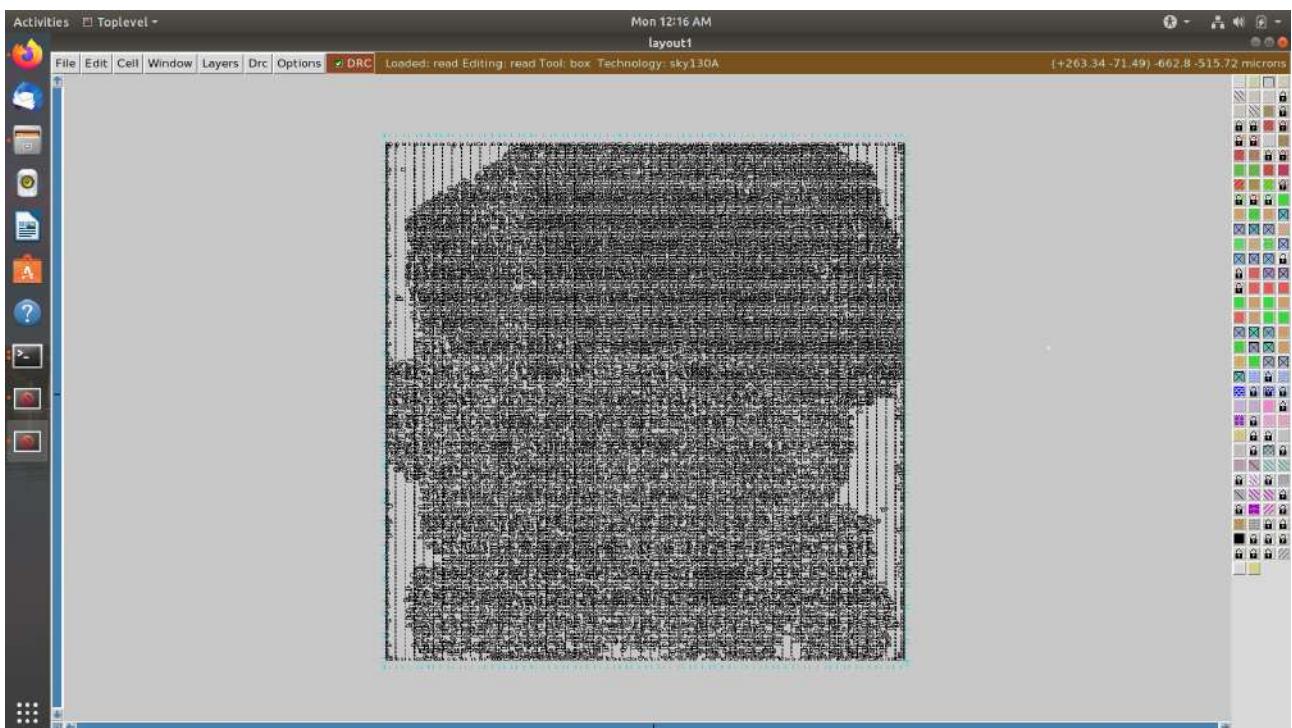
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
24-03_10-03/results/placement/

```

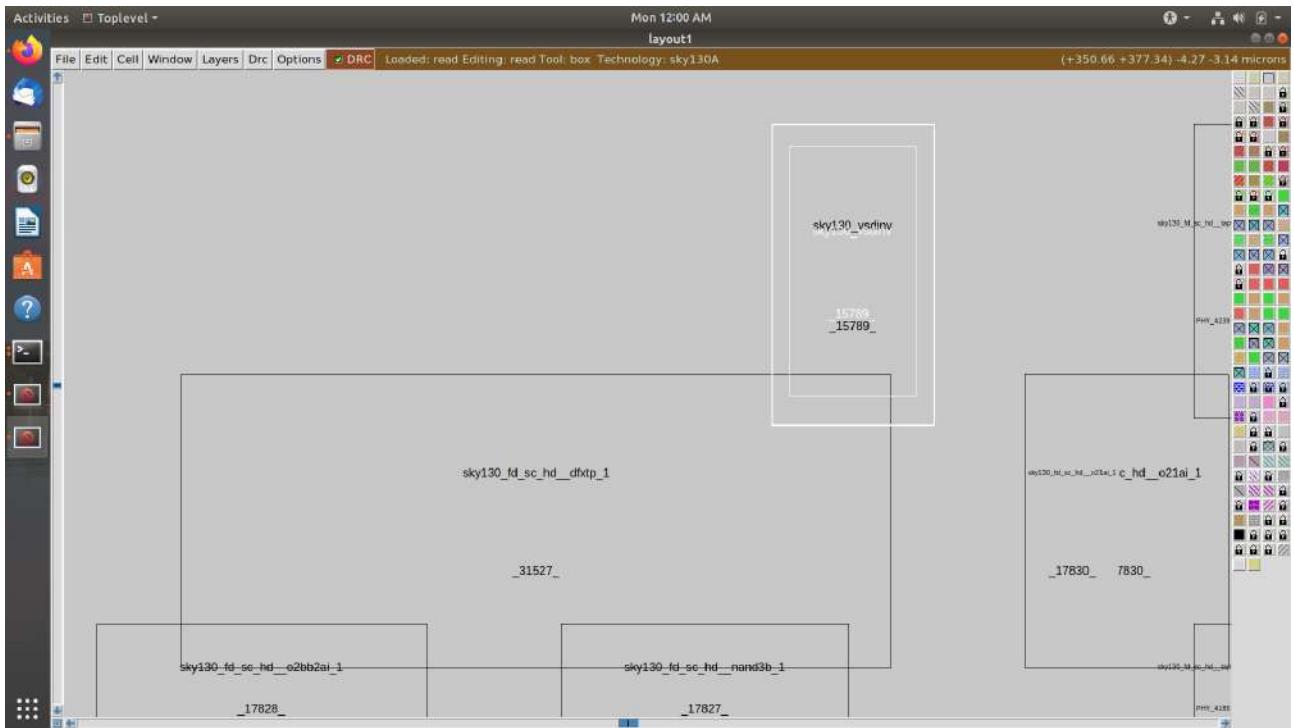
```
# Command to load the placement def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def  
&
```

Screenshot of placement def in magic



Screenshot of custom inverter inserted in placement def with proper abutment

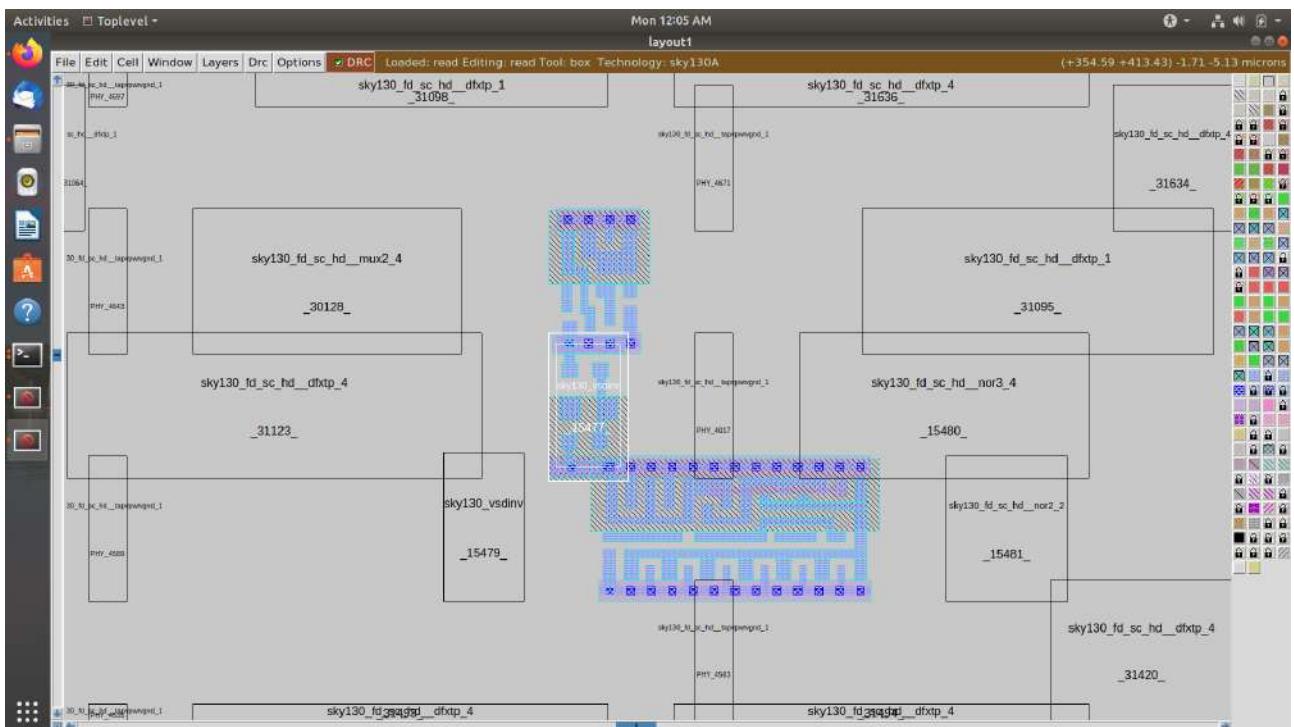
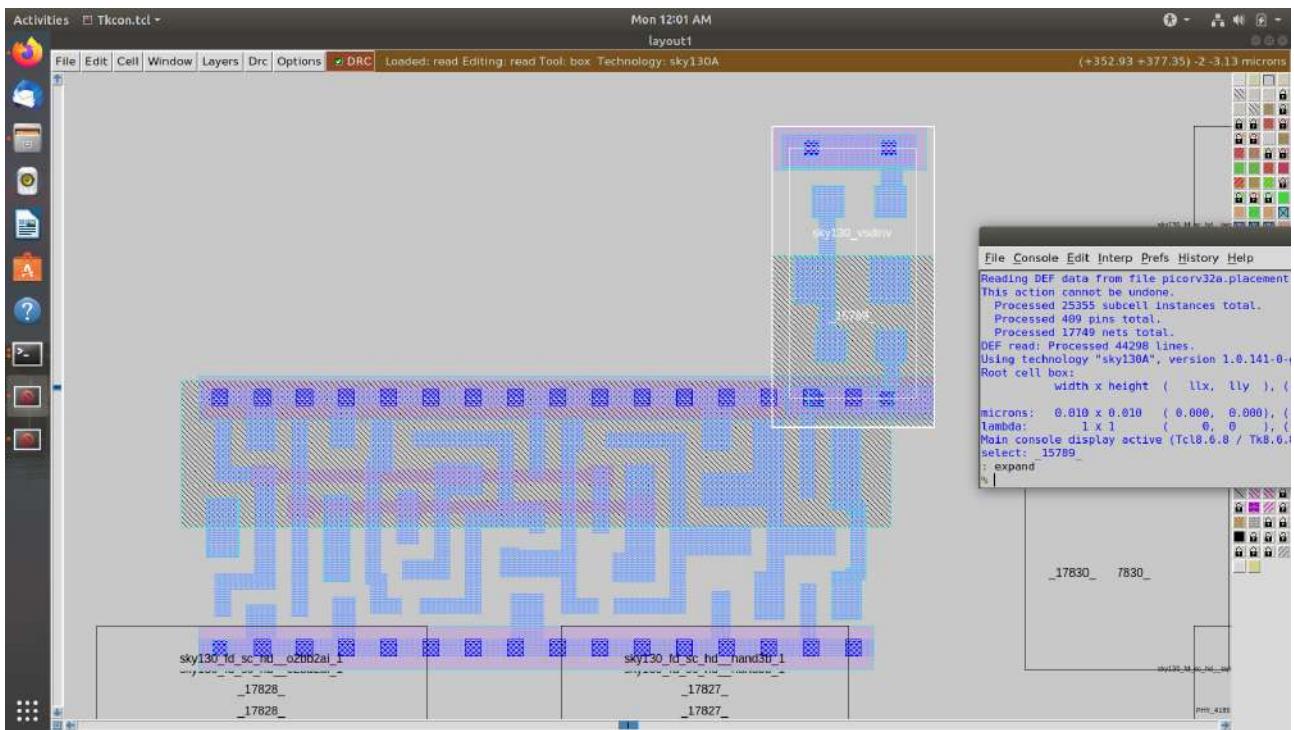


Command for tkcon window to view internal layers of cells

```
# Command to view internal connectivity layers
```

```
expand
```

Abutment of power pins with other cell from library clearly visible



9. Do Post-Synthesis timing analysis with OpenSTA tool.

Since we are having own after improved timing run we are going to do timing analysis on initial run of synthesis which has lots of violations and no parameters were added to improve timing

Commands to invoke the OpenLANE flow include new lef and perform synthesis

Change directory to openlane flow directory

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:vo.21'
```

Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command

```
docker
```

Now that we have entered the OpenLANE flow contained docker sub-system we can invoke the OpenLANE flow in the Interactive mode using the following command

```
./flow.tcl -interactive
```

Now that OpenLANE flow is open we have to input the required packages for proper functionality of the OpenLANE flow

```
package require openlane 0.9
```

Now the OpenLANE flow is ready to run any design and initially we have to prep the design creating some necessary files and directories for running a specific design which in our case is 'picorv32a'

```
prep -design picorv32a
```

```
# Additional commands to include newly added lef to openlane flow
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Now that the design is prepped and ready, we can run synthesis using following command
```

```
run_synthesis
```

Commands run final screenshot

```
Activities Terminal Tue 5:52 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
```

Newly created pre_sta.conf for STA analysis in openlane directory

Newly created `my_base.sdc` for STA analysis in `openlane/designs/picorv32a/src` directory based on the file `openlane/scripts/base.sdc`

```
Activities  M Gvim - Tue 5:55 AM my_base.sdc (~Desktop/work/tools/openlane/openlane/designs/picorv32a/src) - GVIM1
File Edit Tools Syntax Buffers Window Help
1 set ::env(CLOCK_PORT) cLK
2 set ::env(CLOCK_PERIOD) 24.73
3 #set ::env(SYNTH_DRIVING_CELL) sky130_vsdinv
4 set ::env(SYNTH_DRIVING_CELL) sky130_fd_sc_hd_inv_8
5 set ::env(SYNTH_DRIVING_CELL_PIN) Y
6 set ::env(SYNTH_CAP_LOAD) 17.653
7 set ::env(IO_PCT) 0.2
8 set ::env(SYNTH_MAX_FANOUT) 6
9
10 create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
11 set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
12 set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
13 puts "\[INFO\]: Setting output delay to: $output_delay_value"
14 puts "\[INFO\]: Setting input delay to: $input_delay_value"
15
16 set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
17
18 set clk_idx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
19 #set rst_idx [lsearch [all_inputs] [get_port resetn]]
20 set all_inputs_wo_clk [lreplace [all_inputs] $clk_idx $clk_idx]
21 #set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_idx $rst_idx]
22 set all_inputs_wo_clk_rst $all_inputs_wo_clk
23
24 # correct resetn
```

24,16

Top

```
Activities  M Gvim - Tue 5:55 AM my_base.sdc (~Desktop/work/tools/openlane/openlane/designs/picorv32a/src) - GVIM1
File Edit Tools Syntax Buffers Window Help
24 # correct resetn
25 set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
26 #set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
27 set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
28
29 # TODO set this as parameter
30 set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
31 set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
32 puts "\[INFO\]: Setting load to: $cap_load"
33 set_load $cap_load [all_outputs]
```

25,16

Bot

Commands to run STA in another terminal

```
# Change directory to openlane
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# Command to invoke OpenSTA tool with script
```

```
sta pre_sta.conf
```

Screenshots of commands run

```
Activities Terminal Tue 6:04 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ sta pre_sta.conf
OpenSTA 2.4.0 ac3479bc24 Copyright (c) 2021, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type `show copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type `show warranty'.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib line 24, default_fanout_load is 0.0.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib line 23, default_fanout_load is 0.0.
[INFO]: Setting output delay to: 4.946000000000001
[INFO]: Setting input delay to: 4.946000000000001
[INFO]: Setting load to: 0.017653
Startpoint: _26669_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _26669_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _26669/_0 (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.00  0.00  cpuregs[0][0] (net)
          0.03  0.00  0.00 ^ _15938/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _15938/_X (sky130_fd_sc_hd_buf_1)
          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _26669/_D (sky130_fd_sc_hd_dfxtp_2)
          0.02  0.00  0.23  data arrival time
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data arrival time
          -0.02 -0.02  0.00  slack (MET)
```

```
Activities Terminal Tue 6:05 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _26669/_0 (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.00  0.00  cpuregs[0][0] (net)
          0.03  0.00  0.00 ^ _15938/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _15938/_X (sky130_fd_sc_hd_buf_1)
          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _26669/_D (sky130_fd_sc_hd_dfxtp_2)
          0.02  0.00  0.23  data arrival time
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _26669_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data arrival time
          -0.02 -0.02  0.00  slack (MET)
```

```

Activities Terminal - Tue 6:05 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
Startpoint: _27860_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _27762_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
-----
          0.00 0.00 0.00 clock clk (rise edge)
          0.00 0.00 0.00 clock network delay (ideal)
          0.00 0.00 0.00 ^ _27860/_CLK (sky130_fd_sc_hd_dfxtp_2)
          0.10 0.64 0.64 ^ _27860/_Q (sky130_fd_sc_hd_dfxtp_2)
          4   0.01      irq_mask[1] (net)
          0.10 0.00 0.64 ^ _13108/_A (sky130_vsdinv)
          0.13 0.15 0.79 v _13108/_Y (sky130_vsdinv)
          6   0.01      _10510_ (net)
          0.13 0.00 0.79 v _13113/_A1 (sky130_fd_sc_hd_a221o_2)
          0.08 0.65 1.44 v _13113/_X (sky130_fd_sc_hd_a221o_2)
          1   0.00      _10515_ (net)
          0.08 0.00 1.44 v _13132/_A (sky130_fd_sc_hd_or4_2)
          0.21 1.53 2.98 v _13132/_X (sky130_fd_sc_hd_or4_2)
          1   0.00      _10534_ (net)
          0.21 0.00 2.98 v _13160/_A1 (sky130_fd_sc_hd_o2111a_2)
          0.07 0.54 3.52 v _13160/_X (sky130_fd_sc_hd_o2111a_2)
          2   0.00      _10562_ (net)
          0.07 0.00 3.52 v _13161/_C (sky130_fd_sc_hd_or3_2)
          0.17 0.97 4.48 v _13161/_X (sky130_fd_sc_hd_or3_2)
          2   0.00      _10563_ (net)
          0.17 0.00 4.48 v _13164/_A (sky130_fd_sc_hd_or2_2)

```

```

Activities Terminal - Tue 6:08 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
          0.14 0.68 47.22 v _13750/_X (sky130_fd_sc_hd_or2_2)
          3   0.01      10970_ (net)
          0.14 0.00 47.22 v _13751/_B (sky130_fd_sc_hd_or2_2)
          0.12 0.66 47.88 v _13751/_X (sky130_fd_sc_hd_or2_2)
          2   0.00      10971_ (net)
          0.12 0.00 47.88 v _13754/_B2 (sky130_fd_sc_hd_o221a_2)
          0.07 0.44 48.32 v _13754/_X (sky130_fd_sc_hd_o221a_2)
          1   0.00      03928_ (net)
          0.07 0.00 48.32 v _27762/_D (sky130_fd_sc_hd_dfxtp_2)
          48.32 data arrival time
          0.00 24.73 24.73 clock clk (rise edge)
          0.00 24.73 24.73 clock network delay (ideal)
          0.00 24.73 24.73 clock reconvergence pessimism
          24.73 ^ _27762/_CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.29 24.44 library setup time
          24.44 data required time
          24.44 data required time
          -48.32 data arrival time
          -23.89 slack (VIOLATED)

tns -711.59
wns -23.89
%
```

Since more fanout is causing more delay we can add parameter to reduce fanout and do synthesis again

Commands to include new lef and perform synthesis

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the  
design creating some necessary files and directories for running a specific design which in  
our case is 'picorv32a'
```

```
prep -design picorv32a -tag 25-03_18-52 -overwrite
```

```
# Additional commands to include newly added lef to openlane flow
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

```
# Command to set new value for SYNTH_MAX_FANOUT
```

```
set ::env(SYNTH_MAX_FANOUT) 4
```

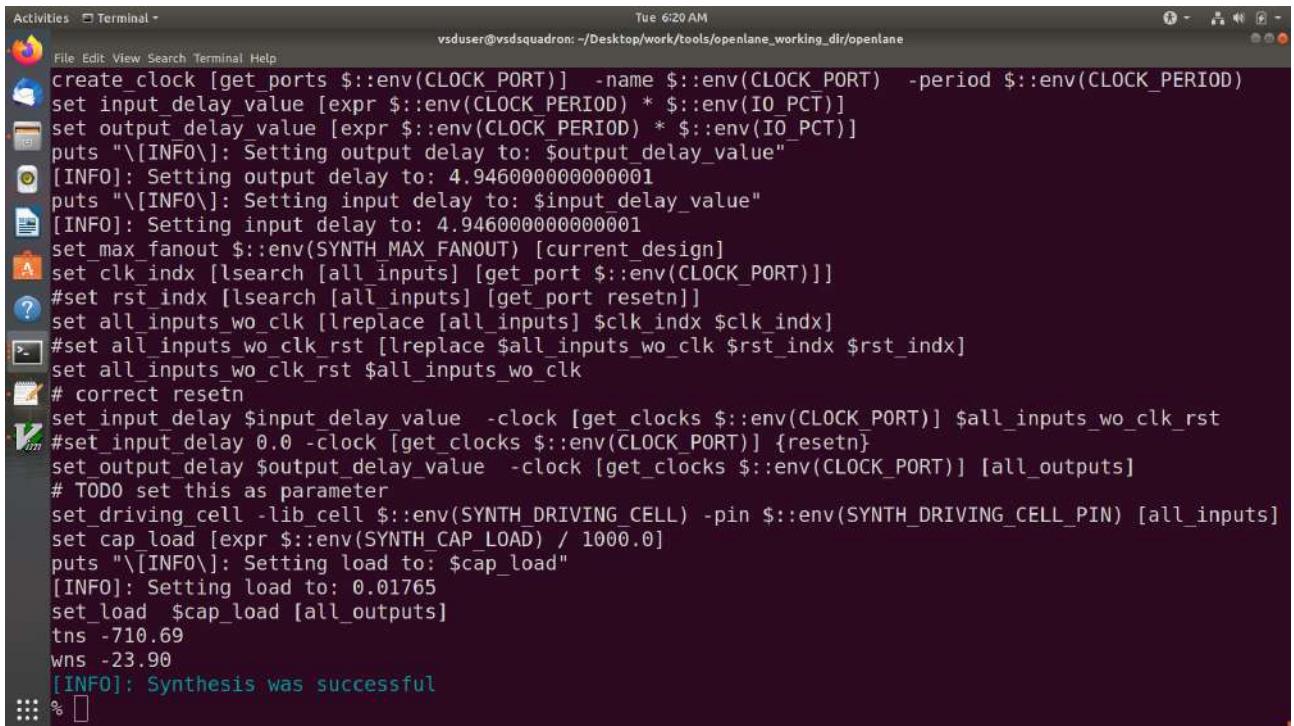
```
# Command to display current value of variable SYNTH_DRIVING_CELL to check whether  
it's the proper cell or not
```

```
echo $::env(SYNTH_DRIVING_CELL)
```

```
# Now that the design is prepped and ready, we can run synthesis using following  
command
```

run_synthesis

Commands run final screenshot



A screenshot of a terminal window titled "Terminal". The window shows a series of commands being run and their corresponding output. The commands relate to setting clock ports, input and output delays, and driving cell parameters. The output includes several "[INFO]" messages indicating the progress of the synthesis process. The terminal window has a dark background with light-colored text.

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set_all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -710.69
wns -23.90
[INFO]: Synthesis was successful
```

Commands to run STA in another terminal

```
# Change directory to openlane
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# Command to invoke OpenSTA tool with script
```

```
sta pre_sta.conf
```

Screenshots of commands run

```

Activities Terminal - Tue 6:22 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ sta pre_sta.conf
OpenSTA 2.4.0 ac3479bc24 Copyright (c) 2021, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type `show copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type `show warranty'.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib line 24, default_fanout_load is 0.0.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib line 23, default_fanout_load is 0.0.
[INFO]: Setting output delay to: 4.9460000000000001
[INFO]: Setting input delay to: 4.9460000000000001
[INFO]: Setting load to: 0.017653
Startpoint: _29347_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _29347_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _29347_/Q (sky130_fd_sc_hd_dfxtp_2)
          2   0.00          cpuregs[0][0] (net)
          0.02  0.00  0.10 ^ _17885/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _17885/_X (sky130_fd_sc_hd_buf_1)
          1   0.00          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _29347/_D (sky130_fd_sc_hd_dfxtp_2)
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data required time
          -0.23 -0.23  0.00  data arrival time
          0.24  slack (MET)

```

```

Activities Terminal - Tue 6:22 AM
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Path Type: min

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.03  0.18  0.18 ^ _29347_/Q (sky130_fd_sc_hd_dfxtp_2)
          2   0.00          cpuregs[0][0] (net)
          0.03  0.00  0.18 ^ _17885/_A (sky130_fd_sc_hd_buf_1)
          0.02  0.04  0.23 ^ _17885/_X (sky130_fd_sc_hd_buf_1)
          1   0.00          0.02  0.00  0.23 ^ _02835_ (net)
          0.02  0.00  0.23 ^ _29347/_D (sky130_fd_sc_hd_dfxtp_2)
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00  clock network delay (ideal)
          0.00  0.00  0.00  clock reconvergence pessimism
          0.00  0.00  0.00 ^ _29347_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.02 -0.02  0.00  library hold time
          -0.02 -0.02  0.00  data required time
          -0.02 -0.02  0.00  data required time
          -0.23 -0.23  0.00  data arrival time
          0.24  slack (MET)

```

Activities Terminal - Tue 6:22 AM
 vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```

Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
-----
          0.00  0.00  0.00  clock clk (rise edge)
          0.00  0.00  0.00 ^ _29052_/CLK (sky130_fd_sc_hd_dfxtp_2)
          0.06  0.58  0.58 v _29052/_Q (sky130_fd_sc_hd_dfxtp_2)
          4   0.01           irq_pending[3] (net)
          0.06  0.00  0.58 v _14460/_A (sky130_vsdinv)
          0.19  0.17  0.75 ^ _14460/_Y (sky130_vsdinv)
          3   0.01           _11622_ (net)
          0.19  0.00  0.75 ^ _14461/_B2 (sky130_fd_sc_hd_o22ai_2)
          0.09  0.14  0.89 v _14461/_Y (sky130_fd_sc_hd_o22ai_2)
          1   0.00           _11623_ (net)
          0.09  0.00  0.89 v _14462/_C1 (sky130_fd_sc_hd_a221o_2)
          0.08  0.55  1.44 v _14462/_X (sky130_fd_sc_hd_a221o_2)
          1   0.00           _11624_ (net)
          0.08  0.00  1.44 v _14481/_A (sky130_fd_sc_hd_or4_2)
          0.21  1.53  2.97 v _14481/_X (sky130_fd_sc_hd_or4_2)
          1   0.00           _11643_ (net)
          0.21  0.00  2.97 v _14509/_A1 (sky130_fd_sc_hd_o2111a_2)
          0.07  0.54  3.51 v _14509/_X (sky130_fd_sc_hd_o2111a_2)
          2   0.00
  
```

Activities Terminal - Tue 6:23 AM
 vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

```

          0.14  0.68  47.23 v _15226/_X (sky130_fd_sc_hd_or2_2)
          3   0.01           _12208_ (net)
          0.14  0.00  47.23 v _15227/_B (sky130_fd_sc_hd_or2_2)
          0.12  0.66  47.89 v _15227/_X (sky130_fd_sc_hd_or2_2)
          2   0.00           _12209_ (net)
          0.12  0.00  47.89 v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
          0.07  0.44  48.33 v _15230/_X (sky130_fd_sc_hd_o221a_2)
          1   0.00           _03928_ (net)
          0.07  0.00  48.33 v _30440/_D (sky130_fd_sc_hd_dfxtp_2)
          48.33 data arrival time
          0.00  24.73  24.73  clock clk (rise edge)
          0.00  24.73  24.73  clock network delay (ideal)
          0.00  24.73  24.73  clock reconvergence pessimism
          24.73 ^ _30440_/CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.29 24.44  24.44  library setup time
          24.44 24.44  24.44  data required time
          24.44 data required time
          -48.33 data arrival time
  ----- -23.90 slack (VIOLATED)

tns -710.69
wns -23.90
  
```

10. Make timing ECO fixes to remove all violations.

OR gate of drive strength 2 is driving 4 fanouts

Activities Terminal Tue 6:55 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

		0.19	0.00	0.75	^ _14461 /B2 (sky130_fd_sc_hd_o22ai_2)
1	0.00	0.09	0.14	0.89 v	_14461 /Y (sky130_fd_sc_hd_o22ai_2)
					11623 (net)
		0.09	0.00	0.89 v	_14462 /C1 (sky130_fd_sc_hd_a22lo_2)
1	0.00	0.08	0.55	1.44 v	_14462 /X (sky130_fd_sc_hd_a22lo_2)
					11624 (net)
		0.08	0.00	1.44 v	_14481 /A (sky130_fd_sc_hd_or4_2)
1	0.00	0.21	1.53	2.97 v	_14481 /X (sky130_fd_sc_hd_or4_2)
					11643 (net)
		0.21	0.00	2.97 v	_14509 /A1 (sky130_fd_sc_hd_o2111a_2)
2	0.00	0.07	0.54	3.51 v	_14509 /X (sky130_fd_sc_hd_o2111a_2)
					11671 (net)
		0.07	0.00	3.51 v	_14510 /C (sky130_fd_sc_hd_or3_2)
4	0.01	0.21	1.04	4.55 v	_14510 /X (sky130_fd_sc_hd_or3_2)
					11672 (net)
		0.21	0.00	4.55 v	_14513 /A (sky130_fd_sc_hd_or2_2)
2	0.00	0.11	0.71	5.26 v	_14513 /X (sky130_fd_sc_hd_or2_2)
					11674 (net)
		0.11	0.00	5.26 v	_14514 /C (sky130_fd_sc_hd_or3_2)
4	0.01	0.20	1.03	6.29 v	_14514 /X (sky130_fd_sc_hd_or3_2)
					11675 (net)
		0.20	0.00	6.29 v	_15166 /B (sky130_fd_sc_hd_or2_2)
2	0.00	0.11	0.67	6.96 v	_15166 /X (sky130_fd_sc_hd_or2_2)
					12148 (net)
		0.11	0.00	6.96 v	_15167 /C (sky130_fd_sc_hd_or3_2)
2	0.00	0.17	0.98	7.94 v	_15167 /X (sky130_fd_sc_hd_or3_2)
					12149 (net)
		0.17	0.00	7.94 v	_15168 /B (sky130_fd_sc_hd_or2_2)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

report_net -connections _11672_

Checking command syntax

help replace_cell

Replacing cell

replace_cell _14510_ sky130_fd_sc_hd_or3_4

Generating custom timing report

```
report_checks -fields {net cap slew input_pins} -digits 4
```

Result - slack reduced

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
----- [-23.90 slack (VIOLATED)]
tns -710.69
wns -23.90
% report_net -connections _11672_
Net _11672_
Driver pins
_14510 /X output (sky130_fd_sc_hd_or3_2)
Load pins
_14513 /A input (sky130_fd_sc_hd_or2_2)
_15505 /B input (sky130_fd_sc_hd_or2_2)
_18231 /A input (sky130_fd_sc_hd_buf_1)
_18326 /B input (sky130_fd_sc_hd_nand2_2)

% help replace_cell
replace_cell instance lib_cell
% replace_cell _14510_ sky130_fd_sc_hd_or3_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Fanout Cap Slew Delay Time Description
```

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Fanout Cap Slew Delay Time Description
-----[clock clk (rise edge)
          0.0000 0.0000 0.0000
          0.0000 0.0000 0.0000 ^ _29052/_CLK (sky130_fd_sc_hd_dfxtp_2)
          0.0572 0.5830 0.5830 v _29052/_Q (sky130_fd_sc_hd_dfxtp_2)
          irq_pending[3] (net)
          4 0.0067
          0.0572 0.0000 0.5830 v _14460/_A (sky130_vsdinv)
          0.1856 0.1667 0.7497 ^ _14460/_Y (sky130_vsdinv)
          11622_ (net)
          3 0.0138
          0.1856 0.0000 0.7497 ^ _14461/_B2 (sky130_fd_sc_hd_o22ai_2)
          0.0878 0.1436 0.8933 v _14461/_Y (sky130_fd_sc_hd_o22ai_2)
          11623_ (net)
          1 0.0021
          0.0878 0.0000 0.8933 v _14462/_C1 (sky130_fd_sc_hd_a221o_2)
          0.0784 0.5469 1.4402 v _14462/_X (sky130_fd_sc_hd_a221o_2)
          11624_ (net)
          1 0.0013
          0.0784 0.0000 1.4402 v _14481/_A (sky130_fd_sc_hd_or4_2)
          0.2106 1.5344 2.9746 v _14481/_X (sky130_fd_sc_hd_or4_2)
          11643_ (net)
          1 0.0024
          0.2106 0.0000 2.9746 v _14509/_A1 (sky130_fd_sc_hd_o2111a_2)
          0.0792 0.5466 3.5212 v _14509/_X (sky130_fd_sc_hd_o2111a_2)
          11671_ (net)]
```

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

Tue 9:42 AM

3	0.0138	0.1856	0.0000	0.7497	^ _11622_ (net)
		0.0878	0.1436	0.8933	v _14461/_B2 (sky130_fd_sc_hd_o22ai_2)
1	0.0021	0.0878	0.0000	0.8933	v _14461/_Y (sky130_fd_sc_hd_o22ai_2)
		0.0784	0.5469	1.4402	v _11623_ (net)
1	0.0013	0.0784	0.0000	1.4402	v _14462/_C1 (sky130_fd_sc_hd_a221o_2)
		0.2106	1.5344	2.9746	v _14462/_X (sky130_fd_sc_hd_a221o_2)
1	0.0024	0.2106	0.0000	2.9746	v _11624_ (net)
		0.0792	0.5466	3.5212	v _14481/_A (sky130_fd_sc_hd_or4_2)
2	0.0044	0.0792	0.0000	3.5212	v _14481/_X (sky130_fd_sc_hd_or4_2)
		0.1349	0.6755	4.1967	v _11643_ (net)
4	0.0089	0.1349	0.0000	4.1967	v _14509/_A1 (sky130_fd_sc_hd_o2111a_2)
		0.1121	0.6770	4.8737	v _14509/_X (sky130_fd_sc_hd_o2111a_2)
2	0.0025	0.1121	0.0000	4.8737	v _11671_ (net)
		0.1967	1.0321	5.9057	v _14514/_C (sky130_fd_sc_hd_or3_2)
4	0.0070	0.1967	0.0000	5.9057	v _14514/_X (sky130_fd_sc_hd_or3_2)
		0.1148	0.6684	6.5742	v _11675_ (net)
2	0.0032	0.1148	0.0000	6.5742	v _15166/_B (sky130_fd_sc_hd_or2_2)
		0.1692	0.9831	7.5573	v _15166/_X (sky130_fd_sc_hd_or2_2)
2	0.0025	0.0000	0.0000	7.5573	v _12148_ (net)
		0.0000	0.0000	7.5573	v _15167/_C (sky130_fd_sc_hd_or3_2)
		0.0000	0.0000	7.5573	v _15167/_X (sky130_fd_sc_hd_or3_2)
		0.0000	0.0000	7.5573	v _12149_ (net)

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

Tue 7:07 AM

2	0.0035	0.1162	0.0000	46.1648	v _12207_ (net)
		0.1421	0.6813	46.8462	v _15226/_B (sky130_fd_sc_hd_or2_2)
3	0.0079	0.1421	0.0000	46.8462	v _15226/_X (sky130_fd_sc_hd_or2_2)
		0.1228	0.6610	47.5072	v _12208_ (net)
2	0.0044	0.1228	0.0000	47.5072	v _15227/_B (sky130_fd_sc_hd_or2_2)
		0.0713	0.4381	47.9453	v _15227/_X (sky130_fd_sc_hd_or2_2)
1	0.0016	0.0713	0.0000	47.9453	v _12209_ (net)
		0.0000	24.7300	24.7300	v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
		0.0000	24.7300	24.7300	v _15230/_X (sky130_fd_sc_hd_o221a_2)
		0.0000	24.7300	24.7300	v _03928_ (net)
		0.0000	24.7300	24.7300	v _30440/_D (sky130_fd_sc_hd_dfxtip_2)
		0.0000	24.7300	24.7300	v data arrival time
		0.0000	24.7300	24.7300	v clock clk (rise edge)
		0.0000	24.7300	24.7300	v clock network delay (ideal)
		0.0000	24.7300	24.7300	v clock reconvergence pessimism
		24.7300	24.7300	24.7300	v ^ _30440/_CLK (sky130_fd_sc_hd_dfxtip_2)
		-0.2939	24.4361	24.4361	v library setup time
		-0.2939	24.4361	24.4361	v data required time
		24.4361	24.4361	24.4361	v data required time
		-47.9453	-47.9453	-47.9453	v data arrival time
		-23.5092	-23.5092	-23.5092	v slack (VIOLATED)

OR gate of drive strength 2 is driving 4 fanouts

Activities Terminal Tue 9:46 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

		0.2106	1.5344	2.9746 v	_14481/_X (sky130_fd_sc_hd_or4_2)
1	0.0024				11643 (net)
		0.2106	0.0000	2.9746 v	_14509/_A1 (sky130_fd_sc_hd_o2111a_2)
		0.0792	0.5466	3.5212 v	_14509/_X (sky130_fd_sc_hd_o2111a_2)
2	0.0044				11671 (net)
		0.0792	0.0000	3.5212 v	_14510/_C (sky130_fd_sc_hd_or3_4)
		0.1349	0.6755	4.1967 v	_14510/_X (sky130_fd_sc_hd_or3_4)
4	0.0089				11672 (net)
		0.1349	0.0000	4.1967 v	_14513/_A (sky130_fd_sc_hd_or2_2)
		0.1121	0.6770	4.8737 v	_14513/_X (sky130_fd_sc_hd_or2_2)
2	0.0025				11674 (net)
		0.1121	0.0000	4.8737 v	_14514/_C (sky130_fd_sc_hd_or3_2)
		0.1967	1.0321	5.9057 v	_14514/_X (sky130_fd_sc_hd_or3_2)
4	0.0070				11675 (net)
		0.1967	0.0000	5.9057 v	_15166/_B (sky130_fd_sc_hd_or2_2)
		0.1148	0.6684	6.5742 v	_15166/_X (sky130_fd_sc_hd_or2_2)
2	0.0032				12148 (net)
		0.1148	0.0000	6.5742 v	_15167/_C (sky130_fd_sc_hd_or3_2)
		0.1692	0.9831	7.5573 v	_15167/_X (sky130_fd_sc_hd_or3_2)
2	0.0035				12149 (net)
		0.1692	0.0000	7.5573 v	_15168/_B (sky130_fd_sc_hd_or2_2)
		0.1422	0.7026	8.2599 v	_15168/_X (sky130_fd_sc_hd_or2_2)
3	0.0079				12150 (net)
		0.1422	0.0000	8.2599 v	_15169/_B (sky130_fd_sc_hd_or2_2)
		0.1162	0.6492	8.9091 v	_15169/_X (sky130_fd_sc_hd_or2_2)
2	0.0035				12151 (net)
		0.1162	0.0000	8.9091 v	_15170/_B (sky130_fd_sc_hd_or2_2)
		0.1422	0.6817	9.5904 v	_15170/_X (sky130_fd_sc_hd_or2_2)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

report_net -connections _11675_

Replacing cell

replace_cell _14514_ sky130_fd_sc_hd_or3_4

Generating custom timing report

report_checks -fields {net cap slew input_pins} -digits 4

Result - slack reduced

```

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Tue 9:49 AM
-47.9453  data arrival time
-----
-23.5092  slack (VIOLATED)

% report_net -connections _11675_
Net _11675_
Driver pins
_14514/_X output (sky130_fd_sc_hd_or3_2)
Load pins
_14515/_A input (sky130_vsdinv)
_14521/_B2 input (sky130_fd_sc_hd_o221a_2)
_14662/_B input (sky130_fd_sc_hd_or2_2)
_15166/_B input (sky130_fd_sc_hd_or2_2)

% replace_cell _14514_ sky130_fd_sc_hd_or3_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout      Cap      Slew      Delay      Time      Description
-----      -----      -----      -----      -----      -----
          0.0000  0.0000  0.0000  clock clk (rise edge)
          0.0000  0.0000  slack network delay (ideal)

```

Tue 9:50 AM						
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane						
Fanout	Cap	Slew	Delay	Time	Description	
1	0.0013				11624_ (net)	
		0.0784	0.0000	1.4402	v 14481/_A (sky130_fd_sc_hd_or4_2)	
		0.2106	1.5344	2.9746	v 14481/_X (sky130_fd_sc_hd_or4_2)	
1	0.0024				11643_ (net)	
		0.2106	0.0000	2.9746	v 14509/_A1 (sky130_fd_sc_hd_o2111a_2)	
		0.0792	0.5466	3.5212	v 14509/_X (sky130_fd_sc_hd_o2111a_2)	
2	0.0044				11671_ (net)	
		0.0792	0.0000	3.5212	v 14510/_C (sky130_fd_sc_hd_or3_4)	
		0.1349	0.6755	4.1967	v 14510/_X (sky130_fd_sc_hd_or3_4)	
4	0.0089				11672_ (net)	
		0.1349	0.0000	4.1967	v 14513/_A (sky130_fd_sc_hd_or2_2)	
		0.1182	0.6880	4.8847	v 14513/_X (sky130_fd_sc_hd_or2_2)	
2	0.0034				11674_ (net)	
		0.1182	0.0000	4.8847	v 14514/_C (sky130_fd_sc_hd_or3_4)	
		0.1290	0.6794	5.5641	v 14514/_X (sky130_fd_sc_hd_or3_4)	
4	0.0070				11675_ (net)	
		0.1290	0.0000	5.5641	v 15166/_B (sky130_fd_sc_hd_or2_2)	
		0.1148	0.6414	6.2055	v 15166/_X (sky130_fd_sc_hd_or2_2)	
2	0.0032				12148_ (net)	
		0.1148	0.0000	6.2055	v 15167/_C (sky130_fd_sc_hd_or3_2)	
		0.1692	0.9831	7.1886	v 15167/_X (sky130_fd_sc_hd_or3_2)	
2	0.0035				12149_ (net)	
		0.1692	0.0000	7.1886	v 15168/_B (sky130_fd_sc_hd_or2_2)	
		0.1422	0.7026	7.8912	v 15168/_X (sky130_fd_sc_hd_or2_2)	
3	0.0079				12150_ (net)	
		0.1422	0.0000	7.8912	v 15169/_B (sky130_fd_sc_hd_or2_2)	
		0.1162	0.6492	8.5404	v 15169/_X (sky130_fd_sc_hd_or2_2)	
2	0.0025				12151_ (net)	

```

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
2 0.0035
    0.1162 0.0000 45.7962 v _12207_(net)
    0.1421 0.6813 46.4775 v _15226/_B(sky130_fd_sc_hd_or2_2)
    0.1421 0.0000 46.4775 v _15226/_X(sky130_fd_sc_hd_or2_2)
    0.1228 0.6610 47.1385 v _12208_(net)
    0.1228 0.0000 47.1385 v _15227/_B(sky130_fd_sc_hd_or2_2)
    0.0713 0.4381 47.5766 v _15227/_X(sky130_fd_sc_hd_o221a_2)
    0.0713 0.0000 47.5766 v _03928_(net)
    0.0713 0.0000 47.5766 v _30440/_D(sky130_fd_sc_hd_dfxtpl_2)
                                         data arrival time
                                         0.0000 24.7300 24.7300 clock clk (rise edge)
                                         0.0000 24.7300 24.7300 clock network delay (ideal)
                                         0.0000 24.7300 24.7300 clock reconvergence pessimism
                                         24.7300 ^ _30440/_CLK(sky130_fd_sc_hd_dfxtpl_2)
                                         -0.2939 24.4361 library setup time
                                         24.4361 data required time
                                         24.4361 24.4361 data arrival time
                                         -----
                                         24.4361 data required time
                                         -47.5766 data arrival time
                                         -----
                                         -23.1405 slack (VIOLATED)

```

OR gate of drive strength 2 driving OA gate has more delay

```

Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Fanout Cap Slew Delay Time Description
-----+
                                         0.0000 0.0000 0.0000 clock clk (rise edge)
                                         0.0000 0.0000 0.0000 clock network delay (ideal)
                                         0.0572 0.5830 0.5830 v _29052/_Q(sky130_fd_sc_hd_dfxtpl_2)
                                         0.0572 0.0000 ^ _29052/_CLK(sky130_fd_sc_hd_dfxtpl_2)
                                         0.1856 0.1667 0.7497 ^ _14460/_Y(sky130_vsdinv)
                                         0.1856 0.0000 0.7497 ^ _14461/_B2(sky130_fd_sc_hd_o22ai_2)
                                         0.0878 0.1436 0.8933 v _14461/_Y(sky130_fd_sc_hd_o22ai_2)
                                         0.0878 0.0000 0.8933 v _14462/_C1(sky130_fd_sc_hd_a221o_2)
                                         0.0784 0.5469 1.4402 v _14462/_X(sky130_fd_sc_hd_a221o_2)
                                         0.0784 0.0000 1.4402 v _14481/_A(sky130_fd_sc_hd_or4_2)
                                         0.2106 1.5344 2.9746 v _14481/_X(sky130_fd_sc_hd_or4_2)
                                         0.2106 0.0000 2.9746 v _11643_(net)
                                         0.0792 0.5466 3.5212 v _14509/_A1(sky130_fd_sc_hd_o2111a_2)
                                         0.0792 0.0000 3.5212 v _14509/_X(sky130_fd_sc_hd_o2111a_2)
                                         0.1349 0.6755 4.1967 v _11671_(net)
                                         0.1349 0.0000 4.1967 v _14510/_C(sky130_fd_sc_hd_or3_4)
                                         0.1182 0.6880 4.8847 v _14510/_X(sky130_fd_sc_hd_or3_4)
                                         0.1182 0.0000 4.8847 v _11672_(net)
                                         0.1349 0.0000 4.1967 v _14513/_A(sky130_fd_sc_hd_or2_2)
                                         0.1182 0.0000 4.8847 v _14513/_X(sky130_fd_sc_hd_or2_2)
                                         0.1182 0.0000 4.8847 v _11674_(net)

```

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

```
report_net -connections _11643_
```

```
# Replacing cell
```

```
replace_cell _14481_ sky130_fd_sc_hd__or4_4
```

```
# Generating custom timing report
```

```
report_checks -fields {net cap slew input_pins} -digits 4
```

Result - slack reduced

```
Activities Terminal - Tue 10:29 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
-47.5766  data arrival time
-----  
-23.1405  slack (VIOLATED)

% report net -connections _11643_
Net _11643_
Driver pins
_14481/_X output (sky130_fd_sc_hd_or4_2)
Load pins
_14509/_A1 input (sky130_fd_sc_hd_o2111a_2)

% replace_cell _14481_ sky130_fd_sc_hd_hd_or4_4
1

% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29043_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout      Cap      Slew      Delay      Time      Description
-----  
0.0000      0.0000      0.0000      0.0000  clock clk (rise edge)
0.0000      0.0000      0.0000      0.0000  clock network delay (ideal)
0.0000      0.0000      0.0000 ^ _29043/_CLK (sky130_fd_sc_hd_dfxtp_2)
0.0581      0.5838      0.5838 v _29043/_Q (sky130_fd_sc_hd_dfxtp_2)
```

```
Activities Terminal + Tue 10:29 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
2 0.0035
          0.1162  0.0000  45.7918 v _12207_(net)
          0.1421  0.6813  46.4731 v _15226/_B (sky130_fd_sc_hd_or2_2)
          0.1421  0.0000  46.4731 v _15226/_X (sky130_fd_sc_hd_or2_2)
3 0.0079
          0.1228  0.6610  47.1341 v _15227/_B (sky130_fd_sc_hd_or2_2)
          0.1228  0.0000  47.1341 v _15227/_X (sky130_fd_sc_hd_or2_2)
2 0.0044
          0.0713  0.4381  47.5723 v _15230/_B2 (sky130_fd_sc_hd_o221a_2)
          0.0713  0.0000  47.5723 v _15230/_X (sky130_fd_sc_hd_o221a_2)
          0.0016
          0.0713  0.0000  47.5723 v _30440/_D (sky130_fd_sc_hd_dfxtp_2)
          0.0713  0.0000  47.5723 data arrival time
          0.0000  24.7300  24.7300  clock clk (rise edge)
          0.0000  24.7300  24.7300  clock network delay (ideal)
          0.0000  24.7300  24.7300  clock reconvergence pessimism
          -0.2939 24.4361 ^ _30440/_CLK (sky130_fd_sc_hd_dfxtp_2)
          24.4361  library setup time
          24.4361  data required time
          24.4361  data required time
          -47.5723  data arrival time
-----
          -23.1362  slack (VIOLATED)
```

OR gate of drive strength 2 driving OA gate has more delay

Activities Terminal Tue 10:32 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

				irq_pending[12] (net)
4	0.0069	0.0581	0.0000	0.5838 v _14484 /A (sky130_vsdinv)
		0.1864	0.1676	0.7515 ^ _14484 /Y (sky130_vsdinv)
3	0.0139	0.1864	0.0000	11646_ (net)
		0.0878	0.1674	0.7515 ^ _14486 /A2 (sky130_fd_sc_hd_o22ai_2)
1	0.0021	0.0878	0.0000	0.9189 v _14486 /Y (sky130_fd_sc_hd_o22ai_2)
		0.0784	0.5469	11648_ (net)
1	0.0013	0.0784	0.0000	1.4658 v _14487 /C1 (sky130_fd_sc_hd_a22lo_2)
		0.2092	1.5317	1.4658 v _14487 /X (sky130_fd_sc_hd_a22lo_2)
1	0.0023	0.2092	0.0000	11649_ (net)
		0.0792	0.5193	2.9975 v _14506 /A (sky130_fd_sc_hd_or4_2)
2	0.0044	0.0792	0.0000	3.5168 v _14506 /X (sky130_fd_sc_hd_or4_2)
		0.1349	0.6755	11668_ (net)
4	0.0089	0.1349	0.0000	3.5168 v _14509 /A2 (sky130_fd_sc_hd_o2111a_2)
		0.1182	0.6880	4.1923 v _14509 /X (sky130_fd_sc_hd_o2111a_2)
2	0.0034	0.1182	0.0000	11671_ (net)
		0.1290	0.6794	4.8803 v _14510 /C (sky130_fd_sc_hd_or3_4)
4	0.0070	0.1290	0.0000	5.5597 v _14510 /X (sky130_fd_sc_hd_or3_4)
		0.1148	0.6414	11672_ (net)
2	0.0022	0.1148	0.0000	4.8803 v _14513 /A (sky130_fd_sc_hd_or2_2)
		0.1290	0.6794	5.5597 v _14513 /X (sky130_fd_sc_hd_or2_2)
4	0.0070	0.1290	0.0000	11674_ (net)
		0.1148	0.6414	6.2011 v _15166 /B (sky130_fd_sc_hd_or2_2)
2	0.0022	0.1148	0.0000	11675_ (net)
		0.1290	0.6794	5.5597 v _15166 /X (sky130_fd_sc_hd_or2_2)
4	0.0070	0.1290	0.0000	11676_ (net)
		0.1148	0.6414	6.2011 v _15166 /B (sky130_fd_sc_hd_or2_2)
2	0.0022	0.1148	0.0000	11677_ (net)

Commands to perform analysis and optimize timing by replacing with OR gate of drive strength 4

Reports all the connections to a net

report_net -connections _11668_

Replacing cell

replace_cell _14506_ sky130_fd_sc_hd_or4_4

Generating custom timing report

report_checks -fields {net cap slew input_pins} -digits 4

Result - slack reduced

```

Activities Terminal - Tue 10:36 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
-47.5723  data arrival time
-----  

-23.1362  slack (VIOLATED)

% report_net -connections _11668_
Net _11668
Driver pins
_14506 /X output (sky130_fd_sc_hd_or4_2)
Load pins
_14509 /A2 input (sky130_fd_sc_hd_o2111a_2)

% replace_cell _14506_ sky130_fd_sc_hd_or4_4
1
% report_checks -fields {net cap slew input_pins} -digits 4
Startpoint: _29052_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Fanout      Cap      Slew      Delay      Time      Description
-----  

          0.0000  0.0000  0.0000  clock clk (rise edge)
          0.0000  0.0000  0.0000  clock network delay (ideal)
          0.0000  0.0000  0.0000 ^ _29052 /CLK (sky130_fd_sc_hd_dfxtp_2)
          0.0572  0.5830  0.5830 v _29052 /Q (sky130_fd_sc_hd_dfxtp_2)
           0.0067  


```

```

Activities Terminal - Tue 10:37 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
2  0.0035
          0.1162  0.0000  45.2729 v _12207_(net)
          0.1421  0.6813  45.9542 v _15226 /B (sky130_fd_sc_hd_or2_2)
          0.1421  0.0000  45.9542 v _15226 /X (sky130_fd_sc_hd_or2_2)
          0.1228  0.6610  46.6153 v _12208_(net)
          0.1228  0.0000  46.6153 v _15227 /B (sky130_fd_sc_hd_or2_2)
          0.1228  0.0000  46.6153 v _15227 /X (sky130_fd_sc_hd_or2_2)
          0.0713  0.4381  47.0534 v _12209_(net)
          0.0713  0.0000  47.0534 v _15230 /B2 (sky130_fd_sc_hd_o221a_2)
          0.0713  0.0000  47.0534 v _15230 /X (sky130_fd_sc_hd_o221a_2)
          0.0713  0.0000  47.0534 v _03928_(net)
          0.0713  0.0000  47.0534 v _30440 /D (sky130_fd_sc_hd_dfxtp_2)
          0.0713  0.0000  47.0534 v data arrival time
          0.0000  24.7300  24.7300  clock clk (rise edge)
          0.0000  24.7300  24.7300  clock network delay (ideal)
          0.0000  24.7300  24.7300  clock reconvergence pessimism
          0.0000  24.7300  24.7300 ^ _30440 /CLK (sky130_fd_sc_hd_dfxtp_2)
          -0.2939  24.4361  library setup time
          24.4361  data required time
          24.4361  data arrival time
-----  

-22.6173  slack (VIOLATED)

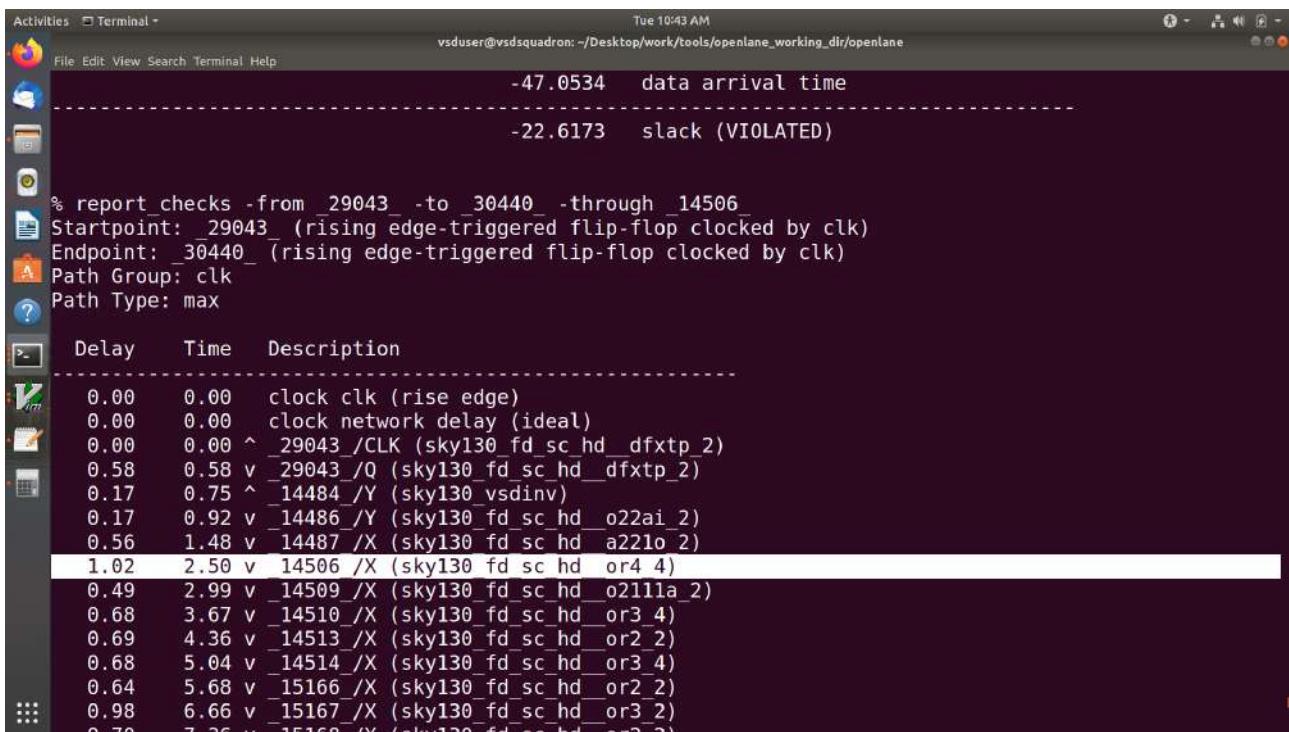
```

Commands to verify instance _14506_ is replaced with sky130_fd_sc_hd_or4_4

Generating custom timing report

report_checks -from _29043_ -to _30440_ -through _14506_

Screenshot of replaced instance



The screenshot shows a terminal window with the following output:

```
Tue 10:43 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
-47.0534  data arrival time
-----
-22.6173  slack (VIOLATED)

% report_checks -from 29043 -to 30440 -through 14506
Startpoint: 29043 (rising edge-triggered flip-flop clocked by clk)
Endpoint: 30440 (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Delay    Time   Description
-----
0.00    0.00   clock clk (rise edge)
0.00    0.00   clock network delay (ideal)
0.00    0.00   ^ 29043 /CLK (sky130_fd_sc_hd_dfxtpl_2)
0.58    0.58   v 29043 /Q (sky130_fd_sc_hd_dfxtpl_2)
0.17    0.75   ^ 14484 /Y (sky130_vsdinv)
0.17    0.92   v 14486 /Y (sky130_fd_sc_hd_o22ai_2)
0.56    1.48   v 14487 /X (sky130_fd_sc_hd_a22lo_2)
1.02    2.50   v 14506 /X (sky130_fd_sc_hd_or4_4)
0.49    2.99   v 14509 /X (sky130_fd_sc_hd_o2111a_2)
0.68    3.67   v 14510 /X (sky130_fd_sc_hd_or3_4)
0.69    4.36   v 14513 /X (sky130_fd_sc_hd_or2_2)
0.68    5.04   v 14514 /X (sky130_fd_sc_hd_or3_4)
0.64    5.68   v 15166 /X (sky130_fd_sc_hd_or2_2)
0.98    6.66   v 15167 /X (sky130_fd_sc_hd_or3_2)
0.70    7.26   v 15168 /X (sky130_fd_sc_hd_or2_2)
```

We started ECO fixes at wns -23.9000 and now we stand at wns -22.6173 we reduced around 1.2827 ns of violation

11. Replace the old netlist with the new netlist generated after timing ECO fix and implement the floorplan, placement and cts.

Now to insert this updated netlist to PnR flow and we can use write_verilog and overwrite the synthesis netlist but before that we are going to make a copy of the old old netlist

Commands to make copy of netlist

```
# Change from home directory to synthesis results directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
25-03_18-52/results/synthesis/
```

```
# List contents of the directory
```

```
ls
```

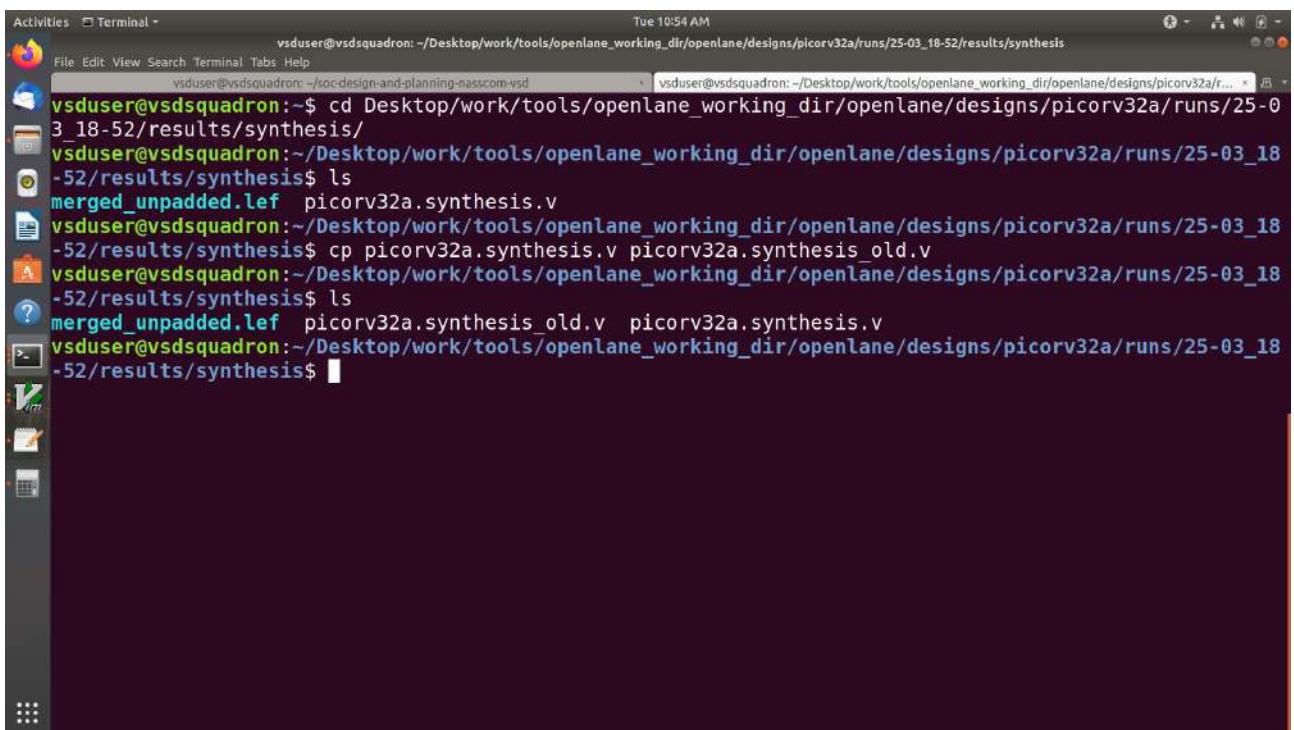
```
# Copy and rename the netlist
```

```
cp picorv32a.synthesis.v picorv32a.synthesis_old.v
```

```
# List contents of the directory
```

```
ls
```

Screenshot of commands run



The screenshot shows a terminal window titled "Terminal" running on a Linux desktop environment. The window title bar includes the text "Activities Terminal" and the date "Tue 10:54 AM". The terminal itself has two tabs open. The current tab displays a command-line session:

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$ ls
merged_unpadded.lef picorv32a.synthesis.v
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$ cp picorv32a.synthesis.v picorv32a.synthesis_old.v
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$ ls
merged_unpadded.lef picorv32a.synthesis_old.v picorv32a.synthesis.v
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis$
```

Commands to write verilog

```
# Check syntax
```

```
help write_verilog
```

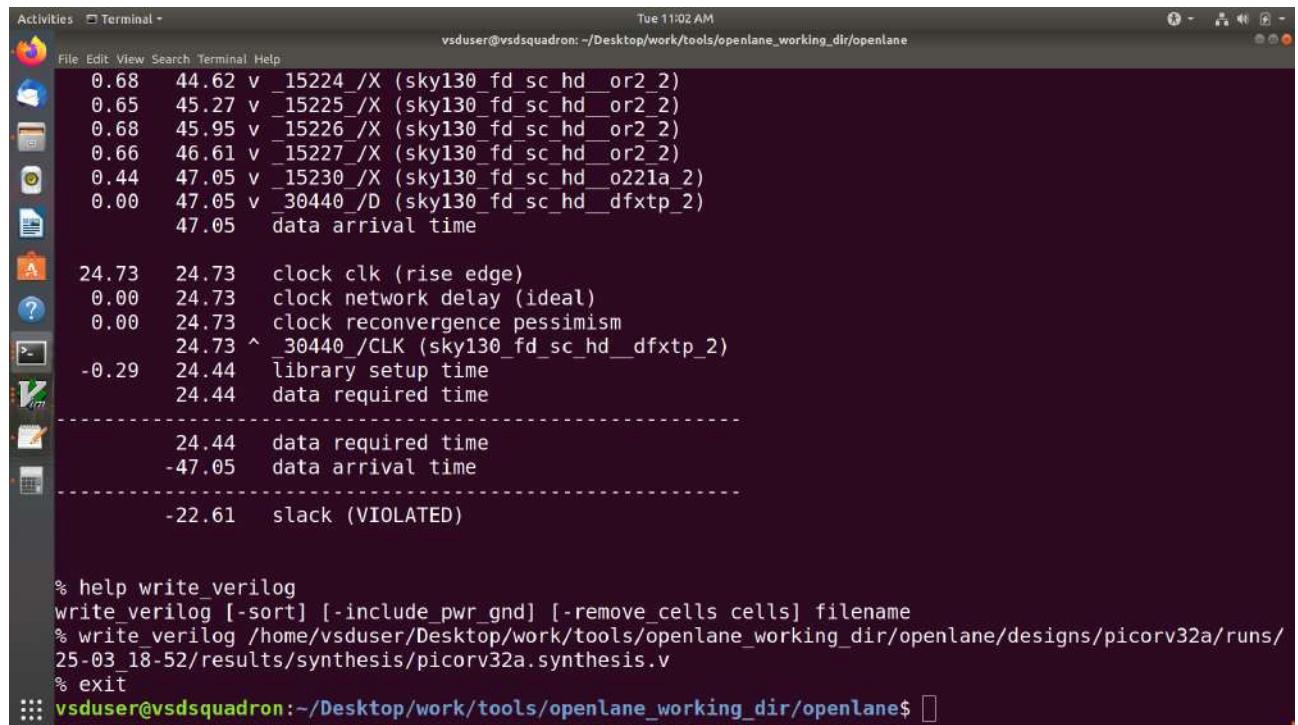
```
# Overwriting current synthesis netlist
```

```
write_verilog /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis/picorv32a.synthesis.v
```

```
# Exit from OpenSTA since timing analysis is done
```

```
exit
```

Screenshot of commands run



The screenshot shows a terminal window with the following content:

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
Tue 11:02 AM
File Edit View Search Terminal Help
0.68 44.62 v _15224_X (sky130_fd_sc_hd_or2_2)
0.65 45.27 v _15225_X (sky130_fd_sc_hd_or2_2)
0.68 45.95 v _15226_X (sky130_fd_sc_hd_or2_2)
0.66 46.61 v _15227_X (sky130_fd_sc_hd_or2_2)
0.44 47.05 v _15230_X (sky130_fd_sc_hd_o221a_2)
0.00 47.05 v _30440_D (sky130_fd_sc_hd_dfxtp_2)
47.05 data arrival time

24.73 24.73 clock clk (rise edge)
0.00 24.73 clock network delay (ideal)
0.00 24.73 clock reconvergence pessimism
24.73 ^ _30440_CLK (sky130_fd_sc_hd_dfxtp_2)
-0.29 24.44 library setup time
24.44 data required time
-----
24.44 data required time
-47.05 data arrival time
-----
-22.61 slack (VIOLATED)

% help write_verilog
write_verilog [-sort] [-include_pwr_gnd] [-remove_cells cells] filename
% write_verilog /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/25-03_18-52/results/synthesis/picorv32a.synthesis.v
% exit
::: vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$
```

Verified that the netlist is overwritten by checking that instance `_14506_` is replaced with `sky130_fd_sc_hd_or4_4`

```

Activities  M. GVim -
Tue 11:01 AM
picorv32a.synthesis.v (~-/Desktop/work/too...ns/25-03_18-52/results/synthesis) - GVIM2
File Edit Tools Syntax Buffers Window Help
16359     .Y(_11665_));
16360   sky130_fd_sc_hd_o22ai_2 _14504_ (.A1(\irq_mask[21]),
16361     .A2(_11664),
16362     .B1(\irq_mask[23]),
16363     .B2(_11665),
16364     .Y(_11666));
16365   sky130_fd_sc_hd_a221o_2 _14505_ (.A1(_11662),
16366     .A2(\irq_pending[20]),
16367     .B1(_11663),
16368     .B2(\irq_pending[22]),
16369     .C1(_11666),
16370     .X(_11667));
16371   sky130_fd_sc_hd_or4_4 _14506_ (.A(_11649),
16372     .B(_11655),
16373     .C(_11661),
16374     .D(_11667),
16375     .X(_11668));
16376   sky130_vsdinv _14507_ (.A(irq_active),
16377     .Y(_11669));
16378   sky130_vsdinv _14508_ (.A(irq_delay),
16379     .Y(_11670));
16380   sky130_fd_sc_hd_o2111a_2 _14509_ (.A1(_11643),
16381     .A2(_11668),
16382     .B1(_11669),
16383     .C1(_11670),
hlsearch
16371,25      21%

```

Since we confirmed that netlist is replaced and will be loaded in PnR but since we want to follow up on the earlier o violation design we are continuing with the clean design to further stages

Commands load the design and run necessary stages

```
# Now once again we have to prep design so as to update variables
```

```
prep -design picorv32a -tag 24-03_10-03 -overwrite
```

```
# Additional commands to include newly added lef to openlane flow merged.lef
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_STRATEGY
```

```
set ::env(SYNTH_STRATEGY) "DELAY 3"

# Command to set new value for SYNTH_SIZING

set ::env(SYNTH_SIZING) 1

# Now that the design is prepped and ready, we can run synthesis using following
# command

run_synthesis

# Following commands are altogether sourced in "run_floorplan" command

init_floorplan

place_io

tap_decap_or

# Now we are ready to run placement

run_placement

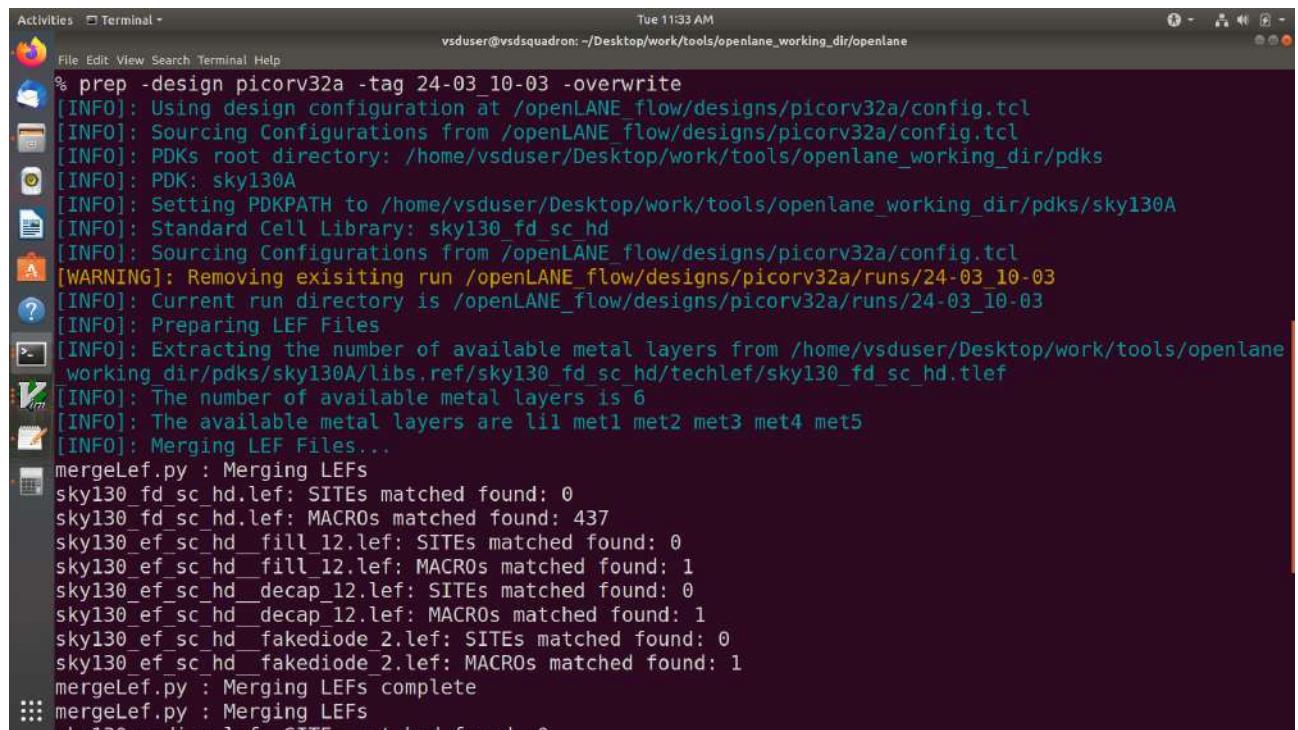
# Incase getting error

unset ::env(LIB_CTS)
```

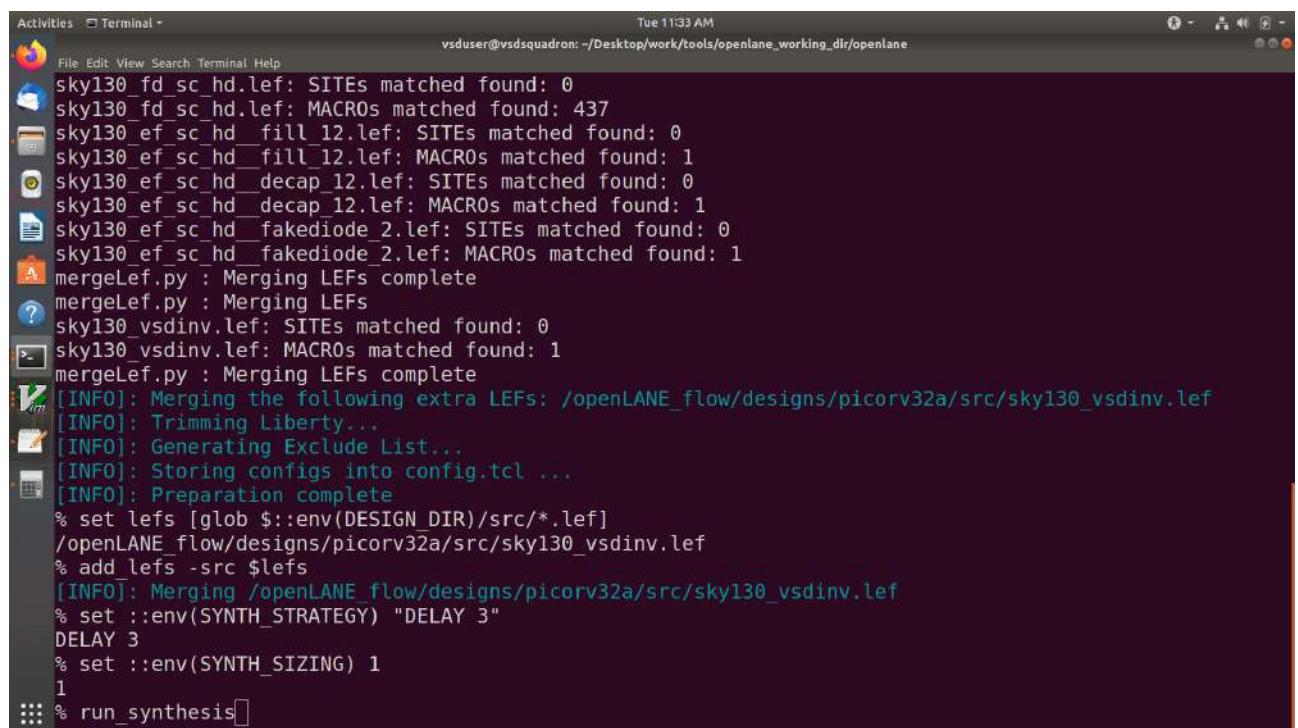
```
# With placement done we are now ready to run CTS
```

```
run_cts
```

Screenshots of commands run



```
Activities Terminal Tue 11:33 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% prep -design picorv32a -tag 24-03_10-03 -overwrite
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130 fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[WARNING]: Removing existing run /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/24-03_10-03
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.tlef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are l1l met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
::: mergeLef.py : Merging LEFs
    120 SITEs and 15 MACROs
```



```
Activities Terminal Tue 11:33 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
sky130_fd_sc_hd.lef: SITEs matched found: 0
sky130_fd_sc_hd.lef: MACROs matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITEs matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% set ::env(SYNTH_STRATEGY) "DELAY 3"
DELAY 3
% set ::env(SYNTH_SIZING) 1
1
::: % run_synthesis
```

```
Activities Terminal - Tue 11:35 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
::: % init_floorplan
```

```
Activities Terminal - Tue 11:36 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
% init_floorplan
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 8
OpenROAD 0.9.0 1415572a73
A This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
[INFO IFP-0001] Added 264 rows of 1566 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 731.615 742.335 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/8-verilog2def.die_area.rpt.
[INFO] Floorplanned on a core area of 5.52 10.88 725.88 728.96 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/reports/floorplan/8-verilog2def.core_area.rpt.
[INFO]: Core area width: 720.36
[INFO]: Core area height: 718.08
[INFO]: Changing layout from 0 to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def
::: % place_io
```

```
Activities Terminal - Tue 11:37 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% place_io
[INFO]: Running IO Placement...
[INFO]: current step index: 9
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def
#Macro blocks found: 0
Using 5u default boundaries offset
Random pin placement
RandomMode Even
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/8-verilog2def_openroad.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def
::: % tap_decap_or
```

```
Activities Terminal - Tue 11:38 AM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% place_io
[INFO]: Running IO Placement...
[INFO]: current step index: 9
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17139 components and 124080 component-terminals.
Notice 0: Created 17241 nets and 58350 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def
Step 1: Cut rows...
[INFO TAP-0001] Macro blocks found: 0
[INFO TAP-0002] #Original rows: 264
[INFO TAP-0003] #Cut rows: 0
Step 2: Insert endcaps...
[INFO TAP-0004] #Endcaps inserted: 528
Step 3: Insert tapcells...
[INFO TAP-0005] #Tapcells inserted: 7180
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/floorplan/9-ioPlacer.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/floorplan/picorv32a.floorplan.def
::: % run_placement
```

```
Activities Terminal - Tue 11:39 AM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
legalized HPWL      910806.5 u
delta HPWL          2 %

[INFO DPL-0020] Mirrored 6650 instances
[INFO DPL-0021] HPWL before      910806.5 u
[INFO DPL-0022] HPWL after       895297.0 u
[INFO DPL-0023] HPWL delta      -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/placement/11-resize.r.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 15
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
% run_cts
```

```
Activities Terminal - Tue 12:00 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 25690 components and 145610 component-terminals.
Notice 0:     Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
[INFO]: Changing netlist from /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis_optimized.v to /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis_cts.v
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 19
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def.png'
Done
[INFO]: Screenshot taken.
% 
```

12. Post-CTS OpenROAD timing analysis.

Commands to be run in OpenLANE flow to do OpenROAD timing analysis with integrated OpenSTA in OpenROAD

```
# Command to run OpenROAD tool
```

```
openroad
```

```
# Reading lef file
```

```
read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
```

```
# Reading def file
```

```
read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
```

```
# Creating an OpenROAD database to work with
```

```
write_db pico_cts.db
```

```
# Loading the created database in OpenROAD
```

```
read_db pico_cts.db
```

```
# Read netlist post CTS
```

```
read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/  
picorv32a.synthesis_cts.v
```

```
# Read library for design
```

```
read_liberty $::env(LIB_SYNTH_COMPLETE)
```

```
# Link design and library

link_design picorv32a

# Read in the custom sdc we created

read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc

# Setting all cloks as propagated clocks

set_propagated_clock [all_clocks]

# Check syntax of 'report_checks' command

help report_checks

# Generating custom timing report

report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format
full_clock_expanded -digits 4

# Exit to OpenLANE flow

exit
```

Screenshots of commands run and timing report generated

```
Activities Terminal - Tue 12:55 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% openroad
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
% read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
% read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 25690 components and 145610 component-terminals.
Notice 0:     Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
% write_db pico_cts.db
% read_db pico_cts.db
% read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis
_cts.v
% read_liberty $::env(LIB_SYNTH_COMPLETE)
1
% link_design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_tapvpwrvgnd_1 has no liberty cell.
```

```

Activities Terminal - Tue 12:58 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
11 0.0206
    0.0650  0.0000  1.6203 ^ _30955/_CLK (sky130_fd_sc_hd_dfxtp_2)
    0.0000  1.6203  clock reconvergence pessimism
   -0.0263  1.5941  library hold time
    1.5941  data required time
-----
    1.5941  data required time
   -1.8059  data arrival time
-----
    0.2119  slack (MET)

Startpoint: resetn (input port clocked by clk)
Endpoint: mem_la_read (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
----- 0.0000 0.0000 0.0000 0.0000 clock clk (rise edge)
          0.0000 0.0000 4.9460 4.9460 ^ input external delay
          0.0172 0.0055 4.9515 ^ resetn (in)
          0.0042 0.0172 0.0000 4.9515 ^ input101/A (sky130_fd_sc_hd_clkbuf_8)
          0.0582 0.1265 5.0780 ^ input101/X (sky130_fd_sc_hd_clkbuf_8)
          0.0234 0.0582 0.0000 5.0780 ^ net101 (net)

```

```

Activities Terminal - Tue 11:09 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
6 0.0270
    0.0947  0.0000  5.2526 ^ 12638_(net)
    0.1284  0.1277  5.3802 v 17093/_C (sky130_fd_sc_hd_nand3_4)
          0.1284  0.0000  5.3802 v 17093/_Y (sky130_fd_sc_hd_nand3_4)
          0.0799  0.1239  5.5041 ^ 13857_(net)
          0.0023 0.0799 0.0000 5.5041 ^ 18867/_B1 (sky130_fd_sc_hd_a21oi_4)
          0.0799  0.0000 5.5041 ^ 18867/_Y (sky130_fd_sc_hd_a21oi_4)
          0.0177 0.1052 0.1596 5.6637 ^ net199_(net)
          0.1052 0.0000 5.6637 ^ output199/A (sky130_fd_sc_hd_clkbuf_2)
          0.1052 0.0000 5.6637 ^ output199/X (sky130_fd_sc_hd_clkbuf_2)
          0.0000 0.0000 24.7300 24.7300 clock clk (rise edge)
          0.0000 0.0000 24.7300 24.7300 clock network delay (propagated)
          0.0000 0.0000 24.7300 24.7300 clock reconvergence pessimism
         -4.9460 19.7840 19.7840 output external delay
         19.7840 19.7840 data required time
         -5.6637 14.1203 14.1203 data arrival time
-----
         19.7840 14.1203 slack (MET)

% exit
%
```

**13. Explore post-CTS OpenROAD timing analysis by removing
'sky130_fd_sc_hd_clkbuf_1' cell from clock buffer list variable
'CTS_CLK_BUFFER_LIST'.**

**Commands to be run in OpenLANE flow to do OpenROAD timing analysis after
changing CTS_CLK_BUFFER_LIST**

```
# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)

# Removing 'sky130_fd_sc_hd_clkbuf_1' from the list

set ::env(CTS_CLK_BUFFER_LIST) [lreplace $::env(CTS_CLK_BUFFER_LIST) 0 0]

# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)

# Checking current value of 'CURRENT_DEF'

echo $::env(CURRENT_DEF)

# Setting def as placement def

set ::env(CURRENT_DEF) /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/
placement/picorv32a.placement.def

# Run CTS again

run_cts

# Checking current value of 'CTS_CLK_BUFFER_LIST'
```

```
echo $::env(CTS_CLK_BUFFER_LIST)

# Command to run OpenROAD tool

openroad

# Reading lef file

read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef

# Reading def file

read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def

# Creating an OpenROAD database to work with

write_db pico_cts1.db

# Loading the created database in OpenROAD

read_db pico_cts.db

# Read netlist post CTS

read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/
picorv32a.synthesis_cts.v
```

```
# Read library for design

read_liberty $::env(LIB_SYNTH_COMPLETE)

# Link design and library

link_design picorv32a

# Read in the custom sdc we created

read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc

# Setting all cloks as propagated clocks

set_propagated_clock [all_clocks]

# Generating custom timing report

report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format
full_clock_expanded -digits 4

# Report hold skew

report_clock_skew -hold
```

```

# Report setup skew

report_clock_skew -setup

# Exit to OpenLANE flow

exit

# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)

# Inserting 'sky130_fd_sc_hd__clkbuf_1' to first index of list

set ::env(CTS_CLK_BUFFER_LIST) [linsert $::env(CTS_CLK_BUFFER_LIST) 0
sky130_fd_sc_hd__clkbuf_1]

# Checking current value of 'CTS_CLK_BUFFER_LIST'

echo $::env(CTS_CLK_BUFFER_LIST)

```

Screenshots of commands run and timing report generated

```
Activities Terminal - Tue 1:42 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_
8
% set ::env(CTS_CLK_BUFFER_LIST) [lreplace $::env(CTS_CLK_BUFFER_LIST) 0 0]
sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
% set ::env(CURRENT_DEF) /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
% run_cts
[INFO]: Running TritonCTS...
[INFO]: current step index: 20
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/placement/picorv32a.placement.def
[INFO]: Done
```

```
Activities Terminal - Tue 1:45 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def.png'
Done
[INFO]: Screenshot taken.
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% openroad
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
% read_lef /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/tmp/merged.lef
% read_def /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 25690 components and 145610 component-terminals.
Notice 0: Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/cts/picorv32a.cts.def
% write_db pico_cts1.db
% read_db pico_cts.db
```

```

Activities Terminal - Tue 1:48 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% write_db pico_cts1.db
% read_db pico_cts.db
% read_verilog /openLANE_flow/designs/picorv32a/runs/24-03_10-03/results/synthesis/picorv32a.synthesis
_cts.v
% read_liberty $::env(LIB_SYNTH_COMPLETE)
1
% link_design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_tapvpwrvgnd_1 has no liberty cell.
% read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
[INFO]: Setting output delay to: 4.946000000000001
[INFO]: Setting input delay to: 4.946000000000001
[INFO]: Setting load to: 0.017653
% set_propagated_clock [all_clocks]
% report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
Startpoint: _30990_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30955_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----  

1 0.0079 0.0225 0.0000 0.0100 ^ clkbuf_0_clk/A (sky130_fd_sc_hd_clkbuf_16)  

0.0225 0.0000 0.0100 ^ clkbuf_0_clk/X (sky130_fd_sc_hd_clkbuf_16)
0.0225 0.0000 0.0100 ^ clkbuf_0_clk/Y (sky130_fd_sc_hd_clkbuf_16)

```

```

Activities Terminal - Tue 1:48 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
0.0520 0.0000 1.2459 ^ _30955/_CLK (sky130_fd_sc_hd_dfxtpl_2)
0.0000 1.2459 clock reconvergence pessimism
-0.0280 1.2179 library hold time
1.2179 data required time
-----  

1.2179 data required time
-1.5305 data arrival time
-----  

0.3125 slack (MET)

Startpoint: resetn (input port clocked by clk)
Endpoint: mem_la_read (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout Cap Slew Delay Time Description
-----  

1 0.0042 0.0172 0.0000 4.9460 0.0000 ^ clock clk (rise edge)
0.0000 0.0000 ^ clock network delay (propagated)
4.9460 4.9460 ^ input external delay
0.0172 0.0055 4.9515 ^ resetn (in)
resetn (net)
7 0.0234 0.0172 0.0000 4.9515 ^ input101/A (sky130_fd_sc_hd_clkbuf_8)
0.0582 0.1265 5.0780 ^ input101/X (sky130_fd_sc_hd_clkbuf_8)
0.0582 0.0000 5.0780 ^ net101 (net)
0.0582 0.0000 5.0780 ^ 15304/A (sky130_fd_sc_hd_clkbuf_4)
0.0042 0.1746 5.2526 ^ 15304/X (sky130_fd_sc_hd_clkbuf_4)

```

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      Tue 1:50 PM
          -4.9460  19.7840  output external delay
          19.7840  data required time
          19.7840  data required time
          -5.6637  data arrival time
          14.1203  slack (MET)

% report_clock_skew -hold
Clock clk
Latency CRPR Skew
_31226 /CLK ^
    1.36
_32416 /CLK ^
    0.94    0.00    0.42

% report_clock_skew -setup
Clock clk
Latency CRPR Skew
_31226 /CLK ^
    1.36
_32416 /CLK ^
    0.94    0.00    0.42

% exit
%
```

```
Activities Terminal - vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      Tue 1:53 PM
          % echo $::env(CTS_CLK_BUFFER_LIST)
          sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
          % set ::env(CTS_CLK_BUFFER_LIST) [linsert $::env(CTS_CLK_BUFFER_LIST) 0 sky130_fd_sc_hd_clkbuf_1]
          sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_
          8
          % echo $::env(CTS_CLK_BUFFER_LIST)
          sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_
          8
%
```

Section 5 - Final steps for RTL2GDS using tritonRoute and openSTA (25/03/2024 - 26/03/2024)

Theory

Implementation

- **Section 5 tasks:-**
25. Perform generation of Power Distribution Network (PDN) and explore the PDN layout.
 26. Perform detailed routing using TritonRoute.
 27. Post-Route parasitic extraction using SPEF extractor.
 28. Post-Route OpenSTA timing analysis with the extracted parasitics of the route.
- All section 5 logs, reports and results can be found in following run folder:

Section 5 Run - 26-03_08-45

1. Perform generation of Power Distribution Network (PDN) and explore the PDN layout.

Commands to perform all necessary stages up until now

```
# Change directory to openlane flow directory
```

```
cd Desktop/work/tools/openlane_working_dir/openlane
```

```
# alias docker='docker run -it -v $(pwd):/openLANE_flow -v $PDK_ROOT:$PDK_ROOT -e PDK_ROOT=$PDK_ROOT -u $(id -u $USER):$(id -g $USER) efabless/openlane:vo.21'
```

```
# Since we have aliased the long command to 'docker' we can invoke the OpenLANE flow docker sub-system by just running this command
```

```
docker
```

```
# Now that we have entered the OpenLANE flow contained docker sub-system we can  
invoke the OpenLANE flow in the Interactive mode using the following command
```

```
./flow.tcl -interactive
```

```
# Now that OpenLANE flow is open we have to input the required packages for proper  
functionality of the OpenLANE flow
```

```
package require openlane 0.9
```

```
# Now the OpenLANE flow is ready to run any design and initially we have to prep the  
design creating some necessary files and directories for running a specific design which in  
our case is 'picorv32a'
```

```
prep -design picorv32a
```

```
# Additional commands to include newly added lef to openlane flow merged.lef
```

```
set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
```

```
add_lefs -src $lefs
```

```
# Command to set new value for SYNTH_STRATEGY
```

```
set ::env(SYNTH_STRATEGY) "DELAY 3"
```

```
# Command to set new value for SYNTH_SIZING
```

```
set ::env(SYNTH_SIZING) 1
```

Now that the design is prepped and ready, we can run synthesis using following command

```
run_synthesis
```

Following commands are altogether sourced in "run_floorplan" command

```
init_floorplan
```

```
place_io
```

```
tap_decap_or
```

Now we are ready to run placement

```
run_placement
```

```
# Incase getting error
```

```
unset ::env(LIB_CTS)
```

With placement done we are now ready to run CTS

```
run_cts
```

Now that CTS is done we can do power distribution network

gen_pdn

Screenshots of power distribution network run

```
Activities Terminal Tue 2:22 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: Screenshot taken.
% gen pdn
[INFO]: Generating PDN...
[INFO]: current step index: 14
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 25690 components and 145610 component-terminals.
Notice 0:     Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/cts/picorv32a.cts.def
[INFO] [PDNG-0016] Power Delivery Network Generator: Generating PDN
[INFO] [PDNG-0016] config: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdkss/sky130A/libs.tech/openlane/common_pdn.tcl
[INFO] [PDNG-0008] Design Name is picorv32a
[INFO] [PDNG-0009] Reading technology data
[INFO] [PDNG-0011] ***** INFO *****
Tunne: stdcell -mid
```

```
Activities Terminal Tue 2:22 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[WARNING PSM-0030] Vsrc location at (705.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 563.420um).
[WARNING PSM-0030] Vsrc location at (425.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 563.420um).
[WARNING PSM-0030] Vsrc location at (705.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 563.420um).
[WARNING PSM-0030] Vsrc location at (565.520um, 710.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 716.600um).
[WARNING PSM-0030] Vsrc location at (705.520um, 710.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 716.600um).
[INFO PSM-0031] Number of nodes on net VGND = 24383.
[INFO PSM-0037] G matrix created successfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/cts/picorv32a.cts.def to /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
% 
```

Commands to load PDN def in magic in another terminal

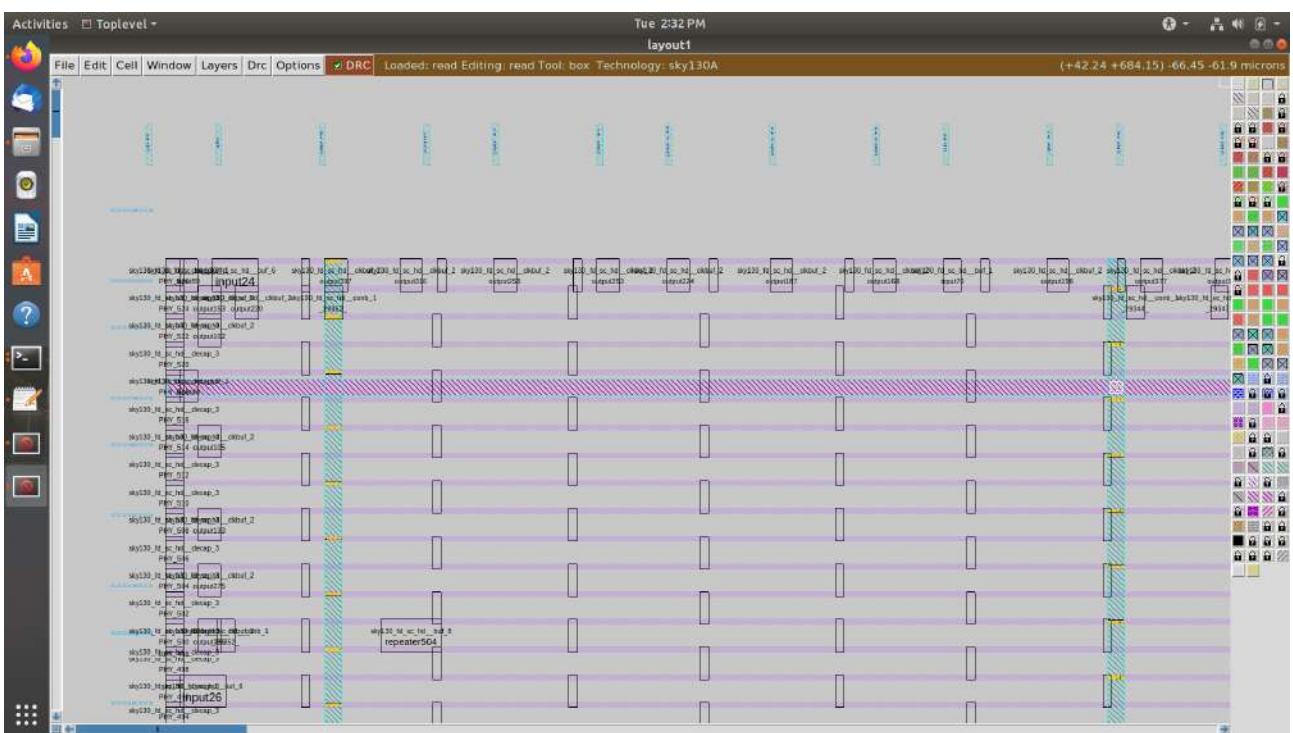
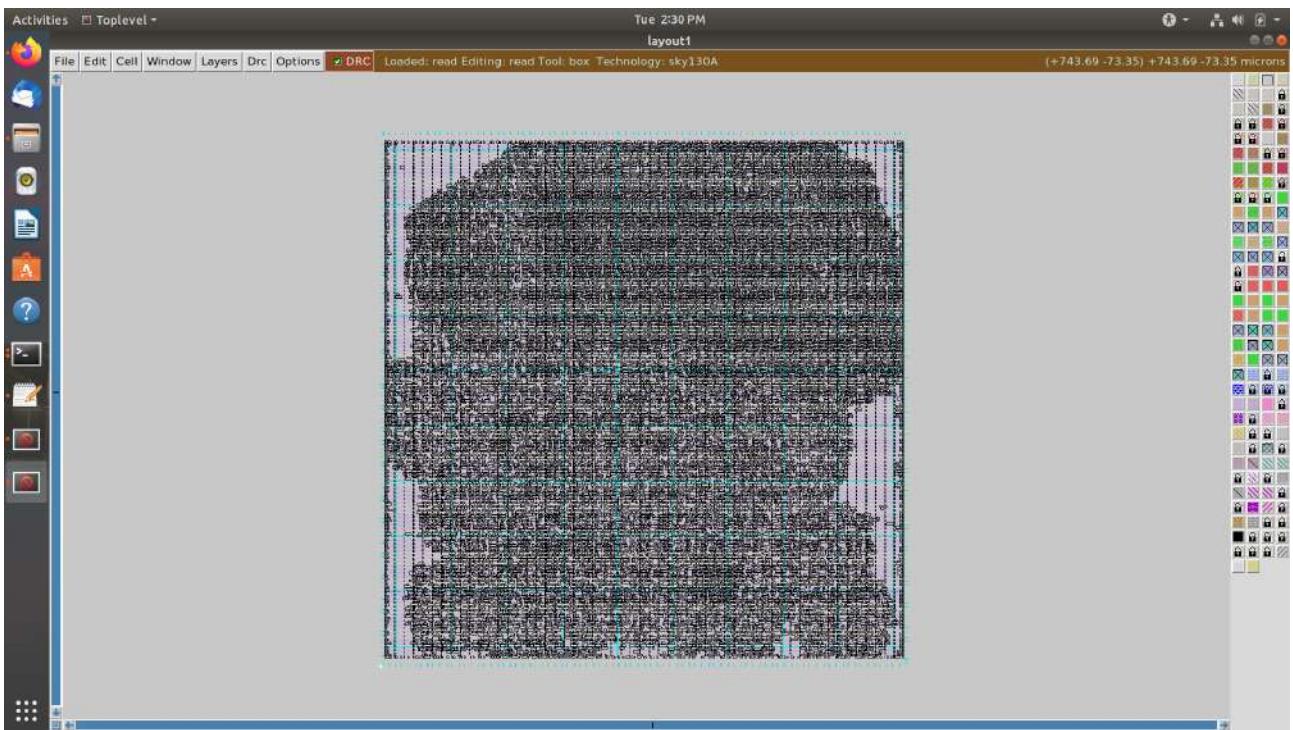
```
# Change directory to path containing generated PDN def
```

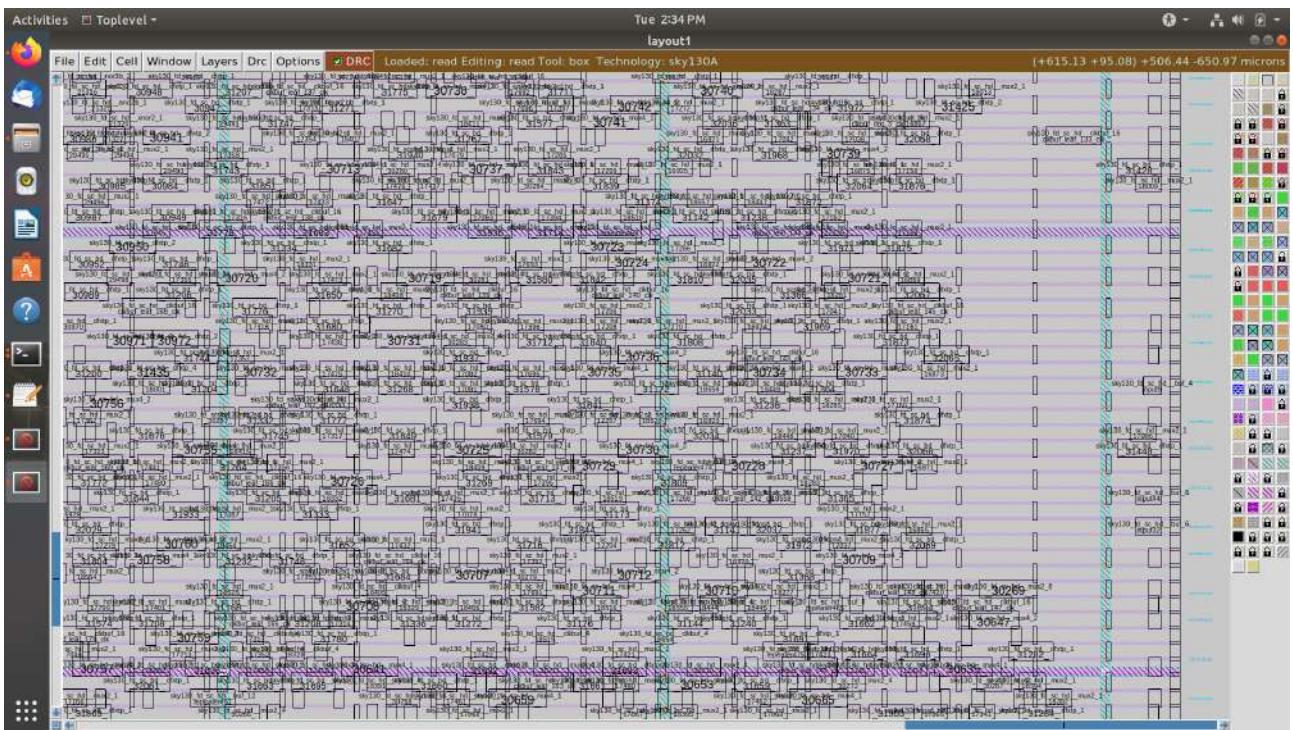
```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/  
26-03_08-45/tmp/floorplan/
```

```
# Command to load the PDN def in magic tool
```

```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/  
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read 14-pdn.def &
```

Screenshots of PDN def





2. Perform detailed routing using TritonRoute and explore the routed layout.

Command to perform routing

```
# Check value of 'CURRENT_DEF'
```

```
echo $::env(CURRENT_DEF)
```

```
# Check value of 'ROUTING_STRATEGY'
```

```
echo $::env(ROUTING_STRATEGY)
```

```
# Command for detailed route using TritonRoute
```

```
run_routing
```

Screenshots of routing run

```
Activities Terminal - Tue 2:48 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
% echo $::env(ROUTING_STRATEGY)
can't read "::env(ROUTING_STRATEGY)": no such variable
% run_routing
[INFO]: Routing...
[INFO]: Running Global Routing...
[INFO]: current step index: 15
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
Notice 0: Design: picorv32a
Notice 0: Created 411 pins.
Notice 0: Created 25690 components and 145610 component-terminals.
Notice 0: Created 2 special nets and 0 connections.
Notice 0: Created 18084 nets and 60036 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/floorplan/14-pdn.def
Min routing layer: 2
Max routing layer: 6
```

```
Activities Terminal - Tue 3:38 PM vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
elapsed time = 00:00:08, memory = 782.73 (MB)
completing 60% with 0 violations
elapsed time = 00:00:10, memory = 782.73 (MB)
completing 70% with 0 violations
elapsed time = 00:00:12, memory = 782.73 (MB)
completing 80% with 0 violations
elapsed time = 00:00:14, memory = 782.73 (MB)
completing 90% with 0 violations
elapsed time = 00:00:15, memory = 782.73 (MB)
completing 100% with 0 violations
elapsed time = 00:00:17, memory = 782.73 (MB)
number of violations = 0
cpu time = 00:00:16, elapsed time = 00:00:17, memory = 782.73 (MB), peak = 854.19 (MB)
total wire length = 1103187 um
total wire length on LAYER l1l = 2639 um
total wire length on LAYER met1 = 483058 um
total wire length on LAYER met2 = 482317 um
total wire length on LAYER met3 = 122196 um
total wire length on LAYER met4 = 12976 um
total wire length on LAYER met5 = 0 um
total number of vias = 145509
up-via summary (total 145509):

-----
FR_MASTERSLICE      0
      l1l    60472
      met1   78129
      met2   6540
```

```

Activities Terminal - Tue 3:29 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Calculating Runtime From the Start...
[INFO]: Routing completed for picorv32a/26-03_08-45 in 1h7m11s
::: %

```

Commands to load routed def in magic in another terminal

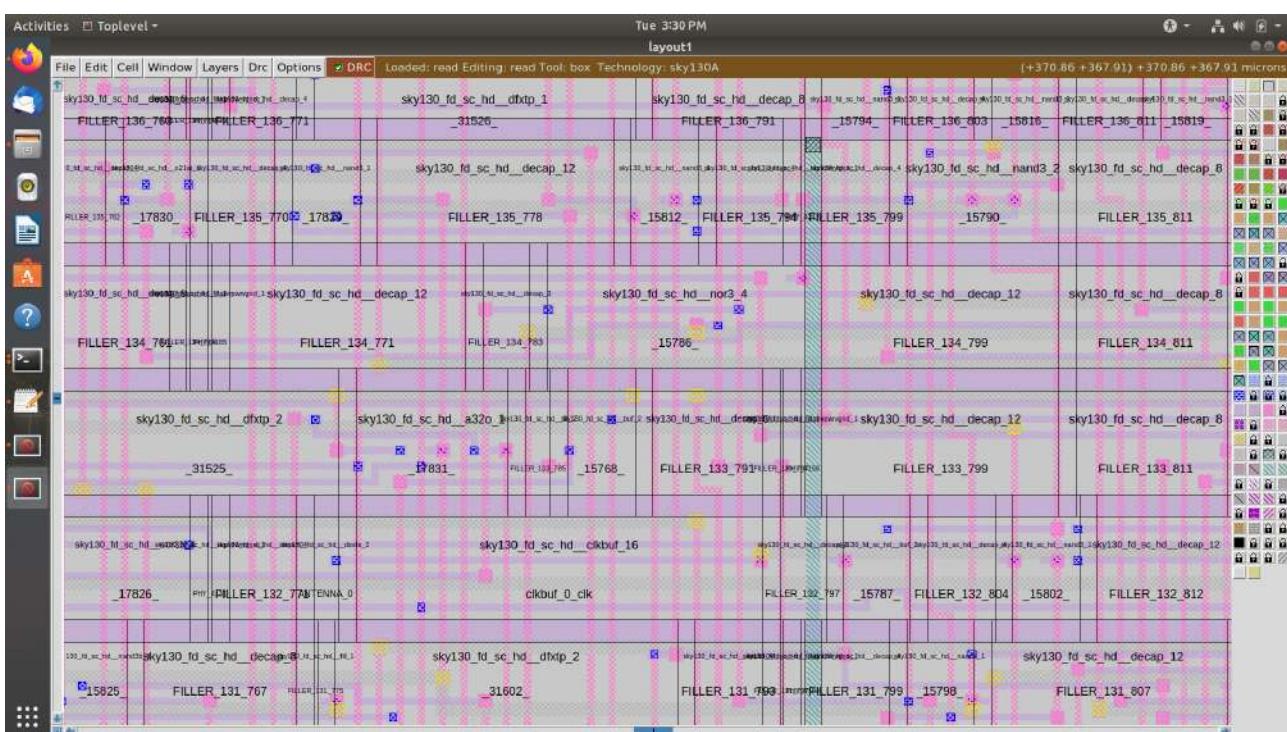
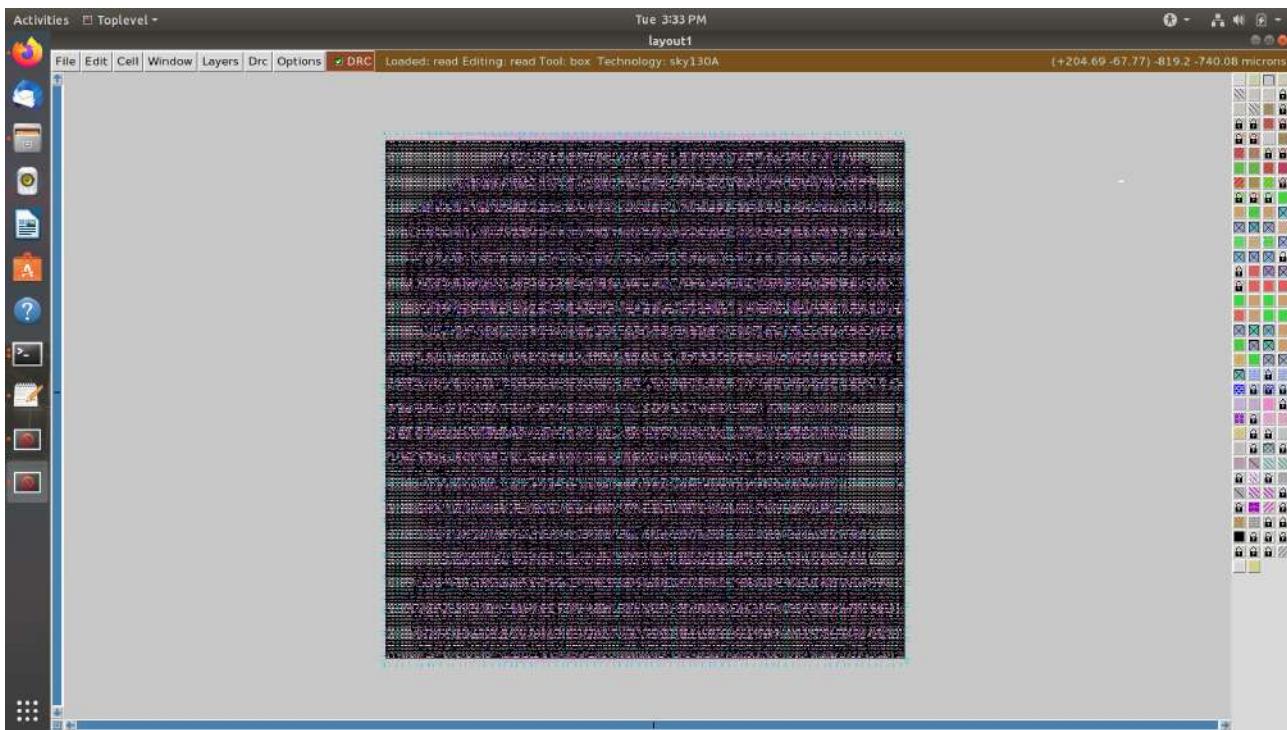
Change directory to path containing routed def

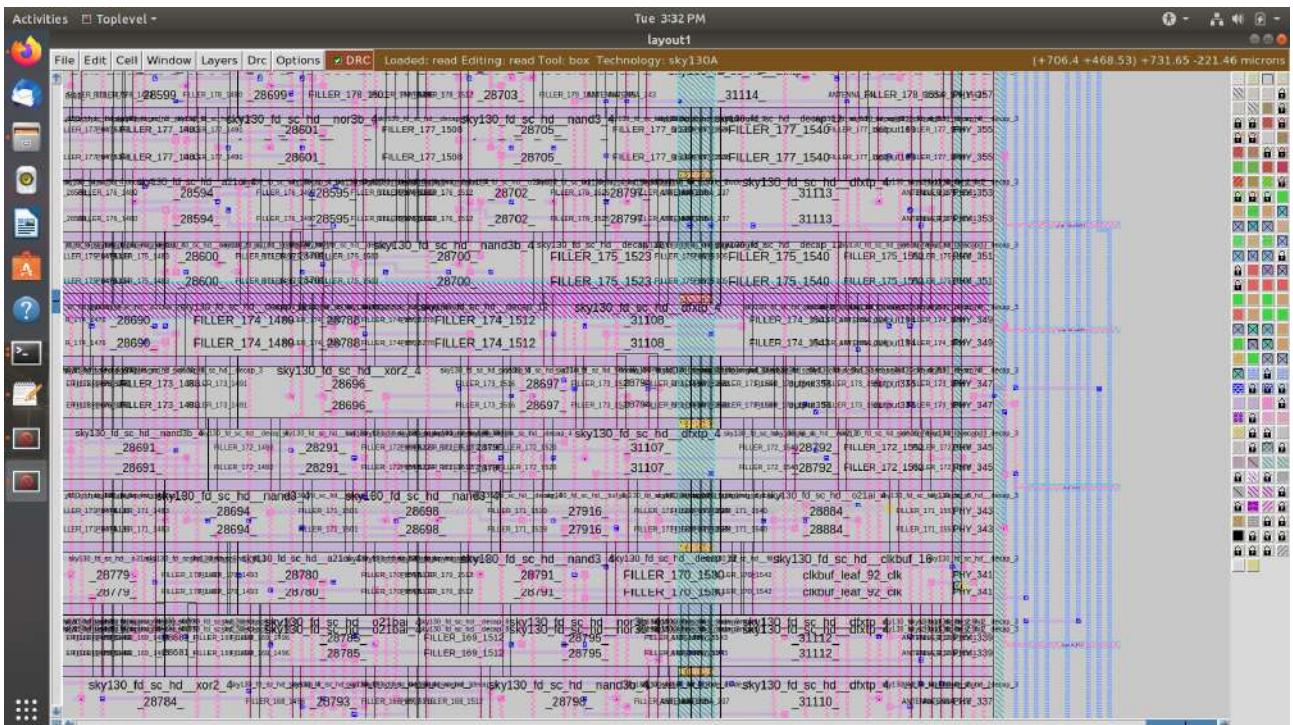
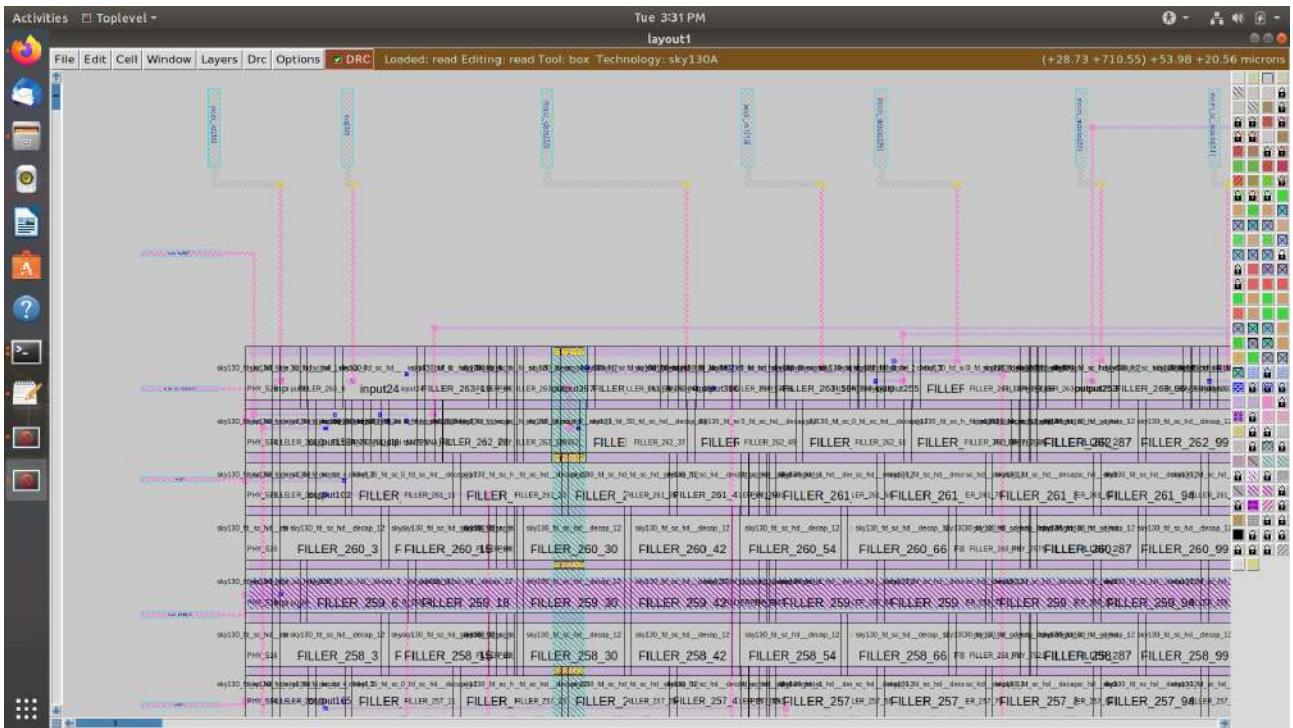
```
cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/
26-03_08-45/results/routing/
```

Command to load the routed def in magic tool

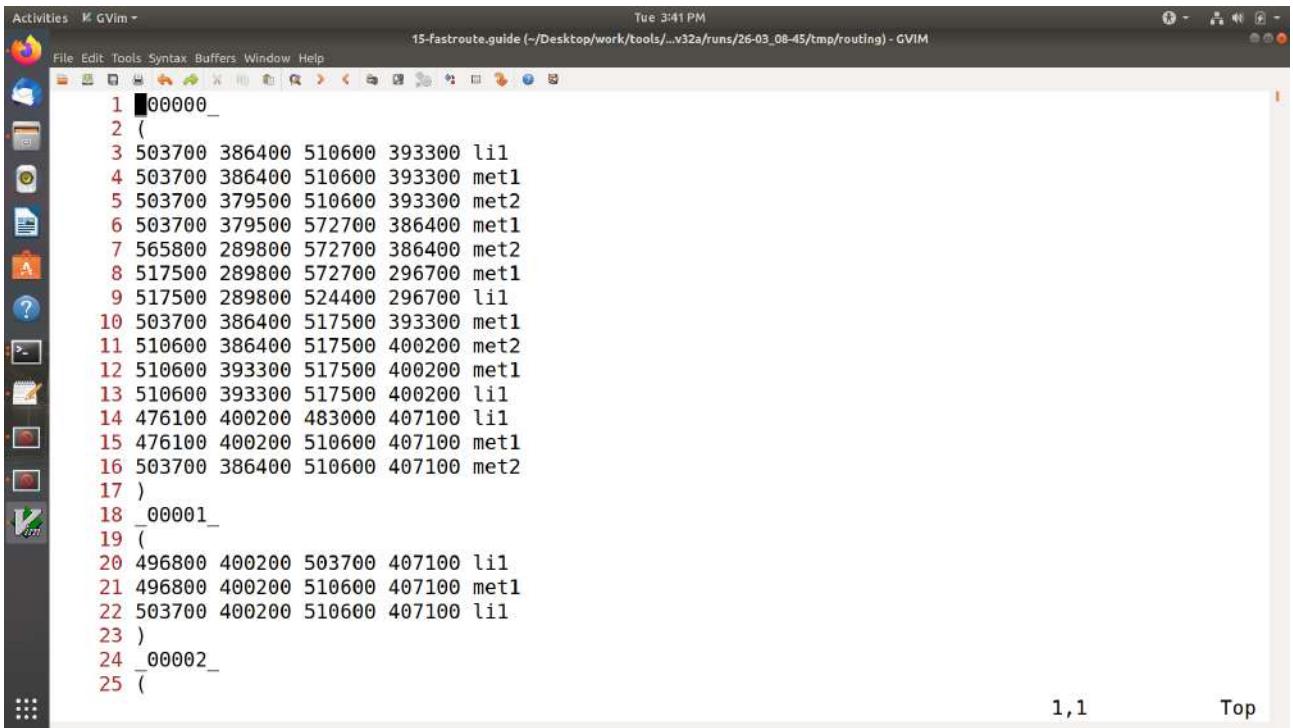
```
magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/
libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.def &
```

Screenshots of routed def





Screenshot of fast route guide present in openlane/designs/picorv32a/runs/26-03_08-45/tmp/routing directory



The screenshot shows a terminal window titled "Activities" with "GVim" selected. The title bar indicates the file is "15-fastroute.guide (~/Desktop/work/tools/...v32a/runs/26-03_08-45/tmp/routing) - GVIM" and the time is "Tue 3:41 PM". The GVim interface has a toolbar with icons for file operations like Open, Save, and Cut/Paste. The left sidebar contains a file tree and a search bar. The main editor area displays the following text:

```
1 _00000_
2 (
3 503700 386400 510600 393300 l1l
4 503700 386400 510600 393300 met1
5 503700 379500 510600 393300 met2
6 503700 379500 572700 386400 met1
7 565800 289800 572700 386400 met2
8 517500 289800 572700 296700 met1
9 517500 289800 524400 296700 l1l
10 503700 386400 517500 393300 met1
11 510600 386400 517500 400200 met2
12 510600 393300 517500 400200 met1
13 510600 393300 517500 400200 l1l
14 476100 400200 483000 407100 l1l
15 476100 400200 510600 407100 met1
16 503700 386400 510600 407100 met2
17 )
18 _00001_
19 (
20 496800 400200 503700 407100 l1l
21 496800 400200 510600 407100 met1
22 503700 400200 510600 407100 l1l
23 )
24 _00002_
25 )
```

The status bar at the bottom right shows "1,1" and "Top".

3. Post-Route parasitic extraction using SPEF extractor.

Commands for SPEF extraction using external tool

```
# Change directory
```

```
cd Desktop/work/tools/SPEF_EXTRACTOR
```

```
# Command extract spef
```

```
python3 main.py /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/
designs/picorv32a/runs/26-03_08-45/tmp/merged.lef /home/vsduser/Desktop/work/tools/
openlane_working_dir/openlane/designs/picorv32a/runs/26-03_08-45/results/routing/
picorv32a.def
```

4. Post-Route OpenSTA timing analysis with the extracted parasitics of the route.

Commands to be run in OpenLANE flow to do OpenROAD timing analysis with integrated OpenSTA in OpenROAD

```
# Command to run OpenROAD tool
```

```
openroad
```

```
# Reading lef file
```

```
read_lef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
```

```
# Reading def file
```

```
read_def /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/  
picorv32a.def
```

```
# Creating an OpenROAD database to work with
```

```
write_db pico_route.db
```

```
# Loading the created database in OpenROAD
```

```
read_db pico_route.db
```

```
# Read netlist post CTS
```

```
read_verilog /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/synthesis/  
picorv32a.synthesis_preroute.v
```

```
# Read library for design

read_liberty $::env(LIB_SYNTH_COMPLETE)

# Link design and library

link_design picorv32a

# Read in the custom sdc we created

read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc

# Setting all cloks as propagated clocks

set_propagated_clock [all_clocks]

# Read SPEF

read_spef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/
picorv32a.spef

# Generating custom timing report

report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format
full_clock_expanded -digits 4
```

```
# Exit to OpenLANE flow
```

```
exit
```

Screenshots of commands run and timing report generated

```

Activities Terminal - Tue 11:16 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% openroad
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
% read_lef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/tmp/merged.lef
% read_def /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.def
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.def
Notice 0: Design: picorv32a
Notice 0: Created 429 pins.
Notice 0: Created 65617 components and 305814 component-terminals.
Notice 0: Created 2 special nets and 0 connections.
Notice 0: Created 18084 nets and 60532 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.def
% write_db pico_route.db
% read_db pico_route.db
% read_verilog /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/synthesis/picorv32a.synthesis_preroute.v
% read_liberty /openLANE_flow/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib
1
::: % link design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_fill_1 has no liberty cell.

```

```

Activities Terminal - Tue 11:17 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
% link_design picorv32a
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_fill_1 has no liberty cell.
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_fill_2 has no liberty cell.
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_tapvpwrvrnd_1 has no liberty cell.
% read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
[INFO]: Setting output delay to: 4.9460000000000001
[INFO]: Setting input delay to: 4.9460000000000001
[INFO]: Setting load to: 0.017653
% set_propagated_clock [all_clocks]
% read_spef /openLANE_flow/designs/picorv32a/runs/26-03_08-45/results/routing/picorv32a.spef
1
% report_checks -path_delay min_max -fields {slew trans net cap input_pins} -format full_clock_expanded -digits 4
Startpoint: _30900_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30910_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Fanout Cap Slew Delay Time Description
-----
                           0.0000  0.0000  clock clk (rise edge)
                           0.0000  0.0000  clock source latency
                           0.0897  0.0624  0.0624 ^ clk (in)
                           0.0563          clk (net)
                           0.0900  0.0000  0.0624 ^ clkbuf_0_clk/A (sky130_fd_sc_hd_clkbuff_16)
                           0.0371  0.1366  0.1990 ^ clkbuf_0_clk/X (sky130_fd_sc_hd_clkbuff_16)
                           2     0.0143          clknet_0_clk (net)

```

```

Activities Terminal - Tue 11:17 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      5  0.0099
      0.0596  0.0002  2.3273 ^ clknet_leaf_220_clk (net)
      0.0000  2.3273  clock reconvergence pessimism
      -0.0274  2.2998  library hold time
      2.2998  data required time
      2.2998  data required time
      -1.9092  data arrival time
      -0.3907  slack (VIOLATED)

Startpoint: resetn (input port clocked by clk)
Endpoint: mem_la_read (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout   Cap     Slew     Delay    Time   Description
-----+-----+-----+-----+-----+
          0.0000  0.0000  clock clk (rise edge)
          0.0000  0.0000  clock network delay (propagated)
          4.9460  4.9460 ^ input external delay
          0.0172  0.0055  4.9515 ^ resetn (in)
          1  0.0042   resetn (net)
          0.0172  0.0000  4.9515 ^ input101/A (sky130_fd_sc_hd_clkbuf_8)
          0.0662  0.1329  5.0843 ^ input101/X (sky130_fd_sc_hd_clkbuf_8)
          7  0.0299   net101 (net)

```

```

Activities Terminal - Tue 11:17 PM
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Help
      6  0.0211
      0.0760  0.0002  5.2498 ^ 12638_(net)
      0.0933  0.0927  5.3425 v 17093/_C (sky130_fd_sc_hd_nand3_4)
      4  0.0143
      0.0933  0.0001  5.3426 v 17093/_Y (sky130_fd_sc_hd_nand3_4)
      0.4344  0.3758  5.7184 ^ 13857_(net)
      2  0.0603
      0.4349  0.0115  5.7299 ^ 18867/_B1 (sky130_fd_sc_hd_a21oi_4)
      0.1189  0.2493  5.9793 ^ 18867/_Y (sky130_fd_sc_hd_a21oi_4)
      1  0.0177
      0.1189  0.0002  5.9795 ^ net199 (net)
      0.1189  0.0002  5.9795 ^ mem_la_read (net)
      24.7300  24.7300  clock clk (rise edge)
      0.0000  24.7300  clock network delay (propagated)
      0.0000  24.7300  clock reconvergence pessimism
      -4.9460  19.7840  output external delay
      19.7840  data required time
      -5.9795  data arrival time
      13.8045  slack (MET)

% exit
%
```

About

2 Week digital VLSI SoC design and planning workshop with complete RTL2GDSII flow organised by VSD in collaboration with NASSCOM (Advanced Physical Design using OpenLANE/Sky130)

Resources