

Description

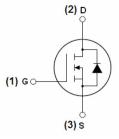
The VS60N10-TC uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- $V_{DS} = 100V, I_D = 60A$ $R_{DS(ON)} < 17mΩ @ V_{GS} = 10V$ (Typ:14mΩ)
- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VS60N10-TC	VS60N10-TC	TO-220-3L	-	н	-

Absolute Maximum Ratings (T_c=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _G s	±20	V
Drain Current-Continuous	I _D	60	A
Drain Current-Continuous(T _C =100°C)	I _D (100℃)	40	Α
Pulsed Drain Current	I _{DM}	160	Α
Maximum Power Dissipation	P _D	160	W
Derating factor	-	1.06	W/℃
Single pulse avalanche energy (Note 5)	E _{AS}	580	mJ

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Operating Junction and Storage Temperature Range	T _J ,T _{STG}	-55 To 175	${\mathbb C}$	
Thermal Characteristic				
Thermal Resistance, Junction-to-Case(Note 2)	R _{eJC}	0.94	°C/W	

Electrical Characteristics (T_c=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics			•			
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250µA	100	110	_	V
Zero Gate Voltage Drain Current	I _{DSS}	I _{DSS} V _{DS} =100V,V _{GS} =0V		-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS}$, $I_{D}=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =28A	-	14	17	mΩ
Forward Transconductance	g FS	V _{DS} =25V,I _D =28A 32		-	-	S
Dynamic Characteristics (Note4)	•					
Input Capacitance	C _{lss}	V _{DS} =25V,V _{GS} =0V,	Ħ	3400	-	PF
Output Capacitance	Coss		-	260	-	PF
Reverse Transfer Capacitance	C _{rss}	F=1.0MHz	-	210	-	PF
Switching Characteristics (Note 4)	•			,		
Turn-on Delay Time	t _{d(on)}		-	15	-	nS
Turn-on Rise Time	t _r	V_{DD} =30V, I_D =2A, R_L =15 Ω	-	11	-	nS
Turn-Off Delay Time	t _{d(off)}	V_{GS} =10V, R_{G} =2.5 Ω	-	52	-	nS
Turn-Off Fall Time	t _f		-	13	-	nS
Total Gate Charge	Qg	V -20V L -20A	-	94	-	nC
Gate-Source Charge	Q _{gs}	$V_{DS}=30V,I_{D}=30A,$ $V_{GS}=10V$	-	16	-	nC
Gate-Drain Charge	Q _{gd}	V _{GS} =10V	-	24	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =28A	-	0.85	1.2	V
Diode Forward Current (Note 2)	Is		-	-	60	Α
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF = 28A	-	33	-	nS
Reverse Recovery Charge	Qrr	di/dt = 100A/µs(Note3)	-	54	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

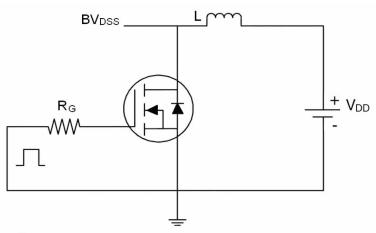
Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- 3. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
- 4. Guaranteed by design, not subject to production
- **5.** EAS condition: Tj=25 $^{\circ}$ C,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25 Ω

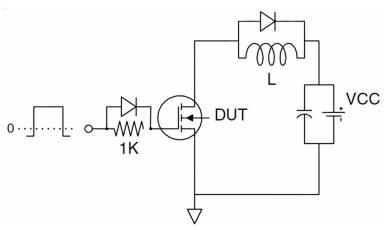


Test Circuit

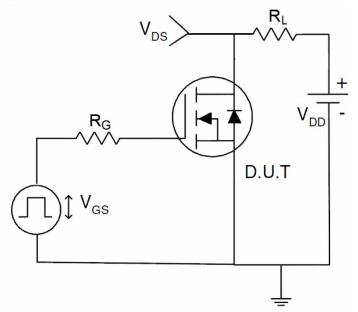
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit





Typical Electrical and Thermal Characteristics (Curves)

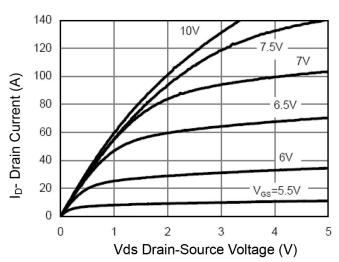


Figure 1 Output Characteristics

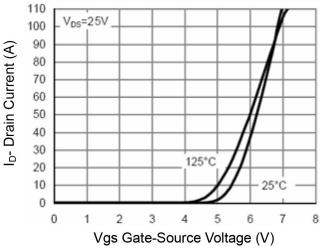


Figure 2 Transfer Characteristics

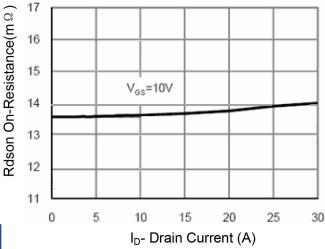


Figure 3 Rdson- Drain Current

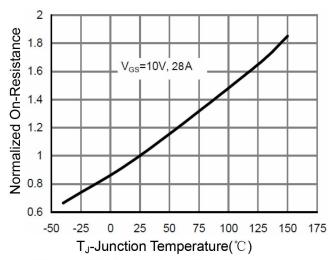


Figure 4 Rdson-Junction Temperature

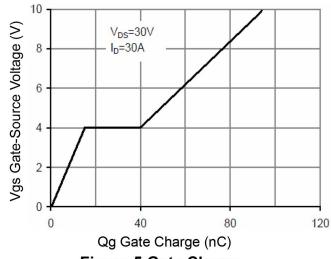


Figure 5 Gate Charge

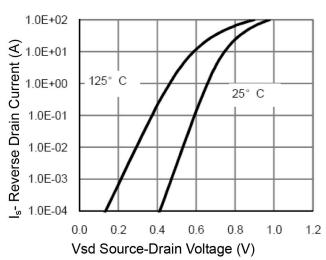


Figure 6 Source- Drain Diode Forward



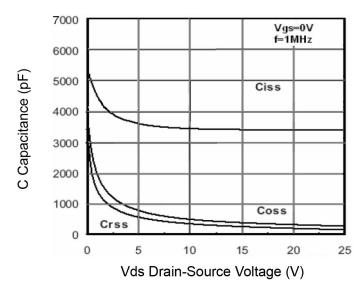


Figure 7 Capacitance vs Vds

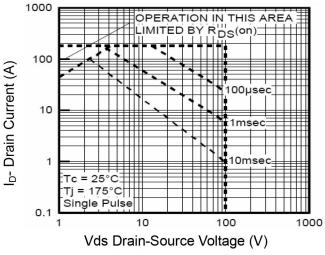
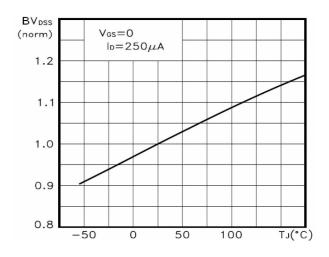


Figure 8 Safe Operation Area



T_J-Junction Temperature(°C)

Figure 9 BV_{DSS} vs Junction Temperature

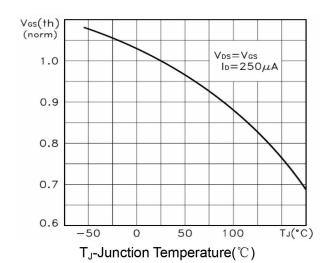
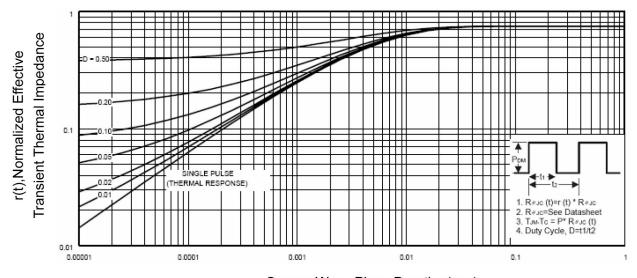


Figure 10 V_{GS(th)} vs Junction Temperature



Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance

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