Description

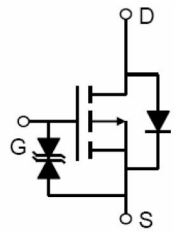
The **VS18P10-T2** uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. It is ESD protested.

General Features

- V_{DS} =-100V,I_D =-18A
  $R_{DS(ON)}$ <100mΩ @ V_{GS}=-10V (Typ:85mΩ)
  $R_{DS(ON)}$ <120mΩ @ V_{GS}=-10V (Typ:95mΩ)
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density cell design for ultra low On-Resistance

Application

- Power management in notebook computer
- Portable equipment and battery powered systems



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VS18P10-T2	VS18P10-T2	TO-252-2L	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-18	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	-12	A
Pulsed Drain Current	I_{DM}	-100	A
Single pulse avalanche energy (Note 5)	E_{AS}	170	mJ
Maximum Power Dissipation	P_D	70	W
Derating factor		0.47	W/℃
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta Jc}$	2.14	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

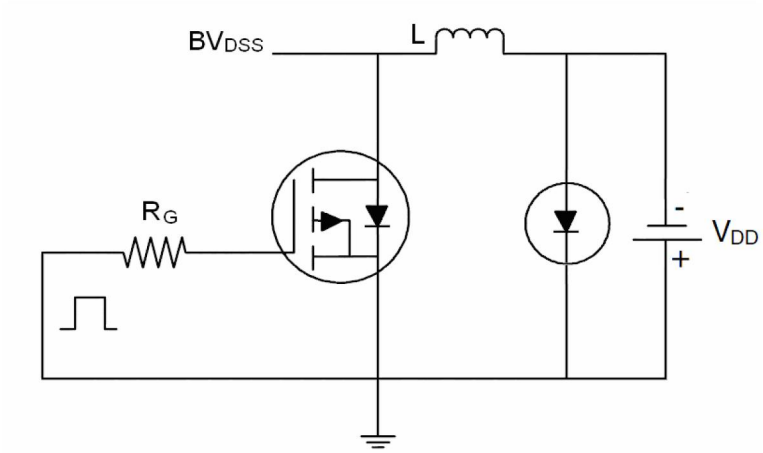
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±20	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1	-1.9	-3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-16A	-	85	100	mΩ
		V_{GS}=-4.5V, I_D=-16A		95	120	
Forward Transconductance	g_{FS}	V_{DS}=-50V,I_D=-10A	5	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-50V,V_{GS}=0V, F=1.0MHz	-	3810	-	PF
Output Capacitance	C_{oss}		-	129	-	PF
Reverse Transfer Capacitance	C_{rss}		-	125	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-50V,I_D=-16A V_{GS}=-10V,R_{GEN}=9.1Ω	-	16	-	nS
Turn-on Rise Time	t_r		-	73	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	34	-	nS
Turn-Off Fall Time	t_f		-	57	-	nS
Total Gate Charge	Q_g	V_{DS}=-50V,I_D=-16A, V_{GS}=-10V	-	70	-	nC
Gate-Source Charge	Q_{gs}		-	12.5	-	nC
Gate-Drain Charge	Q_{gd}		-	15.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-10A	-	-	-1.2	V
Diode Forward Current (Note 2)	I_S	-	-	-	-18	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =-16A di/dt = 100A/μs (Note3)	-	88.3	-	nS
Reverse Recovery Charge	Qrr		-	65.9	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

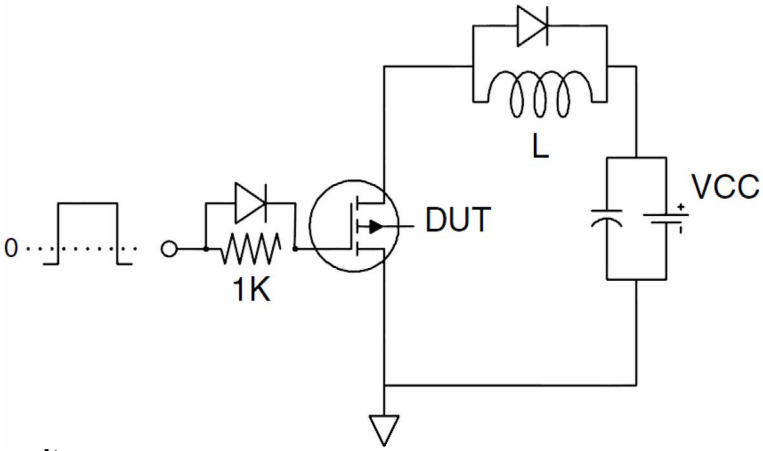
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition：Tj=25℃,V_{DD}=-50V,V_G=-10V,L=0.5mH,Rg=25Ω

Test Circuit

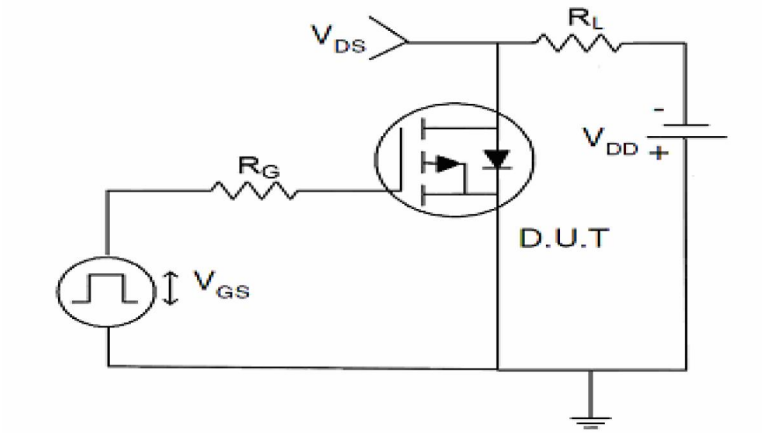
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

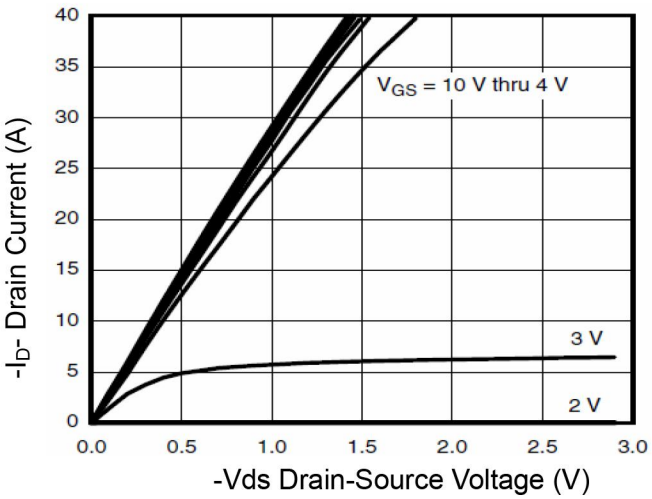


Figure 1 Output Characteristics

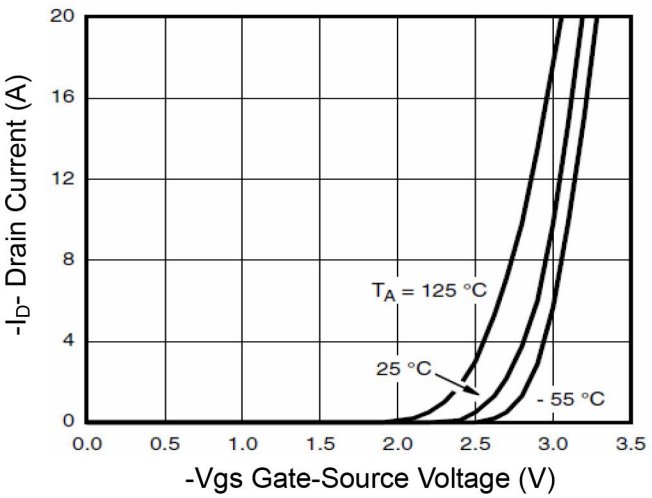


Figure 2 Transfer Characteristics

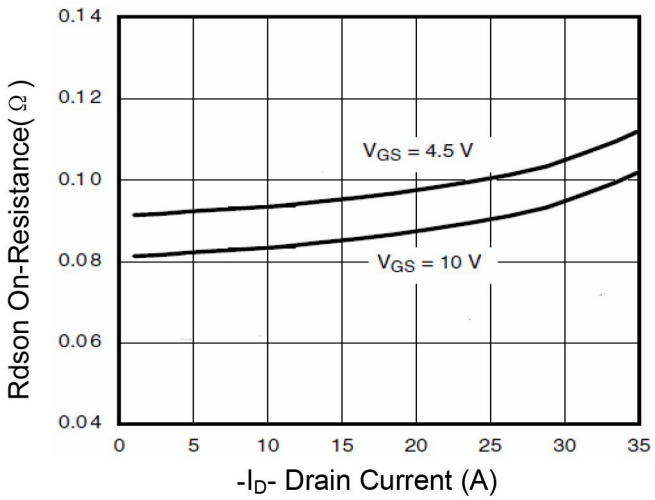


Figure 3 Rdson- Drain Current

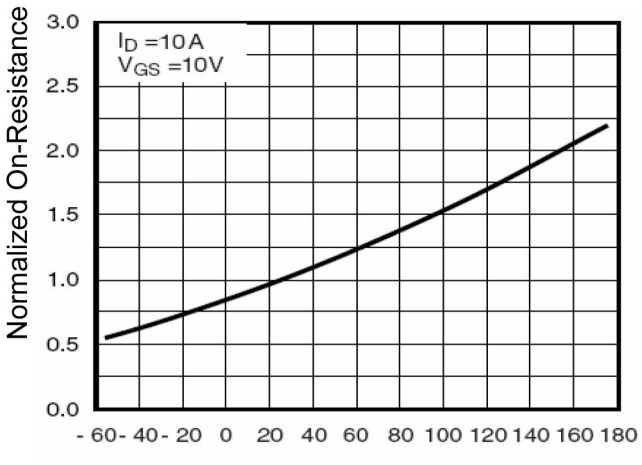


Figure 4 Rdson-JunctionTemperature

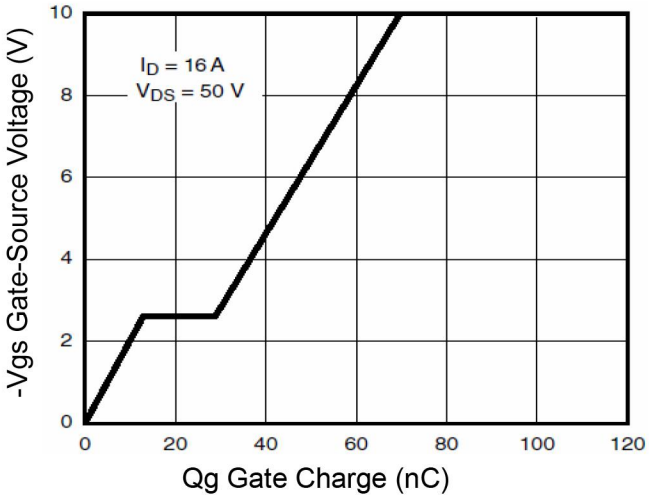


Figure 5 Gate Charge

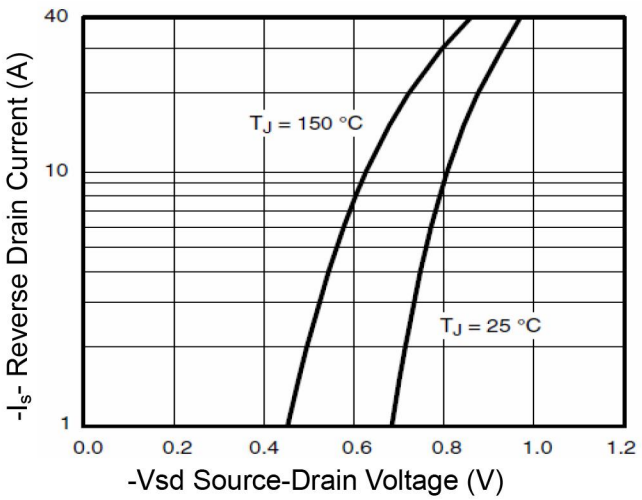


Figure 6 Source- Drain Diode Forward

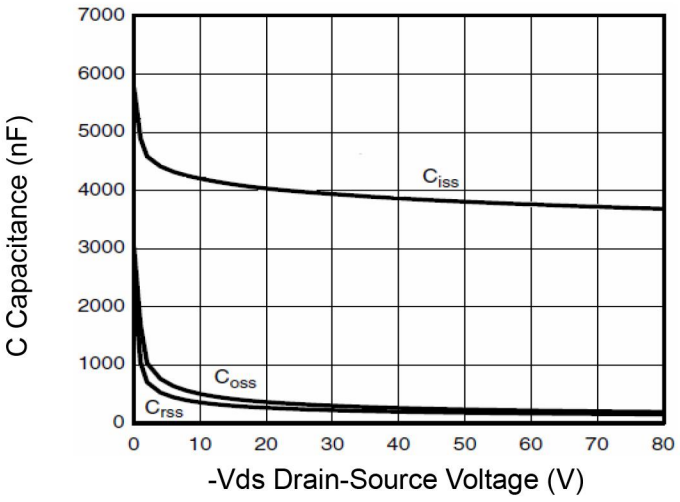


Figure 7 Capacitance vs Vds

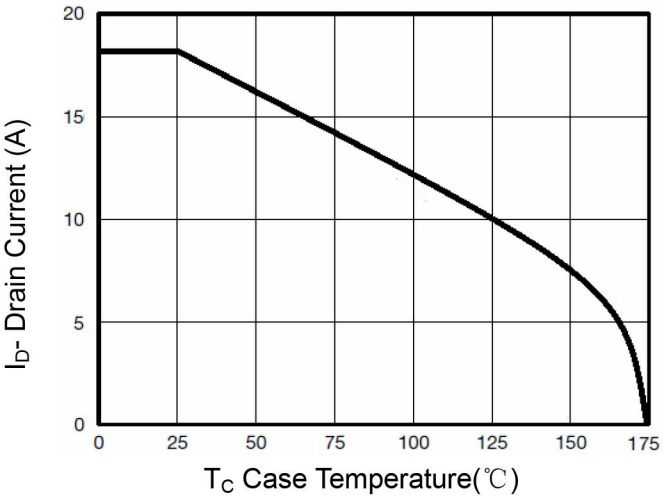


Figure 9 Drain Current vs Case Temperature

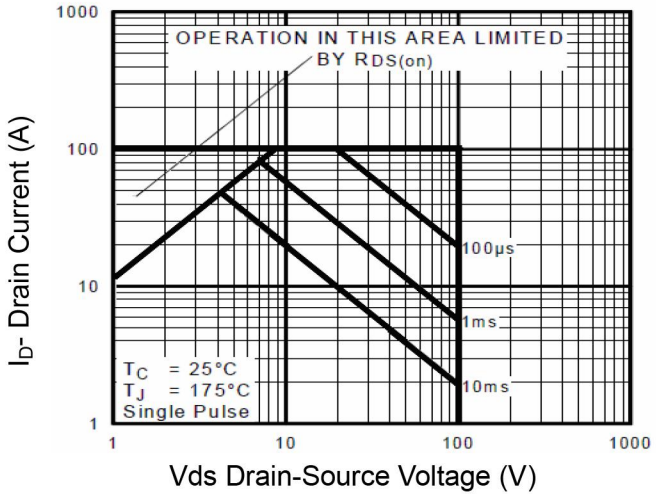


Figure 8 Safe Operation Area

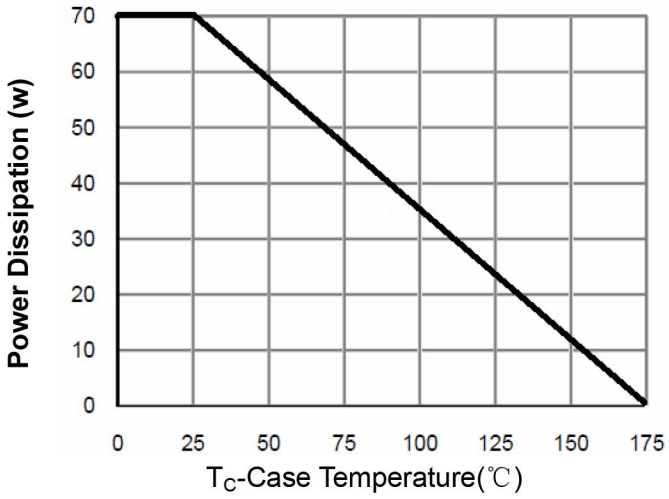


Figure 10 Power De-rating

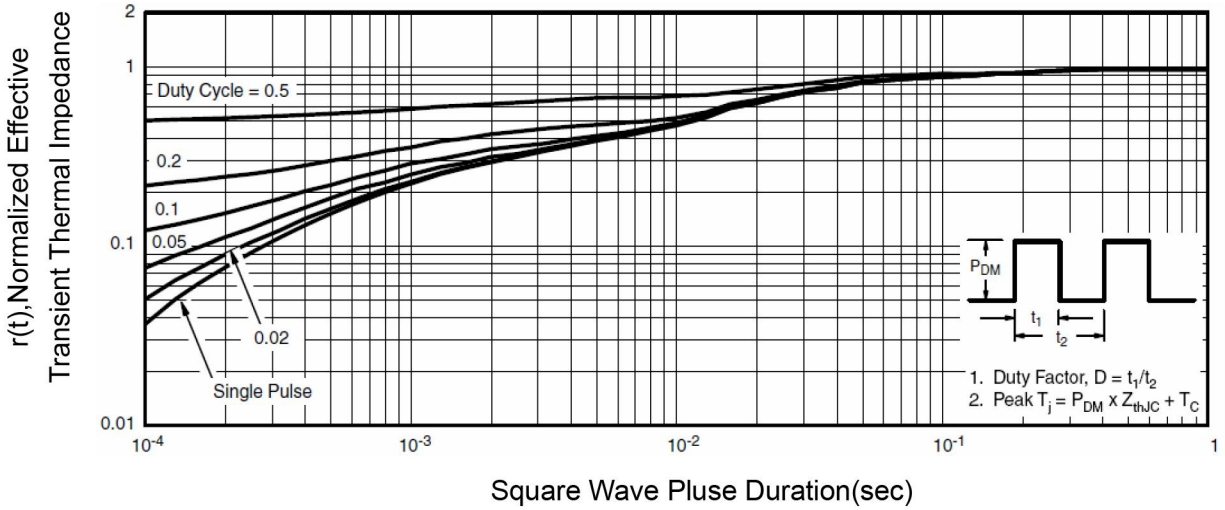


Figure 11 Normalized Maximum Transient Thermal Impedance