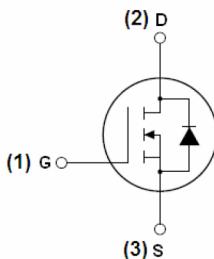


Description

The VS100N08-TC uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- $V_{DS} = 80V, I_D = 100A$
- $R_{DS(ON)} < 8.5m\Omega @ V_{GS}=10V$ (Typ: $6.8m\Omega$)
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability



Schematic diagram



Application

- Automotive applications
- Hard switched and high frequency circuits
- Uninterruptible power supply

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VS100N08-TC	VS100N08-TC	TO-220-3L	-	-	-

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	100	A
Drain Current-Continuous($T_c=100^\circ C$)	$I_D(100^\circ C)$	74	A
Pulsed Drain Current	I_{DM}	420	A
Maximum Power Dissipation	P_D	200	W
Derating factor		1.33	W/ $^\circ C$

Single pulse avalanche energy ^(Note 5)	E_{AS}	800	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.75	°C/W
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Electrical Characteristics ($T_C=25^\circ C$ unless otherwise noted)

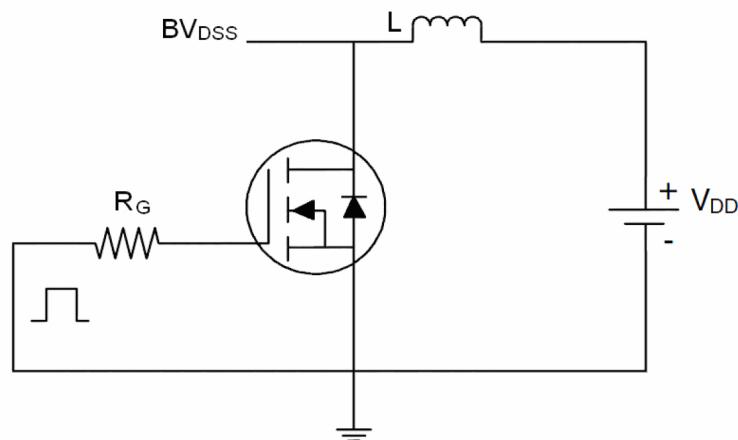
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	80	86	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=40A$	-	6.8	8.5	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS}=25V, I_D=40A$	80	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V, F=1.0MHz$	-	4522	-	PF
Output Capacitance	C_{oss}		-	396	-	PF
Reverse Transfer Capacitance	C_{rss}		-	339	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=40V, I_D=2A, R_L=15\Omega, R_G=2.5\Omega, V_{GS}=10V$	-	20	-	nS
Turn-on Rise Time	t_r		-	19	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	70	-	nS
Turn-Off Fall Time	t_f		-	30	-	nS
Total Gate Charge	Q_g	$I_D=55A, V_{DD}=40V, V_{GS}=10V$	-	117	-	nC
Gate-Source Charge	Q_{gs}		-	24	-	nC
Gate-Drain Charge	Q_{gd}		-	43	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=40A$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	100	A
Reverse Recovery Time	t_{rr}	$T_j=25^\circ C, IF=75A, di/dt=100A/uS$ ^(Note 3)	-	37	-	nS
Reverse Recovery Charge	Q_{rr}		-	58	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

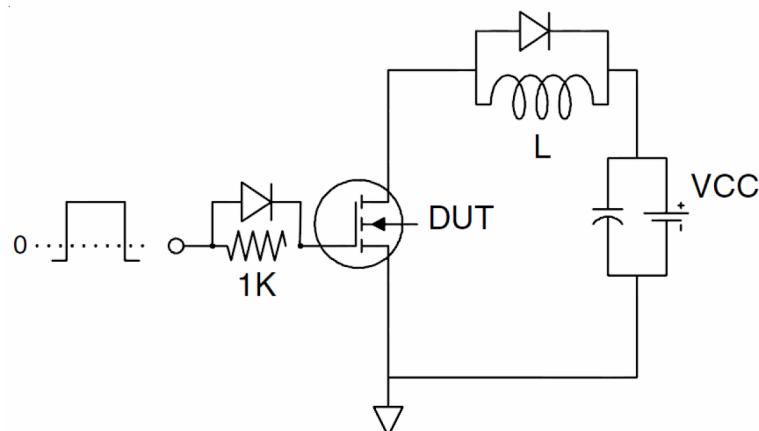
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_j=25^\circ C, V_{DD}=40V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test circuit

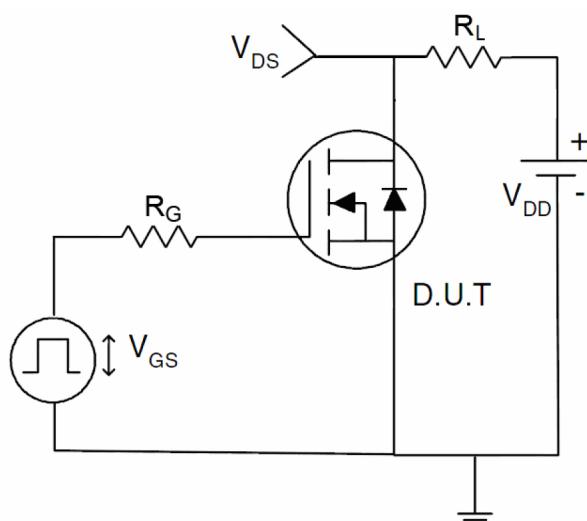
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

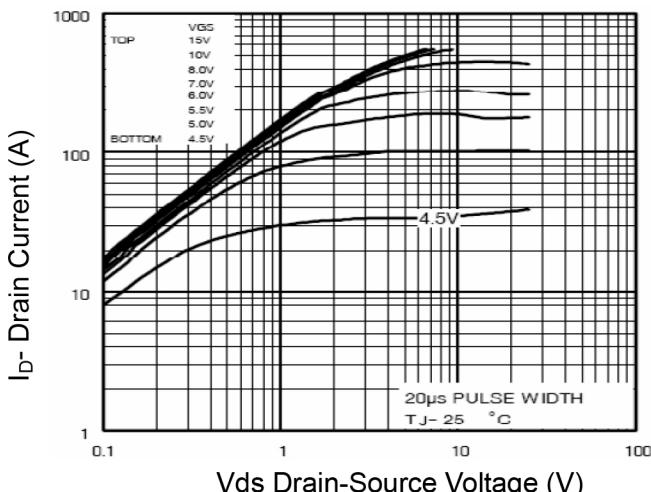


Figure 1 Output Characteristics

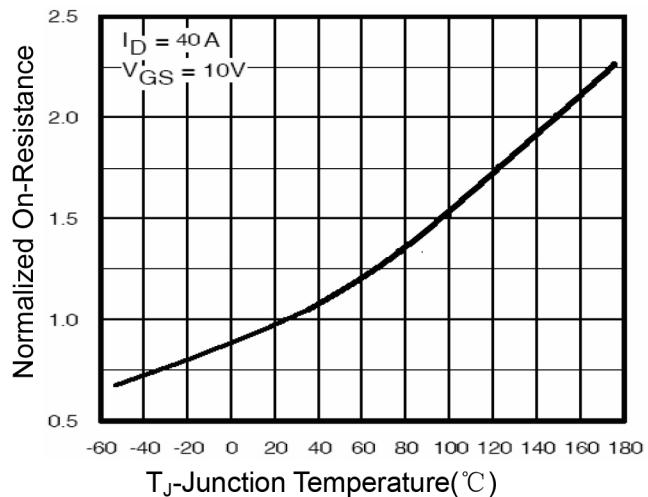


Figure 4 Rdson-JunctionTemperature

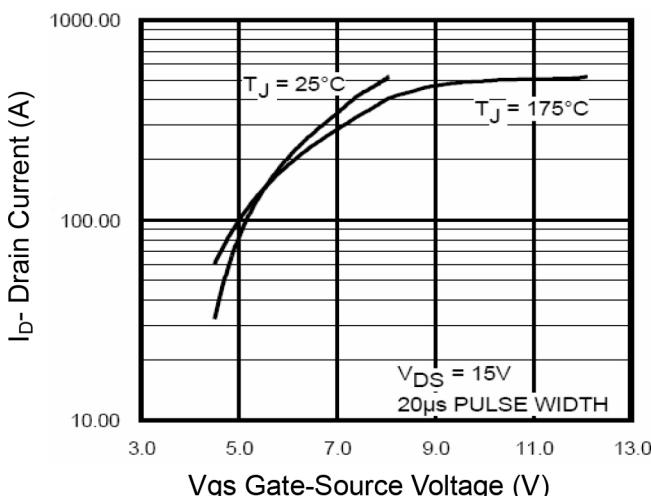


Figure 2 Transfer Characteristics

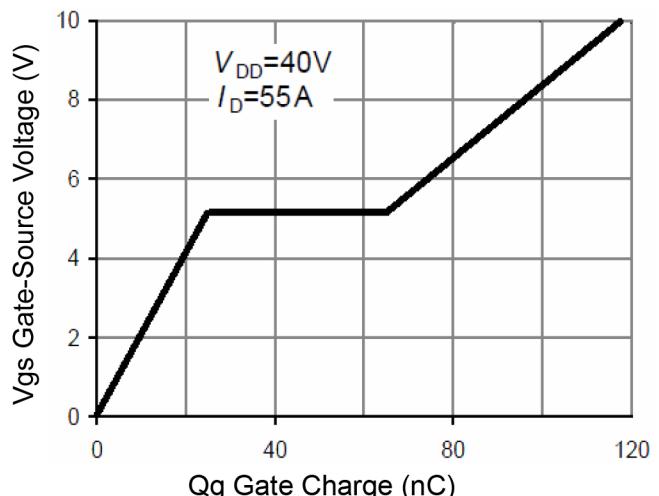


Figure 5 Gate Charge

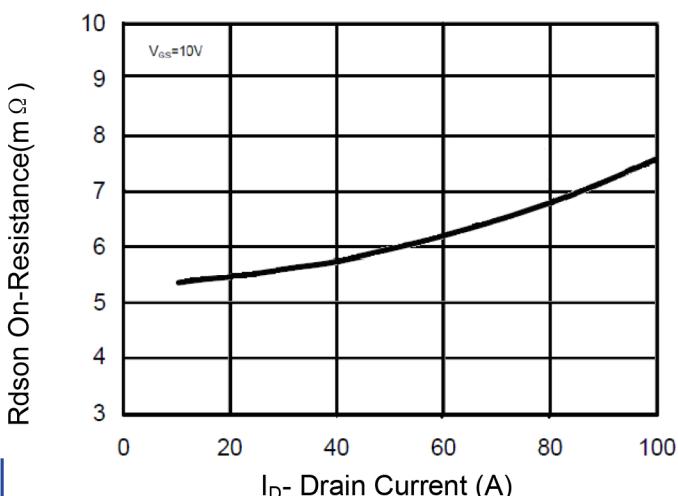


Figure 3 Rdson- Drain Current

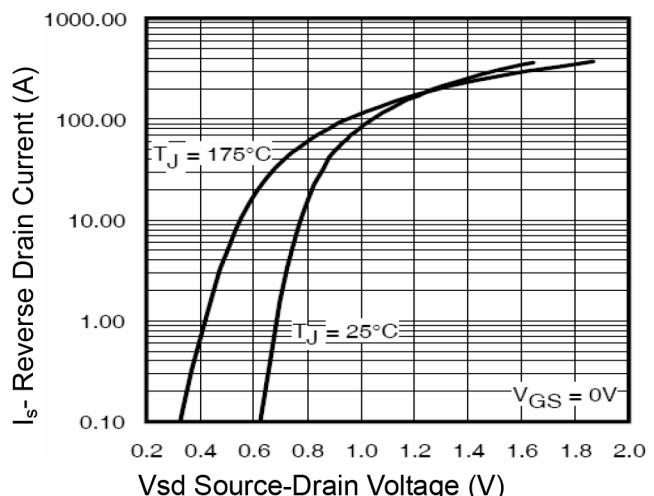
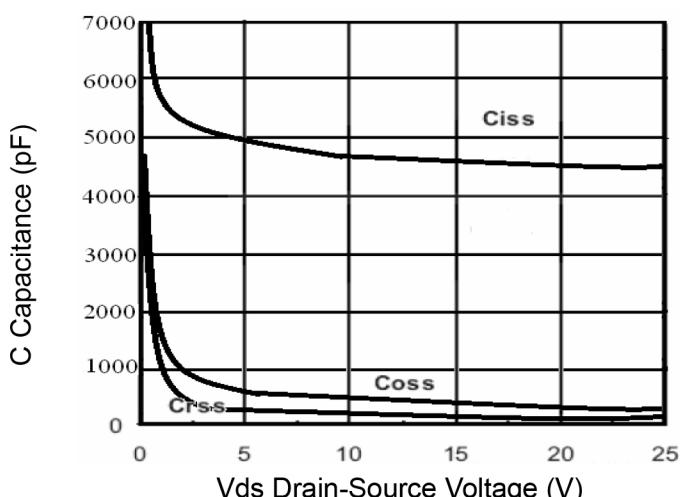
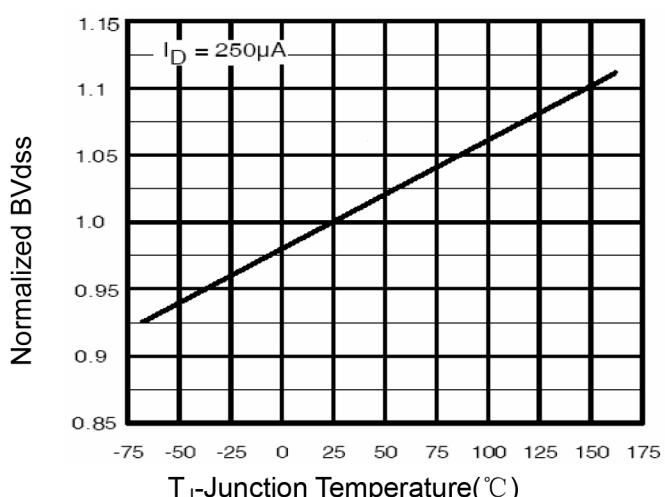
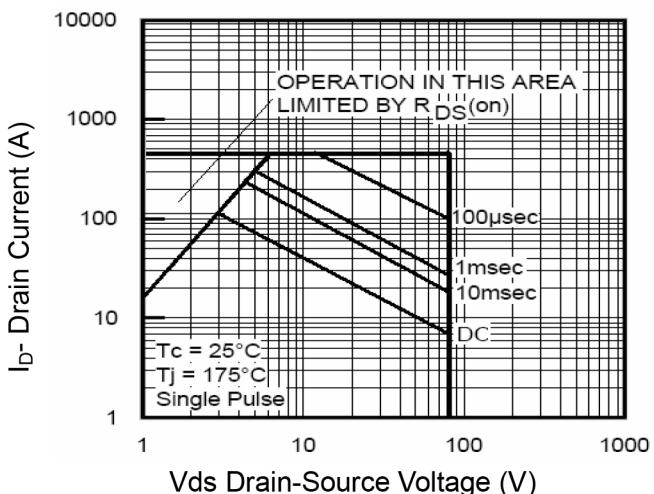
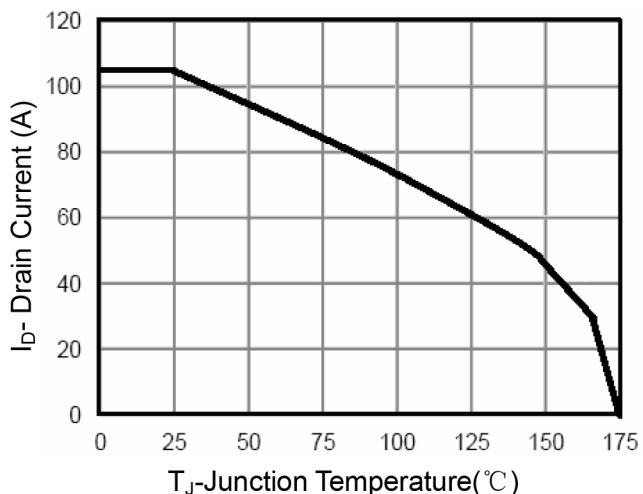
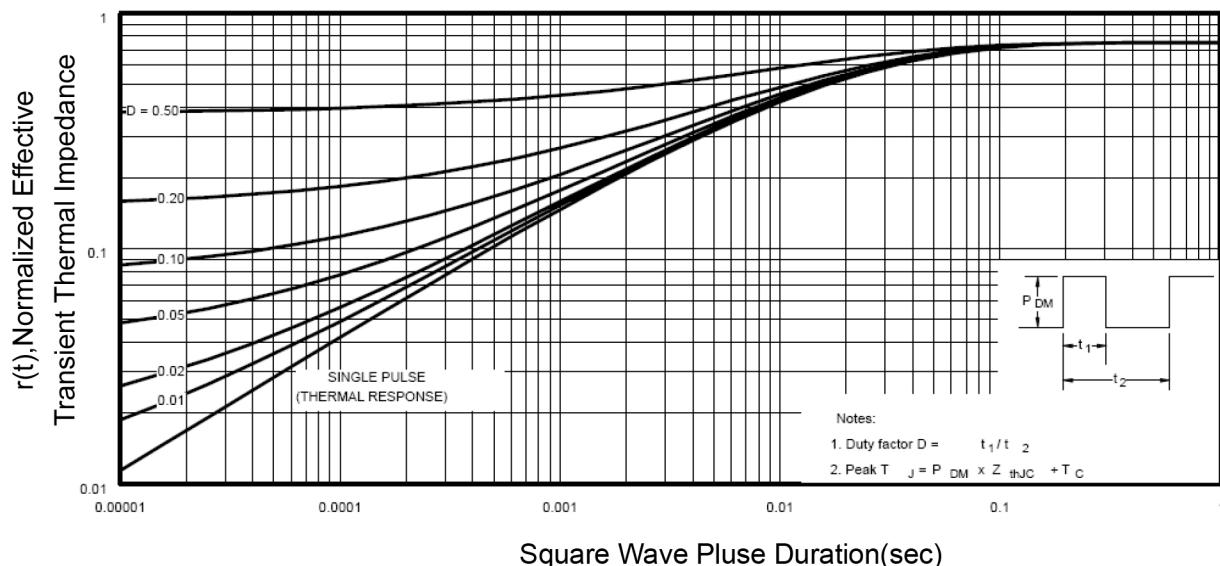


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 BV_{dss} vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 Current vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance