Description

This Product uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

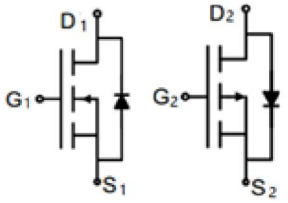
General Features

- **NMOS**
- V_{DS} 60V
- I_D (at V_{GS} = 10V) 3A
- $R_{DS(ON)}$ (at V_{GS} = 10V) < 80mΩ
- $R_{DS(ON)}$ (at V_{GS} = 4.5V) < 100mΩ

- **PMOS**
- V_{DS} -60V
- I_D (at V_{GS} = 10V) -4A
- $R_{DS(ON)}$ (at V_{GS} = 10V) < 95mΩ
- $R_{DS(ON)}$ (at V_{GS} = 4.5V) < 140mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

- Power switch
- DC/DC converters



Schematic diagram

Device	Package	Marking	Packaging
VS4NP06-S8	SOP-8	**VS4NP06-S8**	

Absolute Maximum Ratings T_C = 25°C, unless otherwise noted

Parameter	Symbol	NMOS	PMOS	Unit
Drain-Source Voltage	V_{DS}	60	-60	V
Continuous Drain Current	I_D	3	-4	A
Pulsed Drain Current (note1)	I_{DM}	12	-16	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Power Dissipation	P_D	1.7	3.1	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	-55 To 150	°C

Thermal Resistance

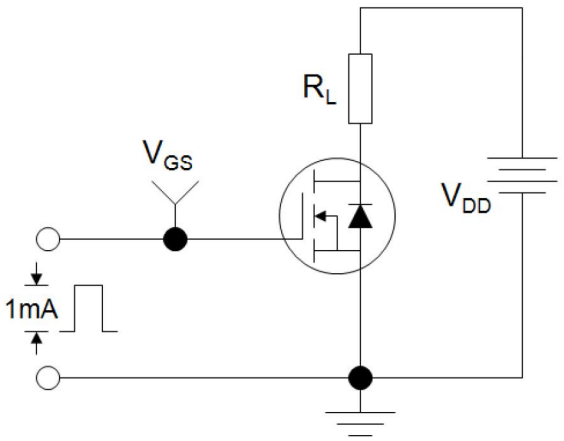
Parameter	Symbol	NMOS	PMOS	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	73.5	75	°C/W

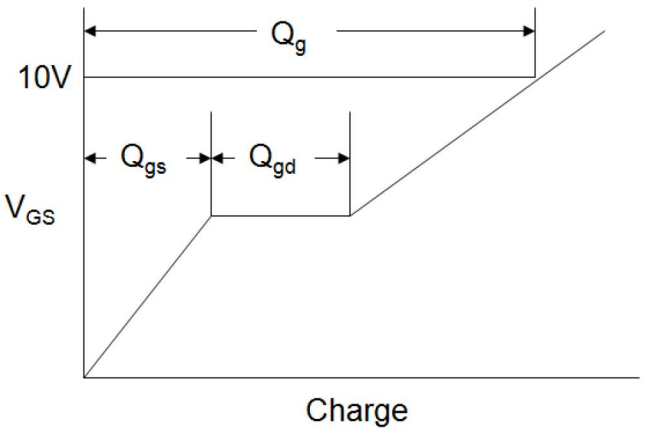
NMOS Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	60	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V, T_J = 25ºC	--	--	1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±16V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1	1.8	3	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 3A	--	62	80	mΩ
		V_{GS} = 4.5V, I_D = 2A	--	74	100	
Forward Transconductance	g_{FS}	V_{DS}=15V,I_D=2A	2	--	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 30V, f = 1.0MHz	--	290	--	pF
Output Capacitance	C_{oss}		--	40	--	
Reverse Transfer Capacitance	C_{rss}		--	23.5	--	
Total Gate Charge	Q_g	V_{DD} = 30V, I_D = 3A, V_{GS} = 4.5V	--	7.2	--	nC
Gate-Source Charge	Q_{gs}		--	1.2	--	
Gate-Drain Charge	Q_{gd}		--	1.6	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 30V, I_D = 1.5A, R_G = 1Ω	--	8	--	ns
Turn-on Rise Time	t_r		--	17	--	
Turn-off Delay Time	$t_{d(off)}$		--	17	--	
Turn-off Fall Time	t_f		--	12	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	3	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = 3A, V_{GS} = 0V	--	--	1.2	V

Notes

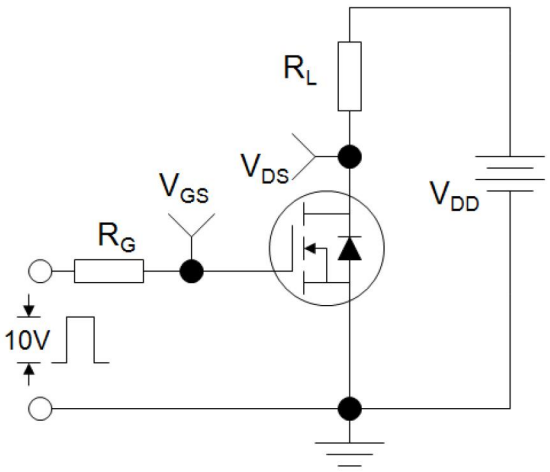
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G

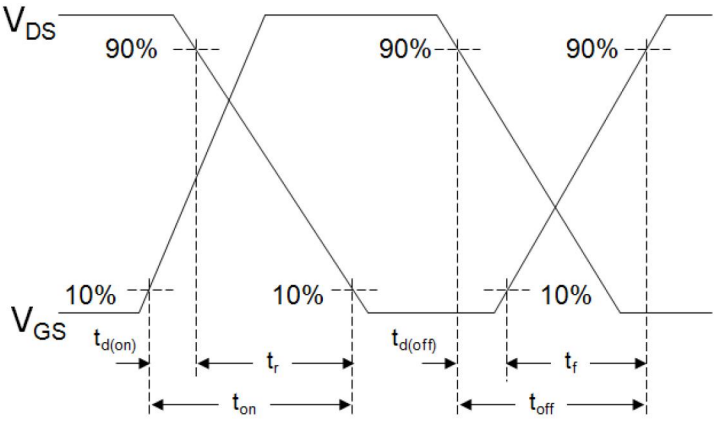
Gate Charge Test Circuit



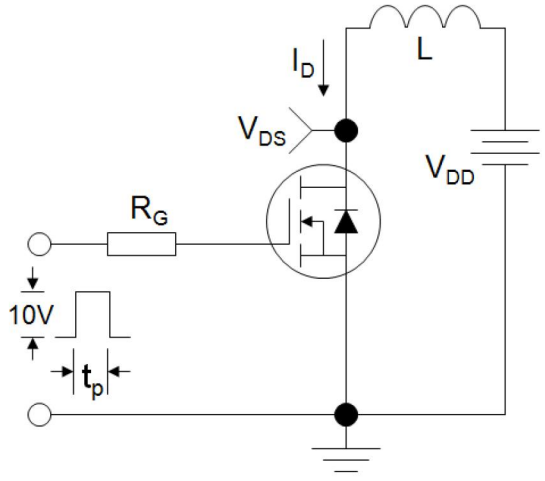


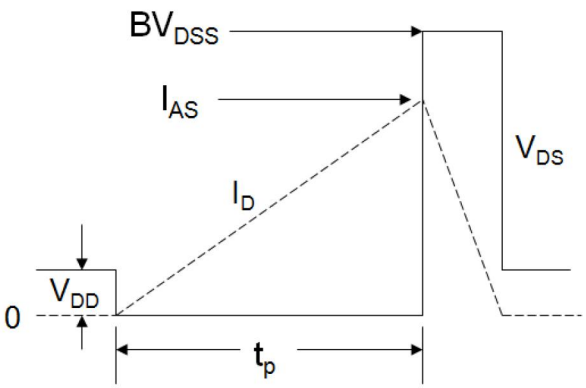
Switch Time Test Circuit





EAS Test Circuit





NMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

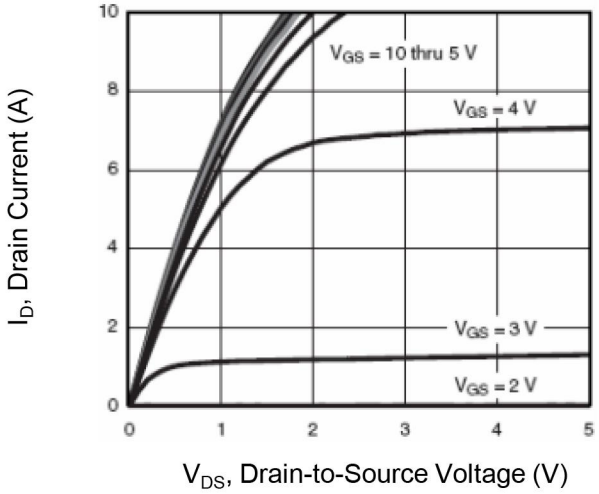


Figure 2. Transfer Characteristics

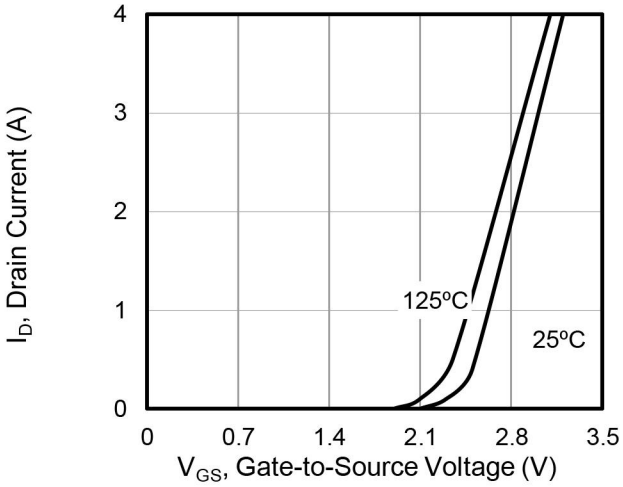


Figure 3.Drain-Source On-Resistance

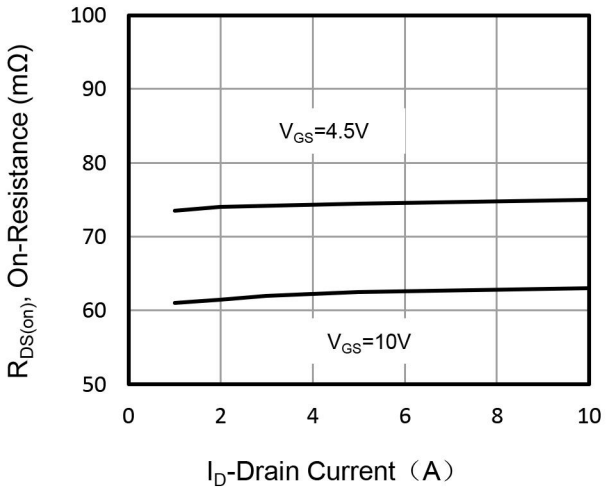


Figure 4. Gate Charge

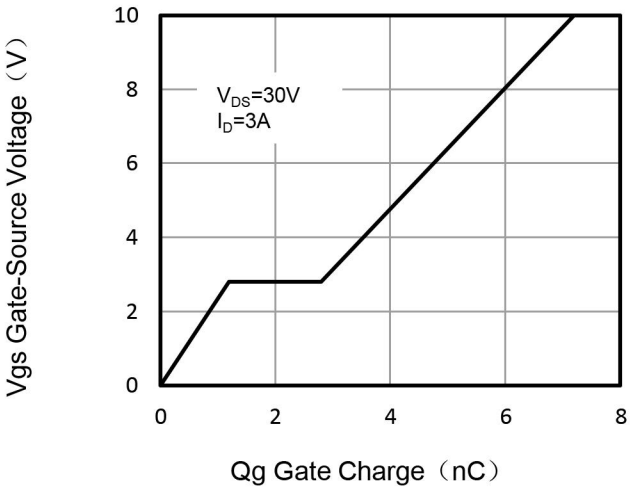


Figure 5. Capacitance

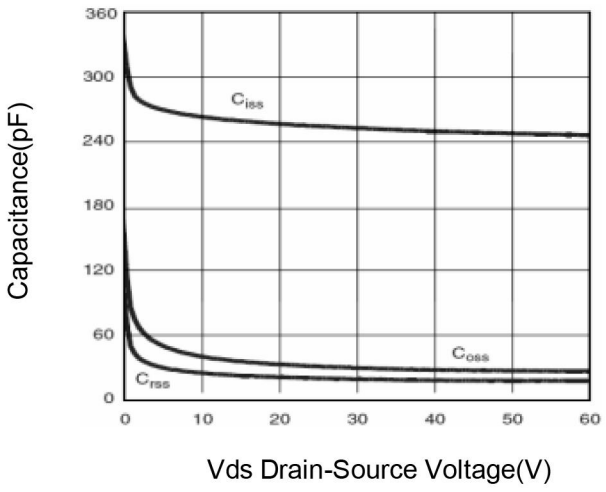
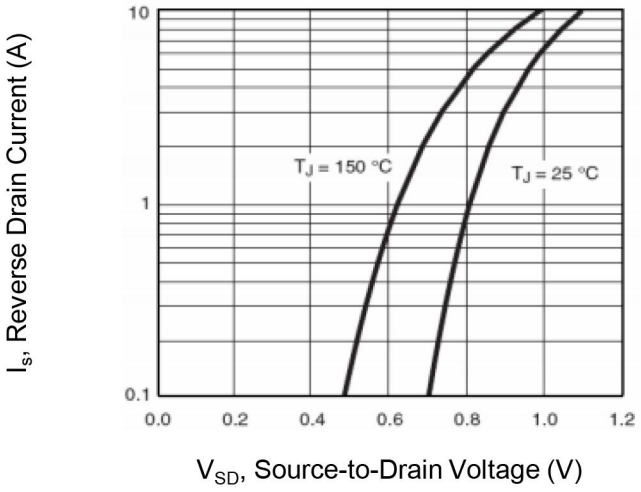


Figure 6. Source-Drain Diode Forward



NMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

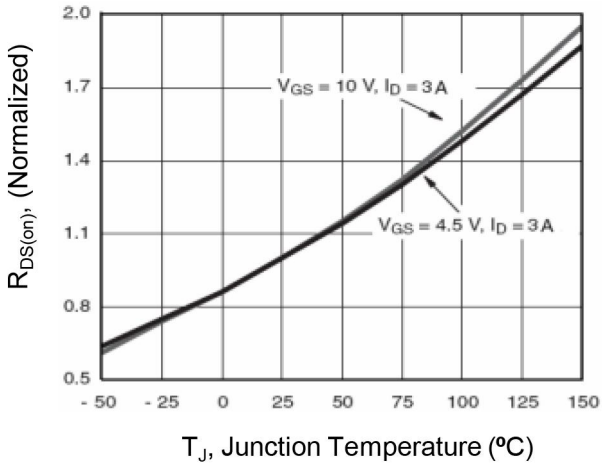


Figure 10. Safe Operation Area

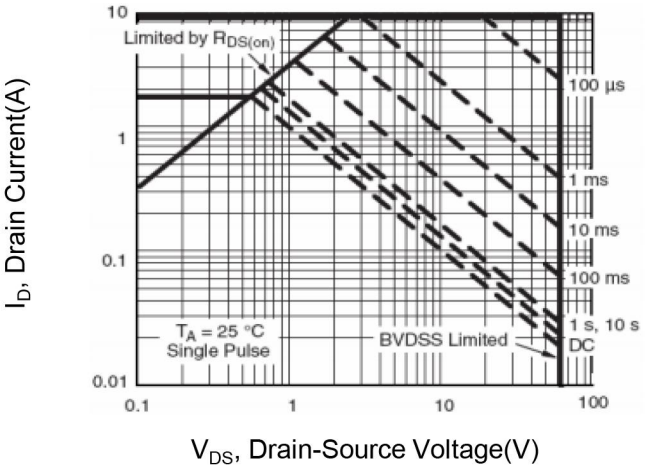
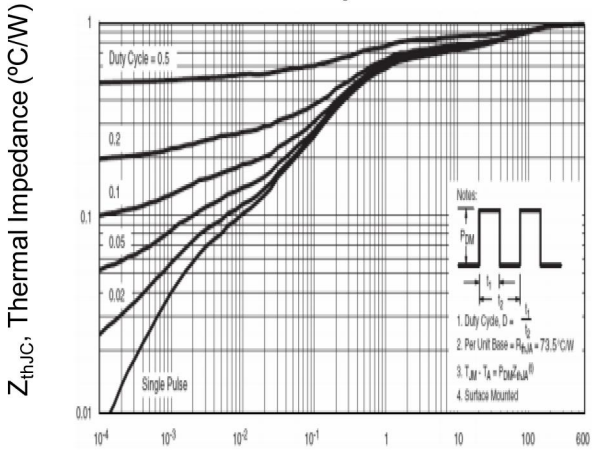


Figure 9. Normalized Maximum Transient Thermal Impedance

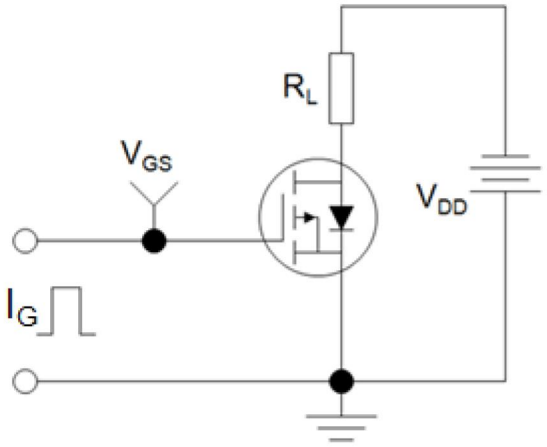


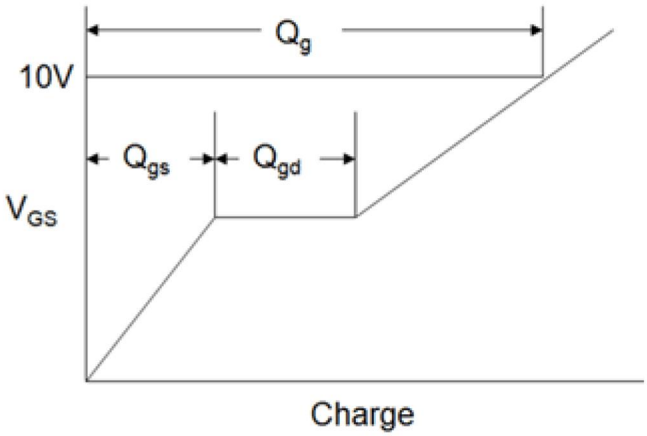
PMOS Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-60	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -60V, V_{GS} = 0V, T_J = 25ºC	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	uA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1	-1.8	-3	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -2A	--	81	95	mΩ
		V_{GS} = -4.5V, I_D = -2A	--	99	140	
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-4A	--	10	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -30V, f = 1.0MHz	--	930	--	pF
Output Capacitance	C_{oss}		--	85	--	
Reverse Transfer Capacitance	C_{rss}		--	35	--	
Total Gate Charge	Q_g	V_{DD} = -30V, I_D = -4A, V_{GS} = -10V	--	16	--	nC
Gate-Source Charge	Q_{gs}		--	2.5	--	
Gate-Drain Charge	Q_{gd}		--	3.2	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = -30V, I_D = -4A, R_G = 3Ω	--	8	--	ns
Turn-on Rise Time	t_r		--	3.8	--	
Turn-off Delay Time	$t_{d(off)}$		--	31.5	--	
Turn-off Fall Time	t_f		--	7.5	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	-4	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = -4A, V_{GS} = 0V	--	--	-1	V

Notes

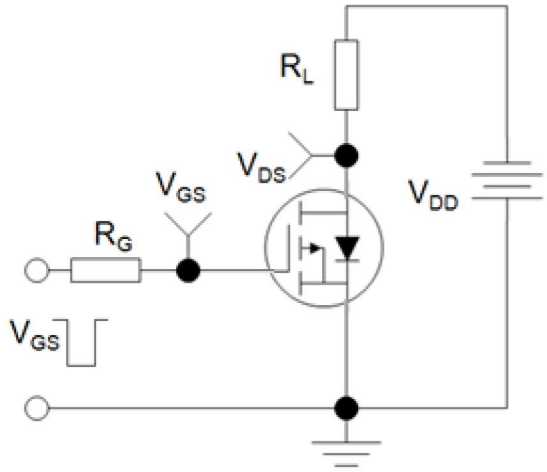
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G

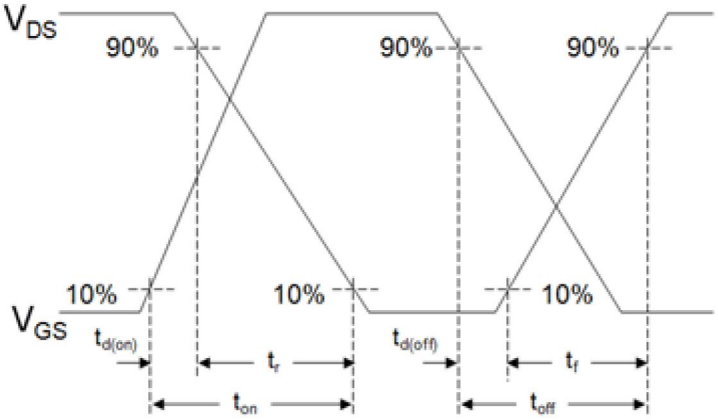
Gate Charge Test Circuit



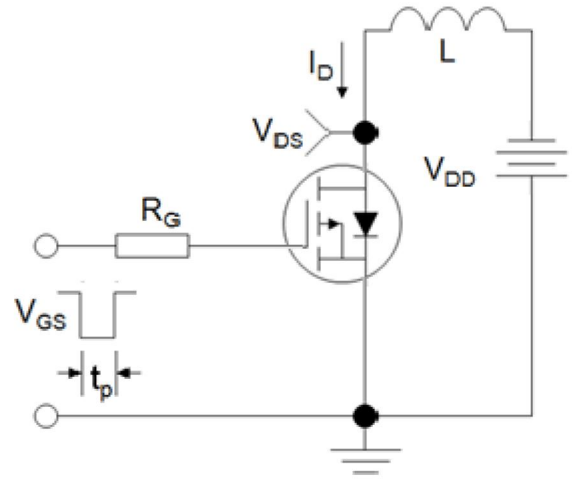


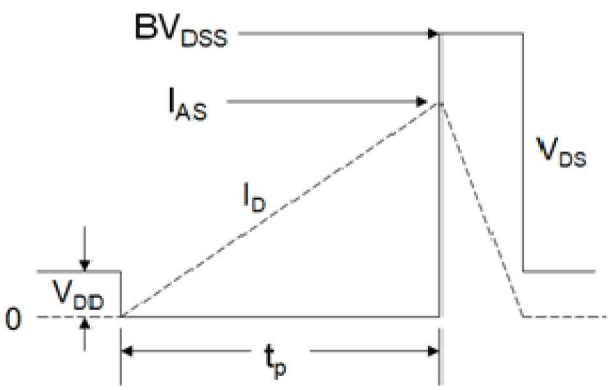
Switch Time Test Circuit





EAS Test Circuit





PMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

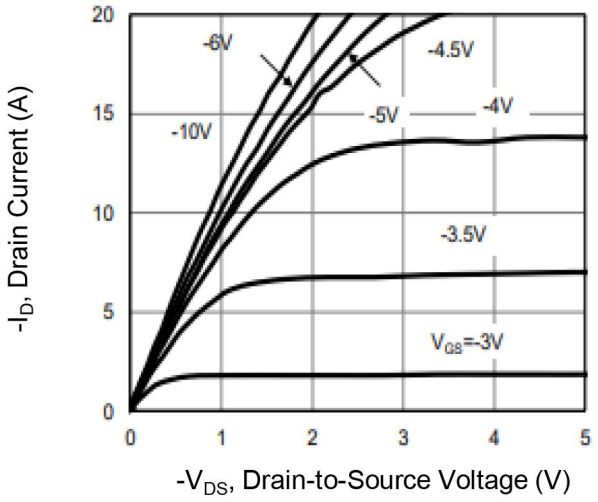


Figure 2. Transfer Characteristics

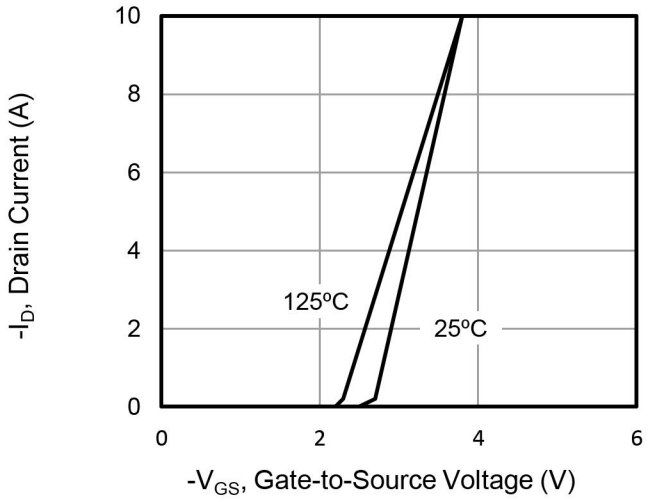


Figure 3. Drain-Source On-Resistance

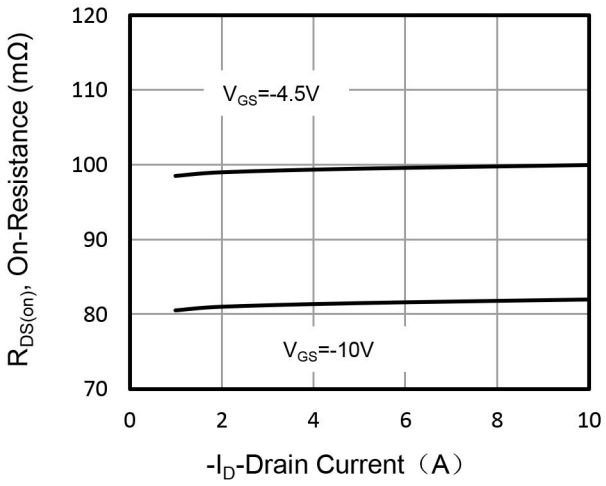


Figure 4. Gate Charge

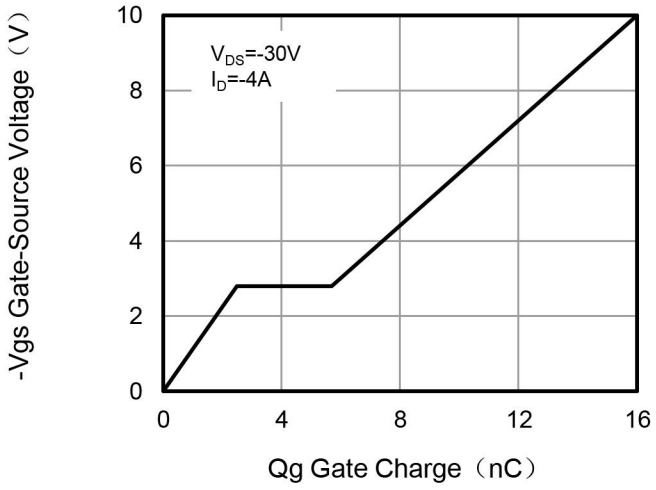


Figure 5. Capacitance

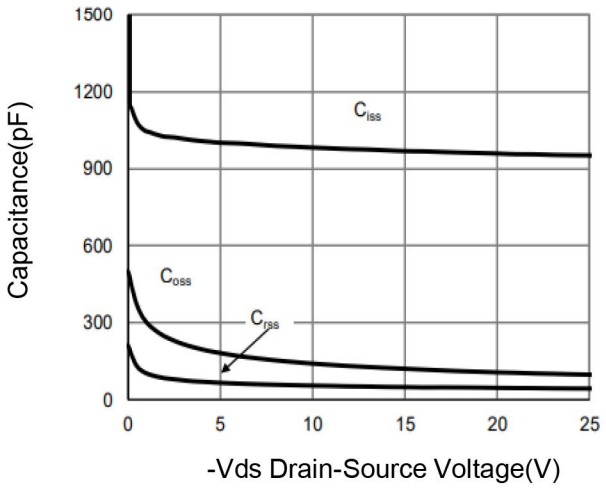
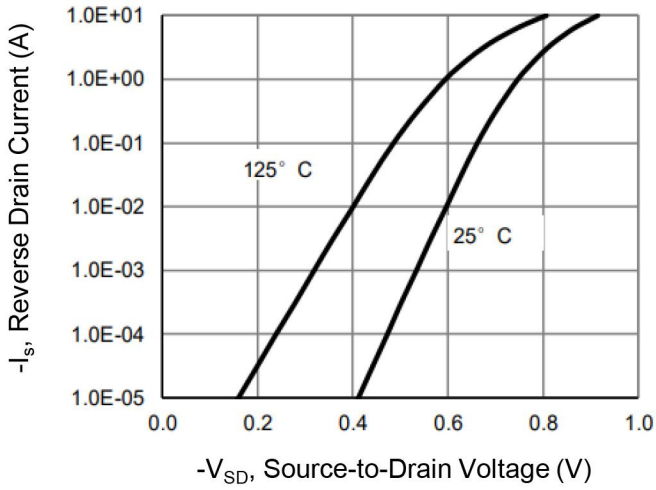


Figure 6. Source-Drain Diode Forward



PMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

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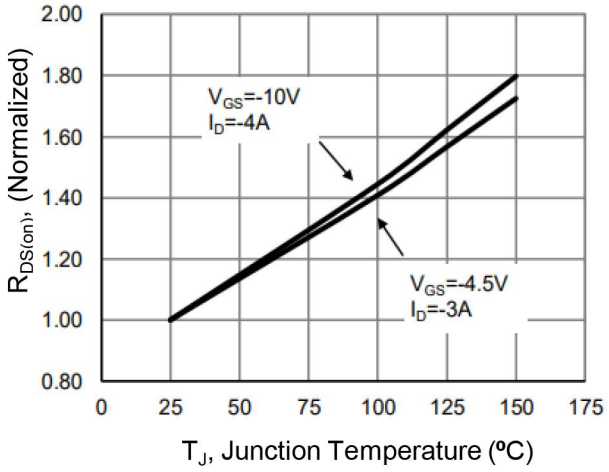

Figure 10. Safe Operation Area

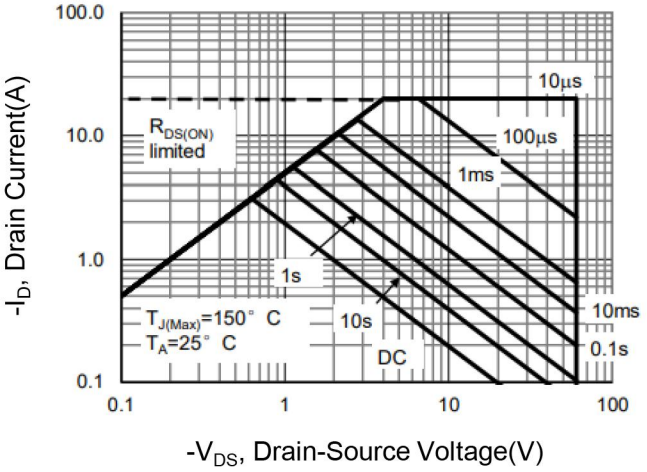

Figure 9. Normalized Maximum Transient Thermal Impedance