

Description

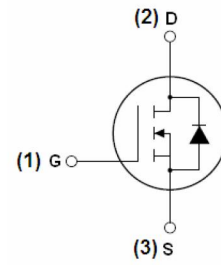
The **VS30N06-T2** uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- $V_{DS} = 60V, I_D = 30A$
 $R_{DS(ON)} < 27m\Omega @ V_{GS} = 10V$
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VS30N06-T2	VS30N06-T2	TO-252-2L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	30	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D (100^\circ C)$	20	A
Pulsed Drain Current	I_{DM}	74	A
Maximum Power Dissipation	P_D	50	W
Derating factor		0.33	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	144	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	3	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

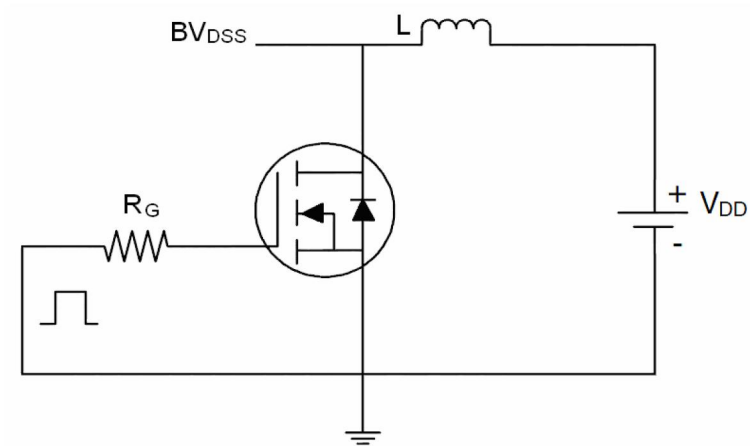
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1.4	1.8	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	23	27	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =20A	-	30	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{iss}	V _{DS} =30V,V _{GS} =0V, F=1.0MHz	-	1900	-	PF
Output Capacitance	C _{oss}		-	130	-	PF
Reverse Transfer Capacitance	C _{rss}		-	95	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DS} =30V, R _L =1.5Ω V _{GS} =10V,R _G =3Ω	-	5	-	nS
Turn-on Rise Time	t _r		-	2.6	-	nS
Turn-Off Delay Time	t _{d(off)}		-	16.1	-	nS
Turn-Off Fall Time	t _f		-	2.3	-	nS
Total Gate Charge	Q _g	V _{DS} =30V,I _D =20A, V _{GS} =10V	-	30		nC
Gate-Source Charge	Q _{gs}		-	4.5		nC
Gate-Drain Charge	Q _{gd}		-	7.5		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _S =30A	-		1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	30	A
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF =20A	-	35	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs ^(Note3)	-	53	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

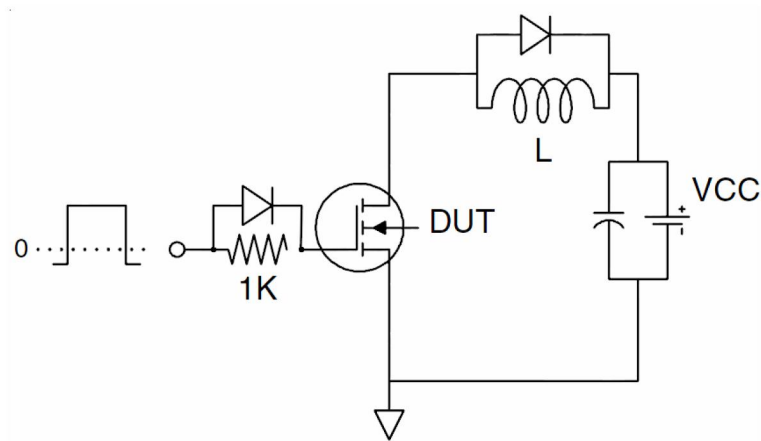
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}$, $V_{DD}=30V$, $V_G=10V$, $L=0.5mH$, $R_g=25\Omega$

Test Circuit

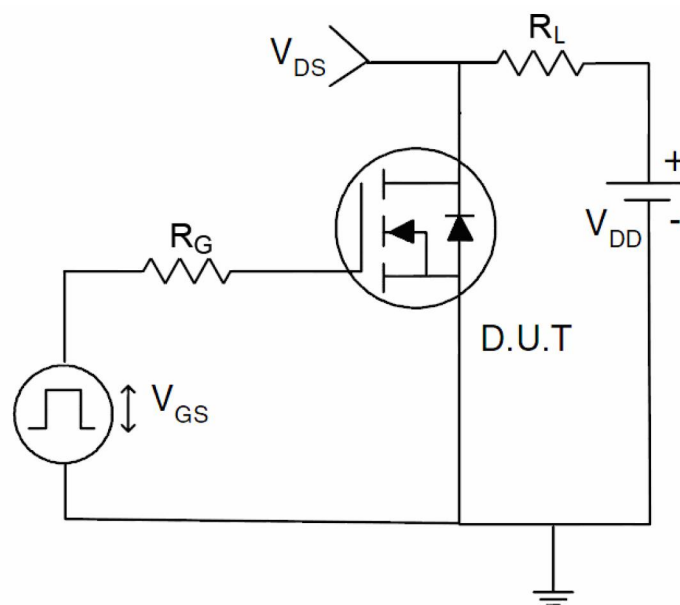
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

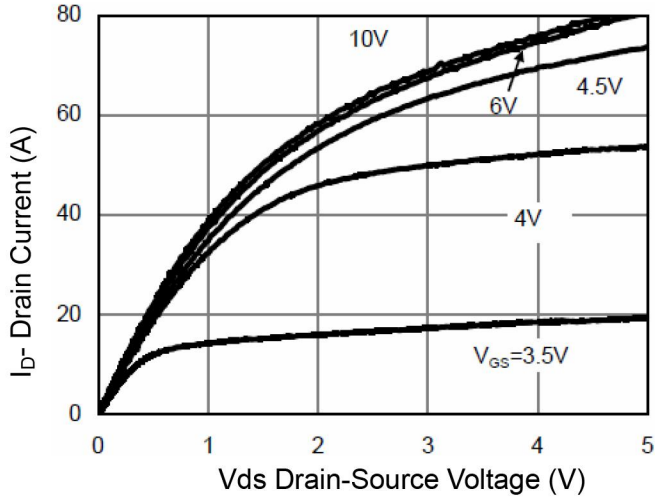


Figure 1 Output Characteristics

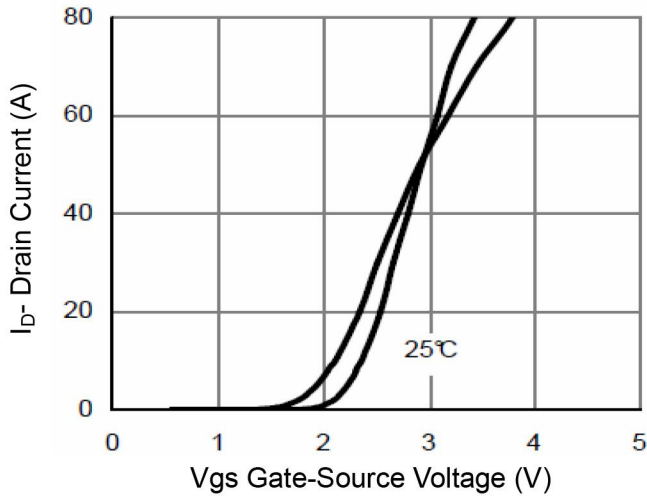


Figure 2 Transfer Characteristics

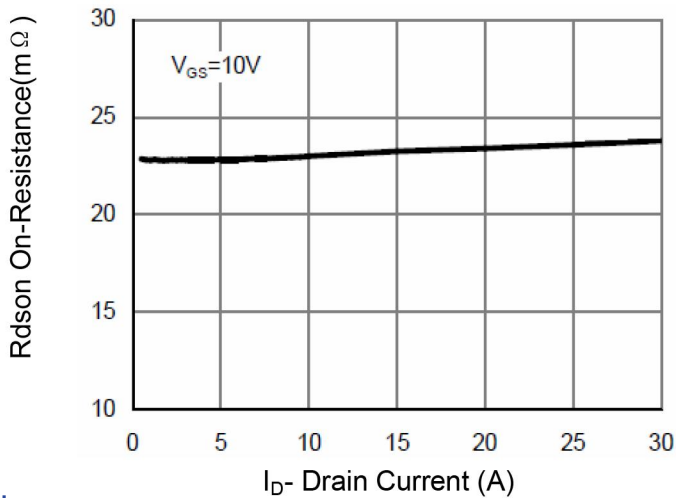


Figure 3 $R_{DS(on)}$ - Drain Current

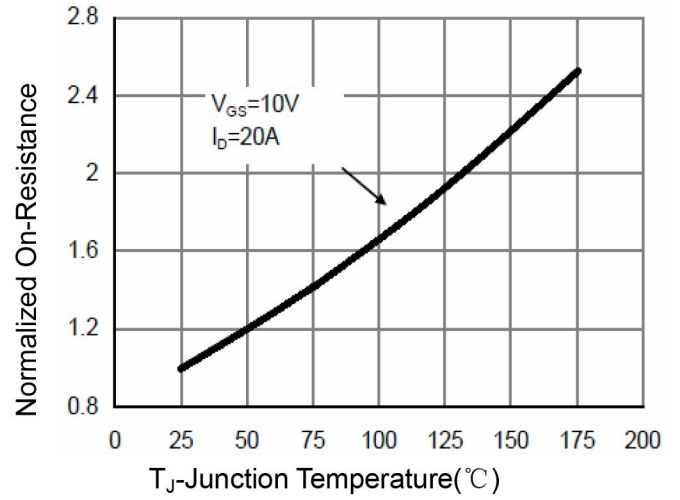


Figure 4 $R_{DS(on)}$ -Junction Temperature

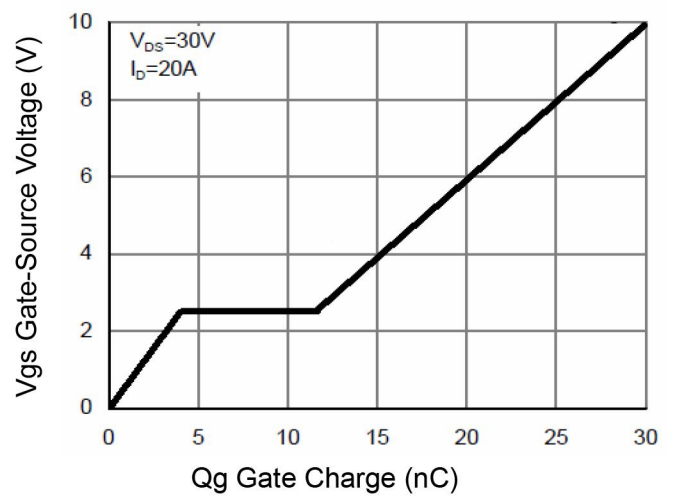


Figure 5 Gate Charge

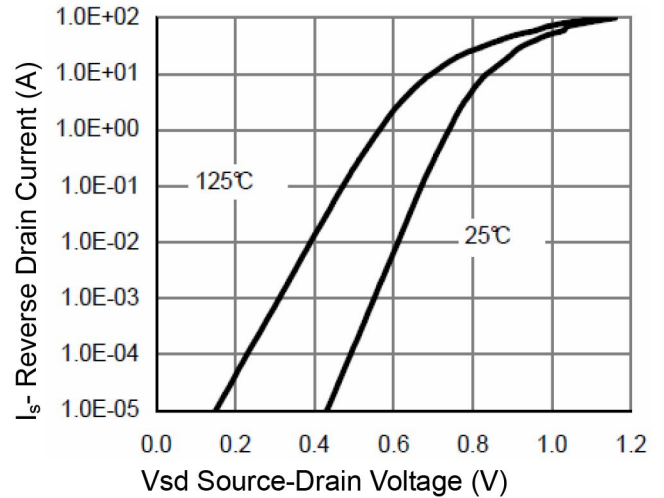


Figure 6 Source- Drain Diode Forward

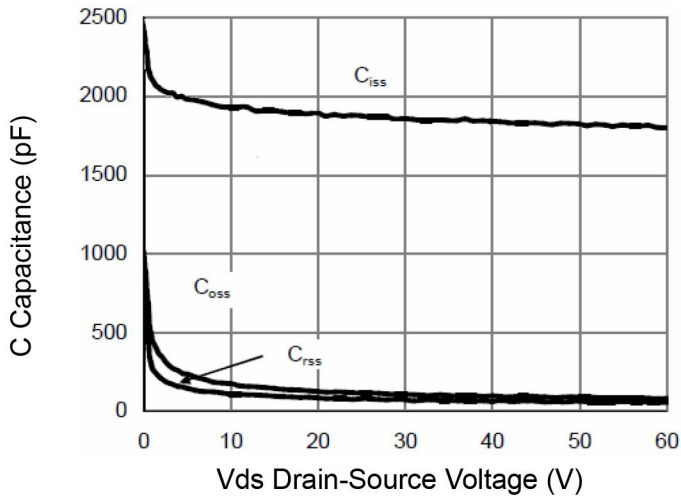


Figure 7 Capacitance vs Vds

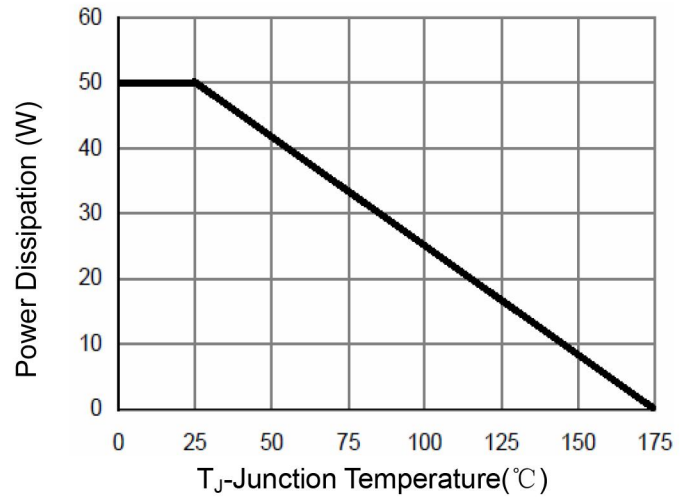


Figure 9 Power De-rating

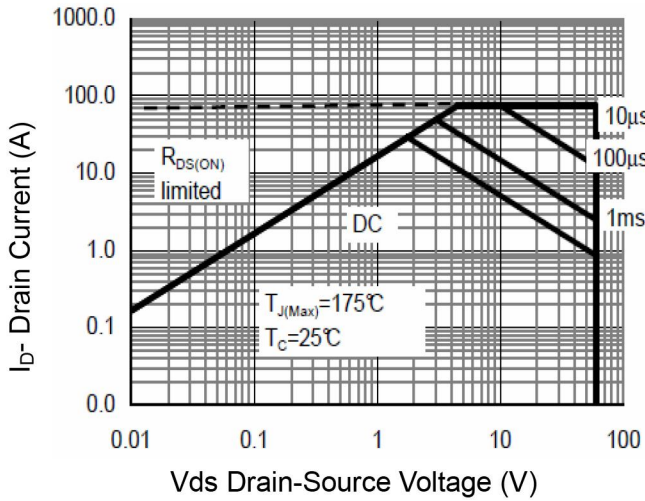


Figure 8 Safe Operation Area

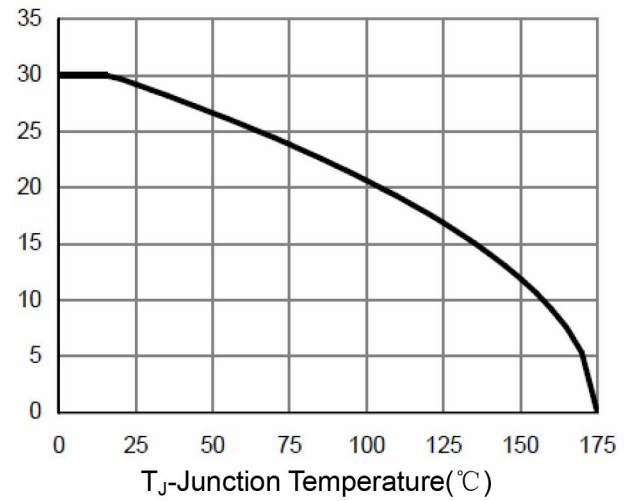
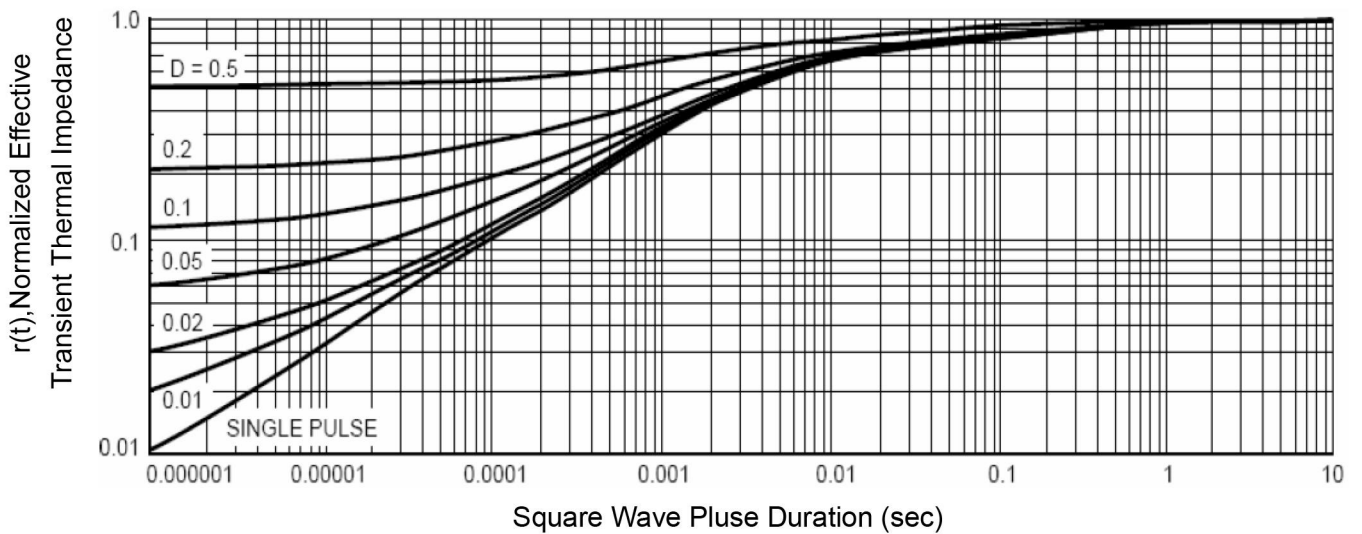

Figure 10 $V_{GS(th)}$ vs Junction Temperature


Figure 11 Normalized Maximum Transient Thermal Impedance