

## Description

The vs13n04-s8 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

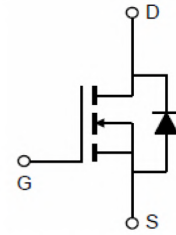
## General Features

$V_{DSS}$	$R_{DS(ON)}$ @ 4.5V (typ)	$R_{DS(ON)}$ @ 10V (typ)	$I_D$
40V	13m $\Omega$	10m $\Omega$	13A

- High density cell design for ultra low  $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- RoHS Compliant

## Application

- Load switching
- Hard switched and high frequency circuits
- Quick charge application



Schematic diagram



## Ordering Information

Part Number	Marking	Case	Packaging
<b>VS13N04-S8</b>	<b>VS13N04-S8</b>	SOP-8	

## Absolute Maximum Ratings ( $T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	13	A
Drain Current-Continuous( $T_C=100^{\circ}\text{C}$ )	$I_D(100^{\circ}\text{C})$	8.2	A
Pulsed Drain Current	$I_{DM}$	52	A
Maximum Power Dissipation	$P_D$	3	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^{\circ}\text{C}$

## Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	41.67	$^{\circ}\text{C/W}$
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# Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

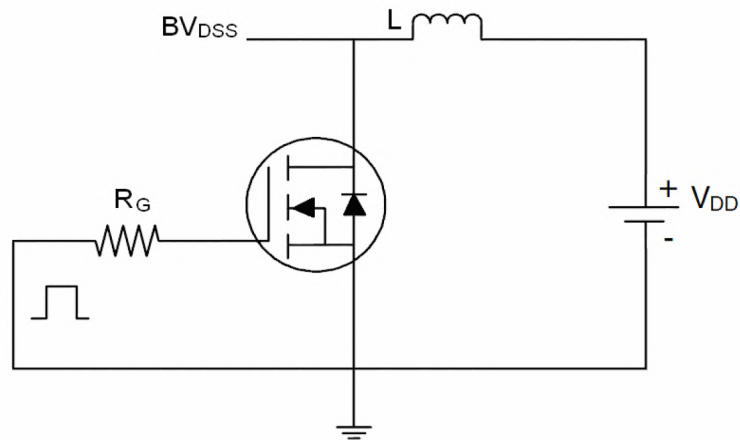
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	40	46	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.6	2.3	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =6.5A	-	10	12	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =6.5A	-	13	16	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =6.5A	-	75	-	S
Dynamic Characteristics <sup>(Note4)</sup>						
Input Capacitance	C <sub>Iss</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, F=1.0MHz	-	1780	-	PF
Output Capacitance	C <sub>Oss</sub>		-	209	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	160	-	PF
Switching Characteristics <sup>(Note 4)</sup>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =20V, R <sub>L</sub> =2Ω V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω	-	6.4	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	17.2	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	29.6	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	16.8	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =20V, I <sub>D</sub> =6.5A, V <sub>GS</sub> =10V	-	30	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	4.2	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	9.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =13A	-	-	1.0	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>S</sub>		-	-	13	A
Reverse Recovery Time	t <sub>rr</sub>	TJ = 25°C, IF = 6.5A	-	29	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100A/μs <sup>(Note3)</sup>	-	26	-	nC

## Notes:

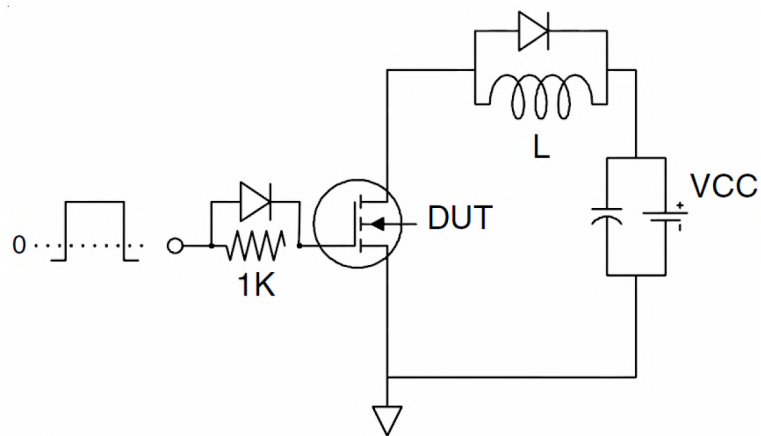
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

## Test circuit

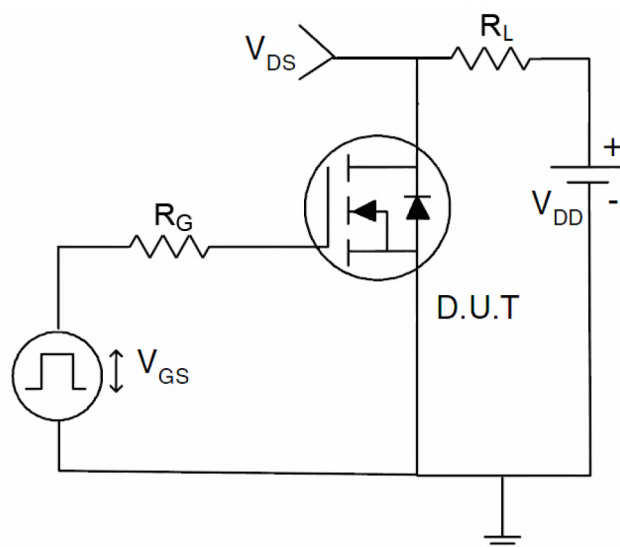
### 1) $E_{AS}$ Test Circuit



### 2) Gate Charge Test Circuit



### 3) Switch Time Test Circuit



## Typical Electrical and Thermal Characteristics (Curves)

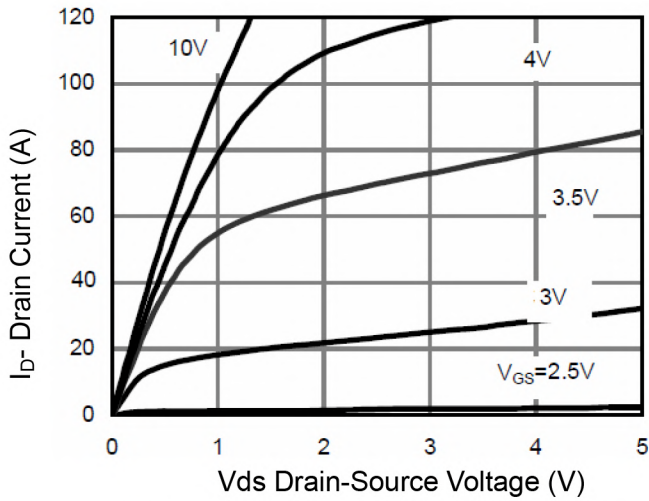


Figure 1 Output Characteristics

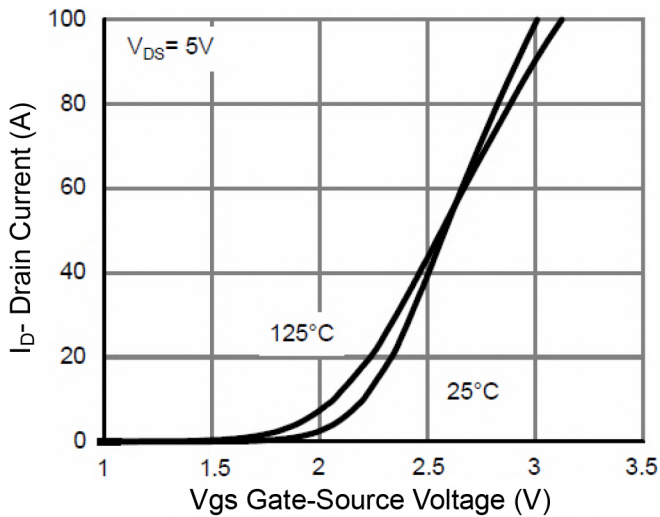


Figure 2 Transfer Characteristics

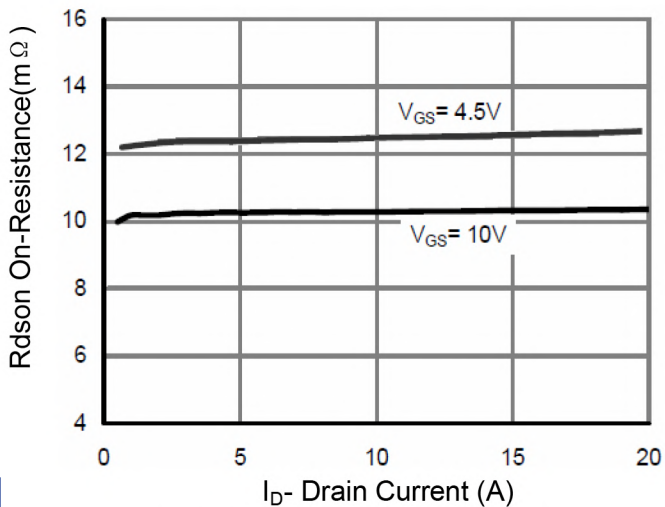


Figure 3  $R_{DS(on)}$ - Drain Current

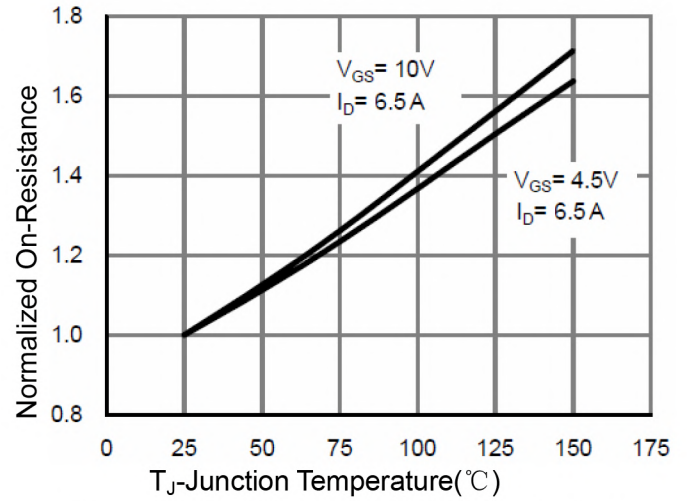


Figure 4  $R_{DS(on)}$ -Junction Temperature

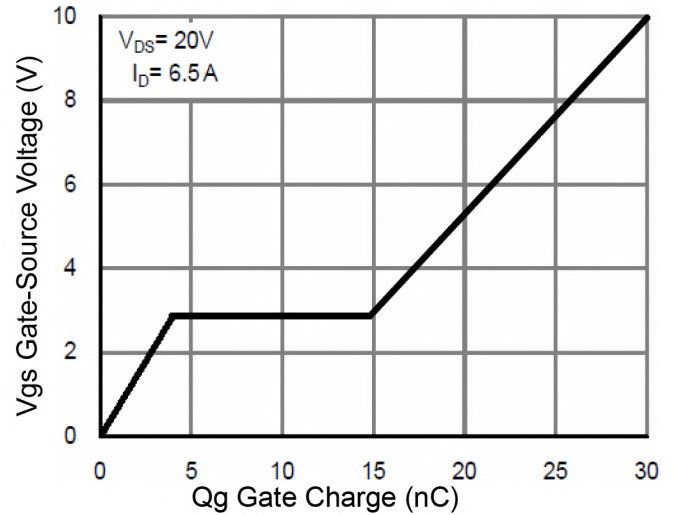


Figure 5 Gate Charge

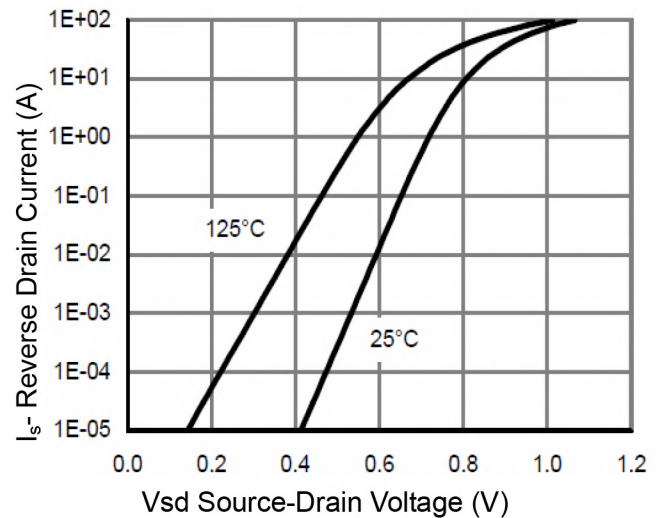


Figure 6 Source- Drain Diode Forward

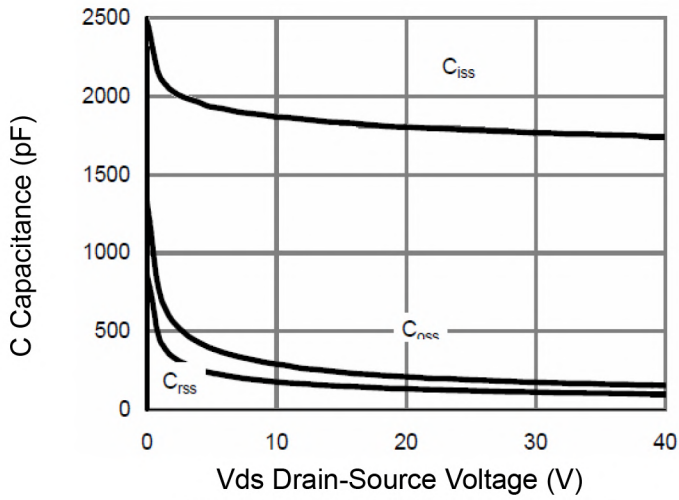


Figure 7 Capacitance vs Vds

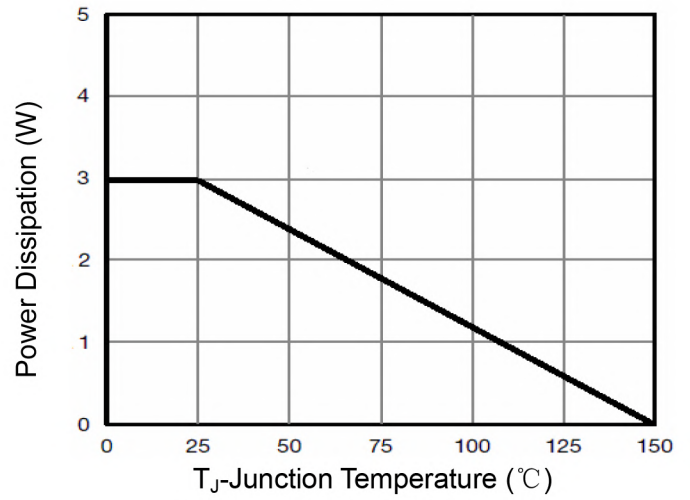


Figure 9 Power De-rating

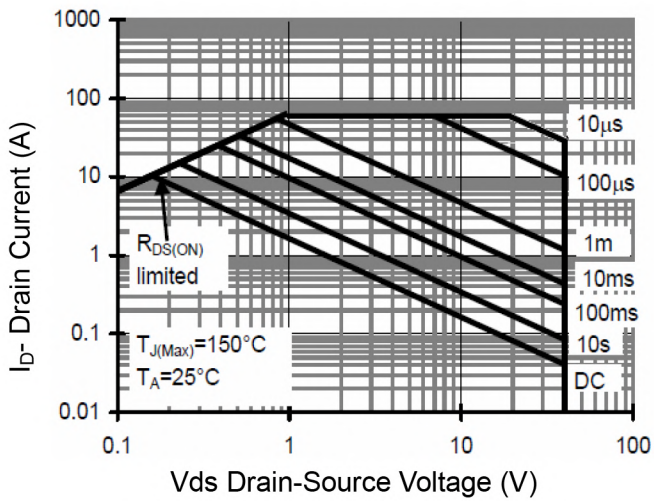


Figure 8 Safe Operation Area

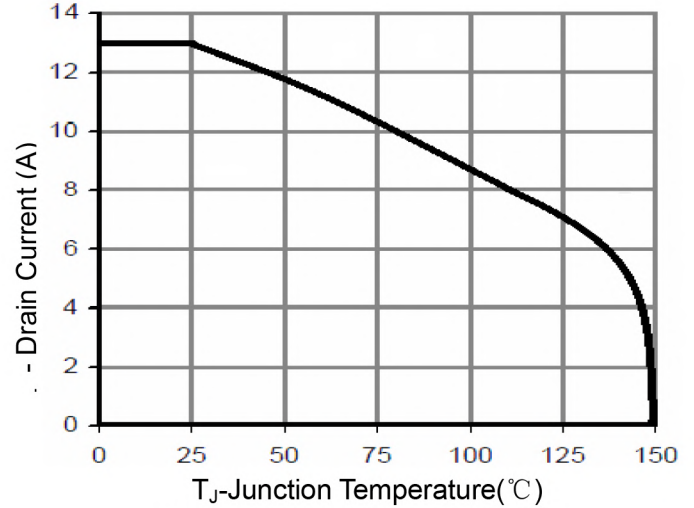


Figure 10 Current De-rating

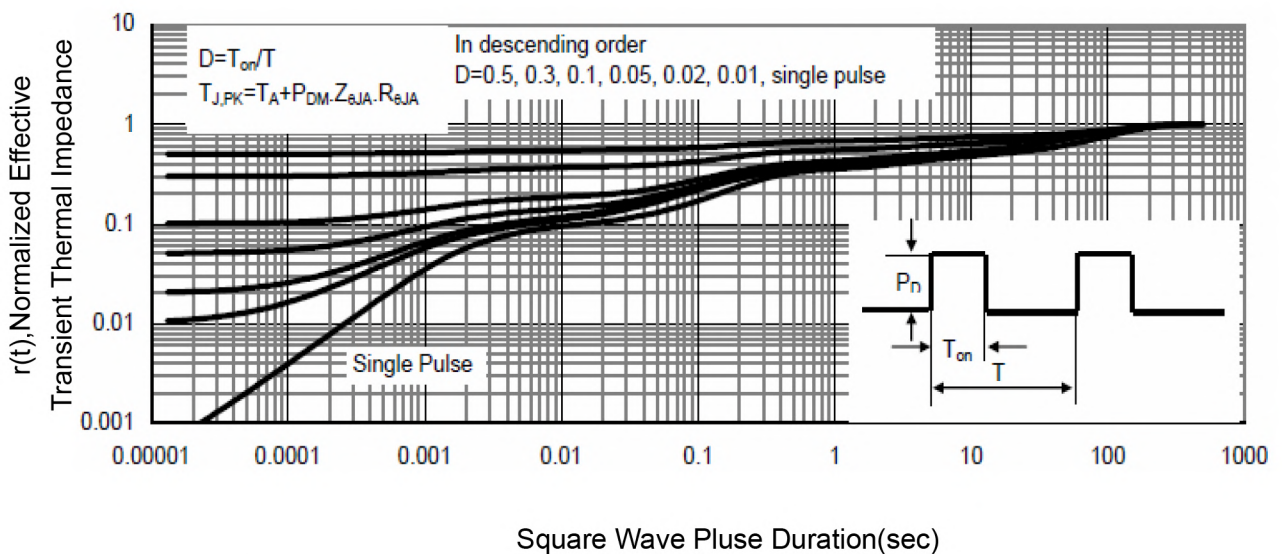


Figure 11 Normalized Maximum Transient Thermal Impedance