

Description

The VSM150N03 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

• $V_{DS} = 30V, I_{D} = 150A$ $R_{DS(ON)} < 3.0 \text{ m}\Omega @ V_{GS} = 10V$

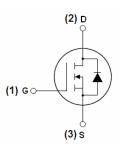
 $R_{DS(ON)}$ <4.0m Ω @ V_{GS} =4.5V

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply





TO-220C

Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM150N03-TC	VSM150N03	TO-220C	-	-	-

Absolute Maximum Ratings (T_C=25 ℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	30	V	
Gate-Source Voltage	Vgs	±20	V	
Drain Current-Continuous	I _D	150	А	
Drain Current-Continuous(T _C =100 °C)	I _D (100℃)	105	А	
Pulsed Drain Current	I _{DM}	600	А	
Maximum Power Dissipation	P _D	130	W	
Derating factor		0.87	W/℃	
Single pulse avalanche energy (Note 5)	E _{AS}	1700	mJ	
Operating Junction and Storage Temperature Range	T_{J} , T_{STG}	-55 To 175	℃	





Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	Rejc	1.15	°C/W
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Electrical Characteristics (T_C=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	30	35	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1.2	1.7	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	2.3	3.0	m0
Diam-Source On-State Resistance		V _{GS} =4.5V, I _D =10A		3.2	4.0	· mΩ
Forward Transconductance	g _{FS}	V _{DS} =10V,I _D =20A	32	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{lss}	\/ -15\/\/ -0\/	-	5000	-	PF
Output Capacitance	Coss	V_{DS} =15V, V_{GS} =0V, F=1.0MHz	-	1135	-	PF
Reverse Transfer Capacitance	C _{rss}	F-1.UIVITZ	-	563	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}		-	26	-	nS
Turn-on Rise Time	t _r	V_{DD} =15V, I_D =2A, R_L =15 Ω	-	24	-	nS
Turn-Off Delay Time	$t_{d(off)}$	V_{GS} =10V, R_{G} =2.5 Ω	-	91	-	nS
Turn-Off Fall Time	t _f		-	39	-	nS
Total Gate Charge	Q_g	V -45V/1 -20A	-	38		nC
Gate-Source Charge	Q _{gs}	$V_{DS}=15V,I_{D}=30A,$ $V_{GS}=10V$	-	9		nC
Gate-Drain Charge	Q _{gd}	V _{GS} -10V	-	13		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =150A	-		1.2	V
Diode Forward Current (Note 2)	Is		-	-	150	Α
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF = 20A	-	42	-	nS
Reverse Recovery Charge	Qrr	di/dt = 100A/μs ^(Note3)	-	39	-	nC
Forward Turn-On Time	ton	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- **3.** Pulse Test: Pulse Width $\leq 300 \mu s$, Duty Cycle $\leq 2\%$.
- **4.** Guaranteed by design, not subject to production
- **5.** E_{AS} condition : Tj=25 $^{\circ}$ C,V_{DD}=20V,V_G=10V,L=1mH,Rg=25 Ω , I_{AS}=58.5A

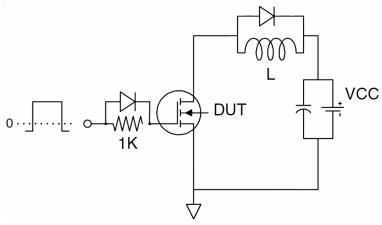


Test circuit

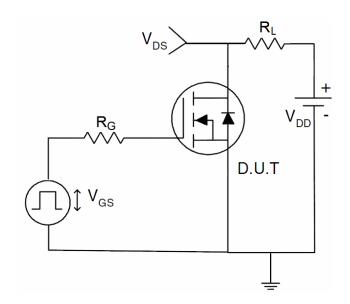
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit





Typical Electrical and Thermal Characteristics (Curves)

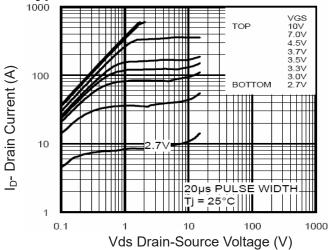


Figure 1 Output Characteristics

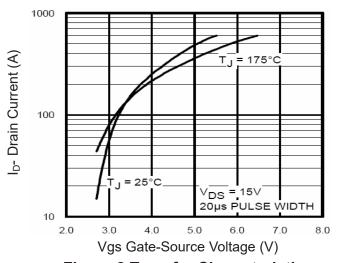


Figure 2 Transfer Characteristics

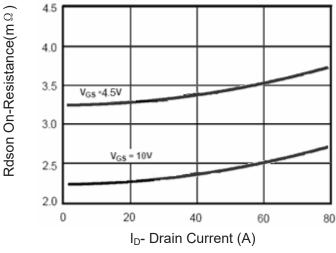


Figure 3 Rdson-Drain Current

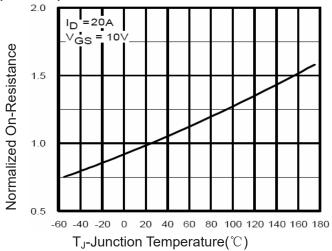


Figure 4 Rdson-JunctionTemperature

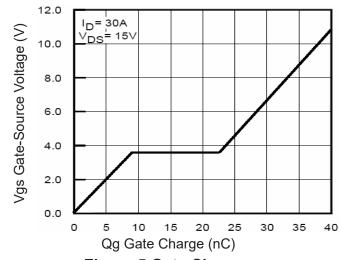


Figure 5 Gate Charge

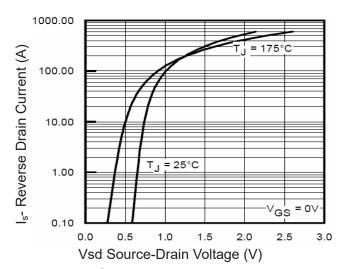
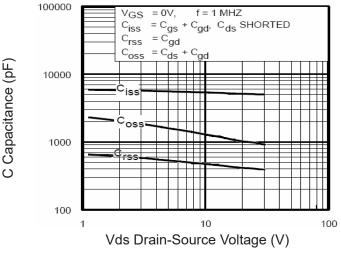
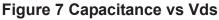


Figure 6 Source- Drain Diode Forward







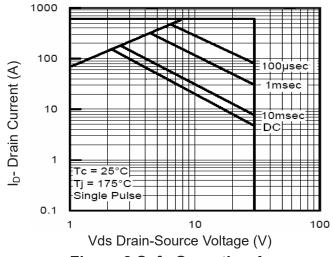


Figure 8 Safe Operation Area

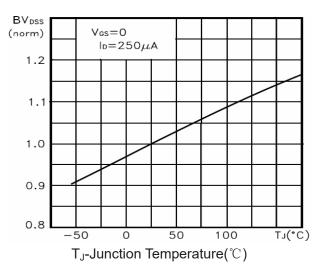


Figure 9 BV_{DSS} vs Junction Temperature

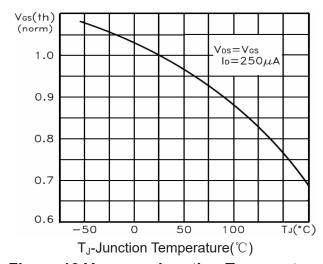


Figure 10 V_{GS(th)} vs Junction Temperature

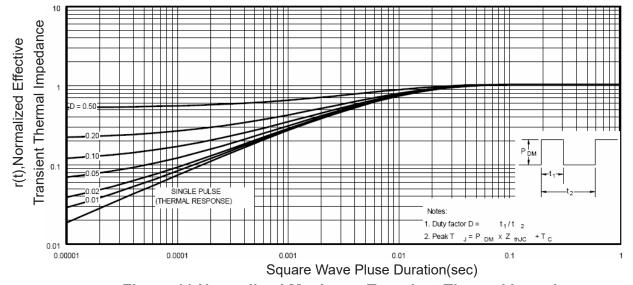


Figure 11 Normalized Maximum Transient Thermal Impedance