Description

TheVSM210N08uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in automotive applications and a wide variety of other applications.

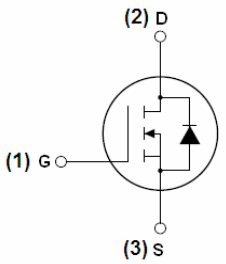
General Features

- V_{DSS} =85V,I_D =210A (Note5)
  $R_{DS(ON)}$ < 3.8mΩ @ V_{GS}=10V
- Good stability and uniformity with high E_{AS}
- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

- Automotive applications
- Hard switched and high frequency circuits
- Uninterruptible power supply

TO-220C



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM210N08-TC	VSM210N08	TO-220C	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	85	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	210 (Note5)	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	150	A
Pulsed Drain Current	I_{DM}	850	A
Maximum Power Dissipation	P_D	310	W
Derating factor		2.07	W/℃

Single pulse avalanche energy (Note 3)	E_{AS}	2200	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 1)	$R_{\theta JC}$	0.48	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

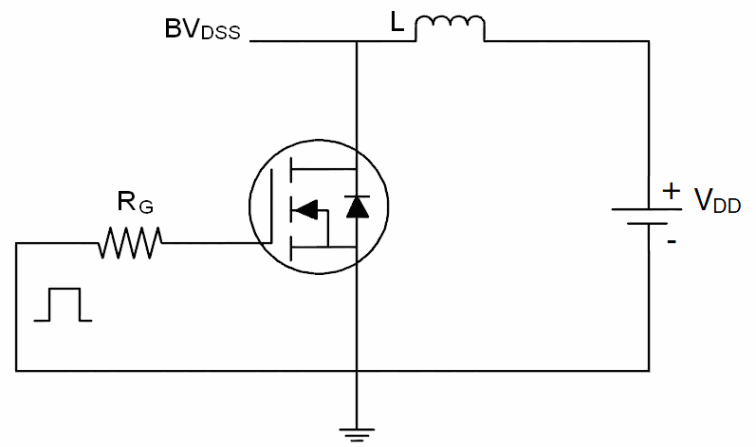
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	85	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=85V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±200	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=40A	-	3.2	3.8	mΩ
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=20A	35	-	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz	-	11000	-	PF
Output Capacitance	C_{oss}		-	914	-	PF
Reverse Transfer Capacitance	C_{rss}		-	695	-	PF
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=38V,I_D=40A V_{GS}=10V,R_{GEN}=1.2Ω(Note2)	-	23	-	nS
Turn-on Rise Time	t_r		-	190	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	130	-	nS
Turn-Off Fall Time	t_f		-	120	-	nS
Total Gate Charge	Q_g	V_{DS}=60V,I_D=40A, V_{GS}=10V(Note2)	-	250	-	nC
Gate-Source Charge	Q_{gs}		-	48	-	nC
Gate-Drain Charge	Q_{gd}		-	98	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=40A	-	-	1.2	V
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 40A di/dt = 100A/μs(Note2)	-	63	-	nS
Reverse Recovery Charge	Qrr		-	98	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

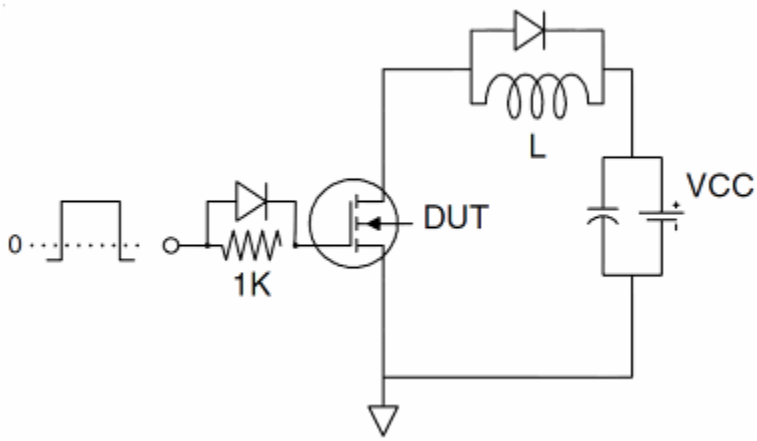
1. Surface Mounted on FR4 Board, t ≤ 10 sec.
2. Pulse Test: Pulse Width ≤ 400μs, Duty Cycle ≤ 2%.
3. EAS condition：Tj=25℃,V_{DD}=42.5V,V_G=10V,L=0.5mH,Rg=25Ω,I_{AS}=37A
4. ISD≤125A, di/dt≤260A/μs, VDD≤V(BR)DSS，TJ ≤175°C
5. Package limitation current is 190A.

Test Circuit

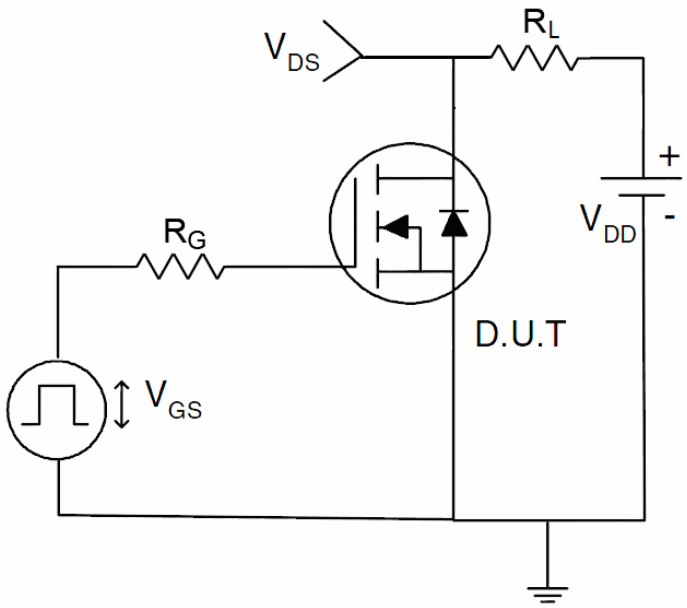
1）E_{AS} test Circuit



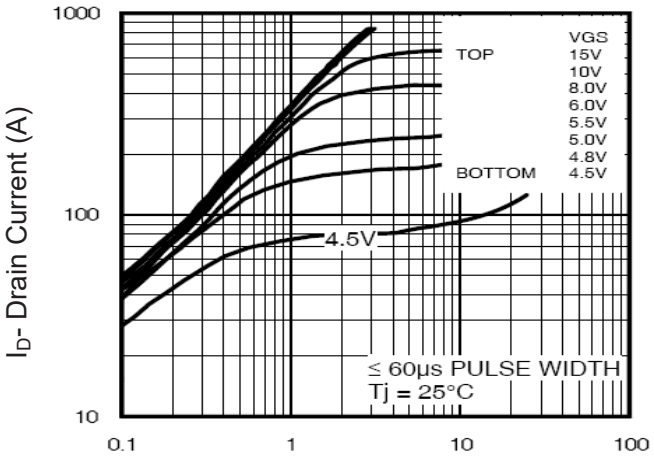
2）Gate charge test Circuit



3）Switch Time Test Circuit

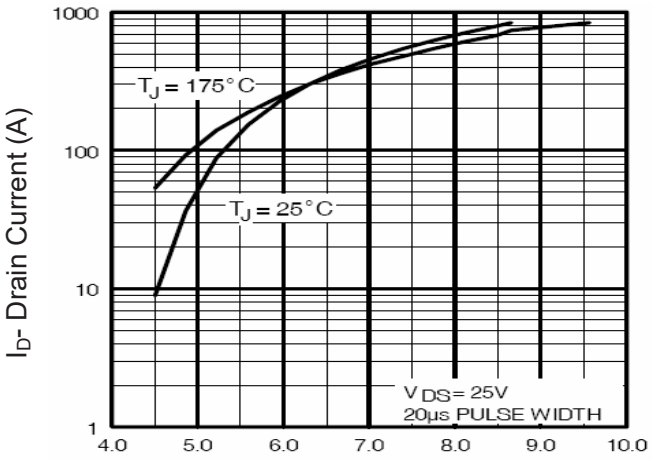


Typical Electrical and Thermal Characteristics



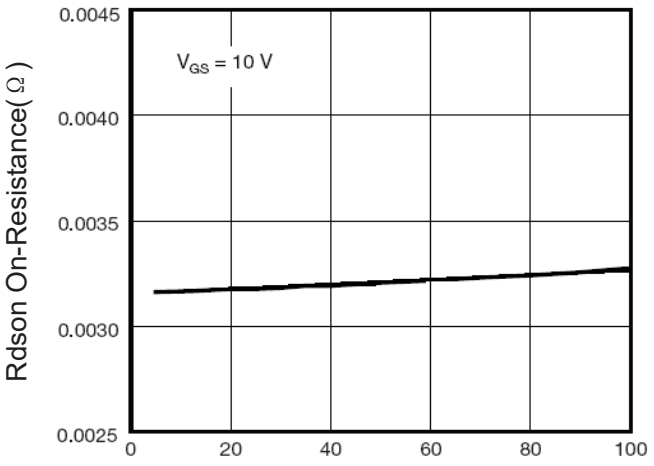
Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



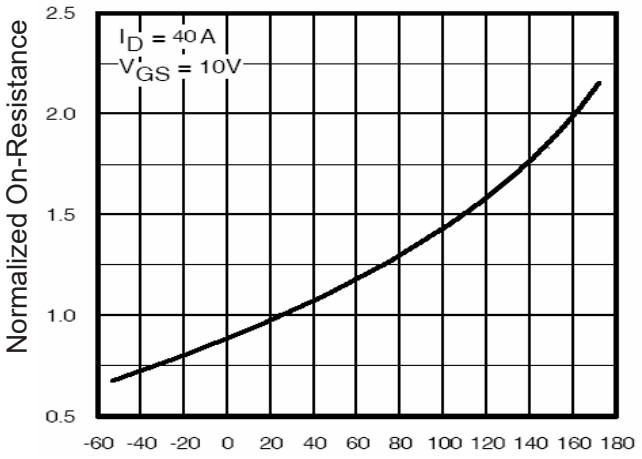
Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



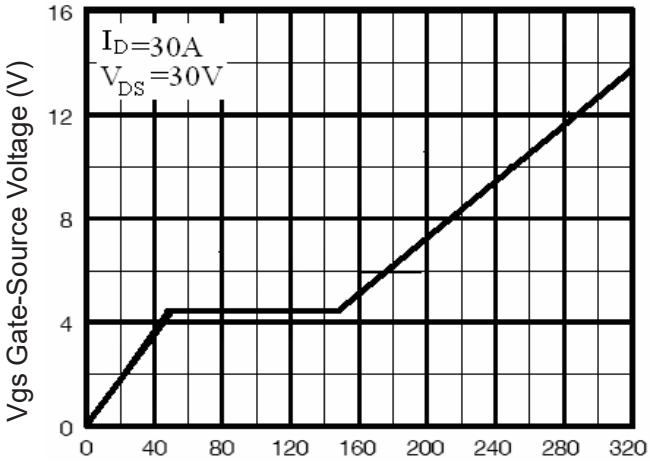
I_D- Drain Current (A)

Figure 3 Rdson- Drain Current



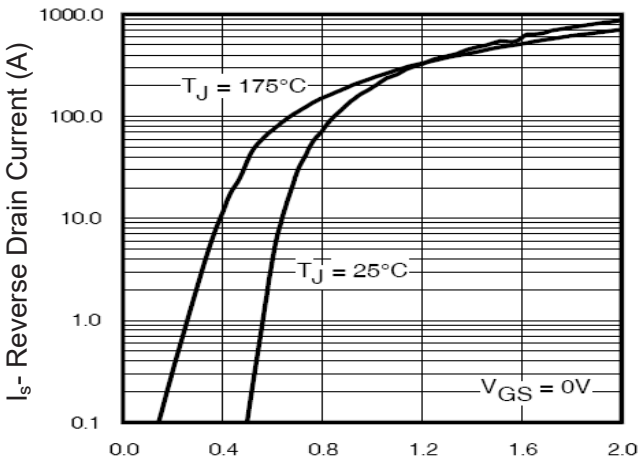
T_J-Junction Temperature(℃)

Figure 4 Rdson-JunctionTemperature



Qg Gate Charge (nC)

Figure 5 Gate Charge



Vsd Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward

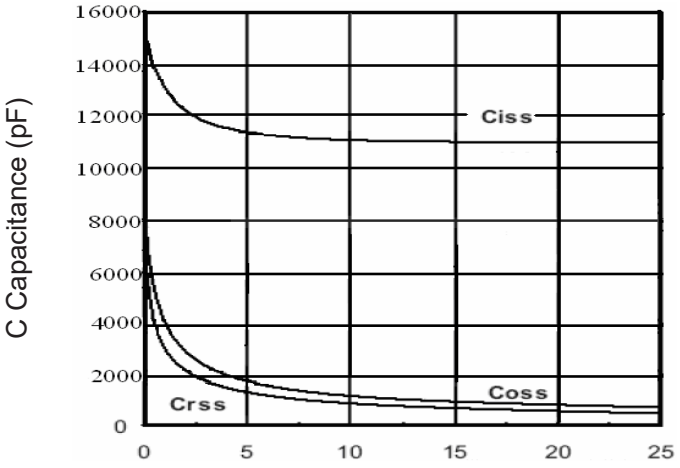


Figure 7 Capacitance vs Vds

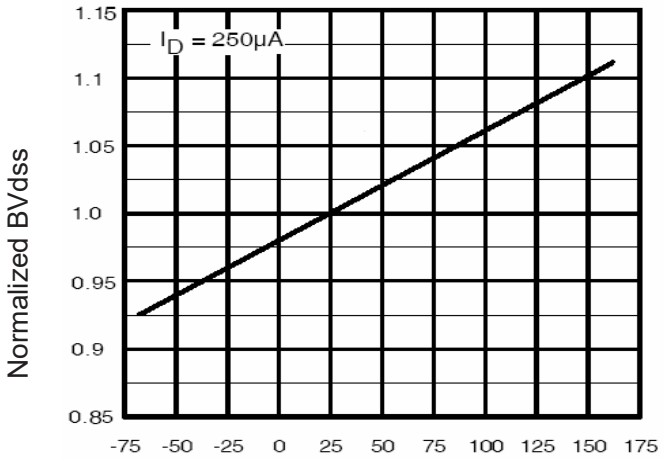


Figure 9 BV_{DSS} vs Junction Temperature

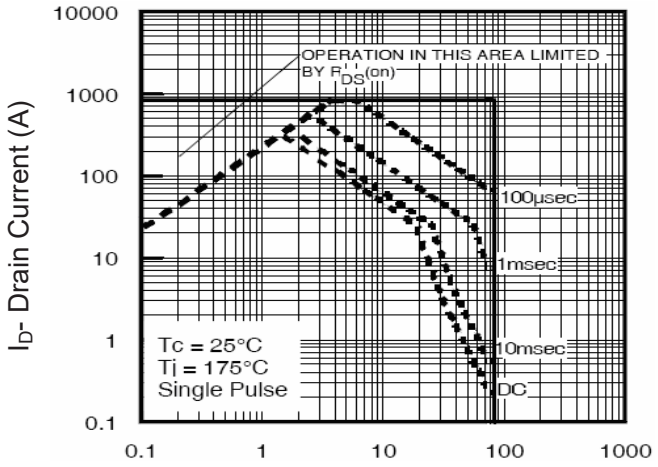


Figure 8 Safe Operation Area

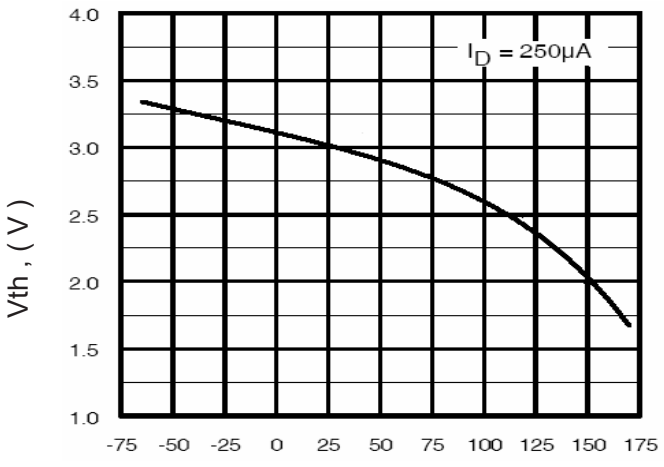


Figure 10 $V_{GS(th)}$ vs Junction Temperature

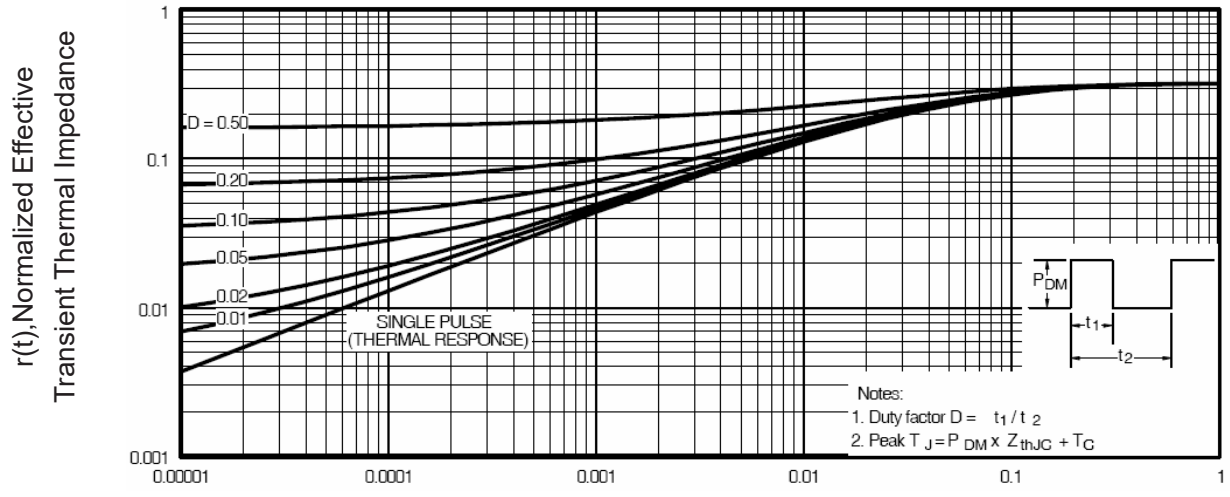


Figure 11 Normalized Maximum Transient Thermal Impedance