

## Description

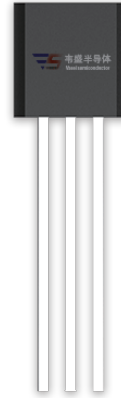
The VSM3N18 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

## General Features

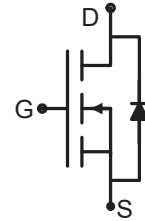
- $V_{DS} = 185V, I_D = 3A$   
 $R_{DS(ON)} < 450m\Omega @ V_{GS}=10V$  (Typ:390m $\Omega$ )  
 $R_{DS(ON)} < 500m\Omega @ V_{GS}=10V$  (Typ:400m $\Omega$ )
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

## Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



TO-92



Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM3N18-T9	VSM3N18	TO-92	-	-	-

## Absolute Maximum Ratings ( $T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	185	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	3	A
Drain Current-Pulsed <sup>(Note 1)</sup>	$I_{DM}$	8	A
Maximum Power Dissipation	$P_D$	3	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^{\circ}C$

## Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	41.7	$^{\circ}C/W$
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## Electrical Characteristics ( $T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	185	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=185V, V_{GS}=0V$	-	-	1	$\mu A$

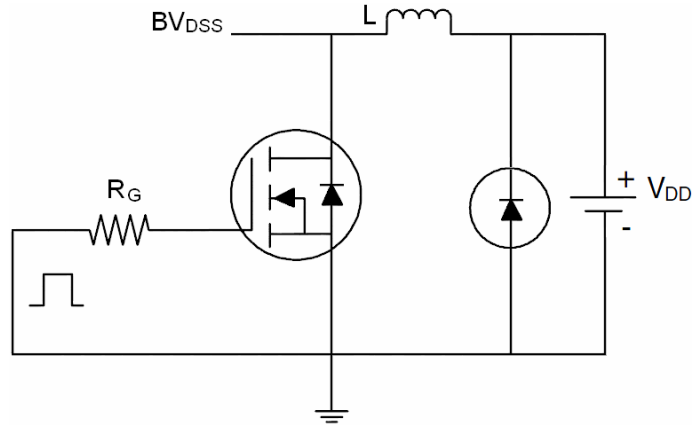
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V,V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> ,I <sub>D</sub> =250μA	1.2	1.8	2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =2A	-	390	450	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =2A	-	400	500	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V,I <sub>D</sub> =2A	-	8	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =50V,V <sub>GS</sub> =0V, F=1.0MHz	-	563	-	PF
Output Capacitance	C <sub>OSS</sub>		-	35	-	PF
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	10	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =100V, R <sub>L</sub> =15Ω V <sub>GS</sub> =10V,R <sub>G</sub> =2.5Ω	-	10	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	12	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	15	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	15	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =100V,I <sub>D</sub> =2A, V <sub>GS</sub> =10V	-	12		nC
Gate-Source Charge	Q <sub>gs</sub>		-	2.5	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	3.8	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =2A	-	-	1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	3	A

## Notes:

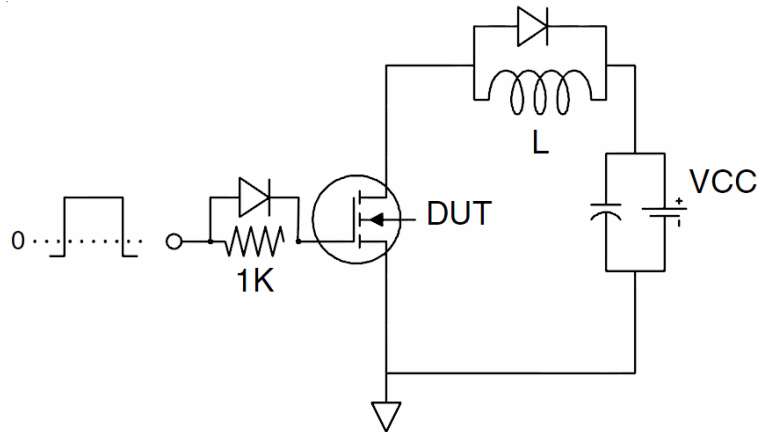
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

## Test Circuit

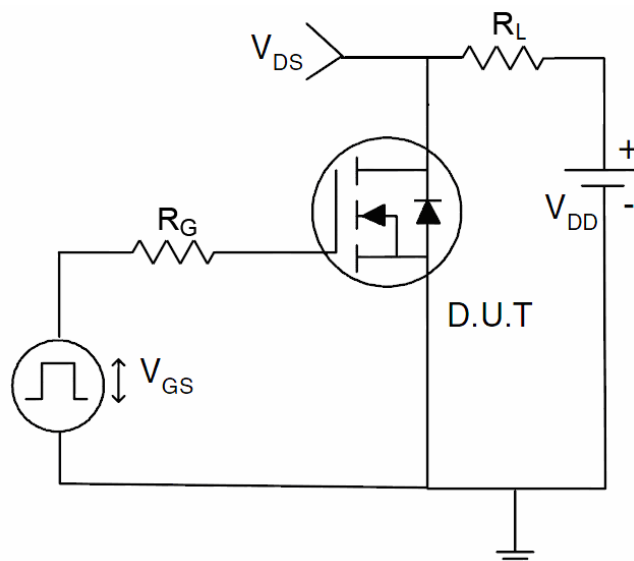
### 1) $E_{AS}$ test circuit



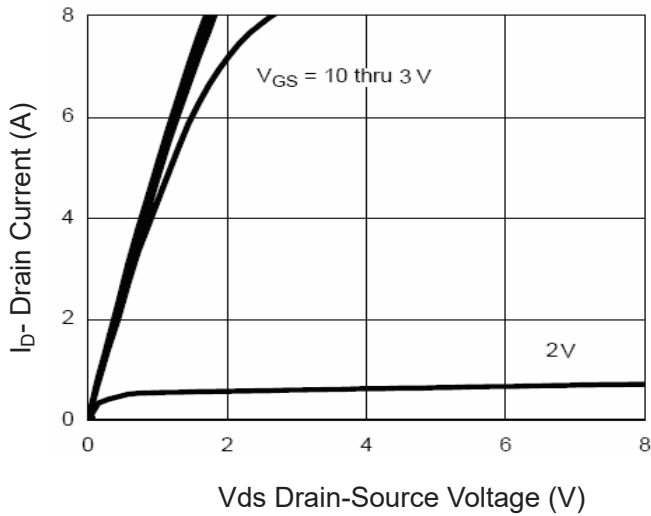
### 2) Gate charge test circuit



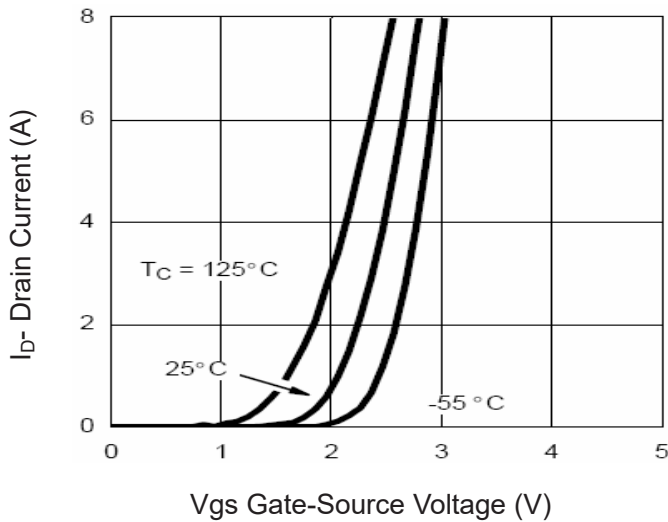
### 3) Switch Time Test Circuit



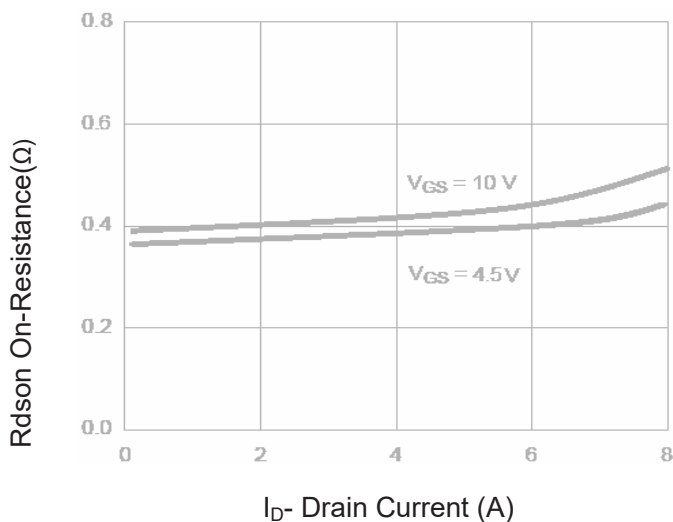
## Typical Electrical and Thermal Characteristics (Curves)



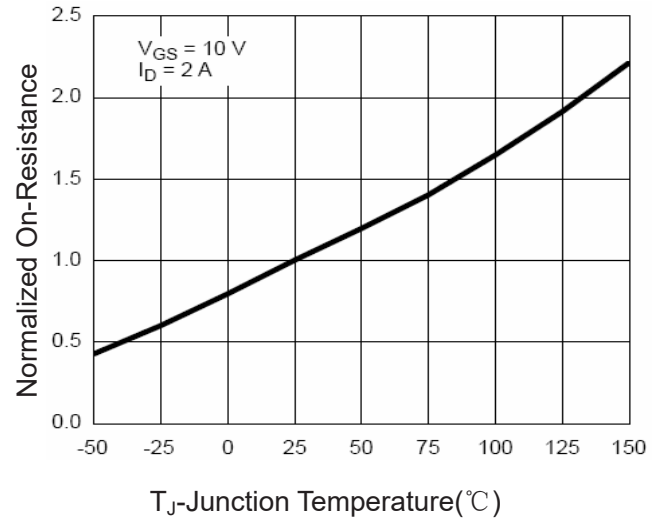
**Figure 1 Output Characteristics**



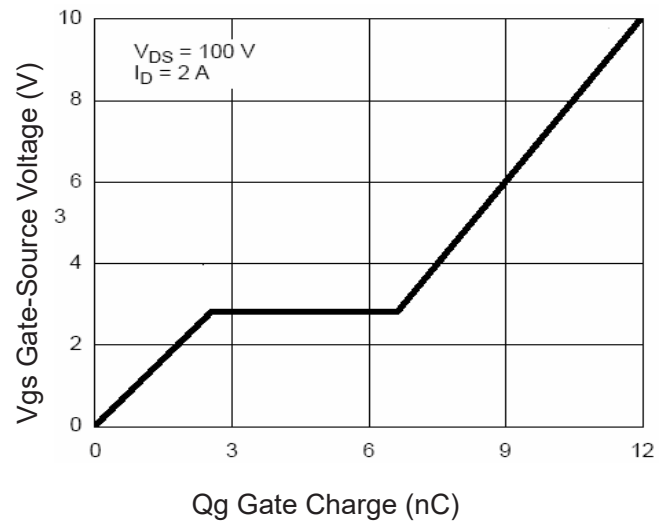
**Figure 2 Transfer Characteristics**



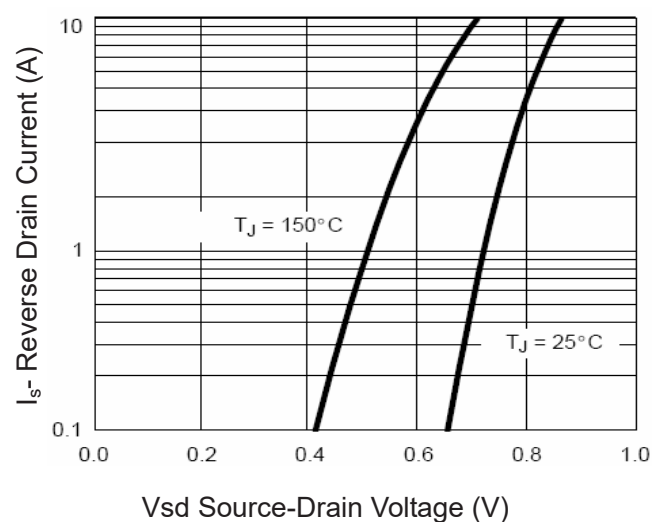
**Figure 3 Rdson- Drain Current**



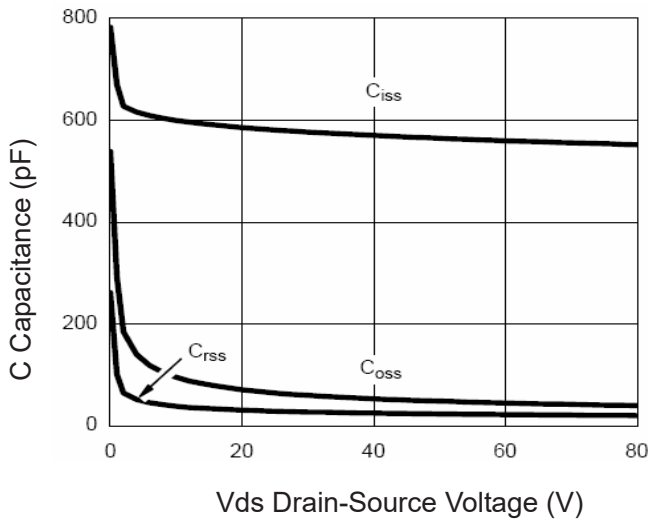
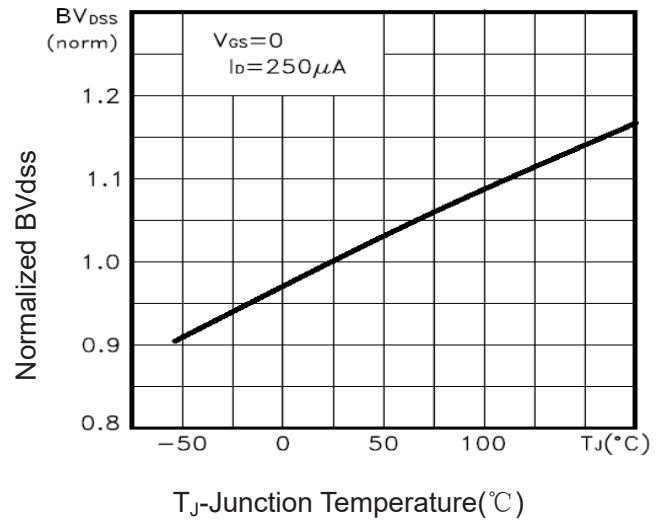
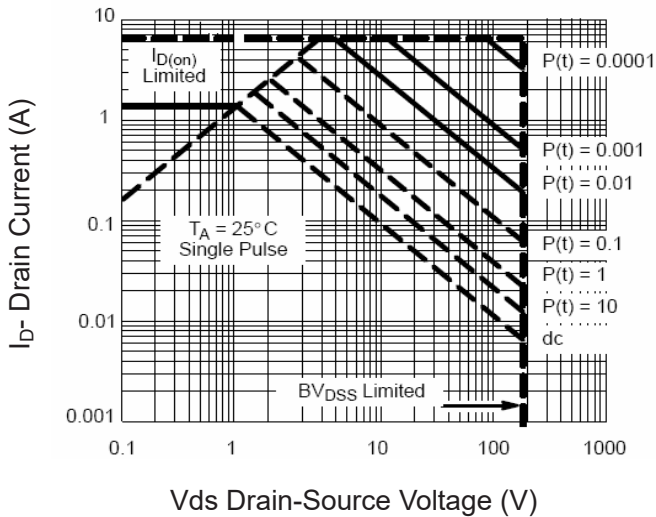
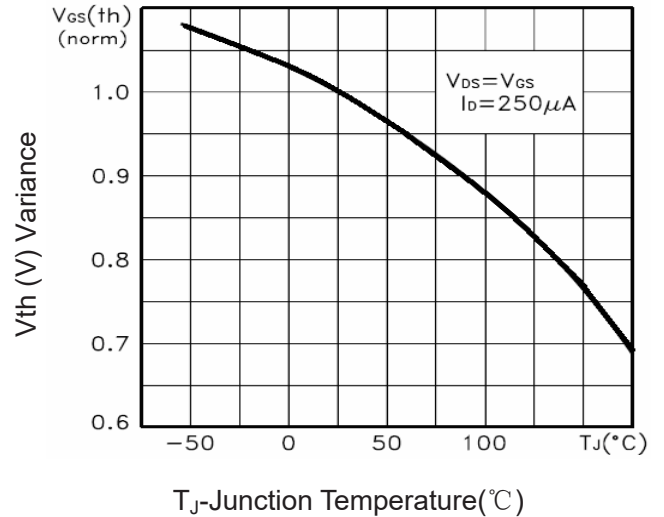
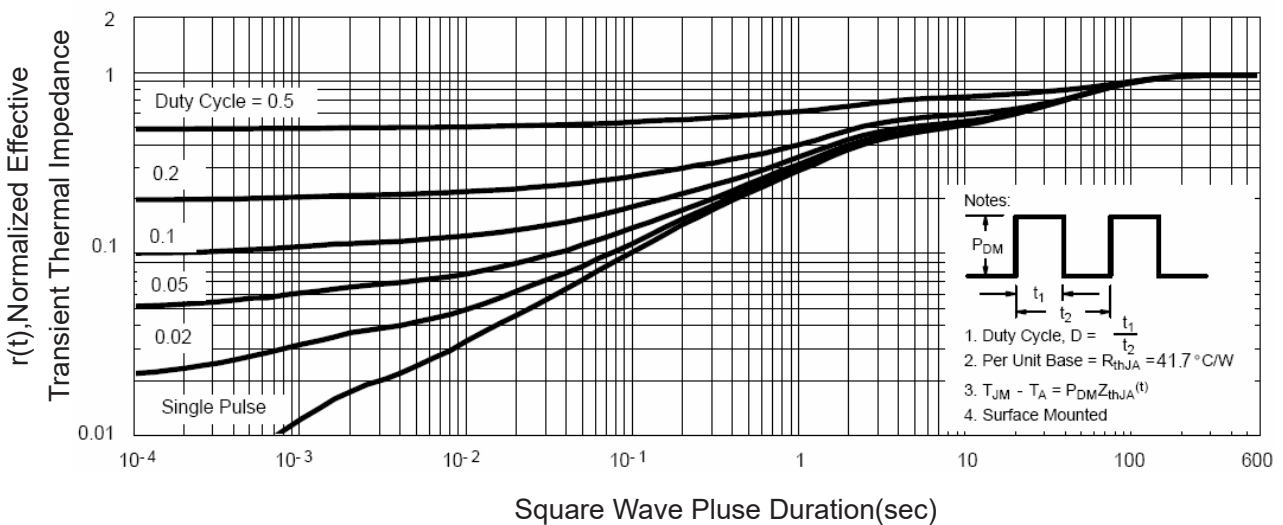
**Figure 4 Rdson-Junction Temperature**



**Figure 5 Gate Charge**



**Figure 6 Source- Drain Diode Forward**


**Figure 7 Capacitance vs Vds**

**Figure 9  $BV_{DSS}$  vs Junction Temperature**

**Figure 8 Safe Operation Area**

**Figure 10  $V_{GS(th)}$  vs Junction Temperature**

**Figure 11 Normalized Maximum Transient Thermal Impedance**