

### Description

The VSM3401Y uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications.

### General Features

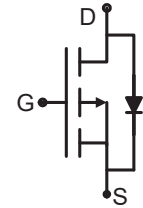
- $V_{DS} = -30V, I_D = -4.2A$   
 $R_{DS(ON)} < 130m\Omega @ V_{GS} = -2.5V$   
 $R_{DS(ON)} < 75m\Omega @ V_{GS} = -4.5V$   
 $R_{DS(ON)} < 55m\Omega @ V_{GS} = -10V$
- High power and current handling capability
- Lead free product is acquired
- Surface mount package

### Application

- PWM applications
- Load switch
- Power management



SOT-23-3



Schematic Diagram

### Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM3401Y-S2	VSM3401Y	SOT-23-3	Ø180mm	8 mm	3000 units

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Drain Current-Continuous	$I_D$	-4.2	A
Drain Current-Pulsed <sup>(Note 1)</sup>	$I_{DM}$	-30	A
Maximum Power Dissipation	$P_D$	1.2	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ\text{C}$

### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	104	$^\circ\text{C/W}$
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### Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30		-	V

Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V	-	-	-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.7	-1	-1.3	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-4.2A	-	47	55	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A	-	56	75	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-1A		72	130	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-5V, I <sub>D</sub> =-4.2A	-	10	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, F=1.0MHz	-	880	-	PF
Output Capacitance	C <sub>OSS</sub>		-	105	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	65	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-15V, I <sub>D</sub> =-4.2A V <sub>GS</sub> =-10V, R <sub>GEN</sub> =6Ω	-	7	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	3	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	30	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	12	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-15V, I <sub>D</sub> =-4.2A, V <sub>GS</sub> =-4.5V	-	8.5	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	1.8	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	2.7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-4.2A	-	-	-1.2	V

## Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

## Typical Electrical and Thermal Characteristics

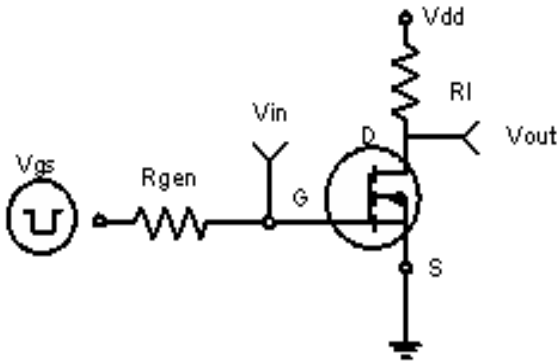


Figure 1: Switching Test Circuit



Figure 2: Switching Waveforms

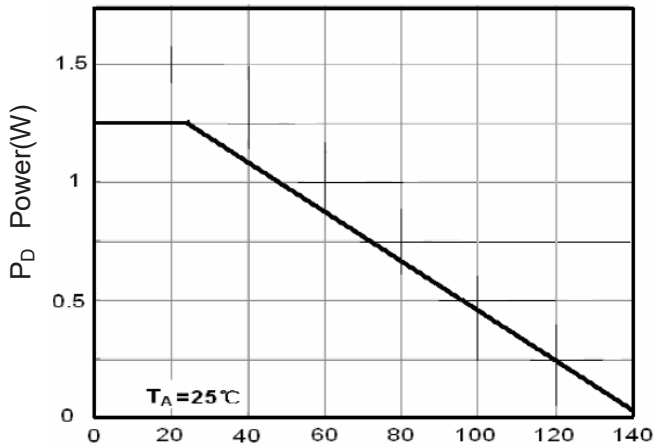


Figure 3 Power Dissipation

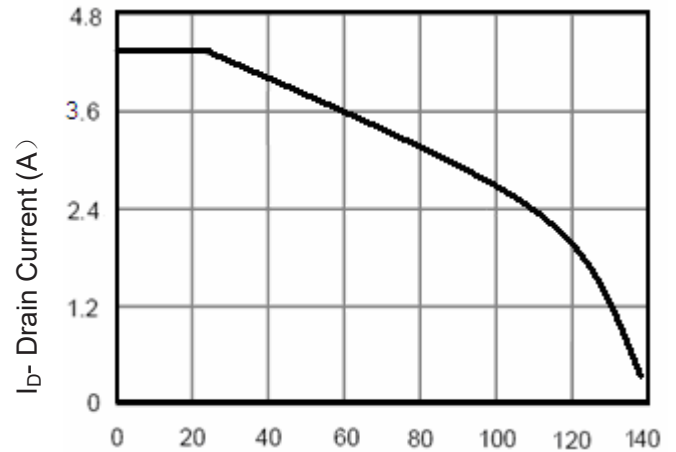


Figure 4 Drain Current

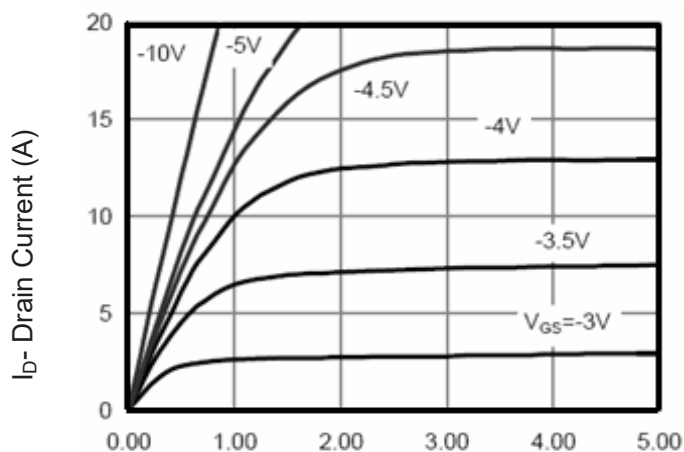


Figure 5 Output Characteristics

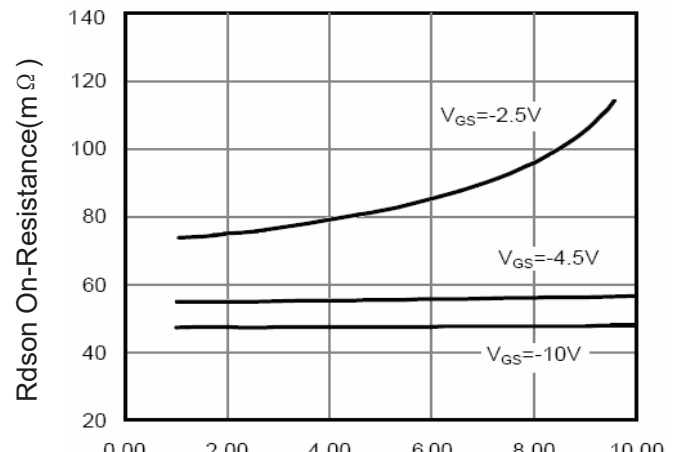


Figure 6 Drain-Source On-Resistance

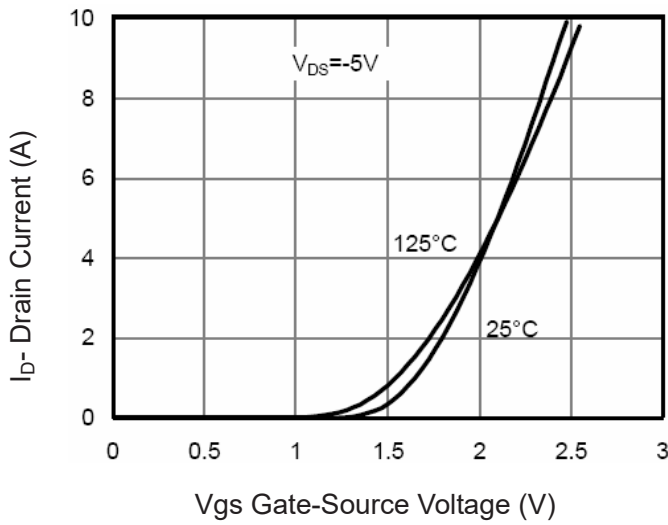


Figure 7 Transfer Characteristics

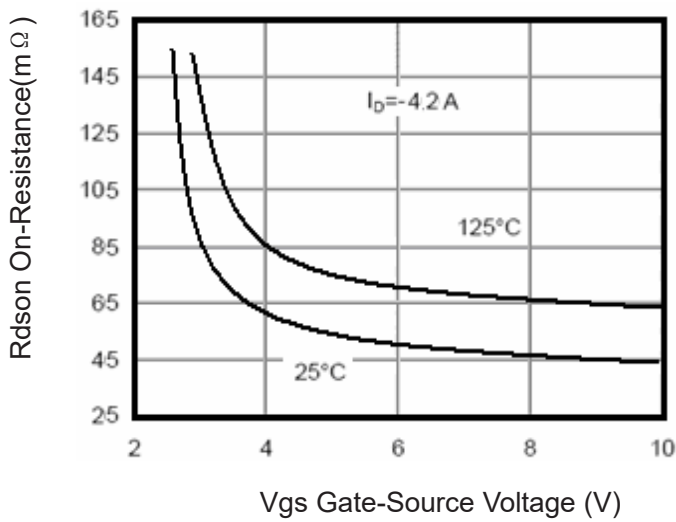
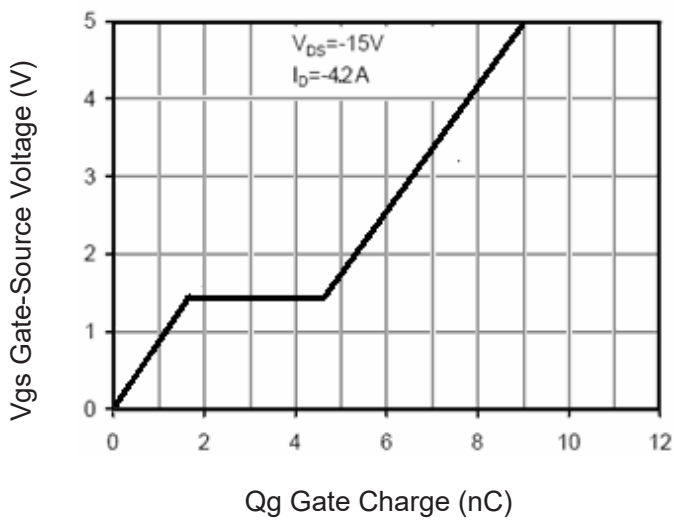

Figure 9  $R_{DS(on)}$  vs  $V_{GS}$ 


Figure 11 Gate Charge

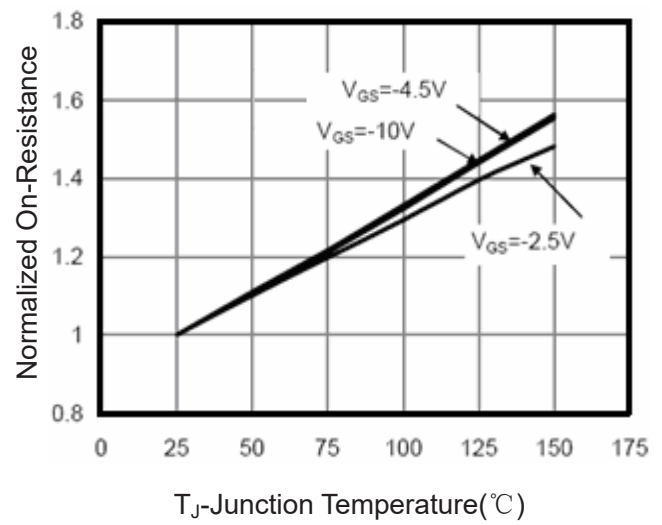


Figure 8 Drain-Source On-Resistance

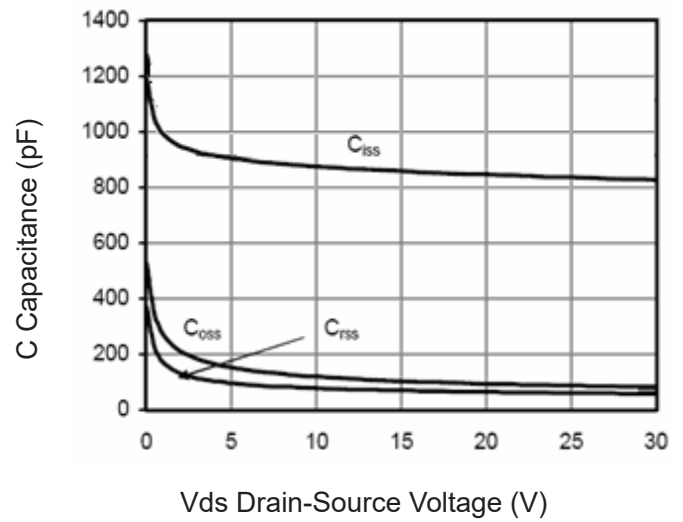
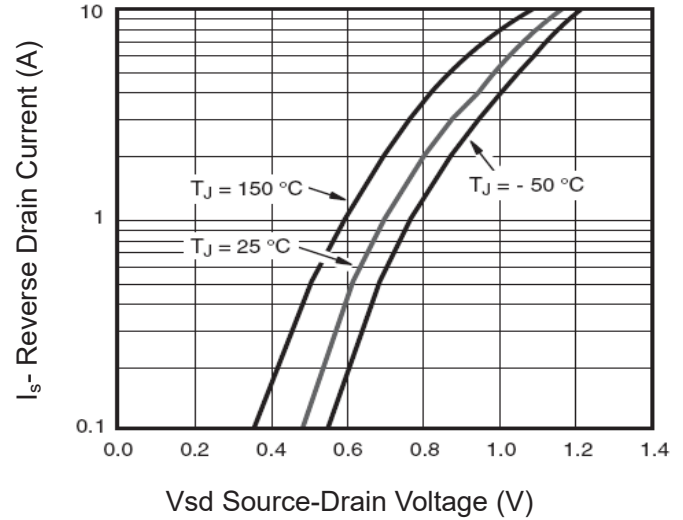

Figure 10 Capacitance vs  $V_{DS}$ 


Figure 12 Source- Drain Diode Forward

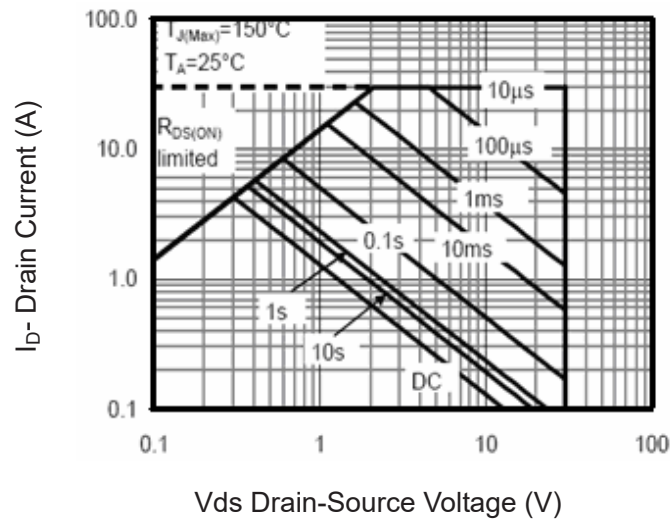


Figure 13 Safe Operation Area

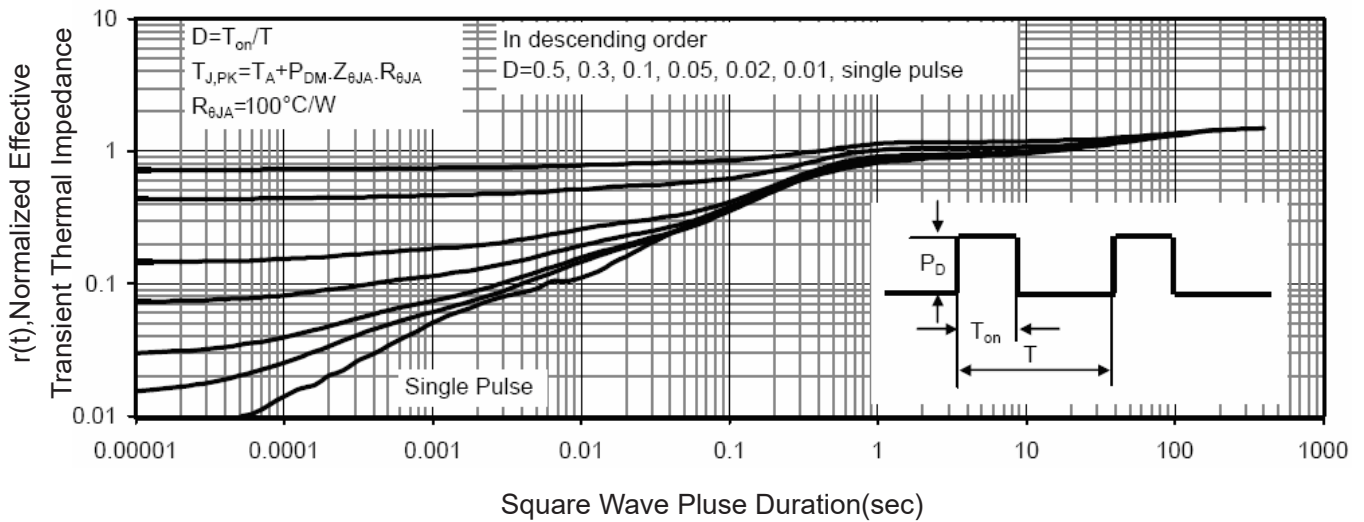


Figure 14 Normalized Maximum Transient Thermal Impedance