VSM12N04-S8

Shenzhen VSEEI Semiconductor Co., Ltd

Description

The VSM12N04 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- V_{DS} =40V, I_D =12A

    $R_{DS(ON)}$ <12mΩ @ V_{GS}=10V (Typ. 8.4 mΩ)

    $R_{DS(ON)}$ <18mΩ @ V_{GS}=4.5V (Typ. 12.3 mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply
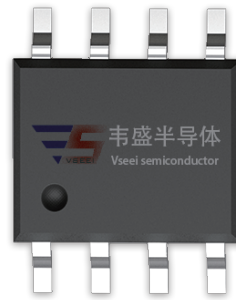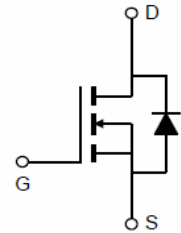
SOP-8   Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM12N04-S8	VSM12N04	SOP-8	Ø330mm	12mm	2500 units

Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	12	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	8.5	A
Pulsed Drain Current	I_{DM}	60	A
Maximum Power Dissipation	P_D	3	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient[Note 2]	$R_{θJA}$	41.7	℃/W

Electrical Characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit

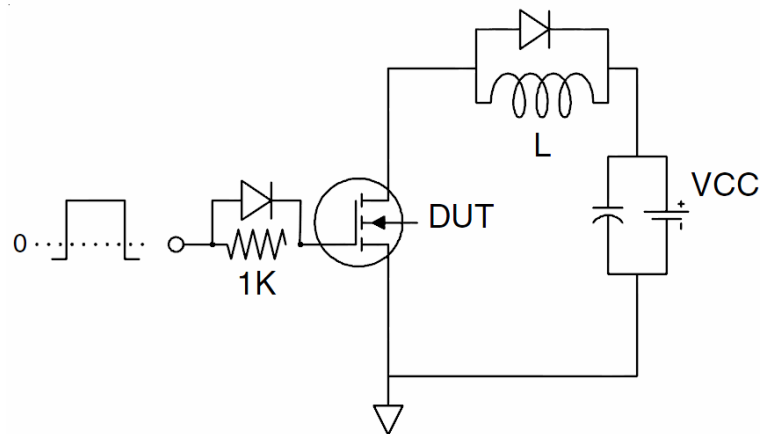| **Off Characteristics**						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V$ $I_D=250\mu A$	40	45	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V,V_{GS}=0V$	-	-	1	µA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm20V,V_{DS}=0V$	-	-	±100	nA
On Characteristics [Note 3]						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS},I_D=250\mu A$	1.2	1.6	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=10A$	-	8.4	12	mΩ
		$V_{GS}=4.5V, I_D=8A$	-	12.3	18	mΩ
Forward Transconductance	g_{FS}	$V_{DS}=5V,I_D=10A$		75	-	S
Dynamic Characteristics [Note4]						
Input Capacitance	C_{Iss}	$V_{DS}=20V,V_{GS}=0V,$ F=1.0MHz	-	1780	-	PF
Output Capacitance	C_{oss}		-	209	-	PF
Reverse Transfer Capacitance	C_{rss}		-	160	-	PF
Switching Characteristics [Note 4]						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, R_L=2\Omega$ $V_{GS}=10V,R_G=3\Omega$	-	6.4	-	nS
Turn-on Rise Time	t_r		-	17.2	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	29.6	-	nS
Turn-Off Fall Time	t_f		-	16.8	-	nS
Total Gate Charge	Q_g	$V_{DS}=20V,I_D=10A,$ $V_{GS}=10V$	-	30		nC
Gate-Source Charge	Q_{gs}		-	4.2		nC
Gate-Drain Charge	Q_{gd}		-	9.5		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage [Note 3]	V_{SD}	$V_{GS}=0V,I_S=10A$	-		1.2	V
Diode Forward Current [Note 2]	I_S		-	-	12	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 10A di/dt = 100A/µs [Note3]	-	29	-	nS
Reverse Recovery Charge	Qrr		-	26	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. Surface Mounted on FR4 Board, t ≤ 10 sec.

3. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production
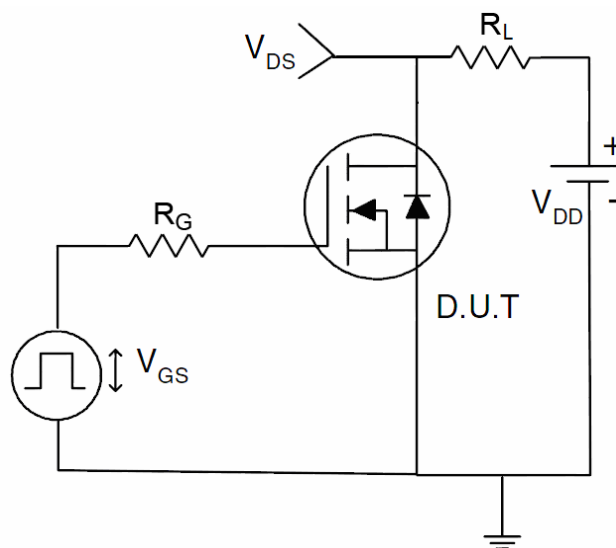
Test circuit
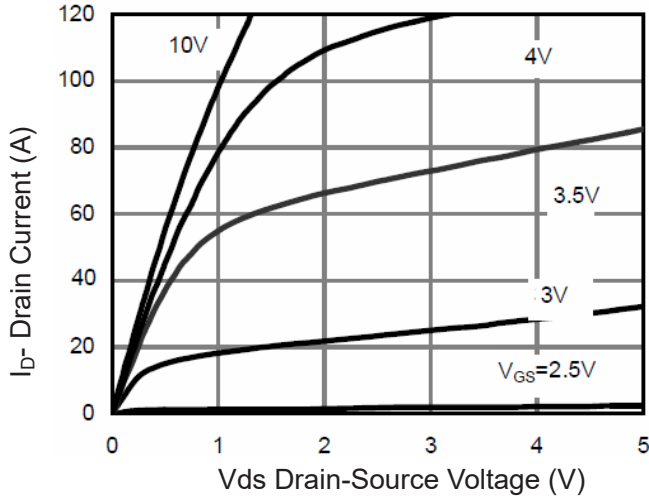
1) E$_{AS}$ Test Circuit
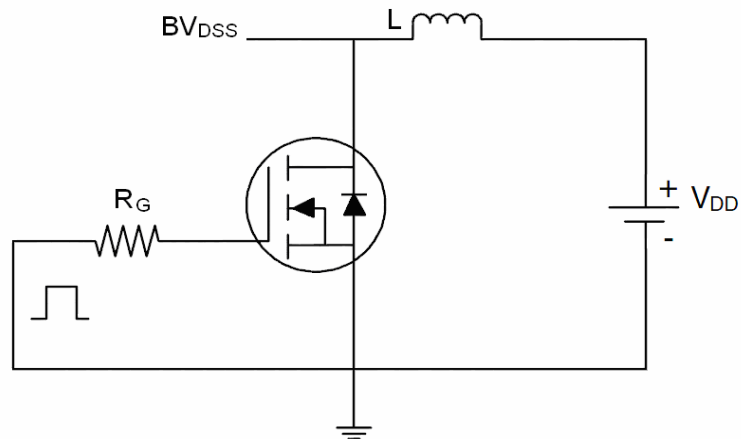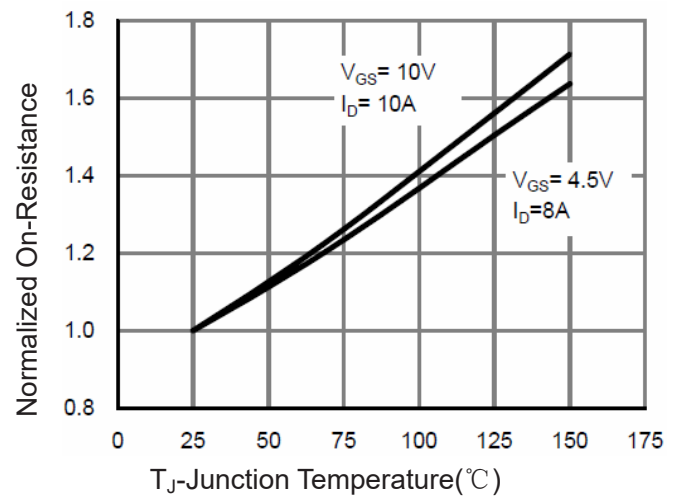

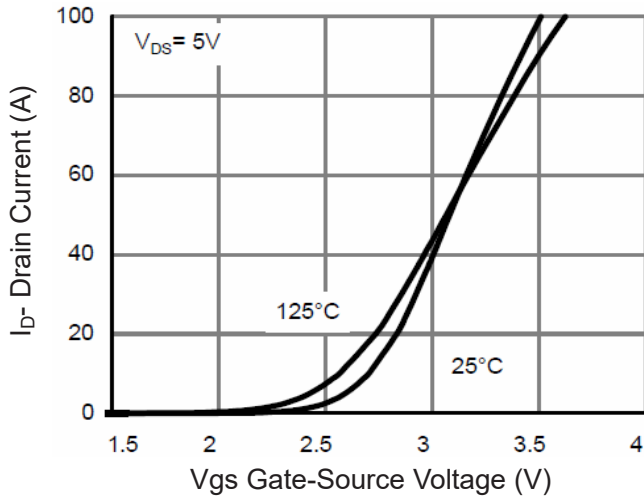### 2) Gate Charge Test Circuit

3) Switch Time Test Circuit

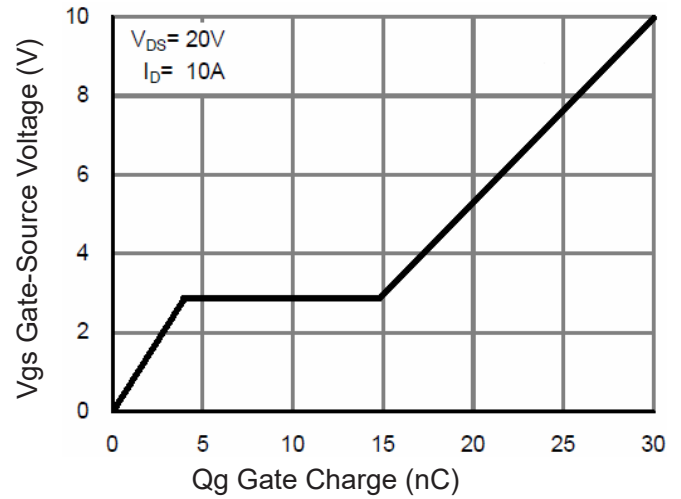## Typical Electrical and Thermal Characteristics (Curves)
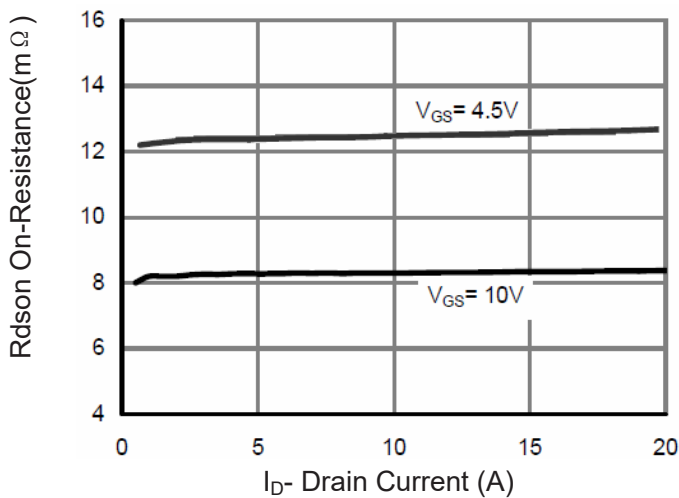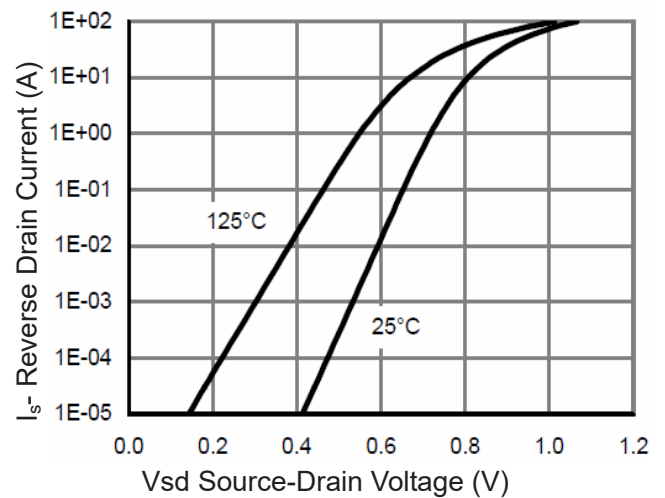

Figure 1 Output Characteristics

Figure 4 Rdson-JunctionTemperature

Figure 2 Transfer Characteristics

Figure 5 Gate Charge
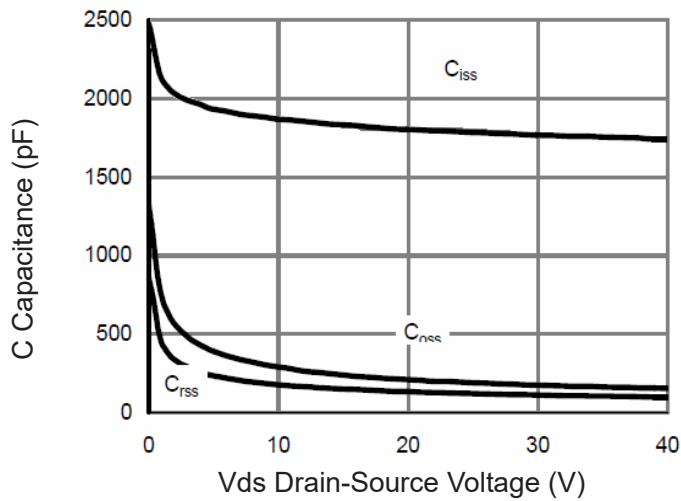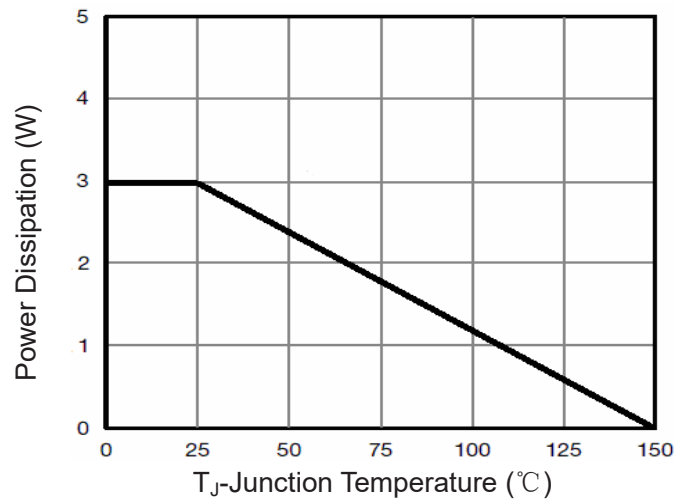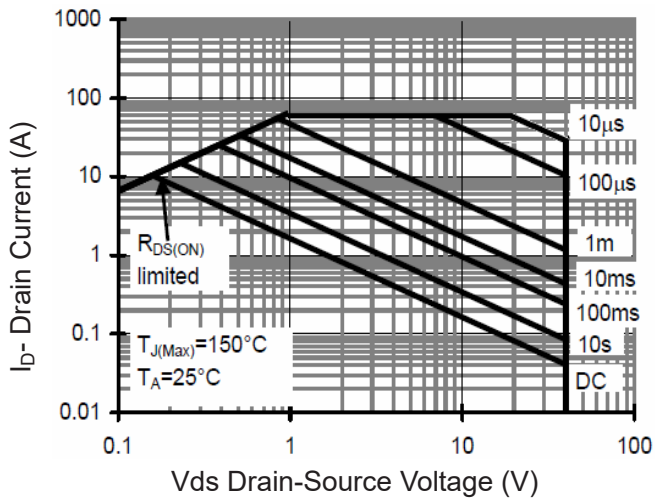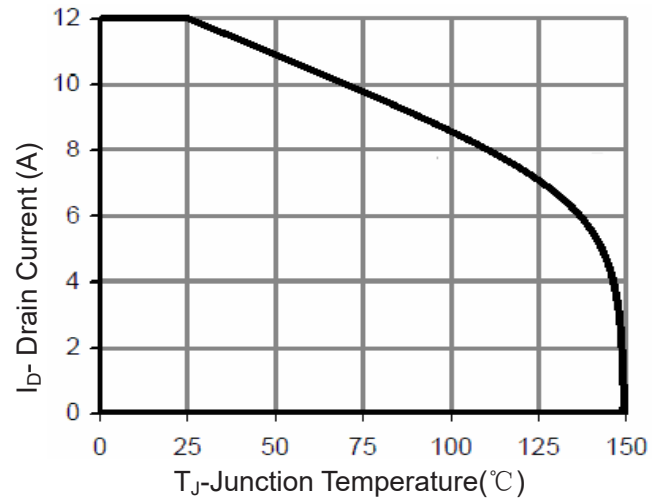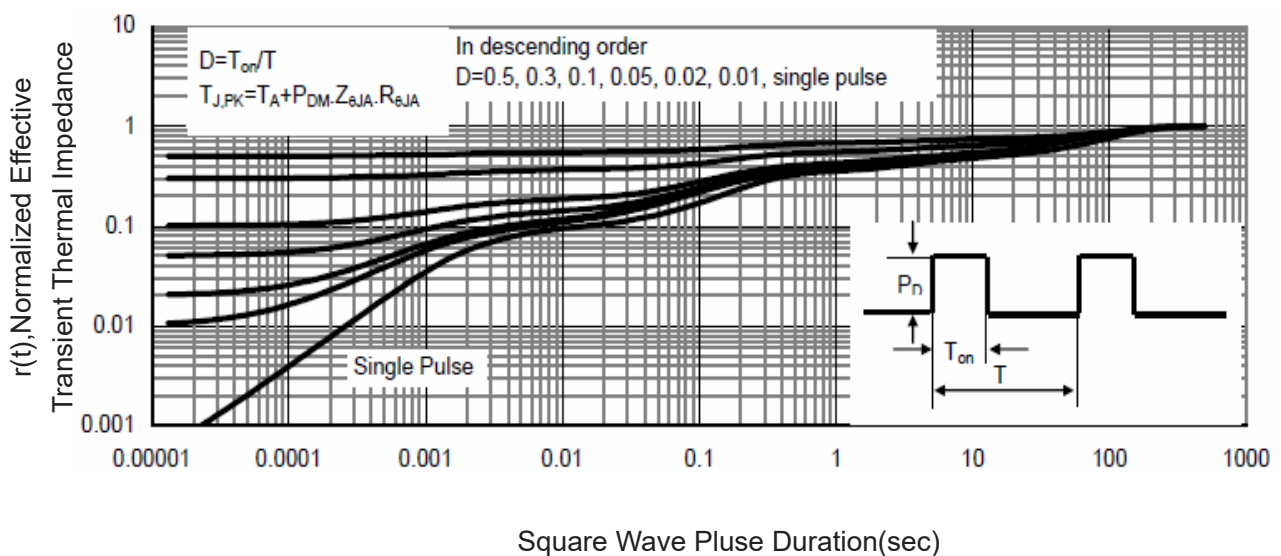

Figure 3 Rdson- Drain Current

Figure 6 Source- Drain Diode Forward

Figure 7 Capacitance vs Vds

Figure 9 Power De-rating

Figure 8 Safe Operation Area

Figure 10 Current De-rating

Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance