

Description

The NCEP60T12A uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

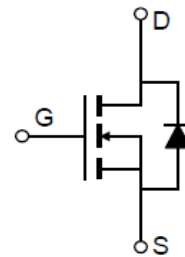
- $V_{DS}=60V, I_D=120A$
 $R_{DS(ON)} < 4.0m\Omega @ V_{GS}=10V$ (Typ:3.5m Ω)
 $R_{DS(ON)} < 5.0m\Omega @ V_{GS}=4.5V$ (Typ:4.0m Ω)
- Excellent gate charge x $R_{DS(on)}$ product
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



TO-220C



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VST06N035-TC	VST06N035	TO-220C	-	-	-

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Silicon Limited)	I_D	120	A
Drain Current-Continuous($T_C=100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	100	A
Pulsed Drain Current	I_{DM}	480	A
Maximum Power Dissipation	P_D	180	W
Derating factor		1.2	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	500	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.83	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

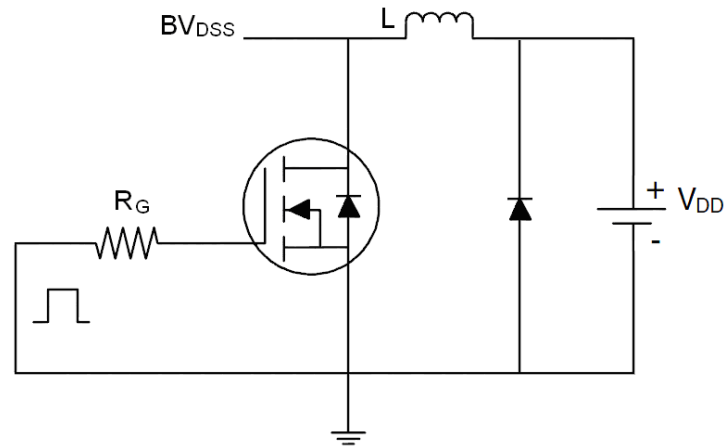
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250 μ A	60		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μ A
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250 μ A	1.0	1.7	2.4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =60A	-	3.5	4.0	m Ω
		V _{GS} =4.5V, I _D =60A	-	4.0	5.0	m Ω
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =60A	40	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{ISS}	V _{DS} =30V, V _{GS} =0V, F=1.0MHz	-	4000	-	PF
Output Capacitance	C _{OSS}		-	680	-	PF
Reverse Transfer Capacitance	C _{RSS}		-	23	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, I _D =60A V _{GS} =10V, R _G =4.7 Ω	-	11	-	nS
Turn-on Rise Time	t _r		-	5	-	nS
Turn-Off Delay Time	t _{d(off)}		-	56	-	nS
Turn-Off Fall Time	t _f		-	12	-	nS
Total Gate Charge	Q _g	V _{DS} =30V, I _D =60A, V _{GS} =10V	-	67		nC
Gate-Source Charge	Q _{gs}		-	12		nC
Gate-Drain Charge	Q _{gd}		-	8.5		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =120A	-		1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	120	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S di/dt = 100A/ μ s ^(Note3)	-	48		nS
Reverse Recovery Charge	Q _{rr}		-	60		nC

Notes:

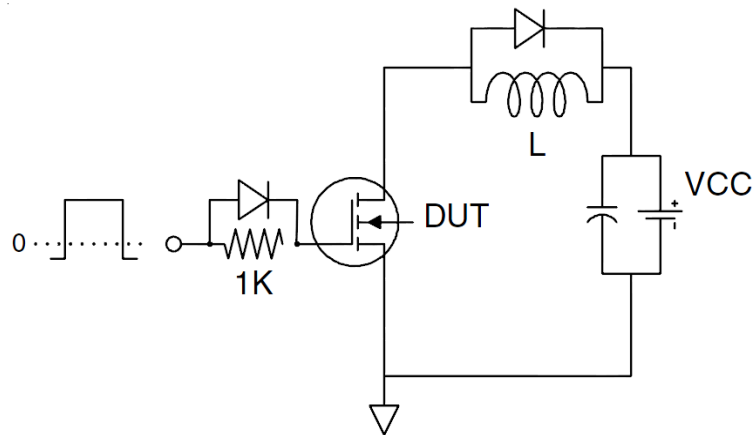
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=30V, V_G=10V, L=0.5mH, R_G=25\Omega$

Test Circuit

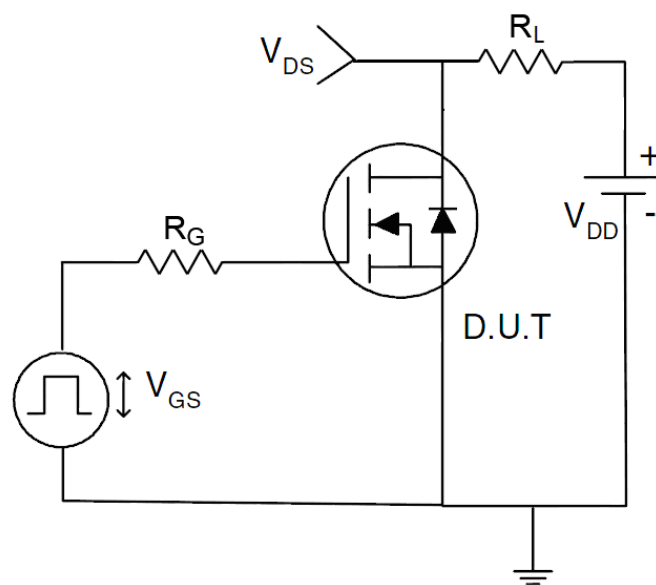
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

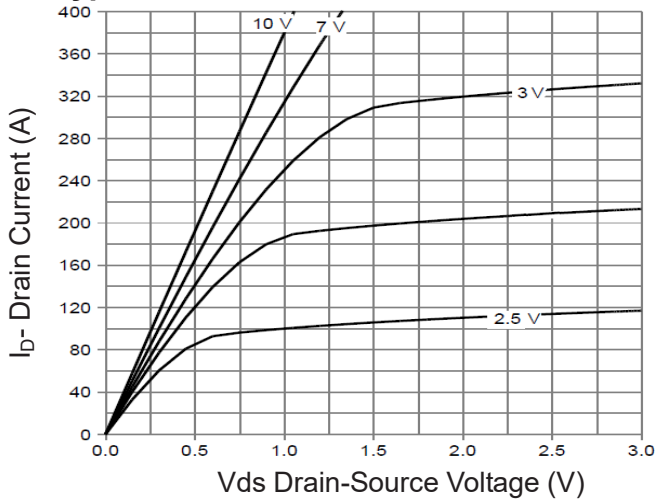


Figure 1 Output Characteristics

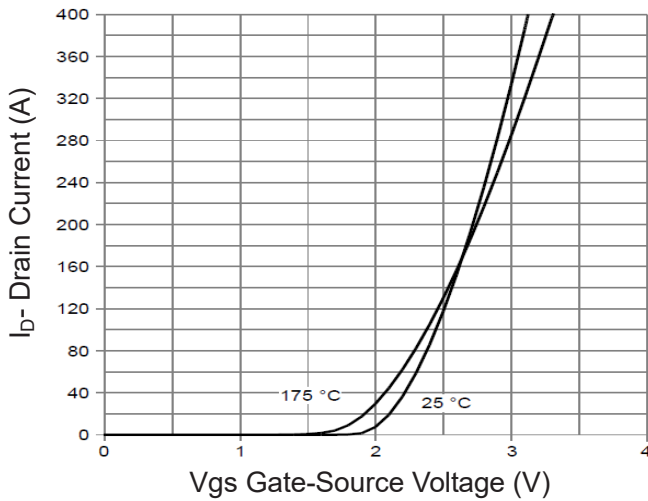


Figure 2 Transfer Characteristics

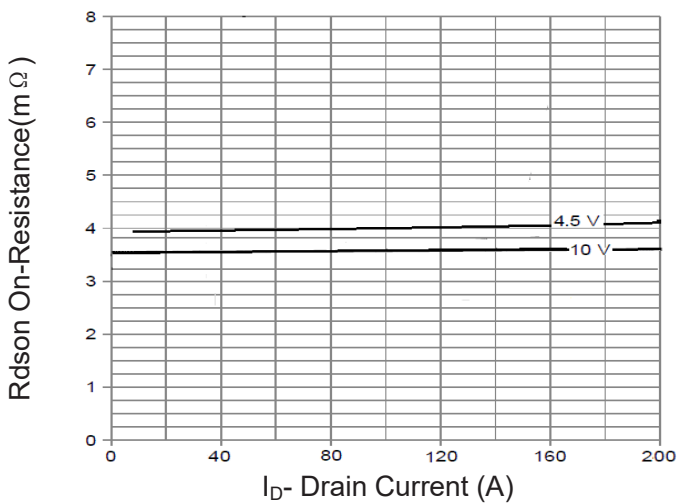


Figure 3 Rdson- Drain Current

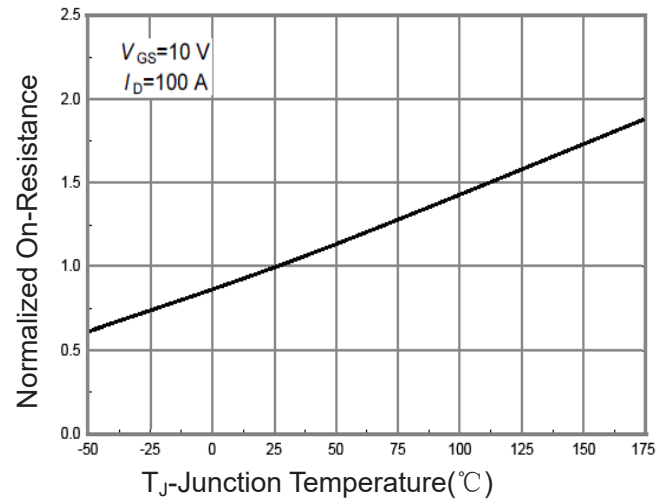


Figure 4 Rdson-Junction Temperature

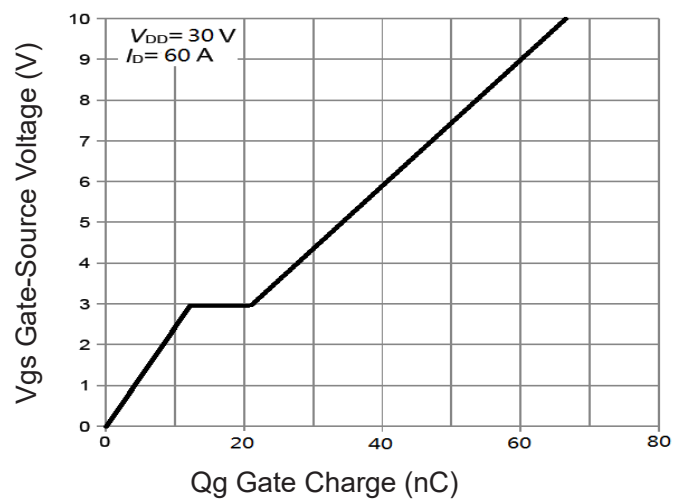


Figure 5 Gate Charge

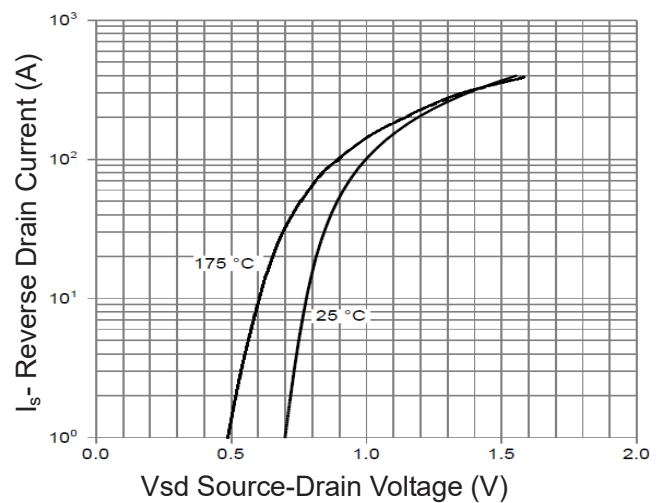
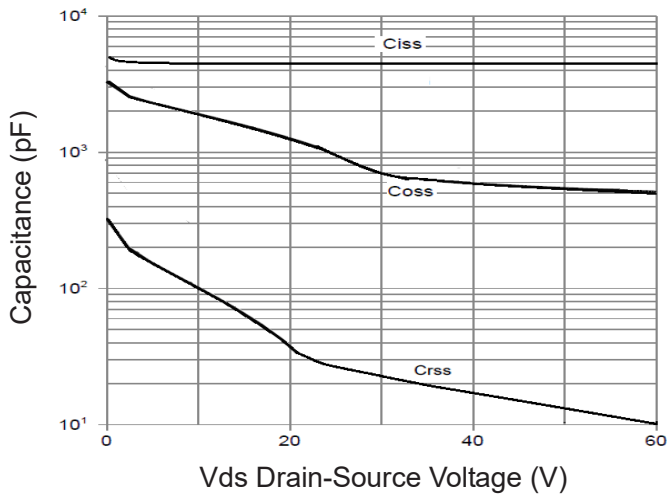
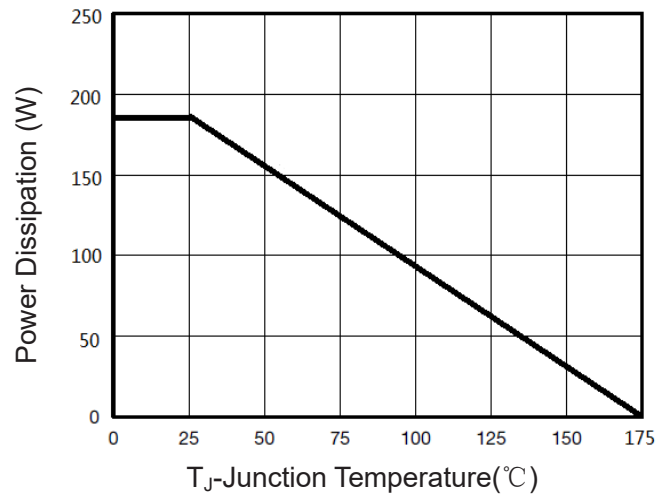
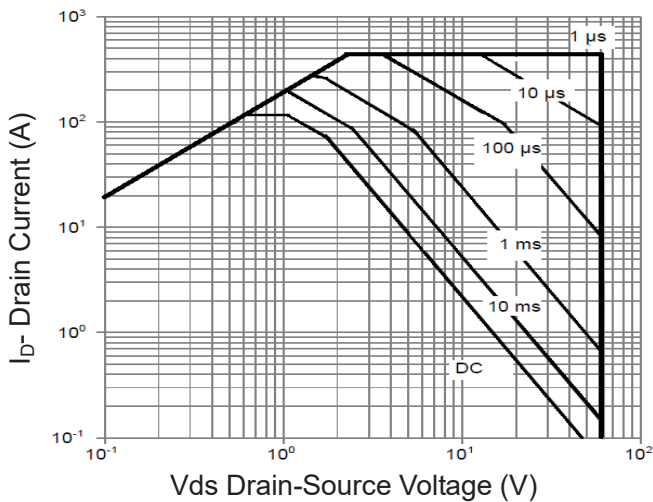
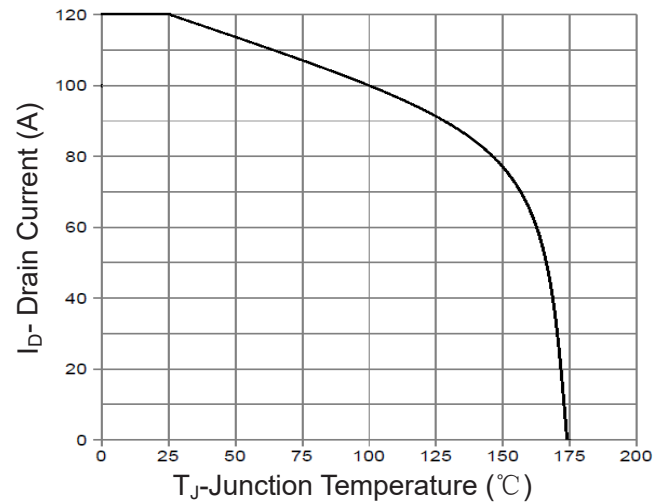
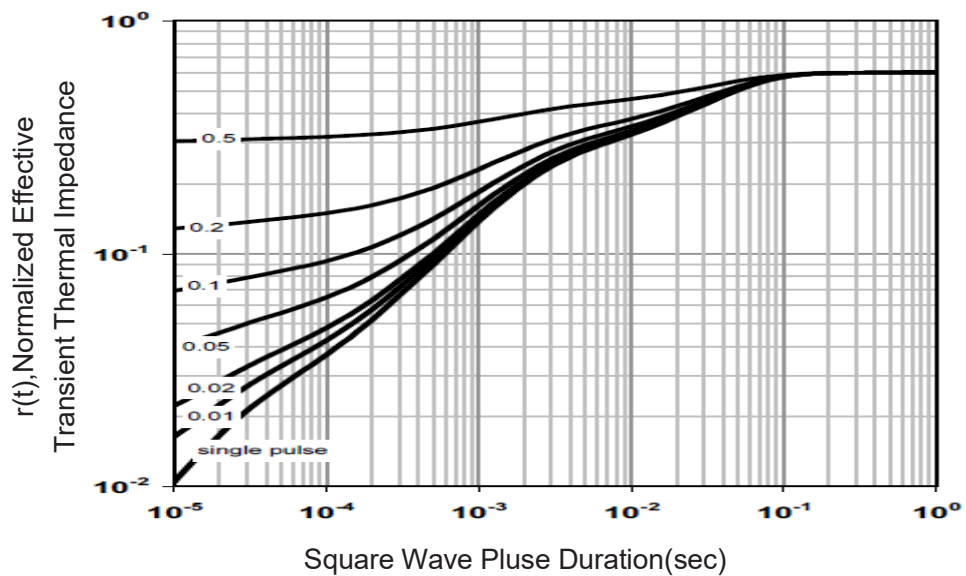


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 Power De-rating

Figure 8 Safe Operation Area

Figure 10 Current De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance