

## Description

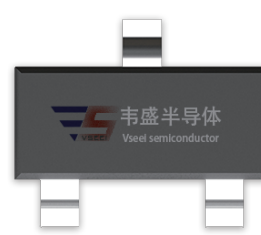
The VSM0103Y uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

## General Features

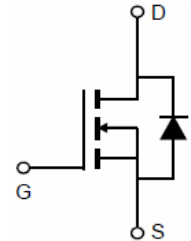
- $V_{DS} = 100V, I_D = 3A$   
 $R_{DS(ON)} < 160m\Omega @ V_{GS}=10V$  (Typ:136m $\Omega$ )  
 $R_{DS(ON)} < 170m\Omega @ V_{GS}=4.5V$  (Typ:140m $\Omega$ )
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

## Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



SOT-23-3



Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM0103Y-S2	VSM0103Y	SOT-23-3	Ø180mm	8 mm	3000 units

## Absolute Maximum Ratings ( $T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	3	A
Drain Current-Pulsed <sup>(Note 1)</sup>	$I_{DM}$	20	A
Maximum Power Dissipation	$P_D$	1.5	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^{\circ}C$

## Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	100	$^{\circ}C/W$
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## Electrical Characteristics ( $T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$

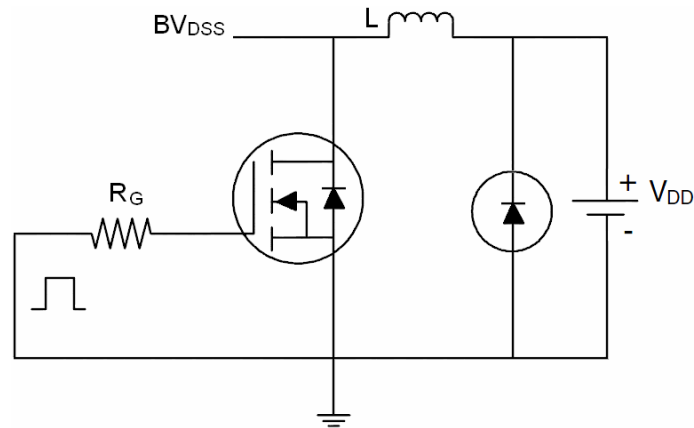
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.5	2.0	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =3A	-	136	160	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =3A	-	140	170	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =3A	-	5	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, F=1.0MHz	-	650	-	PF
Output Capacitance	C <sub>OSS</sub>		-	24	-	PF
Reverse Transfer Capacitance	C <sub>rSS</sub>		-	20	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =50V, R <sub>L</sub> =19Ω V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω	-	6	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	4	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	20	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	4	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =50V, I <sub>D</sub> =3A, V <sub>GS</sub> =10V	-	20		nC
Gate-Source Charge	Q <sub>gs</sub>		-	2.1	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	3.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =3A	-	-	1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	3	A

## Notes:

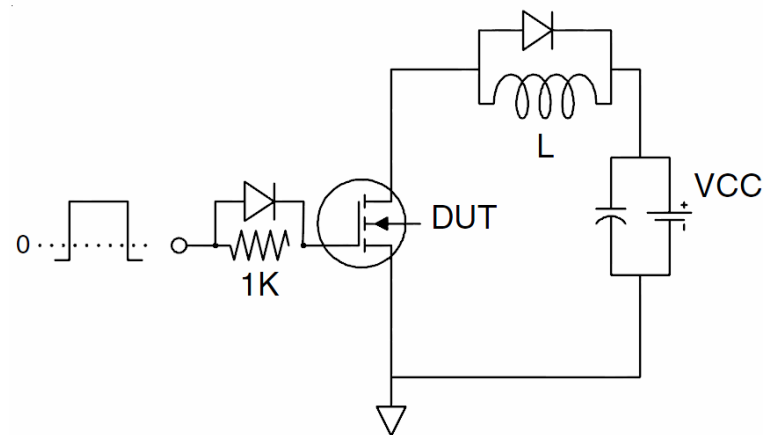
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

## Test Circuit

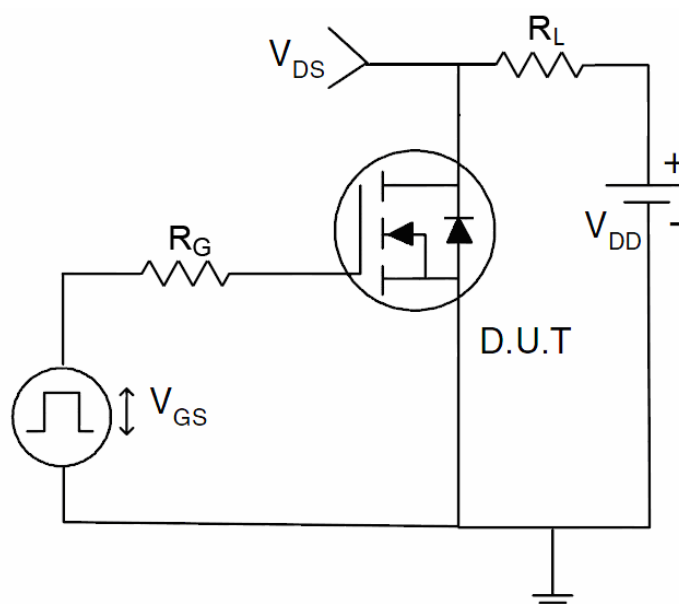
### 1) $E_{AS}$ test circuit



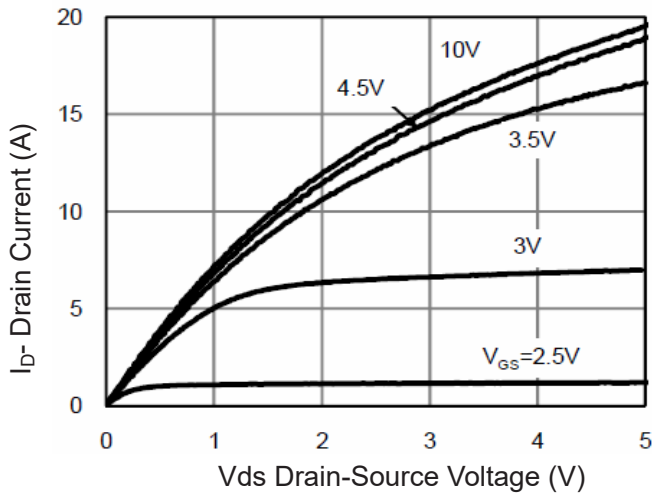
### 2) Gate charge test circuit



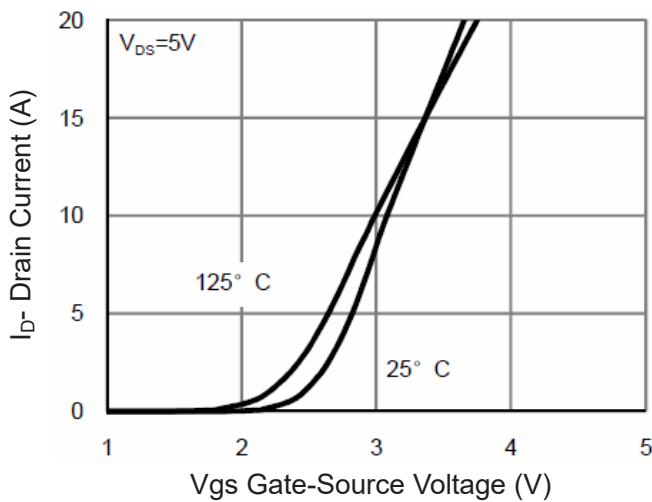
### 3) Switch Time Test Circuit



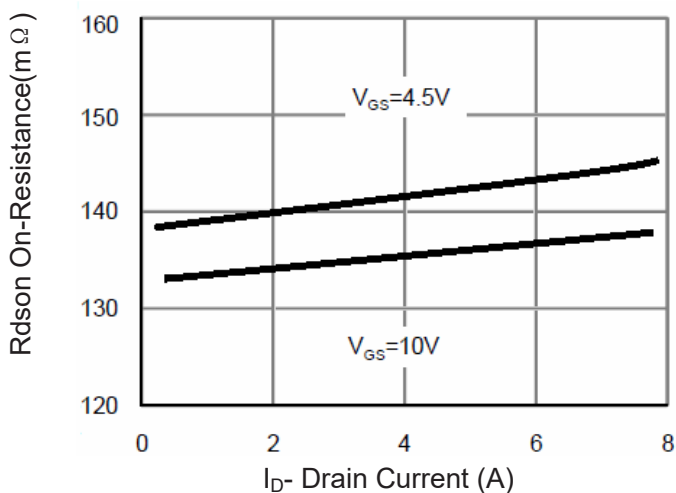
## Typical Electrical and Thermal Characteristics (Curves)



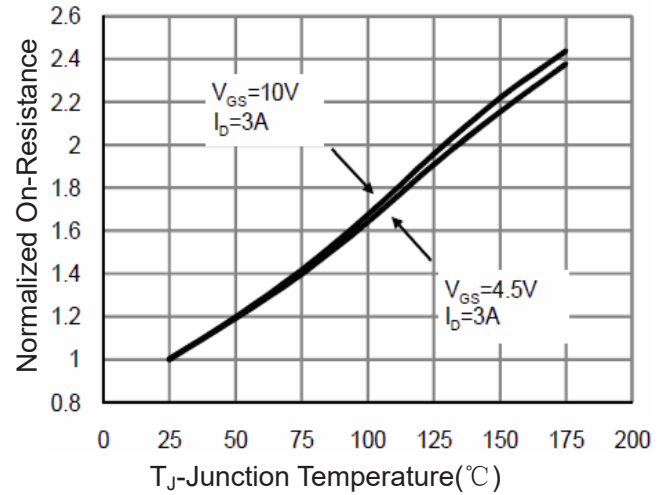
**Figure 1 Output Characteristics**



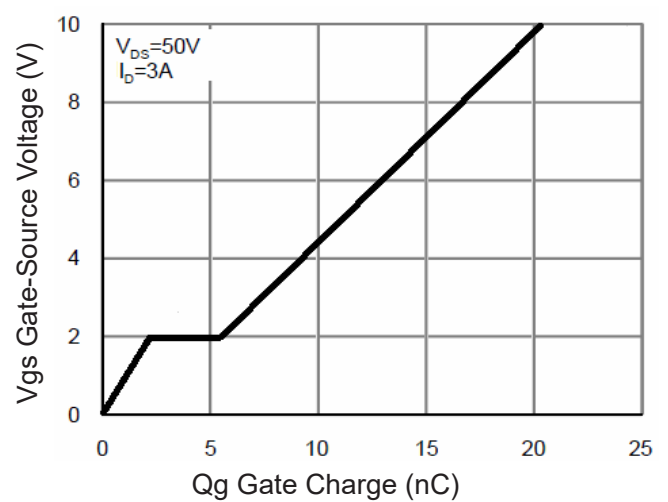
**Figure 2 Transfer Characteristics**



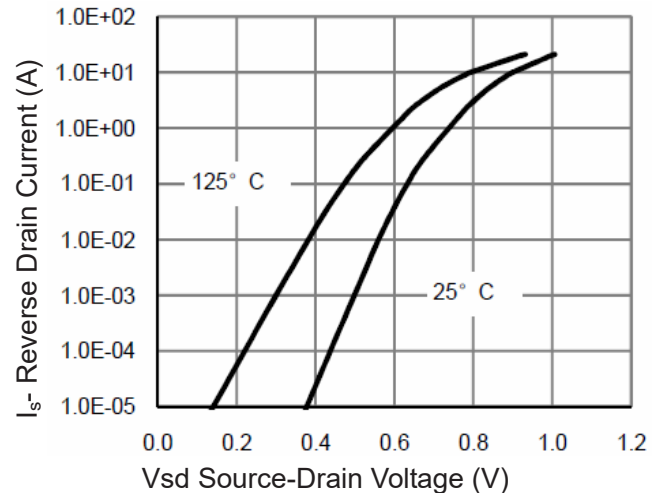
**Figure 3 Rdson- Drain Current**



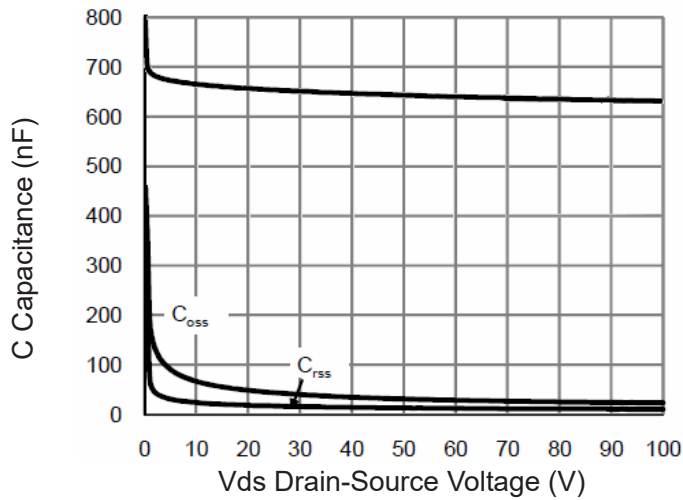
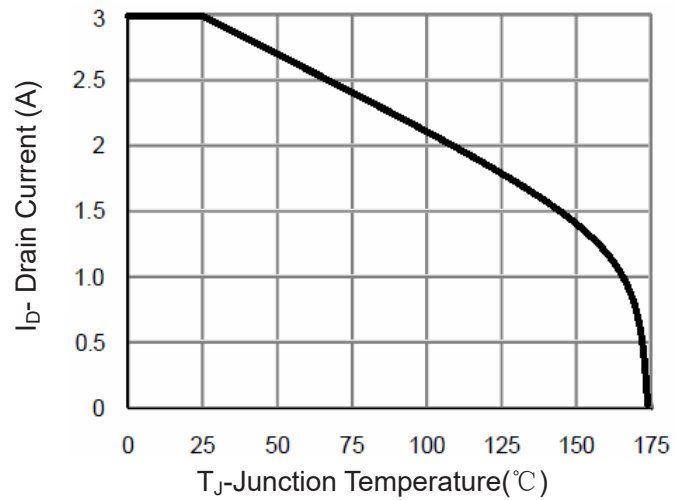
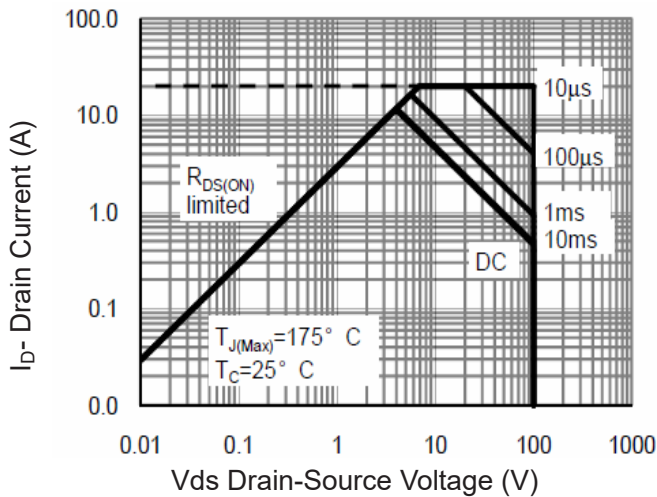
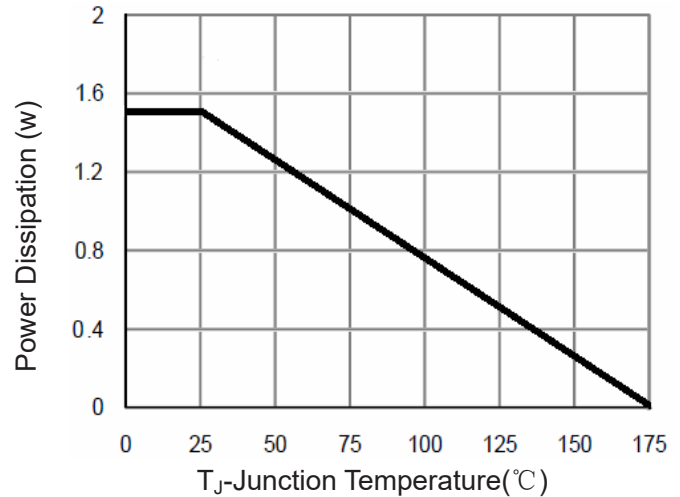
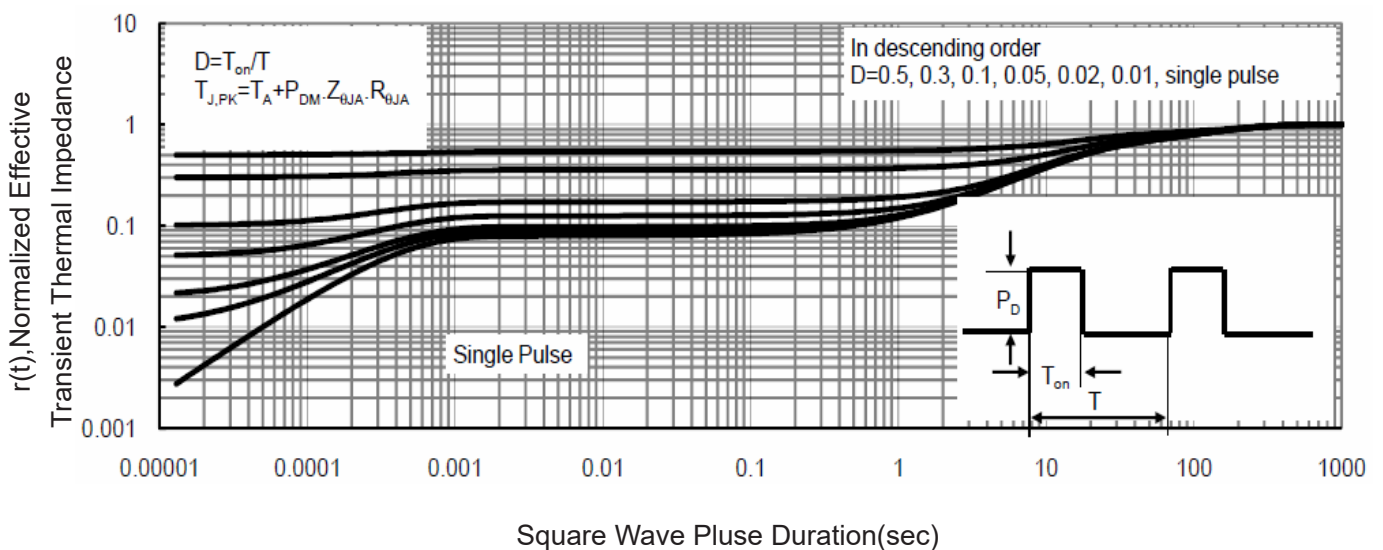
**Figure 4 Rdson-Junction Temperature**



**Figure 5 Gate Charge**



**Figure 6 Source- Drain Diode Forward**


**Figure 7 Capacitance vs Vds**

**Figure 9  $BV_{DSS}$  vs Junction Temperature**

**Figure 8 Safe Operation Area**

**Figure 10 Power De-rating**

**Figure 11 Normalized Maximum Transient Thermal Impedance**