

Description

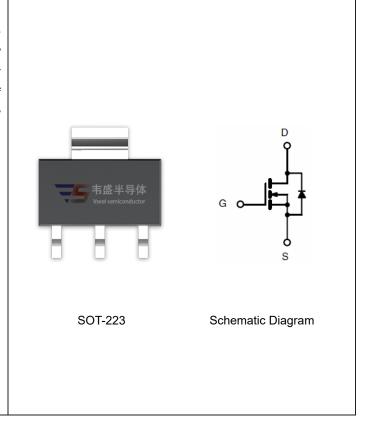
The VST10N750 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{\text{DS(ON)}}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

- $V_{DS} = 100V, I_D = 7A$ $R_{DS(ON)} < 85m\Omega @ V_{GS} = 10V (Typ:75m\Omega)$ $R_{DS(ON)} < 105m\Omega @ V_{GS} = 4.5V (Typ:85m\Omega)$
- Excellent gate charge x R_{DS(on)} product(FOM)
- Very low on-resistance R_{DS(on)}
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VST10N750-S23	VST10N750	SOT-223	Ø330mm	12mm	2500 units

Absolute Maximum Ratings (T_A=25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	100	V	
Gate-Source Voltage	V _{GS}	±20	V	
Drain Current-Continuous	I _D	7	Α	
Drain Current-Pulsed (Note 1)	I _{DM}	28	Α	
Single pulse avalanche energy (Note 5)	E _{AS}	20	mJ	
Maximum Power Dissipation	P _D	2.5	W	
Operating Junction and Storage Temperature Range	T_{J}, T_{STG}	-55 To 150	°C	

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	50	°C/W
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Electrical Characteristics (T_A =25 $^{\circ}$ C unless otherwise noted)

Parameter	Symbol	Symbol Condition		Тур	Max	Unit
Off Characteristics			•	•		
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V,V _{GS} =0V	-	-	1	μΑ
Gate-Body Leakage Current	I _{GSS}	$V_{GS}=\pm20V, V_{DS}=0V$	-	-	±100	nA
On Characteristics (Note 3)			1	•		•
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS},I_{D}=250\mu A$	1.2	1.9	2.5	V
David Course On Otata Daviatana		V _{GS} =10V, I _D =7A	-	75	85	mΩ
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D =7A	-	85	105	mΩ
Forward Transconductance g _{FS}		$V_{DS}=5V,I_{D}=7A$	-	8	-	S
Dynamic Characteristics (Note4)			1	•		•
Input Capacitance	C _{lss}	V 50VVV 0V	-	443	-	PF
Output Capacitance	Coss	$V_{DS}=50V, V_{GS}=0V,$	-	80	-	PF
Reverse Transfer Capacitance	C _{rss}	F=1.0MHz	-	15.4	-	PF
Switching Characteristics (Note 4)			1	•		•
Turn-on Delay Time	t _{d(on)}		-	6	-	nS
Turn-on Rise Time	t _r	V_{DD} =50V, R_L =7 Ω	-	2.5	-	nS
Turn-Off Delay Time	$t_{\sf d(off)}$	V_{GS} =10 V , R_{G} =2.5 Ω	-	18	-	nS
Turn-Off Fall Time	t _f		-	2.5	-	nS
Total Gate Charge	Qg	\/ F0\/ 7A	-	7.2		nC
Gate-Source Charge	Q _{gs}	$V_{DS}=50V,I_{D}=7A,$	-	1.3	-	nC
Gate-Drain Charge	Q_gd	V _{GS} =10V	-	1.0	-	nC
Drain-Source Diode Characteristics			1	•		•
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =7A	-	-	1.2	V
Diode Forward Current (Note 2)	Is		-	-	7	Α
Reverse Recovery Time	trr	$T_J = 25^{\circ}C, I_F = 3.5A$	-	31.2	-	nS
Reverse Recovery Charge	Qrr	$di/dt = 100A/\mu s^{(Note3)}$	-	41.2	-	nC

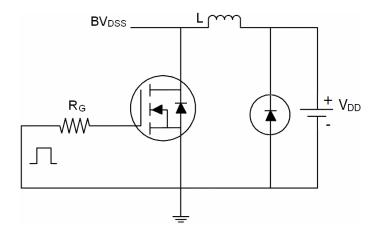
Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- **3.** Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
- 4. Guaranteed by design, not subject to product
- **5.** EAS condition: Tj=25 $^{\circ}$ C,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25 Ω

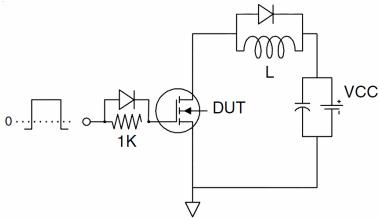


Test Circuit

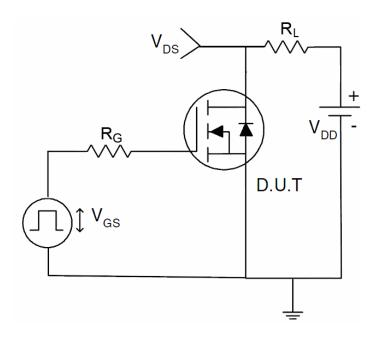
1) E_{AS} test circuit



2) Gate charge test circuit



3) Switch Time Test Circuit





Typical Electrical and Thermal Characteristics

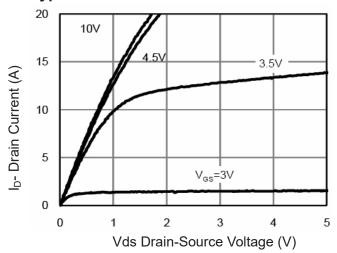


Figure 1 Output Characteristics

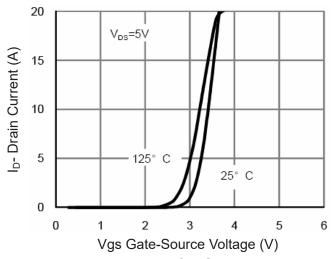


Figure 2 Transfer Characteristics

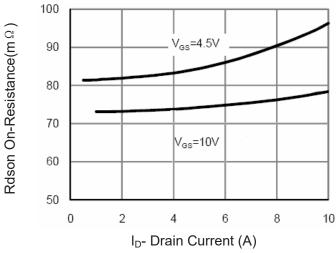


Figure 3 Rdson- Drain Current

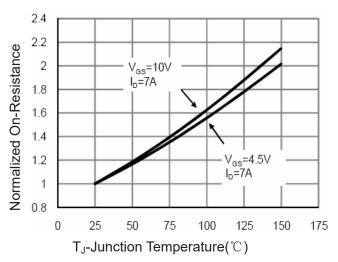


Figure 4 Rdson-Junction Temperature

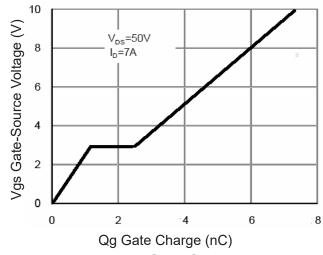


Figure 5 Gate Charge

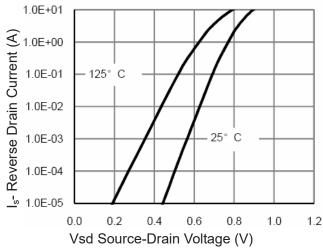


Figure 6 Source- Drain Diode Forward



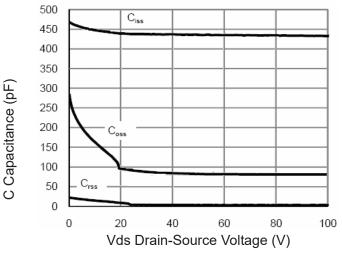


Figure 7 Capacitance vs Vds

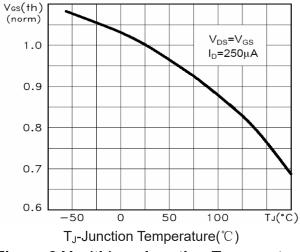


Figure 9 V_{GS}(th) vs Junction Temperature

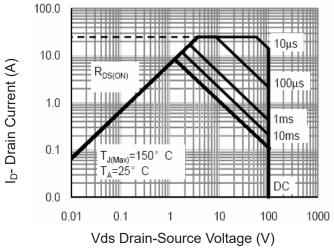


Figure 8 Safe Operation Area

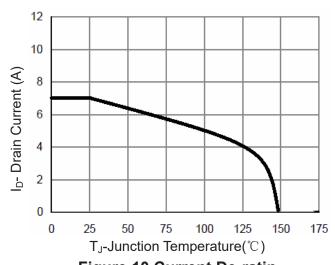


Figure 10 Current De-ratin

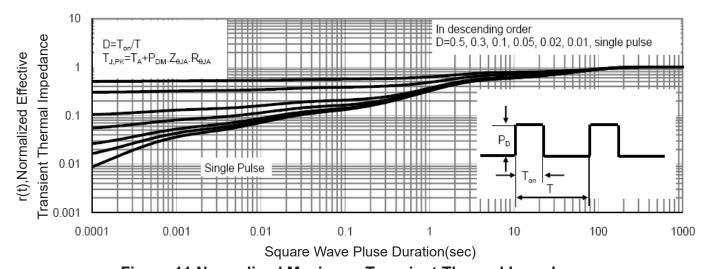


Figure 11 Normalized Maximum Transient Thermal Impedance