

## Description

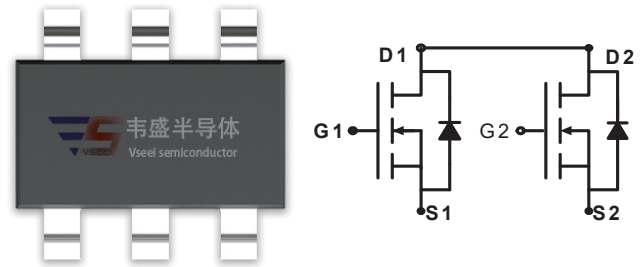
The VSM8205 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

## General Features

- $V_{DS} = 20V, I_D = 4A$   
 $R_{DS(ON)} < 37m\Omega @ V_{GS}=2.5V$   
 $R_{DS(ON)} < 27m\Omega @ V_{GS}=4.5V$
- High Power and current handing capability
- Lead free product is acquired
- Surface Mount Package

## Application

- Battery protection
- Load switch
- Power management



SOT-23-6

Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM8205-S6	VSM8205	SOT-23-6	Ø180mm	8mm	3000 units

## Absolute Maximum Ratings ( $T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 10$	V
Drain Current-Continuous	$I_D$	4	A
Drain Current-Pulsed (Note 1)	$I_{DM}$	25	A
Maximum Power Dissipation	$P_D$	1.25	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^{\circ}C$

## Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	$^{\circ}C/W$
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## Electrical Characteristics ( $T_A=25^{\circ}C$ unless otherwise noted)

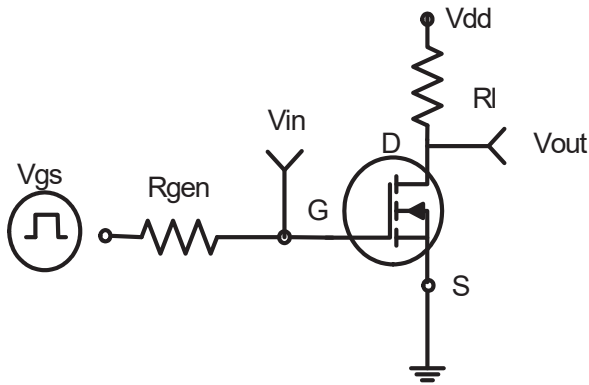
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	20	21	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=19.5V, V_{GS}=0V$	-	-	1	$\mu A$

Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±10V,V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> ,I <sub>D</sub> =250μA	0.5	0.7	1.2	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =4A	-	19.5	27	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =3A	-	25	37	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V,I <sub>D</sub> =4A	-	10	-	S
Dynamic Characteristics <sup>(Note4)</sup>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =8V,V <sub>GS</sub> =0V, F=1.0MHz	-	600	-	PF
Output Capacitance	C <sub>OSS</sub>		-	330	-	PF
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	140	-	PF
Switching Characteristics <sup>(Note 4)</sup>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =10V,I <sub>D</sub> =1A V <sub>GS</sub> =4V,R <sub>GEN</sub> =10Ω	-	18	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	5	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	43	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	20	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =10V,I <sub>D</sub> =4A, V <sub>GS</sub> =4.5V	-	11	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	2.3	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	2.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =2A	-	0.8	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>S</sub>		-	-	2	A

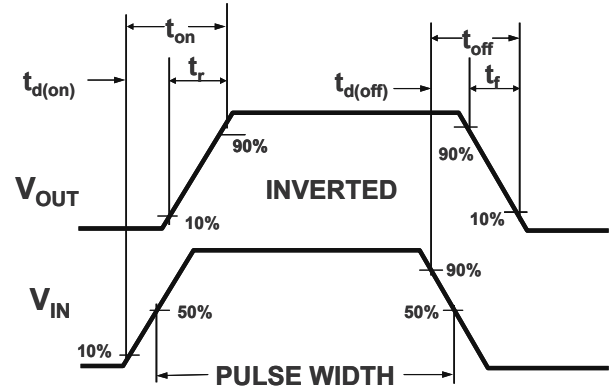
## Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

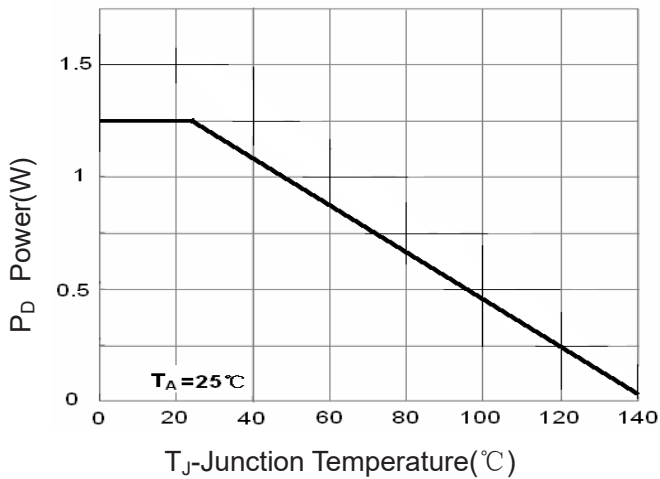
## Typical Electrical and Thermal Characteristics



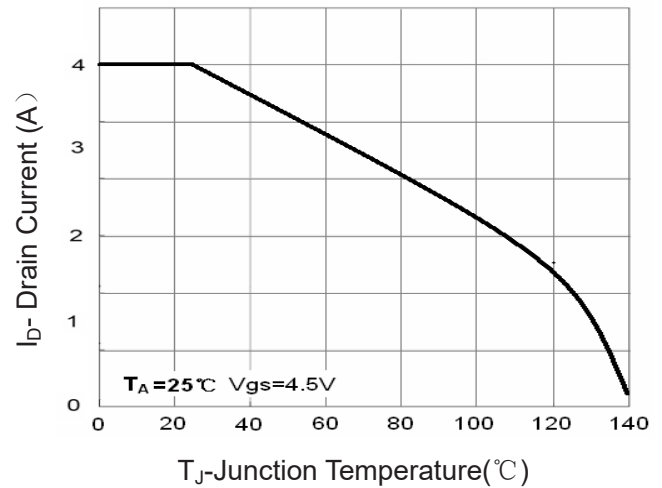
**Figure 1: Switching Test Circuit**



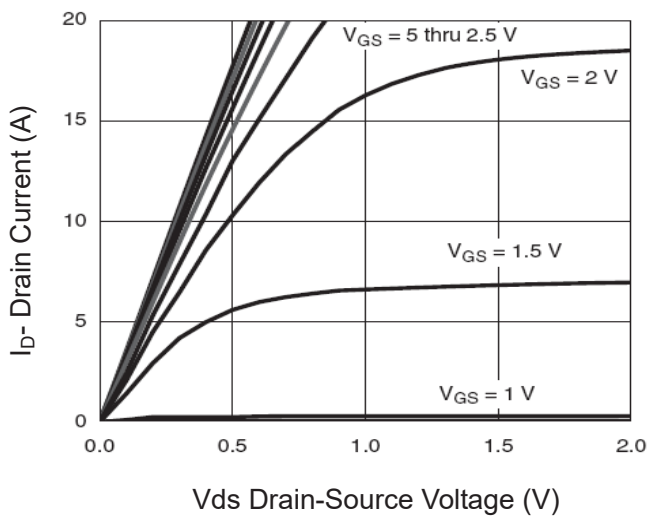
**Figure 2: Switching Waveforms**



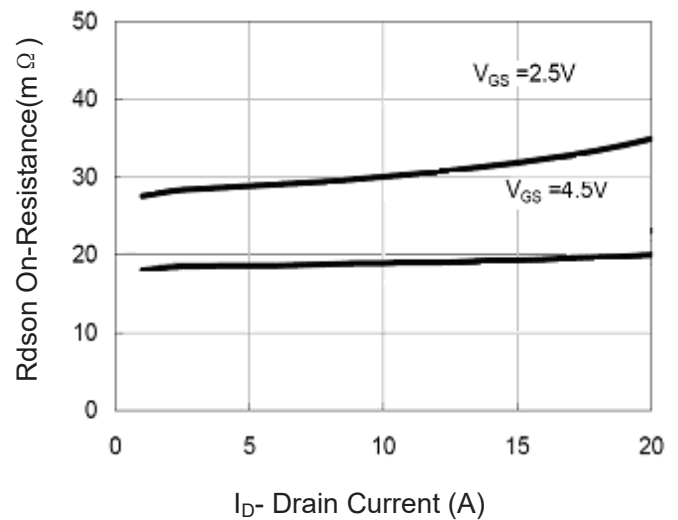
**Figure 3 Power Dissipation**



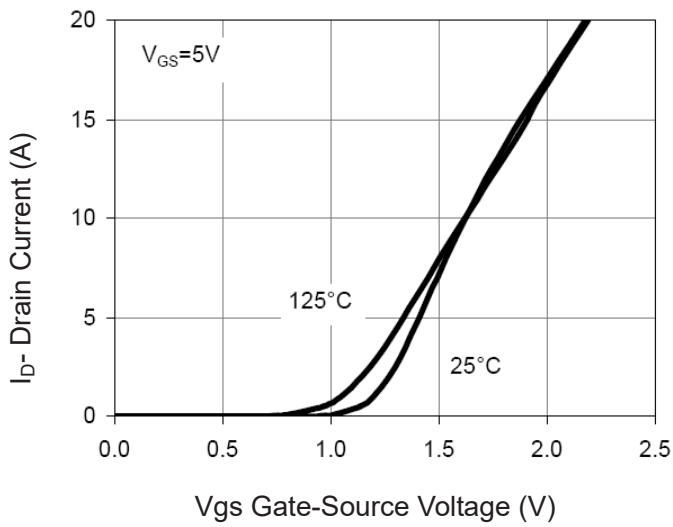
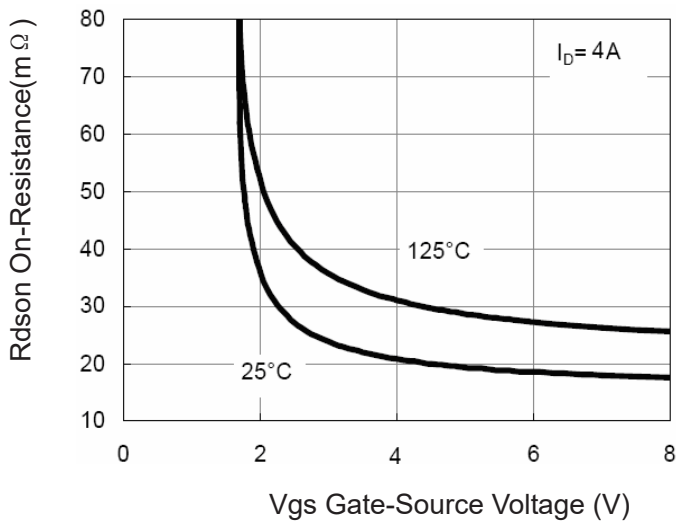
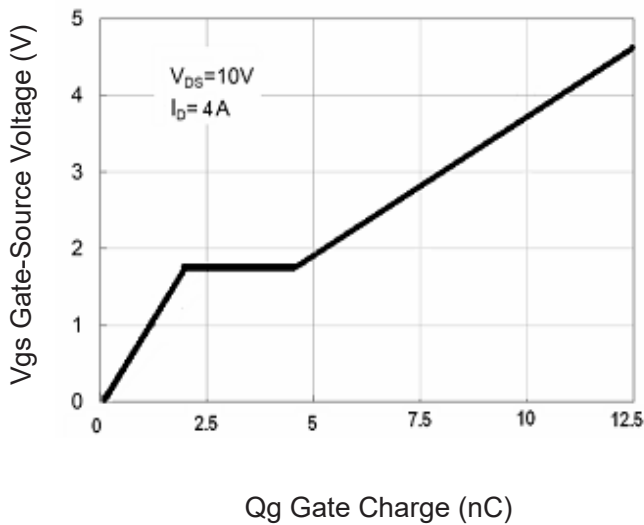
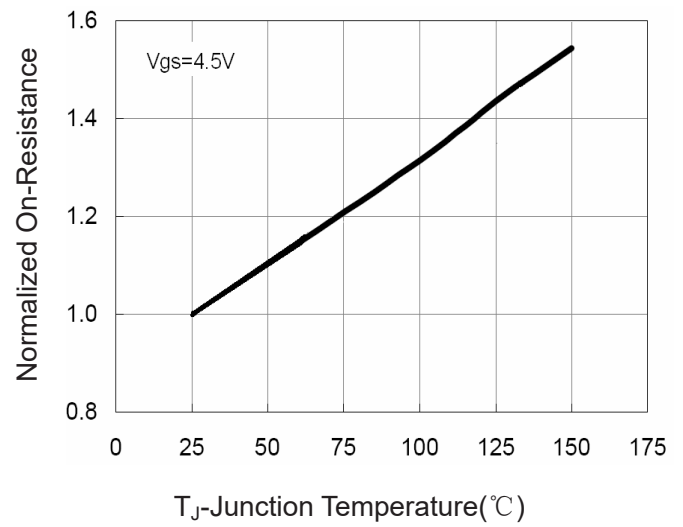
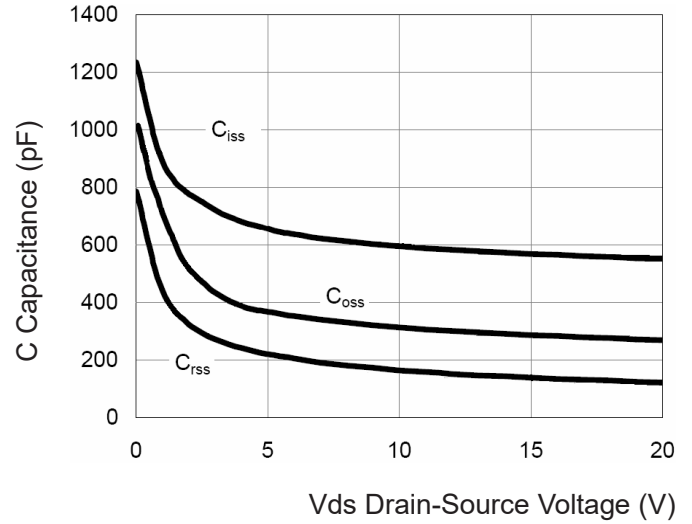
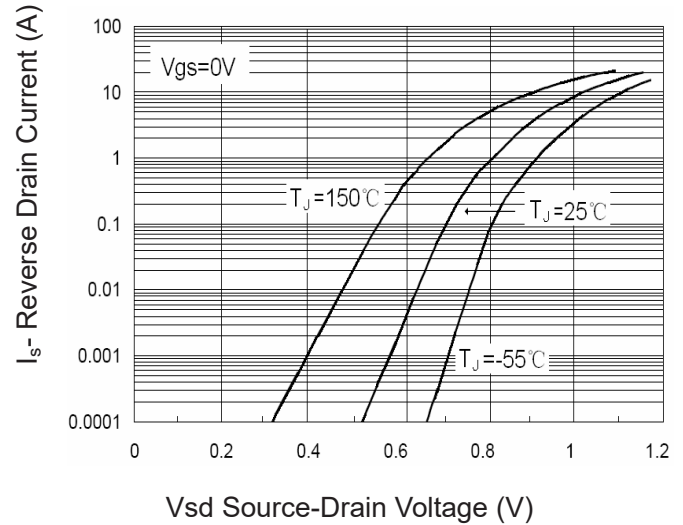
**Figure 4 Drain Current**

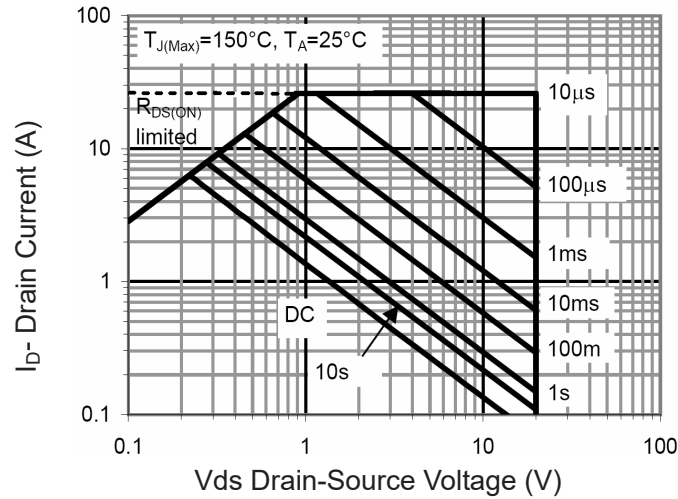


**Figure 5 Output Characteristics**

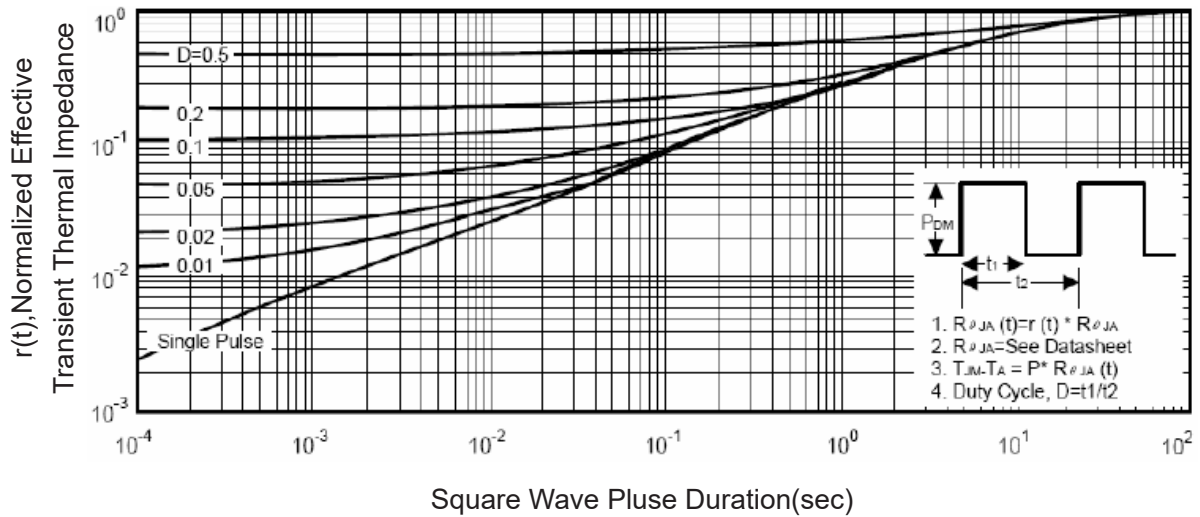


**Figure 6 Drain-Source On-Resistance**


**Figure 7 Transfer Characteristics**

**Figure 9 Rdson vs Vgs**

**Figure 11 Gate Charge**

**Figure 8 Drain-Source On-Resistance**

**Figure 10 Capacitance vs Vds**

**Figure 12 Source- Drain Diode Forward**



**Figure 13 Safe Operation Area**



**Figure 14 Normalized Maximum Transient Thermal Impedance**