

## **Description**

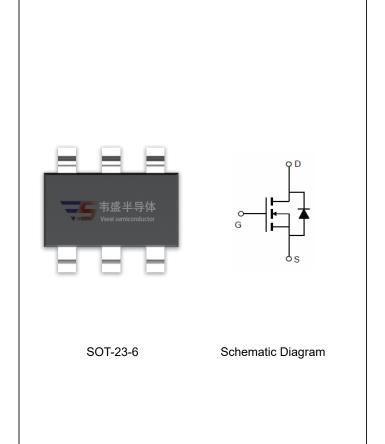
The VSM0104AN uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

#### **General Features**

- V<sub>DS</sub>=100V,I<sub>D</sub>=4A
  - $R_{DS(ON)}\!<\!100m\Omega$  @  $V_{GS}\!=\!10V$  (Typ.84m $\Omega$ )
  - $R_{DS(ON)}$  <118m $\Omega$  @  $V_{GS}$ =4.5V (Typ.94m $\Omega$ )
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E<sub>AS</sub>
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

## **Application**

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



### **Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM0104AN-S6	VSM0104AN	SOT-23-6	Ø180mm	8 mm	3000 units

### Absolute Maximum Ratings (T<sub>A</sub>=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	100	V	
Gate-Source Voltage	Vgs	±20	V	
Drain Current-Continuous	I <sub>D</sub>	4	А	
Drain Current-Continuous(T <sub>C</sub> =100 °C)	I <sub>D</sub> (100℃)	2.8	Α	
Pulsed Drain Current	I <sub>DM</sub>	20	Α	
Maximum Power Dissipation	P <sub>D</sub>	2	W	
Operating Junction and Storage Temperature Range	$T_{J}, T_{STG}$	-55 To 150	$^{\circ}\mathbb{C}$	

### **Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient (Note 2)	R <sub>0JA</sub>	62.5	°C/W
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# Electrical Characteristics (T<sub>A</sub>=25<sup>°</sup>Cunless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics			•			
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V,V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V,V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics (Note 3)			•			
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS}=V_{GS},I_{D}=250\mu A$	1.2	1.5	2.0	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =2A	-	84	100	mΩ
	R <sub>DS(ON)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =2A	-	94	118	mΩ
Forward Transconductance	<b>G</b> FS	V <sub>DS</sub> =5V,I <sub>D</sub> =2A	11	-	-	S
Dynamic Characteristics (Note4)			•			
Input Capacitance	C <sub>lss</sub>	\/ -50\/\/ -0\/	-	882	-	PF
Output Capacitance	Coss	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$	-	54.6	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>	r-1.0Winz	-	36.1	-	PF
Switching Characteristics (Note 4)			•			
Turn-on Delay Time	t <sub>d(on)</sub>	$V_{DD}$ =50V, $R_L$ =25 $\Omega$ $V_{GS}$ =10V, $R_G$ =3 $\Omega$	-	8	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	3	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	24	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	5	-	nS
Total Gate Charge	Qg	V <sub>DS</sub> =50V,I <sub>D</sub> =2A,	-	24.1		nC
Gate-Source Charge	Q <sub>gs</sub>		-	3.1		nC
Gate-Drain Charge	Q <sub>gd</sub>	V <sub>GS</sub> =10V	-	5.5		nC
Drain-Source Diode Characteristics			•			
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =2A	-		1.2	V
Diode Forward Current (Note 2)	Is		-	-	4	Α

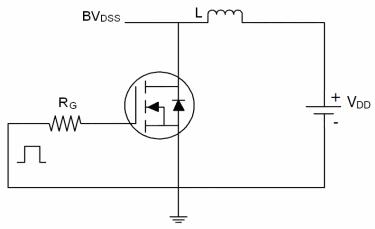
#### Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- 3. Pulse Test: Pulse Width  $\leq$  300µs, Duty Cycle  $\leq$  2%.
- **4.** Guaranteed by design, not subject to production

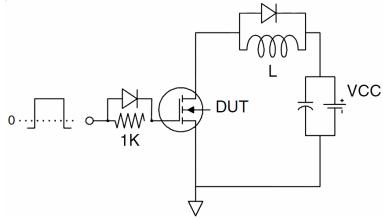


## **Test Circuit**

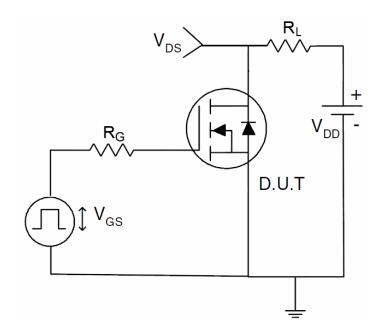
# 1) E<sub>AS</sub> test Circuit



## 2) Gate charge test Circuit

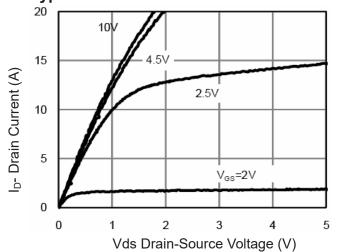


## 3) Switch Time Test Circuit

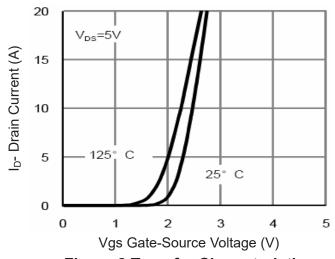




## **Typical Electrical and Thermal Characteristics (Curves)**



**Figure 1 Output Characteristics** 



**Figure 2 Transfer Characteristics** 

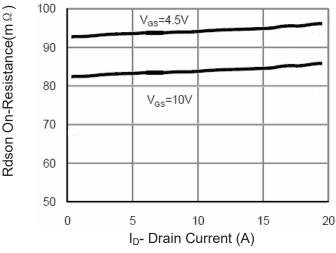
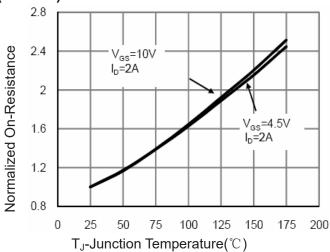


Figure 3 Rdson-Drain Current



**Figure 4 Rdson-Junction Temperature** 

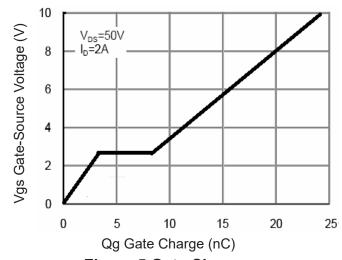


Figure 5 Gate Charge

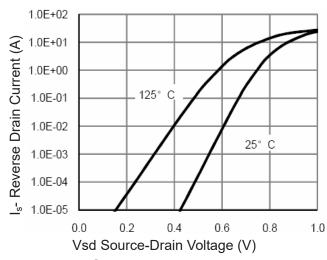


Figure 6 Source- Drain Diode Forward



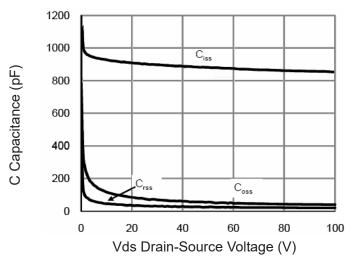
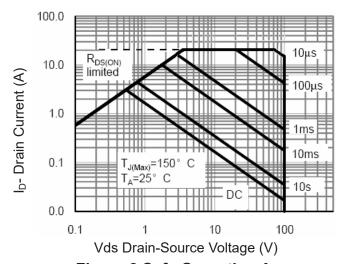


Figure 7 Capacitance vs Vds



**Figure 8 Safe Operation Area** 

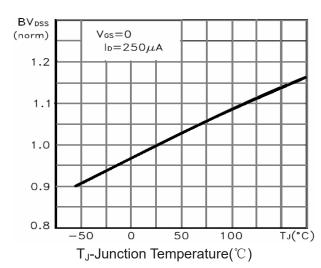


Figure 9 BV<sub>DSS</sub> vs Junction Temperature

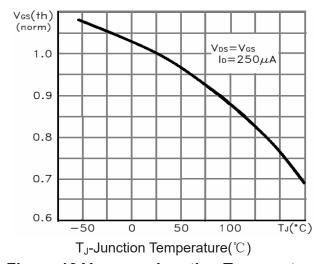


Figure 10 V<sub>GS(th)</sub> vs Junction Temperature

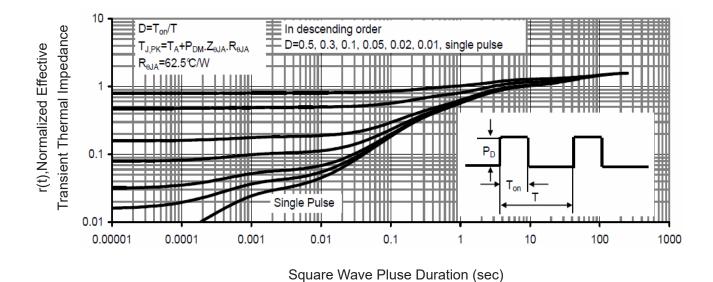


Figure 11 Normalized Maximum Transient Thermal Impedance