

## Description

The VSM57N10 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

## General Features

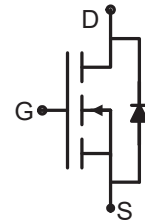
- $V_{DS} = 100V, I_D = 57A$   
 $R_{DS(ON)} < 16m\Omega @ V_{GS}=10V$  (Typ:12m $\Omega$ )
- Special process technology for high ESD capability
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

## Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



TO-251



Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM57N10-T1	VSM57N10	TO-251	-	-	-

## Absolute Maximum Ratings ( $T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	57	A
Drain Current-Continuous( $T_C=100^{\circ}C$ )	$I_D(100^{\circ}C)$	40	A
Pulsed Drain Current	$I_{DM}$	190	A
Maximum Power Dissipation	$P_D$	170	W
Derating factor		1.13	W/ $^{\circ}C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	342	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^{\circ}C$

## Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	0.88	$^{\circ}\text{C/W}$
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## Electrical Characteristics ( $T_c=25^{\circ}\text{C}$ unless otherwise noted)

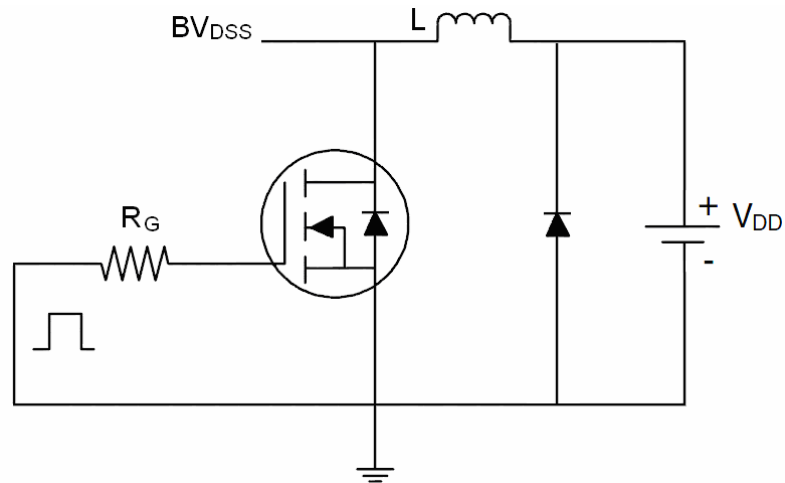
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	100	110	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.5	1.8	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	12	16	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	32	-	-	S
Dynamic Characteristics <sup>(Note4)</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, F=1.0MHz	-	4118	-	PF
Output Capacitance	C <sub>oss</sub>		-	210	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	169	-	PF
Switching Characteristics <sup>(Note 4)</sup>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =50V, I <sub>D</sub> =20A V <sub>GS</sub> =10V, R <sub>GEN</sub> =2.5Ω	-	12	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	55	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	45	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	47	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =50V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	-	111	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	11.5	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	24	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	-	0.85	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>S</sub>		-	-	57	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> = 20A di/dt = 100A/μs <sup>(Note3)</sup>	-	36	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	56	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

## Notes:

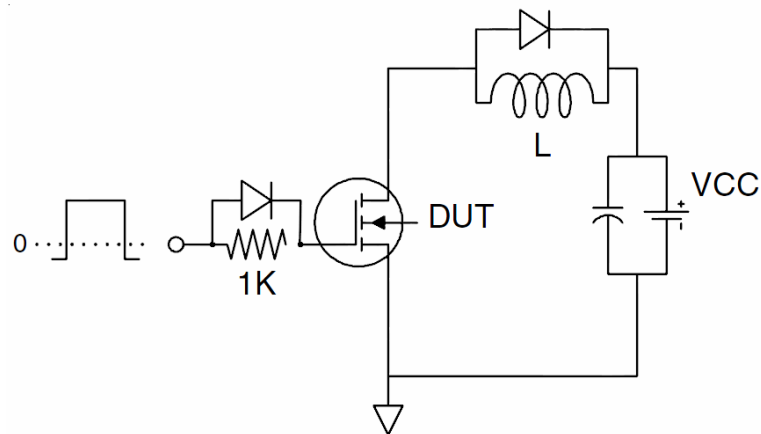
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

## Test Circuit

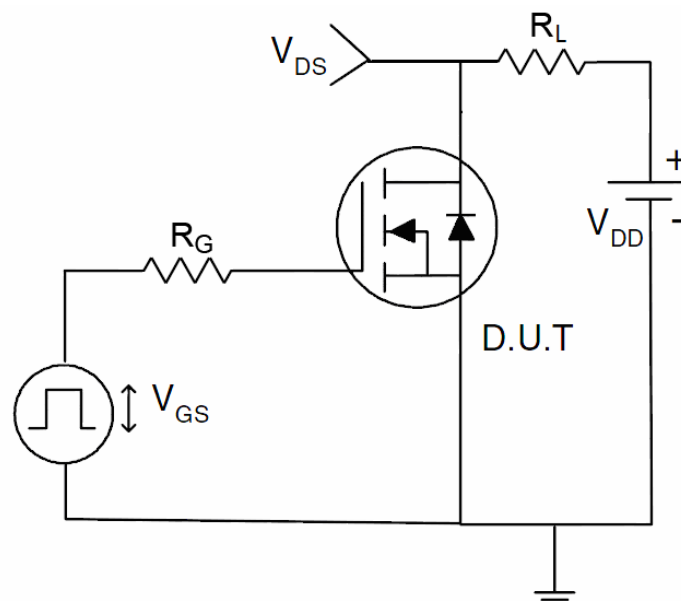
### 1) $E_{AS}$ test Circuit



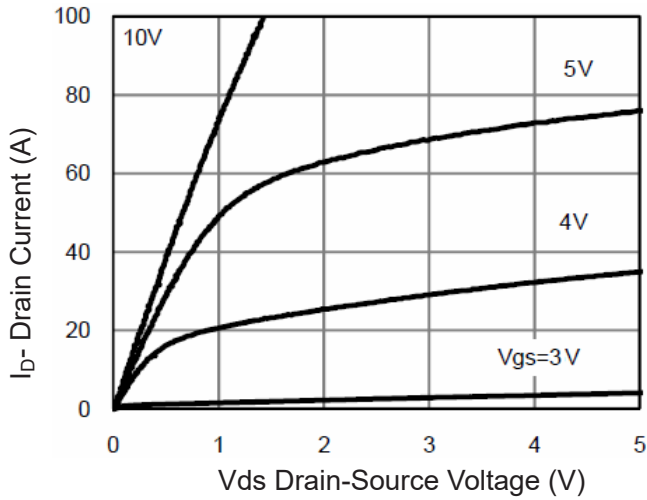
### 2) Gate charge test Circuit



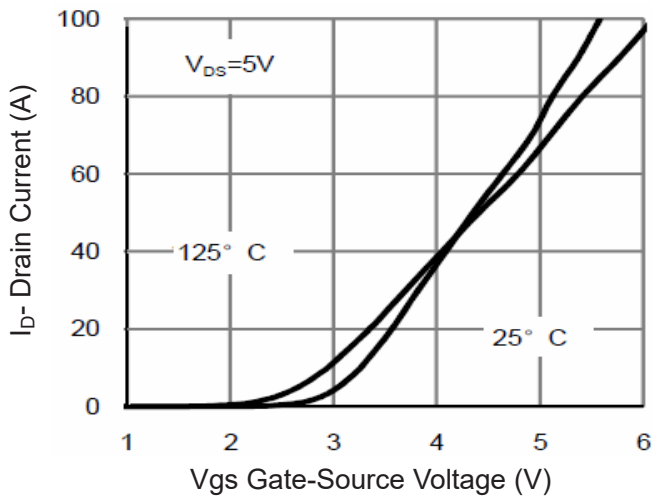
### 3) Switch Time Test Circuit



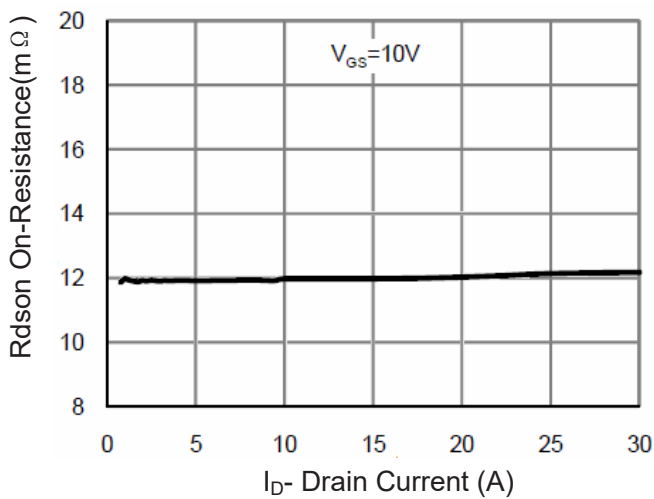
## Typical Electrical and Thermal Characteristics (Curves)



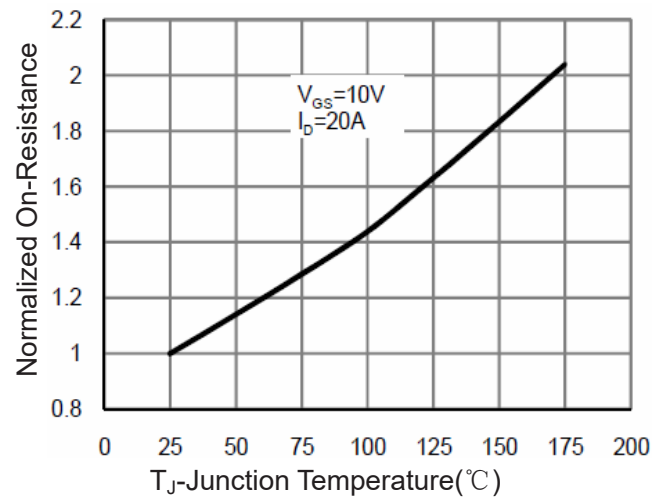
**Figure 1 Output Characteristics**



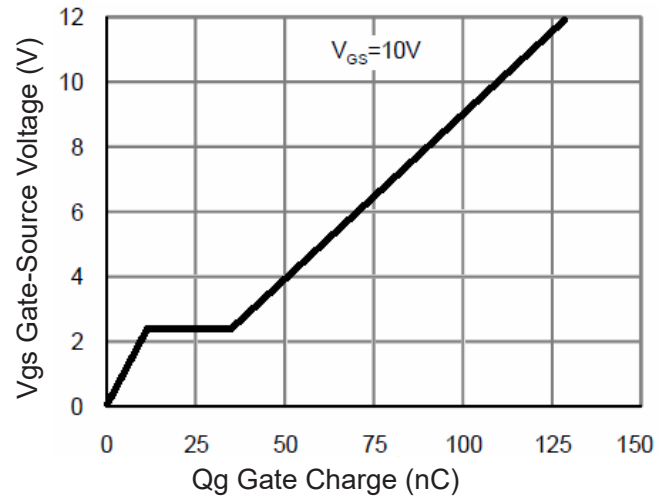
**Figure 2 Transfer Characteristics**



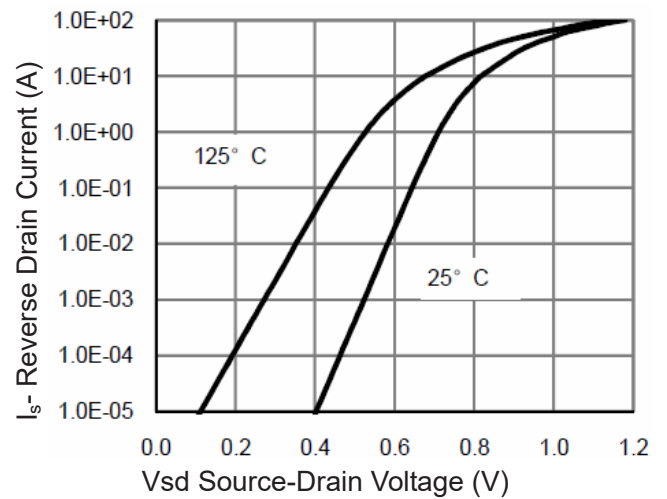
**Figure 3  $R_{DS(on)}$ - Drain Current**



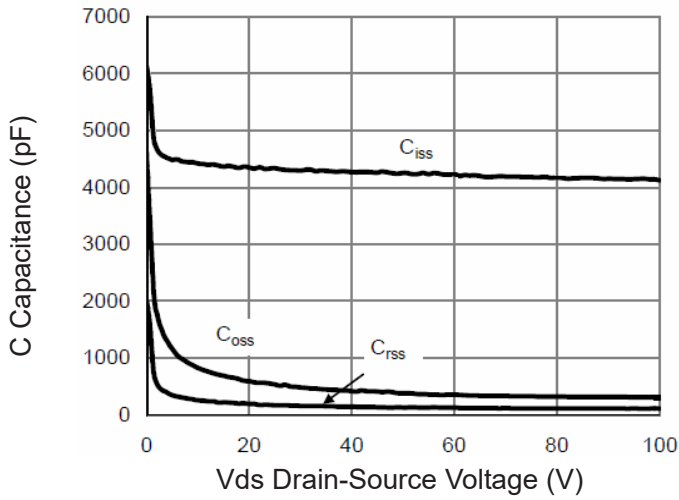
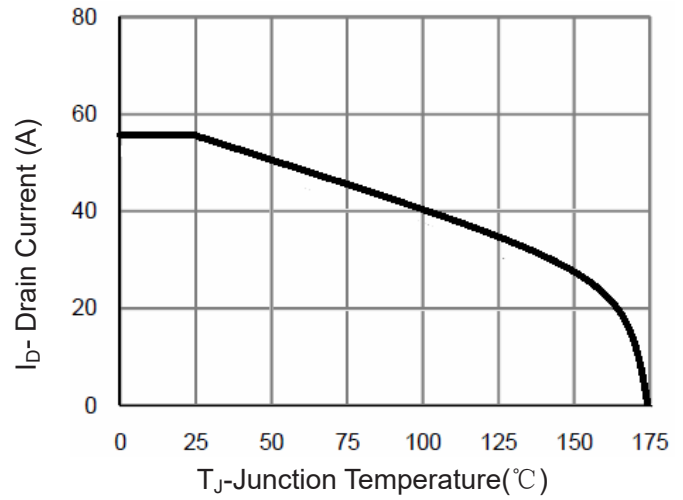
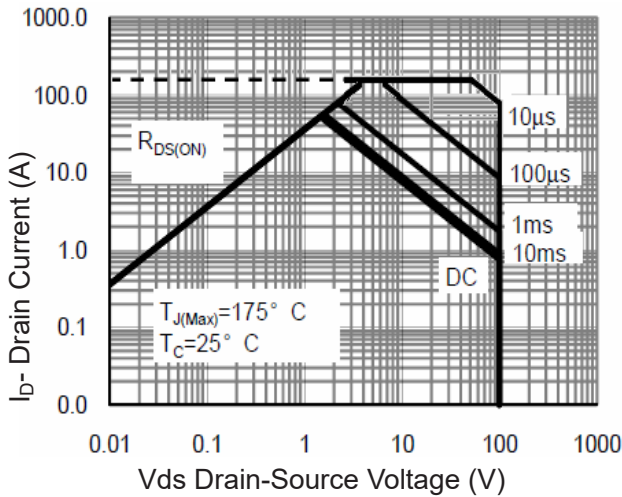
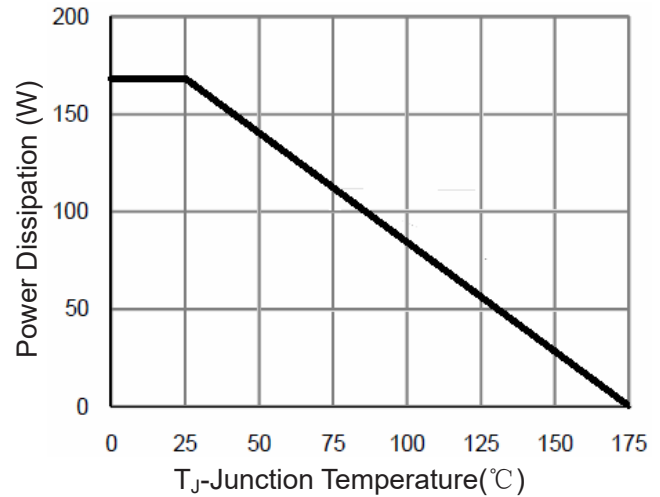
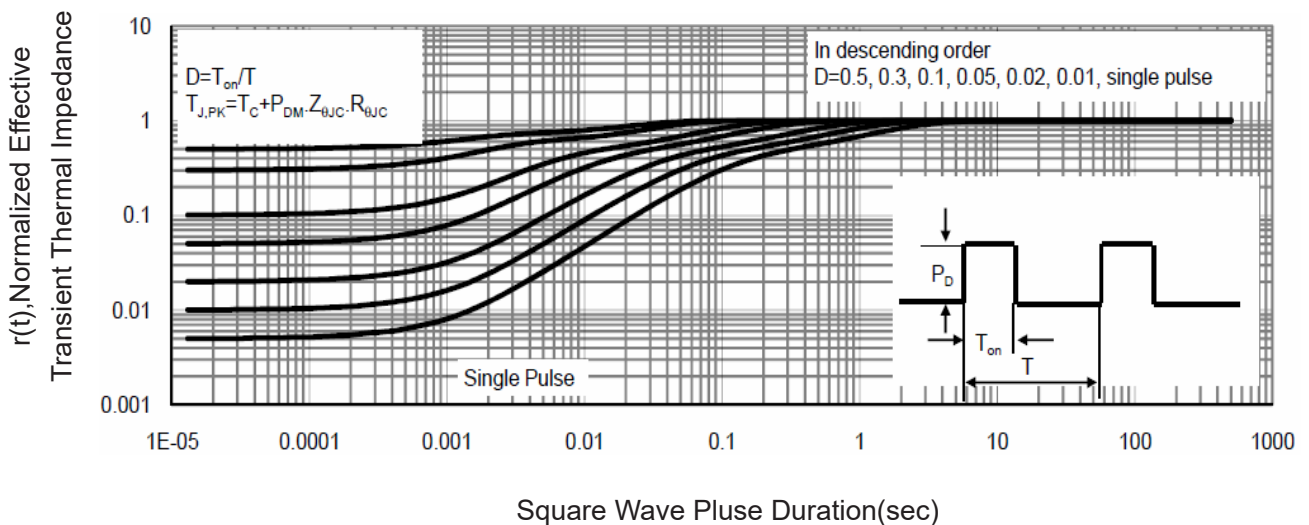
**Figure 4  $R_{DS(on)}$ -Junction Temperature**



**Figure 5 Gate Charge**



**Figure 6 Source- Drain Diode Forward**


**Figure 7 Capacitance vs Vds**

**Figure 9 Id Current De-rating**

**Figure 8 Safe Operation Area**

**Figure 10 Power De-rating**

**Figure 11 Normalized Maximum Transient Thermal Impedance**