

Description

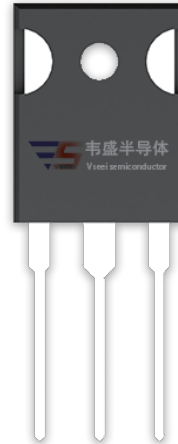
The VSM290N10 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of other applications.

General Features

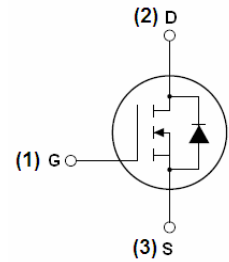
- $V_{DSS} = 100V, I_D = 290A$
 $R_{DS(ON)} < 3.2m\Omega @ V_{GS}=10V$ (Typ: $2.7m\Omega$)
- Good stability and uniformity with high E_{AS}
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

- DC motor drive
- High efficiency synchronous rectification in SMPS
- Uninterruptible power supply
- High speed power switching
- Hard switched and high frequency circuits



TO-247



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM290N10-T7	VSM290N10	TO-247	-	-	-

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	290	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D(100^\circ C)$	200	A
Pulsed Drain Current	I_{DM}	1120	A
Maximum Power Dissipation	P_D	460	W
Derating factor		3.07	W/ $^\circ C$
Single pulse avalanche energy ^(Note 3)	E_{AS}	3500	mJ
Peak Diode Recovery dv/dt ^(Note 4)	dv/dt	10	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 1)	$R_{\theta JC}$	0.33	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

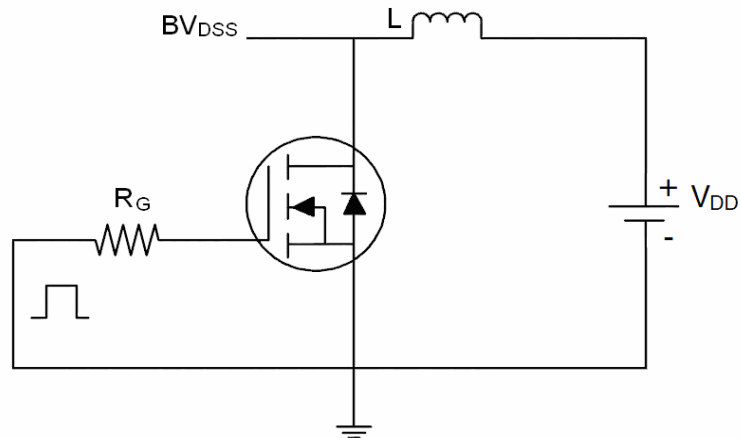
Parameter		Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V I _D =250μA	100	110	-	V
Zero Gate Voltage Drain Current		I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current		I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±200	nA
On Characteristics							
Gate Threshold Voltage		V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
Drain-Source On-State Resistance	25°C	R _{DS(ON)}	V _{GS} =10V, I _D =40A	-	2.7	3.2	mΩ
Forward Transconductance		g _{FS}	V _{DS} =25V, I _D =40A	310	-	-	S
Dynamic Characteristics							
Input Capacitance		C _{iss}	V _{DS} =50V, V _{GS} =0V, F=1.0MHz	-	16000	-	PF
Output Capacitance		C _{oss}		-	1352	-	PF
Reverse Transfer Capacitance		C _{rss}		-	1061	-	PF
Switching Characteristics							
Turn-on Delay Time		t _{d(on)}	V _{DD} =50V, I _D =40A V _{GS} =10V, R _{GEN} =1.2Ω (Note2)	-	44.6	-	nS
Turn-on Rise Time		t _r		-	29.4	-	nS
Turn-Off Delay Time		t _{d(off)}		-	139.8	-	nS
Turn-Off Fall Time		t _f		-	36.4	-	nS
Total Gate Charge		Q _g	V _{DS} =30V, I _D =30A V _{GS} =10V	-	469	-	nC
Gate-Source Charge		Q _{gs}		-	99	-	nC
Gate-Drain Charge		Q _{gd}		-	148	-	nC
Drain-Source Diode Characteristics							
Diode Forward Voltage		V _{SD}	V _{GS} =0V, I _S =40A	-	-	1.2	V
Reverse Recovery Time		t _{rr}	T _J = 25°C, I _F = 40A di/dt = 100A/μs ^(Note2)	-	87.9	-	nS
Reverse Recovery Charge		Q _{rr}		-	129	-	nC
Forward Turn-On Time		t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes

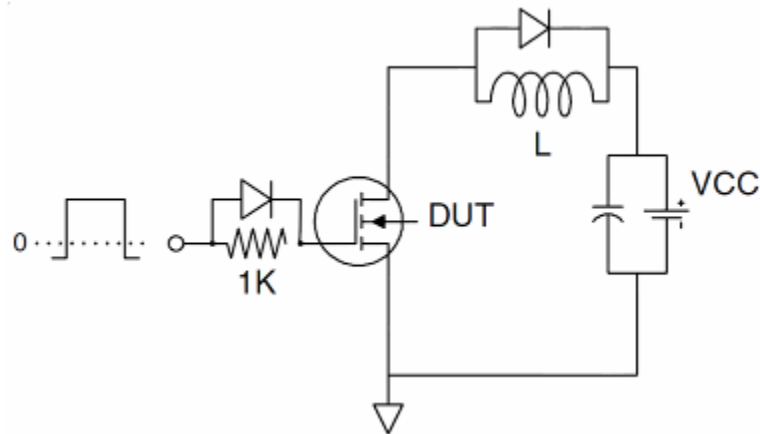
1. Surface Mounted on FR4 Board, $t \leq 10$ sec.
2. Pulse Test: Pulse Width $\leq 400\mu s$, Duty Cycle $\leq 2\%$.
3. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_{GS}=10V, L=1\text{mH}, R_g=25\Omega$
4. $I_{SD} \leq 125A, di/dt \leq 260A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^{\circ}\text{C}$

Test Circuit

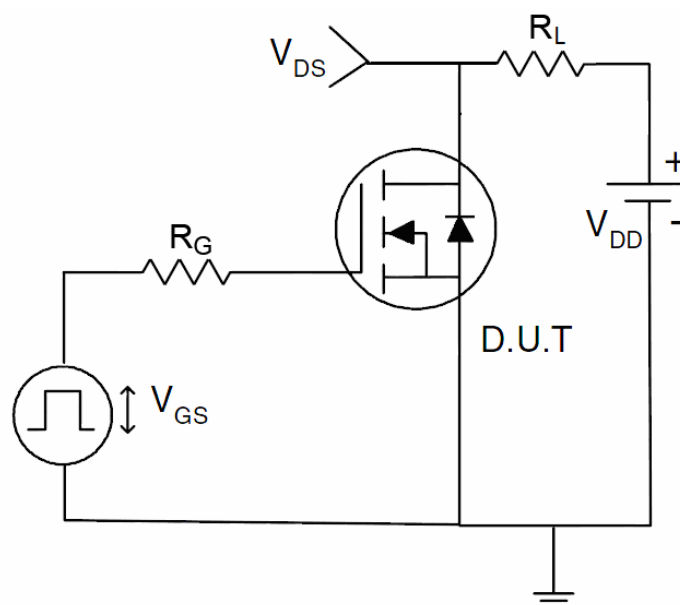
1) E_{AS} Test Circuits



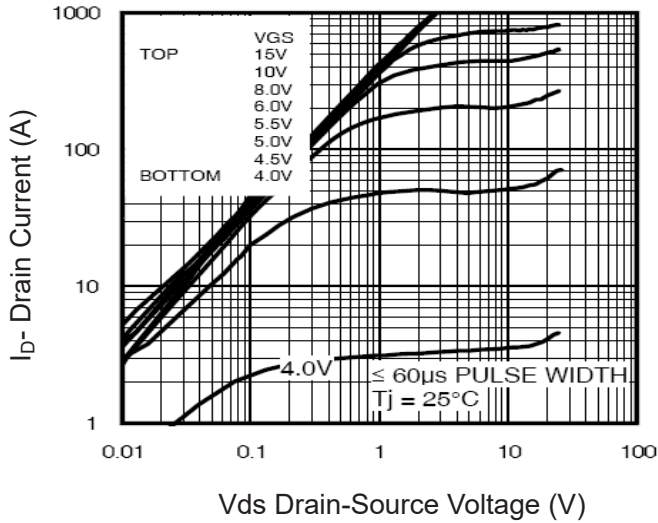
2) Gate Charge Test Circuit:



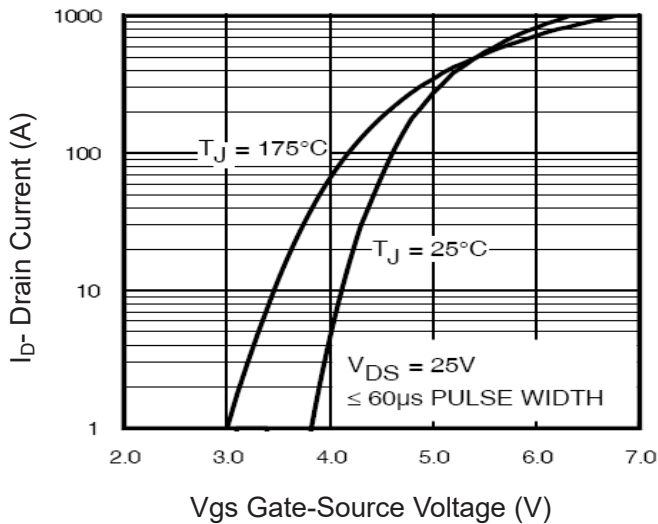
3) Switch Time Test Circuit:



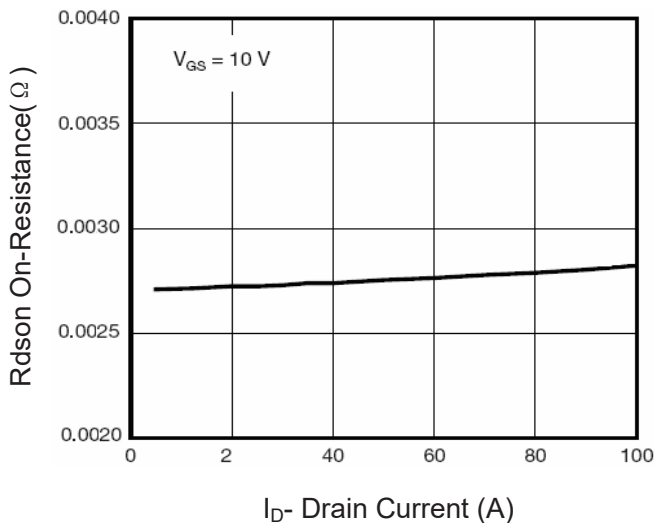
Typical Electrical and Thermal Characteristics



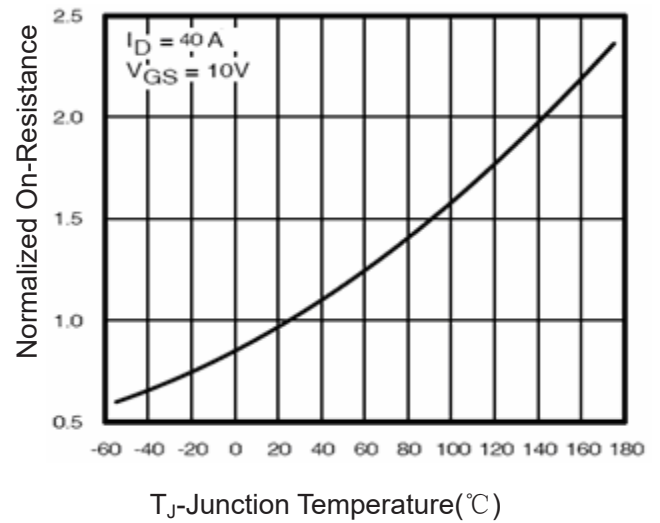
V_{DS} Drain-Source Voltage (V)
Figure 1 Output Characteristics



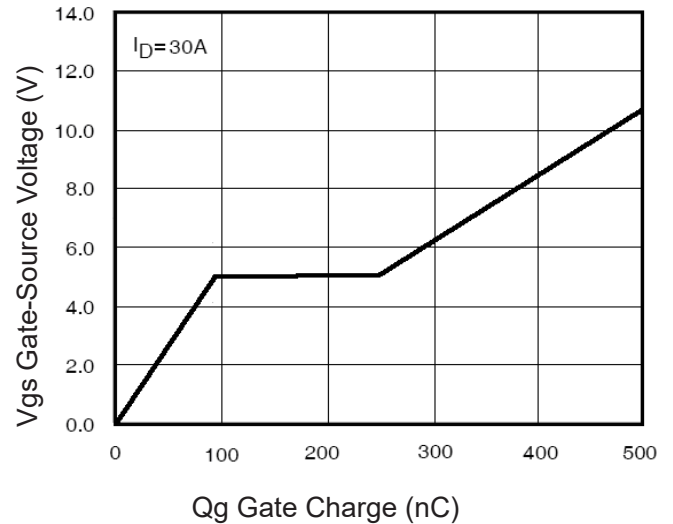
V_{GS} Gate-Source Voltage (V)
Figure 2 Transfer Characteristics



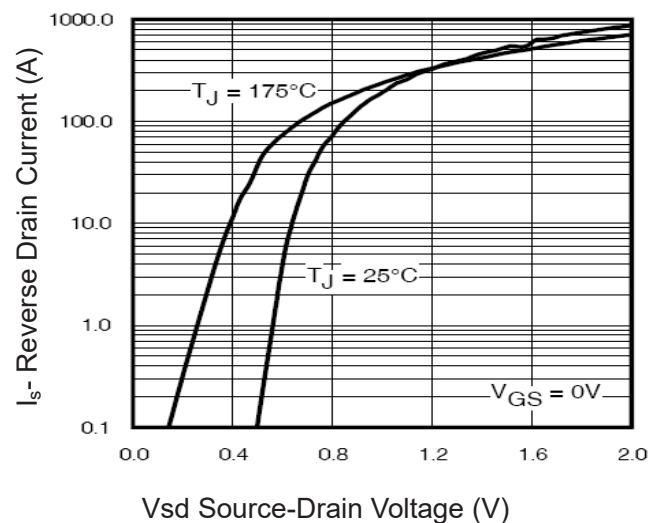
I_D - Drain Current (A)
Figure 3 $R_{DS(on)}$ - Drain Current



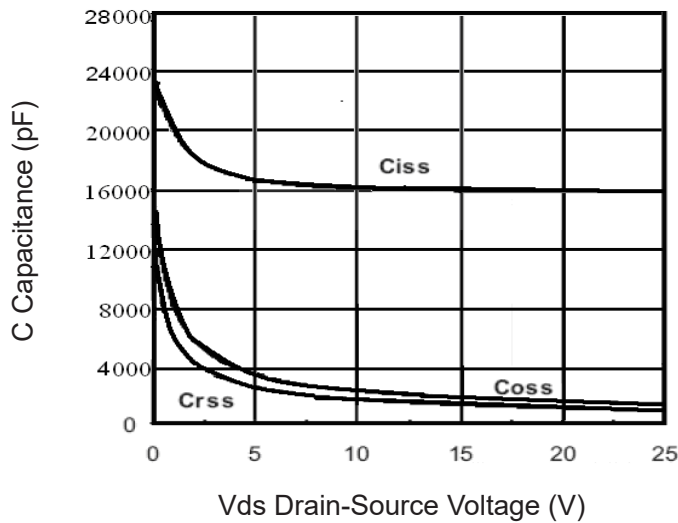
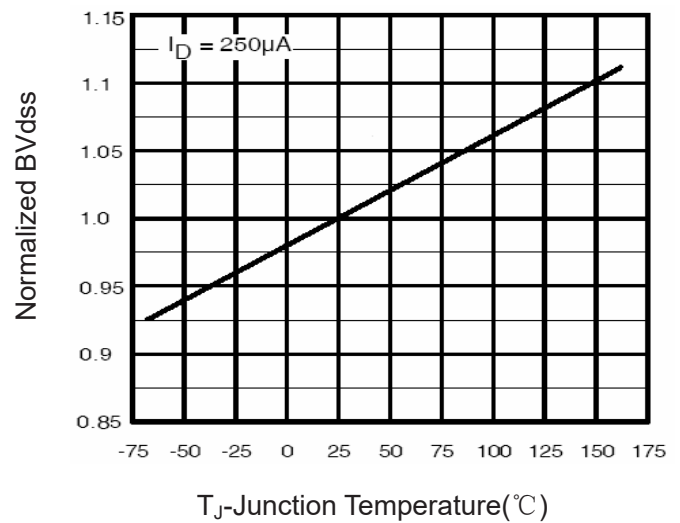
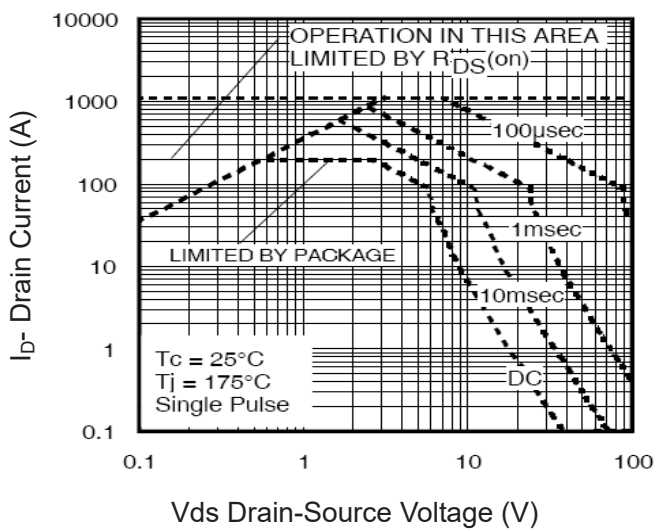
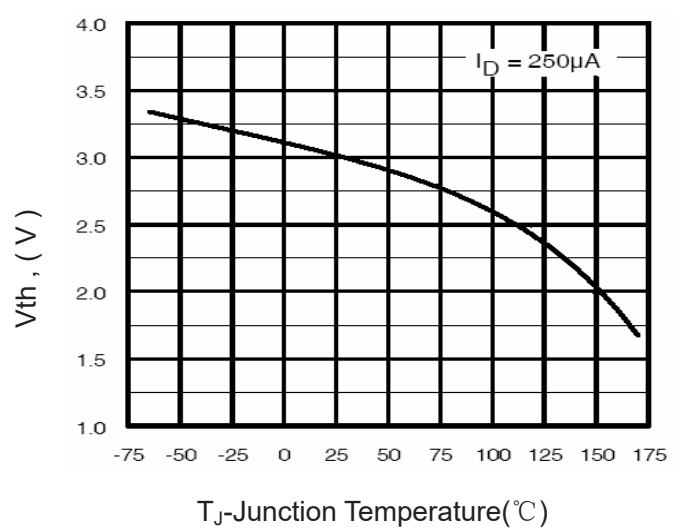
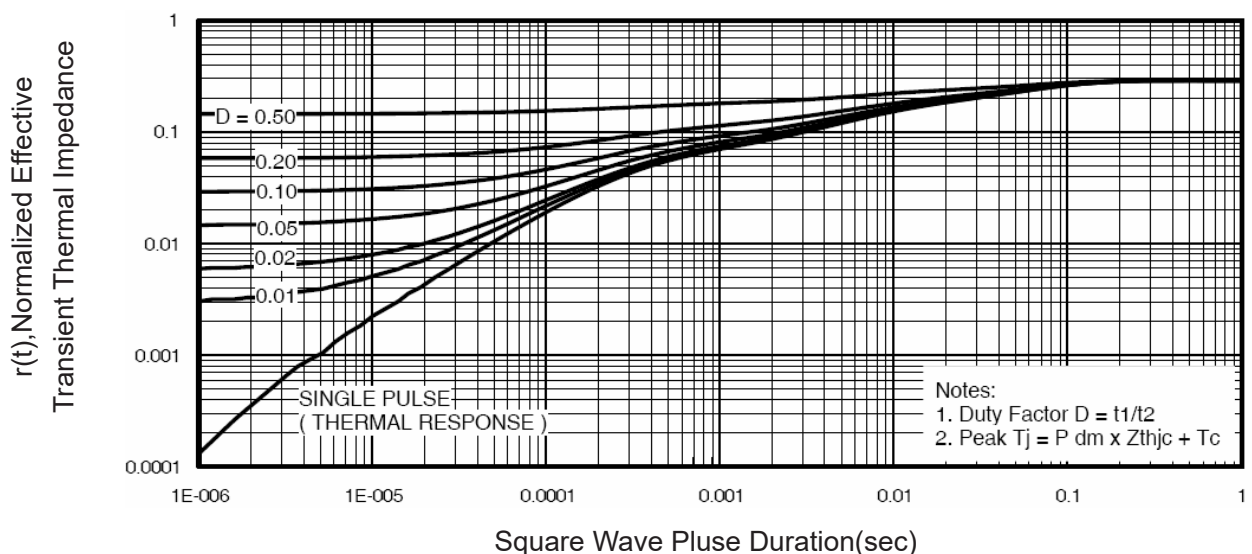
T_J -Junction Temperature($^\circ\text{C}$)
Figure 4 $R_{DS(on)}$ -Junction Temperature



Q_g Gate Charge (nC)
Figure 5 Gate Charge



V_{SD} Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 BV_{DSS} vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 V_{GS(th)} vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance