Description

The VSM120N04 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

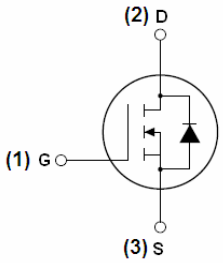
General Features

- V_{DS} =40V,I_D =120A
  $R_{DS(ON)}$ <4 mΩ @ V_{GS}=10V
  $R_{DS(ON)}$ <7 mΩ @ V_{GS}=4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

TO-220C



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM120N04-TC	VSM120N04	TO-220C	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	120	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	85	A
Pulsed Drain Current	I_{DM}	330	A
Maximum Power Dissipation	P_D	130	W
Derating factor		0.87	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	1080	mJ

Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	1.15	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

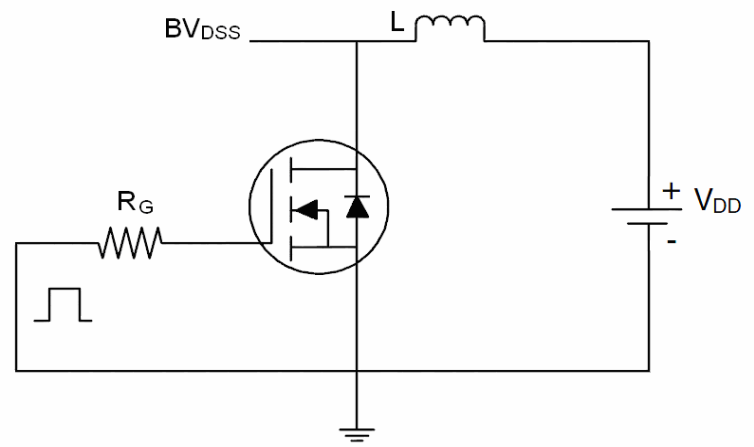
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	40	45	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.2	1.9	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	3.2	4.0	mΩ
		V_{GS}=4.5V, I_D=10A	-	5.5	7.0	
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=20A	26	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=20V,V_{GS}=0V, F=1.0MHz	-	5400	-	PF
Output Capacitance	C_{oss}		-	970	-	PF
Reverse Transfer Capacitance	C_{rss}		-	380	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=20V,I_D=2A,R_L=1Ω V_{GS}=10V,R_G=3Ω	-	15	-	nS
Turn-on Rise Time	t_r		-	18	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	52	-	nS
Turn-Off Fall Time	t_f		-	23	-	nS
Total Gate Charge	Q_g	V_{DS}=20V,I_D=20A, V_{GS}=10V	-	75		nC
Gate-Source Charge	Q_{gs}		-	10.5		nC
Gate-Drain Charge	Q_{gd}		-	17		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=40A	-		1.2	V
Diode Forward Current (Note 2)	I_S		-	-	120	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 40A di/dt = 100A/μs (Note3)	-	42	-	nS
Reverse Recovery Charge	Qrr		-	45	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

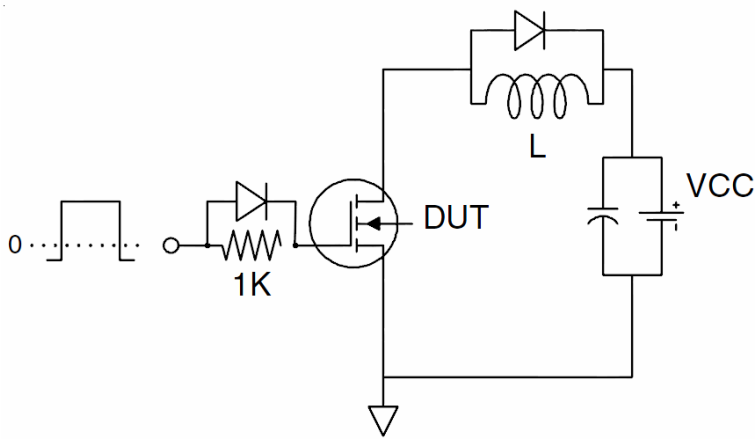
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E_{AS} condition : Tj=25℃,V_{DD}=20V,V_G=10V,L=1mH,Rg=25Ω，I_{AS}=46.5A

Test circuit

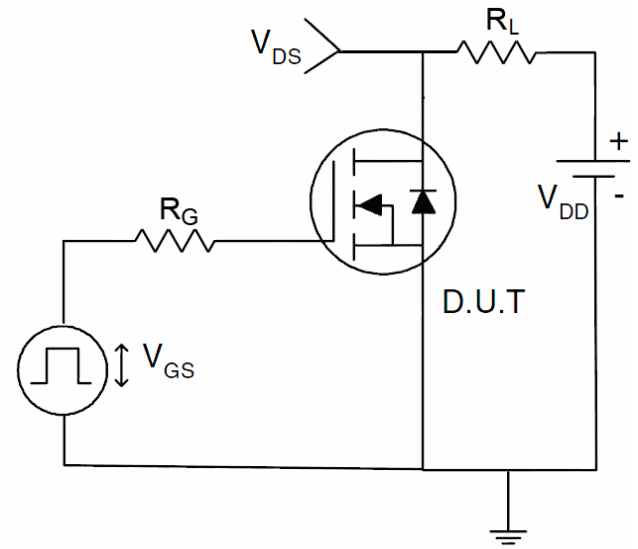
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

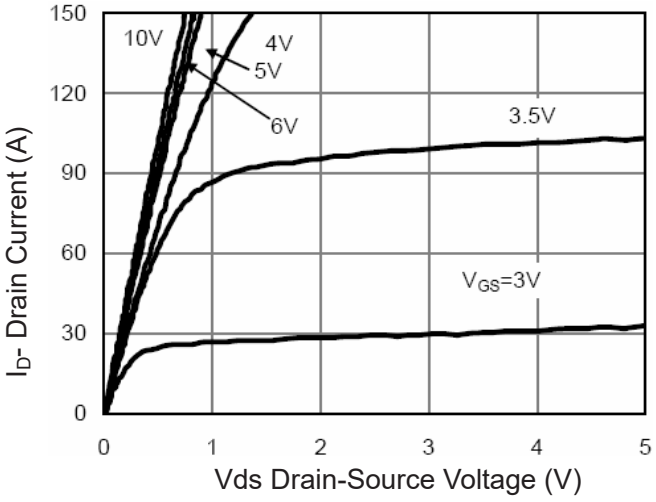


Figure 1 Output Characteristics

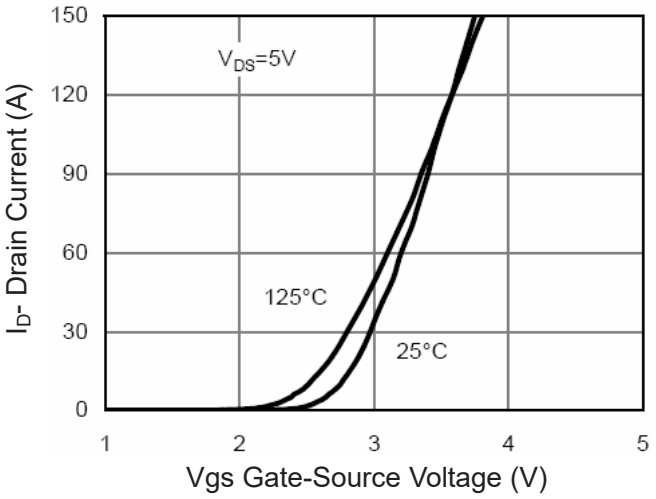


Figure 2 Transfer Characteristics

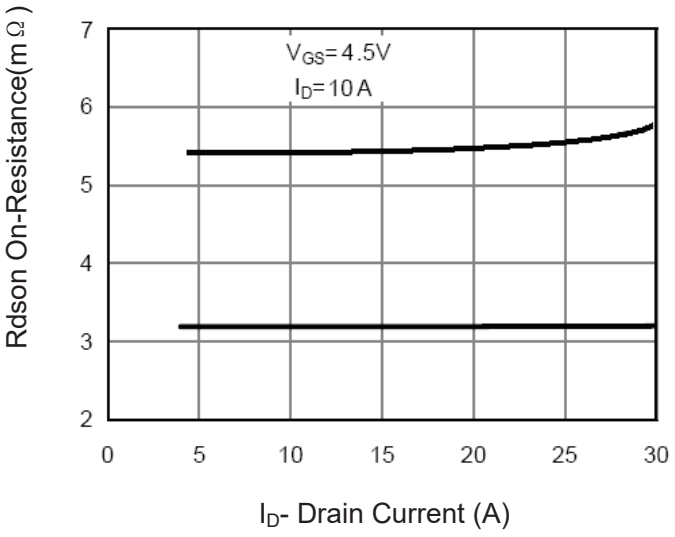


Figure 3 Rdson- Drain Current

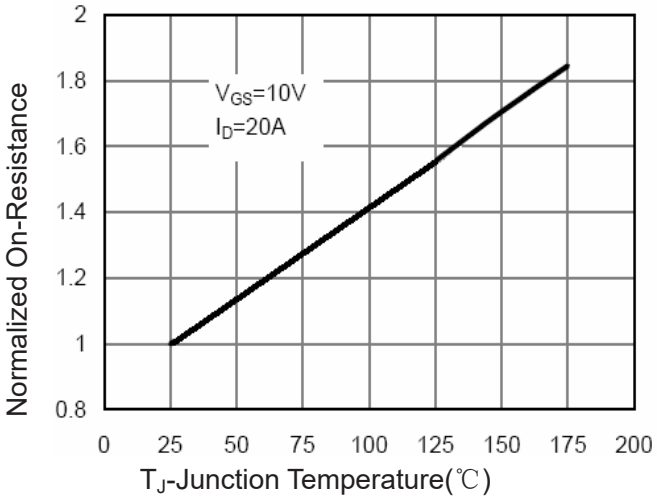


Figure 4 Rdson-JunctionTemperature

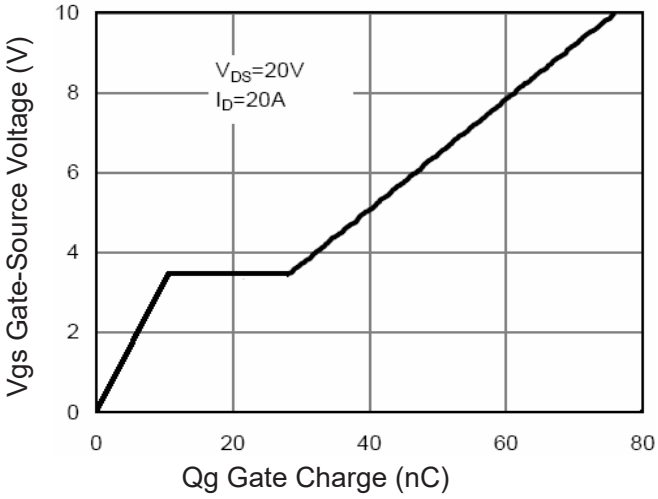


Figure 5 Gate Charge

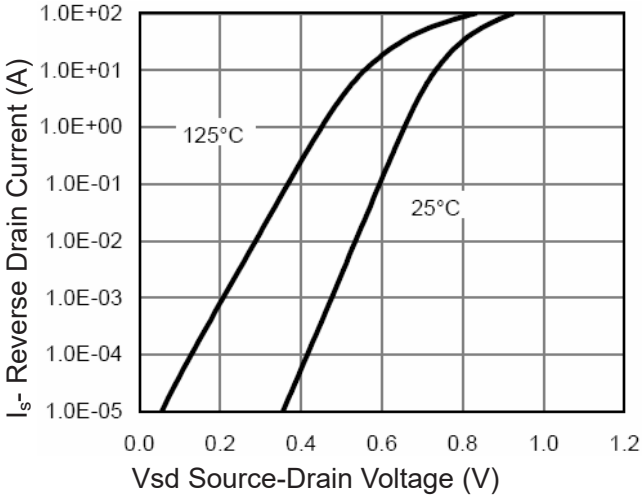


Figure 6 Source- Drain Diode Forward

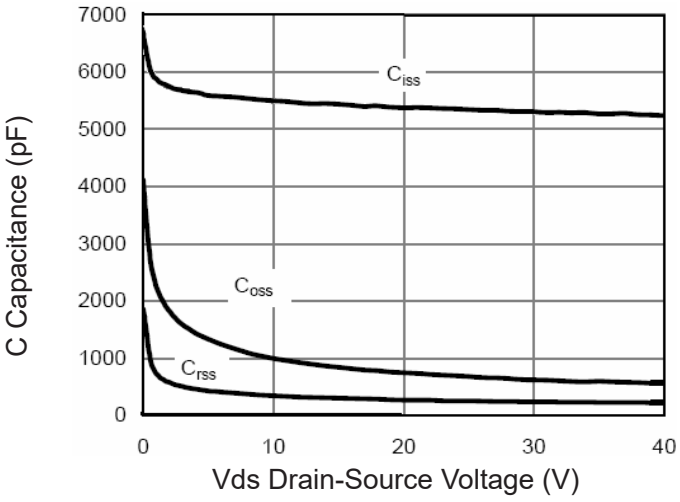


Figure 7 Capacitance vs Vds

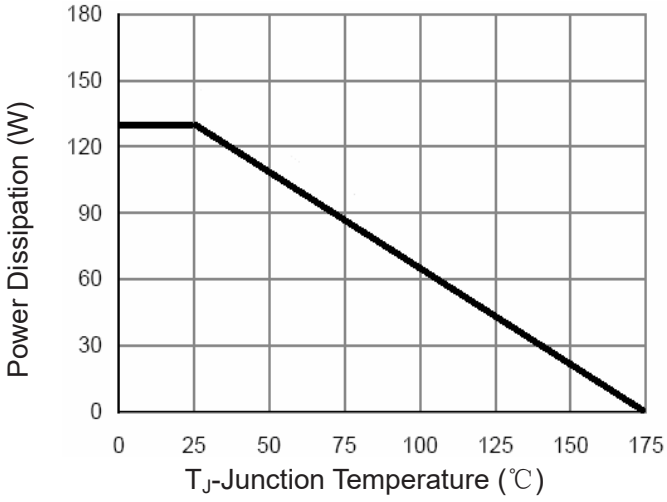


Figure 9 Power De-rating

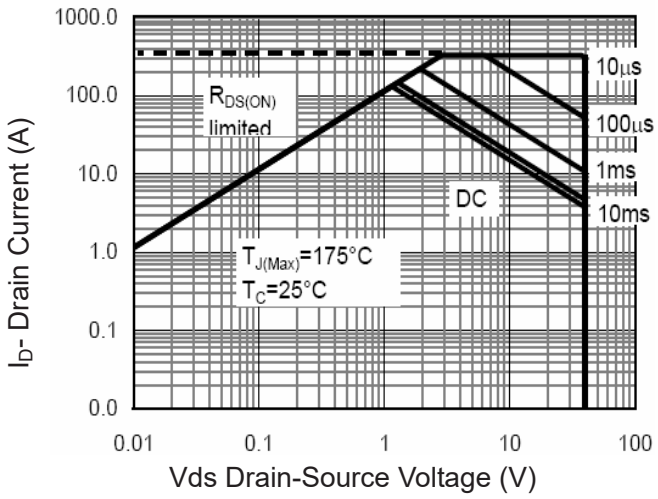


Figure 8 Safe Operation Area

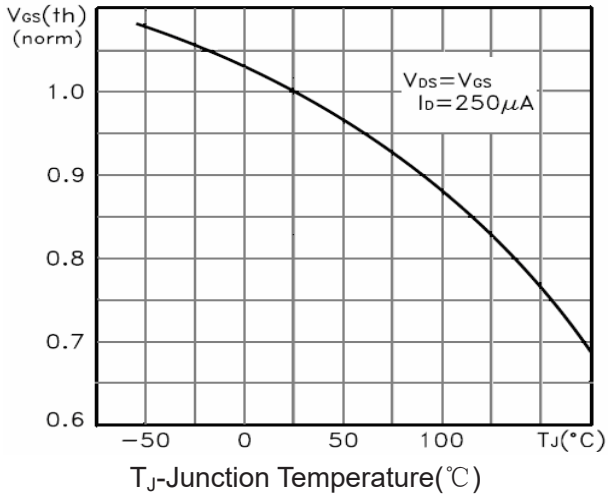


Figure 10 $V_{GS(th)}$ vs Junction Temperature

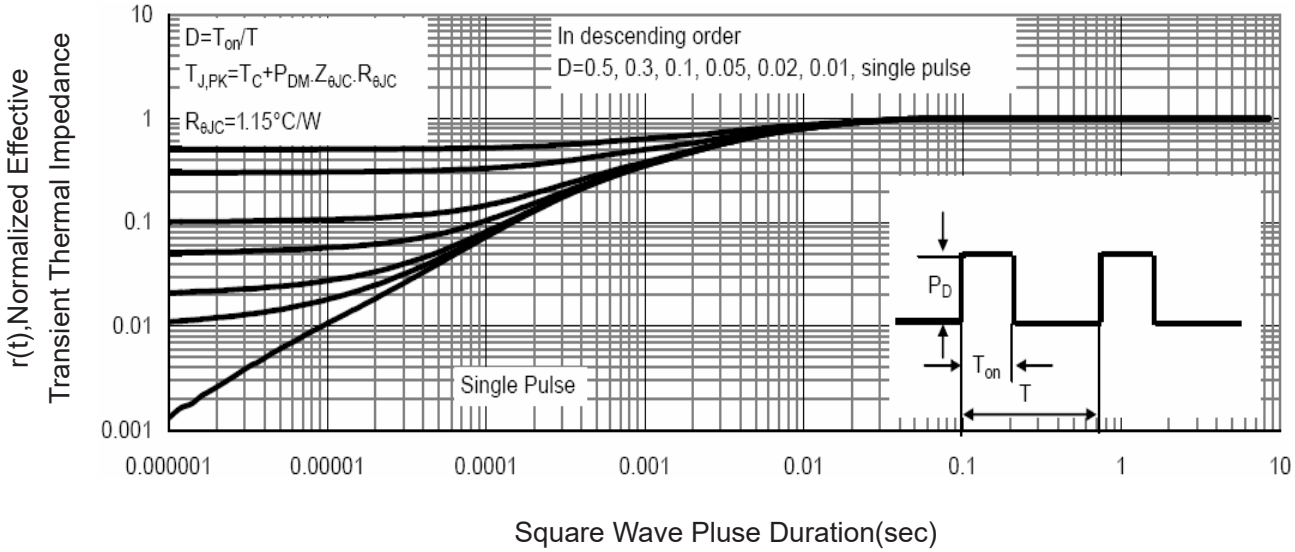


Figure 11 Normalized Maximum Transient Thermal Impedance