

Description

The VSM120N04 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

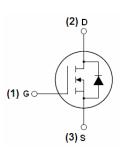
General Features

- V_{DS} =40V, I_{D} =120A $R_{DS(ON)}$ <4.0mΩ @ V_{GS} =10V $R_{DS(ON)}$ <7mΩ @ V_{GS} =4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply





TO-252

Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM120N04-T2	VSM120N04	TO-252	-	-	-

Absolute Maximum Ratings (T_C=25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	40	V	
Gate-Source Voltage	V _G s	±20	V	
Drain Current-Continuous	I _D	120	А	
Drain Current-Continuous(T _C =100 °C)	I _D (100℃)	85	Α	
Pulsed Drain Current	I _{DM}	330	Α	
Maximum Power Dissipation	P _D	120	W	
Derating factor		0.8	W/℃	
Single pulse avalanche energy (Note 5)	E _{AS}	1080	mJ	
Operating Junction and Storage Temperature Range	T_{J}, T_{STG}	-55 To 175	$^{\circ}\!\mathbb{C}$	



Thermal Characteristic

Thermal Resistance,Junction-to-Case ^(Note 2)	$R_{ heta JC}$	1.25	°C/W	
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Electrical Characteristics (T_C=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics			•	•		
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	40	45	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)			•	•		
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250µA	1.2	1.8	2.5	V
Orain-Source On-State Resistance	В	V _{GS} =10V, I _D =20A	-	3.6	4.0	mΩ
	R _{DS(ON)}	V _{GS} =4.5V, I _D =10A	-	5.8	7.0	
Forward Transconductance	g FS	V _{DS} =10V,I _D =20A	26	-	-	S
Dynamic Characteristics (Note4)			•			
Input Capacitance	C _{lss}	.,	-	5400	-	PF
Output Capacitance	C _{oss}	V_{DS} =20V, V_{GS} =0V, F=1.0MHz	-	970	-	PF
Reverse Transfer Capacitance	C _{rss}	F-1.0IVIDZ	-	380	-	PF
Switching Characteristics (Note 4)			•			
Turn-on Delay Time	t _{d(on)}	V_{DD} =20V, I_D =2A, R_L =1 Ω	-	15	-	nS
Turn-on Rise Time	t _r		-	18	-	nS
Turn-Off Delay Time	t _{d(off)}	V_{GS} =10 V , R_{G} =3 Ω	-	52	-	nS
Turn-Off Fall Time	t _f		-	23	-	nS
Total Gate Charge	Qg	V -20V I -20A	-	75		nC
Gate-Source Charge	Q _{gs}	$V_{DS}=20V,I_{D}=20A,$ $V_{GS}=10V$	-	10.5		nC
Gate-Drain Charge	Q_{gd}	V _{GS} -10V	-	17		nC
Drain-Source Diode Characteristics	•		•	•		
Diode Forward Voltage (Note 3)	V_{SD}	V _{GS} =0V,I _S =40A	-		1.2	V
Diode Forward Current (Note 2)	Is		-	-	120	Α
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF = 40A	-	42	-	nS
Reverse Recovery Charge	Qrr	di/dt = 100A/µs ^(Note3)	-	45	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

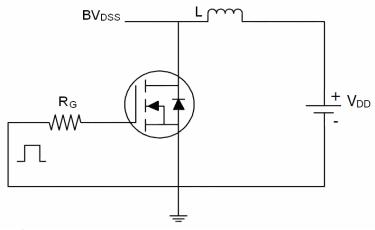
Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- **3.** Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.
- **4.** Guaranteed by design, not subject to production
- $\textbf{5.}~E_{AS}~condition: Tj=25\,^{\circ}\text{C}, V_{DD}=20\text{V}, V_{G}=10\text{V}, L=1\text{mH}, Rg=25\Omega,~I_{AS}=46.5\text{A}$

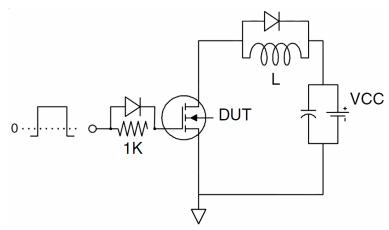


Test circuit

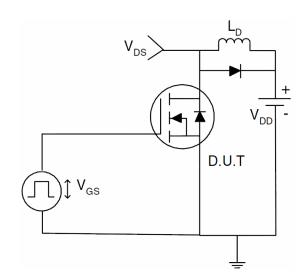
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit





Typical Electrical and Thermal Characteristics (Curves)

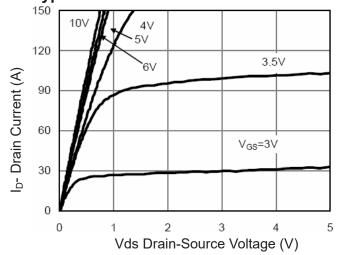


Figure 1 Output Characteristics

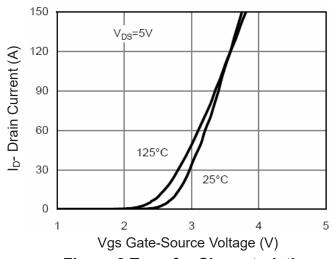


Figure 2 Transfer Characteristics

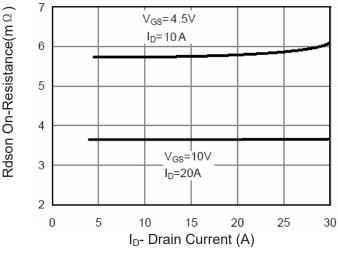


Figure 3 Rdson-Drain Current

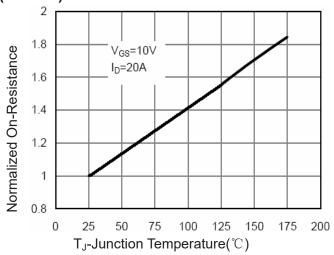


Figure 4 Rdson-JunctionTemperature

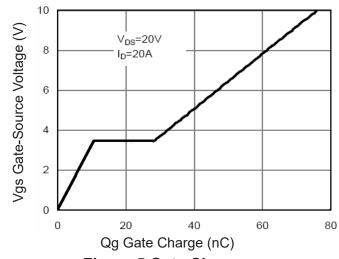


Figure 5 Gate Charge

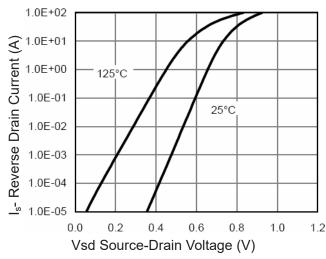
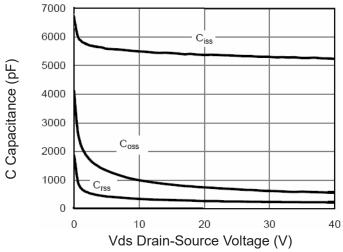


Figure 6 Source- Drain Diode Forward

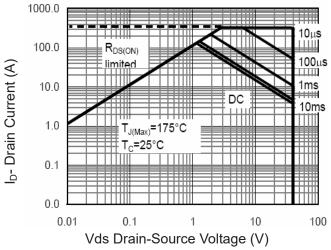




180 150 Power Dissipation (W) 120 90 60 30 0 0 25 50 75 100 125 150 175 T_J-Junction Temperature (°C)

Figure 7 Capacitance vs Vds

Figure 9 Power De-rating



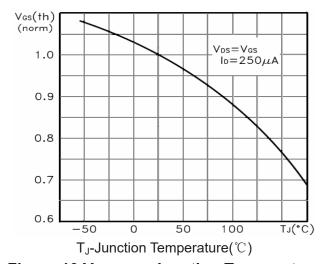


Figure 8 Safe Operation Area

Figure 10 V_{GS(th)} vs Junction Temperature

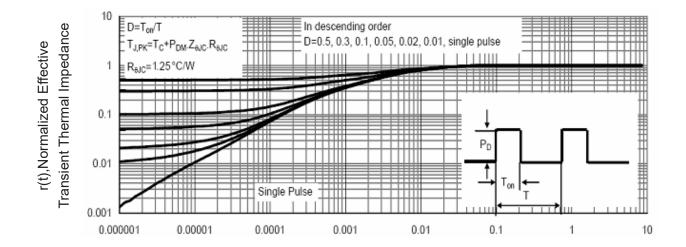


Figure 11 Normalized Maximum Transient Thermal Impedance

Square Wave Pluse Duration(sec)