

Description

The VSM150N15 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in Automotive applications and a wide variety of other applications.

General Features

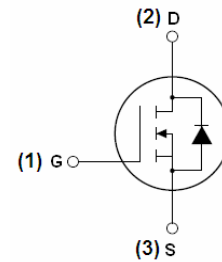
- $V_{DSS} = 150V, I_D = 150A$
 $R_{DS(ON)} < 8m\Omega @ V_{GS}=10V$ (Typ: 6.6 m Ω)
- Good stability and uniformity with high E_{AS}
- Special process technology for high ESD capability
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

- Automotive applications
- Hard switched and high frequency circuits
- Uninterruptible power supply



TO-247



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM150N15-T7	VSM150N15	TO-247	-	-	-

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	150	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	150	A
Drain Current-Continuous($T_C=100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	106	A
Pulsed Drain Current	I_{DM}	600	A
Maximum Power Dissipation	P_D	460	W
Derating factor		3.07	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 3)	E_{AS}	3100	mJ
Peak Diode Recovery dv/dt ^(Note 4)	dv/dt	18.5	V/ns

Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C
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Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 1)	$R_{\theta JC}$	0.33	°C/W
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

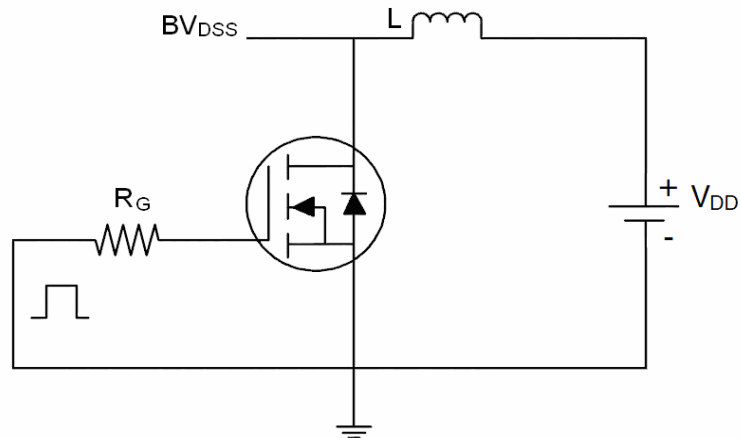
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	150	170	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =150V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±200	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =40A	-	6.6	8	mΩ
Forward Transconductance	g _{FS}	V _{DS} =50V, I _D =40A	150	-	-	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, F=1.0MHz	-	21000	-	PF
Output Capacitance	C _{oss}		-	1446	-	PF
Reverse Transfer Capacitance	C _{rss}		-	1120	-	PF
Switching Characteristics						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, I _D =2A, R _L =15Ω V _{GS} =10V, R _G =2.5Ω	-	20	-	nS
Turn-on Rise Time	t _r		-	110	-	nS
Turn-Off Delay Time	t _{d(off)}		-	45	-	nS
Turn-Off Fall Time	t _f		-	70	-	nS
Total Gate Charge	Q _g	V _{DS} =30V, I _D =30A V _{GS} =10V	-	586	-	nC
Gate-Source Charge	Q _{gs}		-	123	-	nC
Gate-Drain Charge	Q _{gd}		-	184	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =40A	-	-	1.2	V
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 75A di/dt = 100A/μs ^(Note2)	-	71	-	nS
Reverse Recovery Charge	Q _{rr}		-	106	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

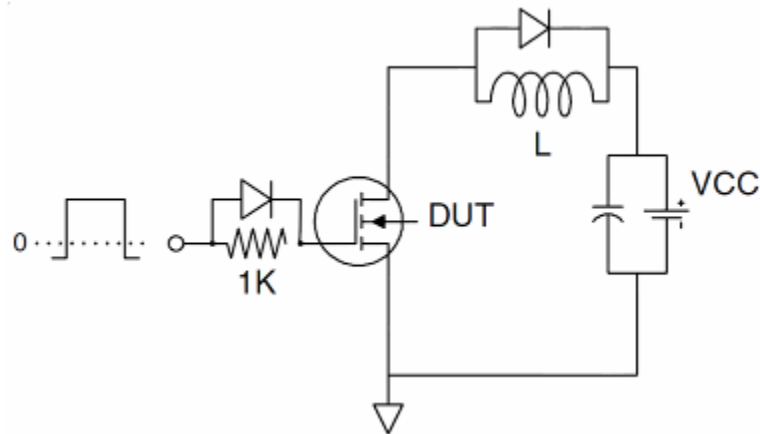
1. Surface Mounted on FR4 Board, $t \leq 10$ sec.
2. Pulse Test: Pulse Width $\leq 400\mu s$, Duty Cycle $\leq 2\%$.
3. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=75V, V_G=10V, L=0.5mH, R_g=25\Omega$
4. $I_{SD} \leq 125A, di/dt \leq 260A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^{\circ}\text{C}$

Test circuit

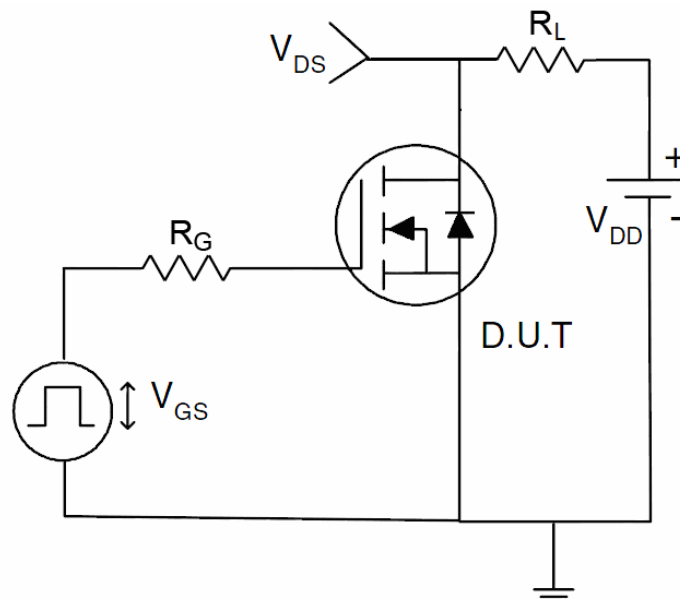
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics

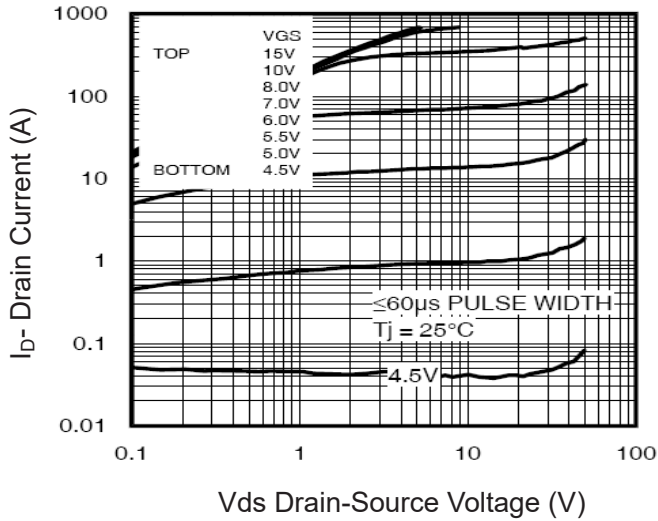


Figure 1 Output Characteristics

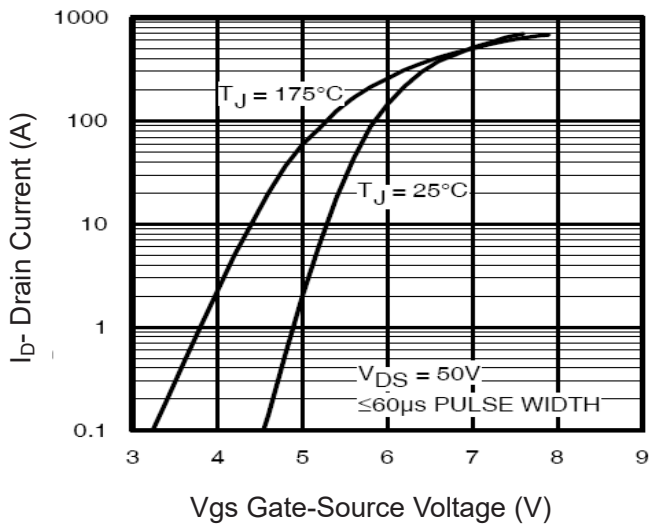


Figure 2 Transfer Characteristics

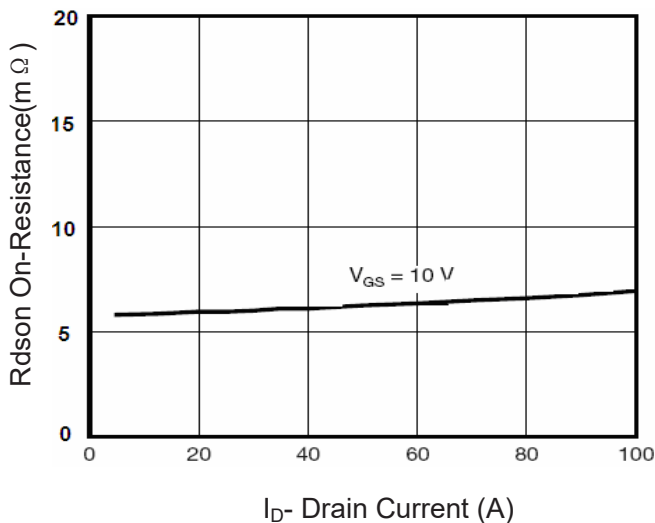


Figure 3 Rdson- Drain Current

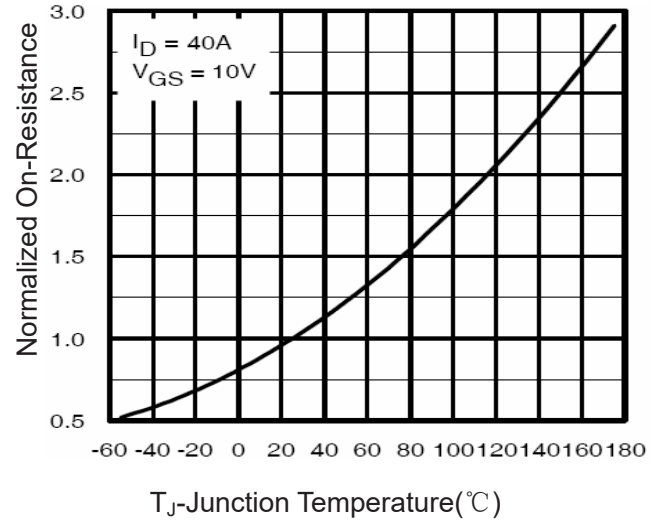


Figure 4 Rdson-Junction Temperature

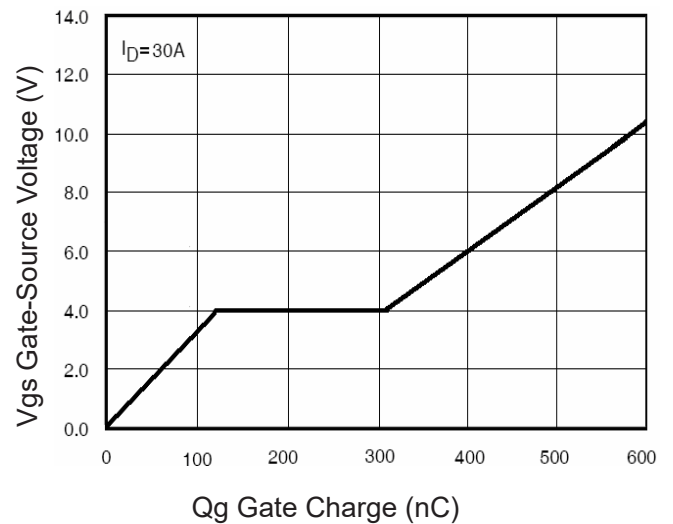


Figure 5 Gate Charge

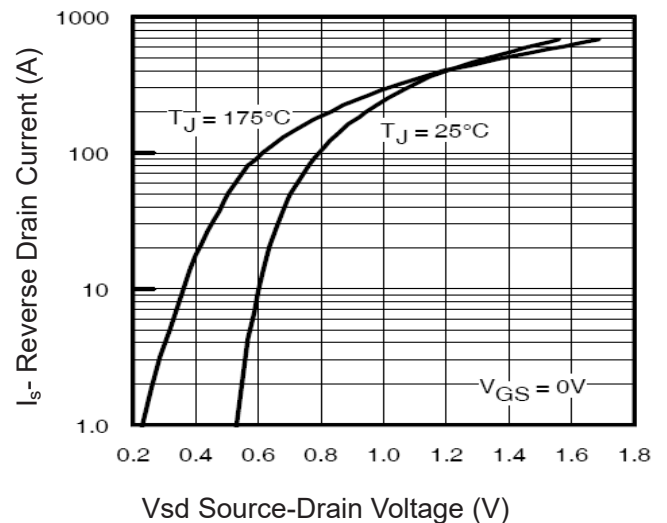
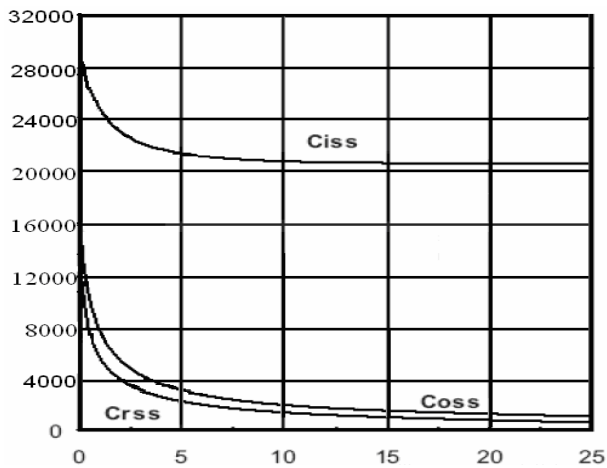
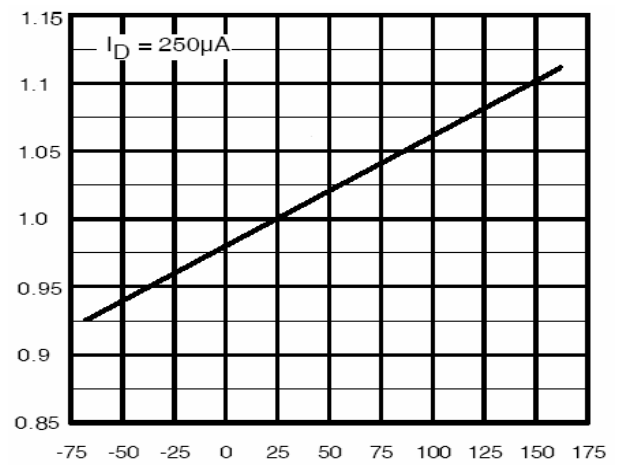


Figure 6 Source- Drain Diode Forward



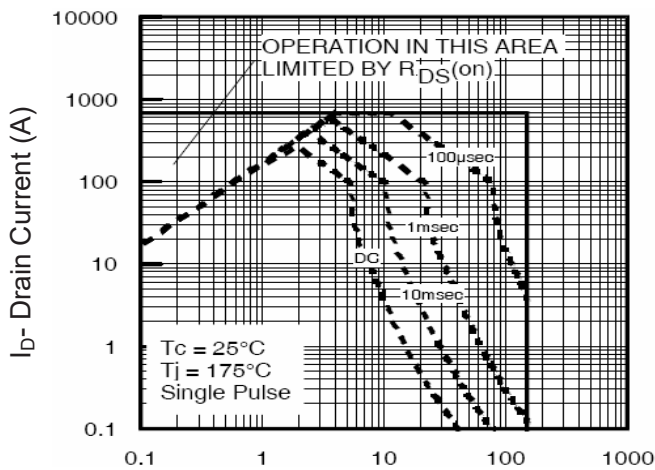
Vds Drain-Source Voltage (V)

Figure 7 Capacitance vs Vds



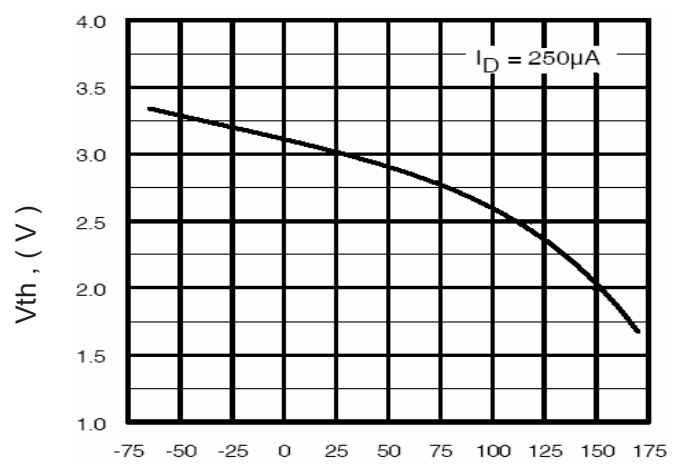
T_J-Junction Temperature(°C)

Figure 9 BV_{DSS} vs Junction Temperature



Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



T_J-Junction Temperature(°C)

Figure 10 V_{GS(th)} vs Junction Temperature

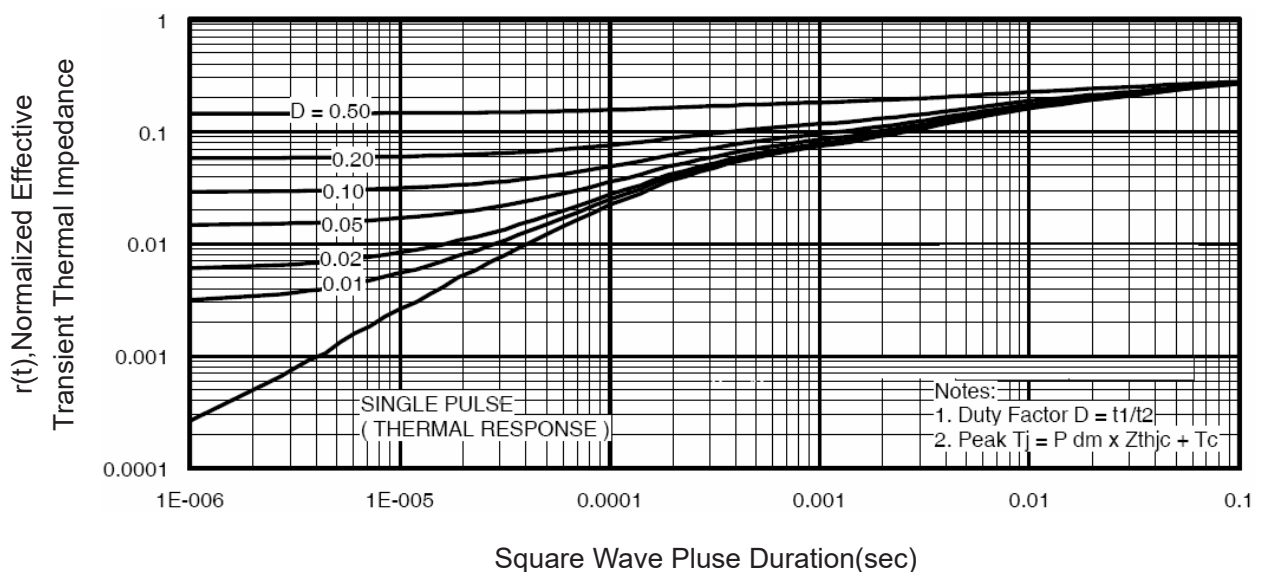


Figure 11 Normalized Maximum Transient Thermal Impedance