

Description

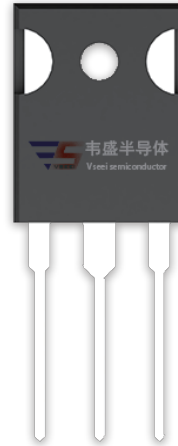
The VSM80N07 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

General Features

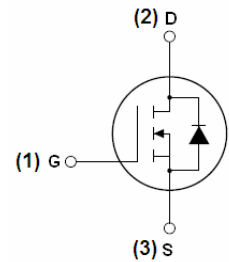
- $V_{DS} = 75V, I_D = 80A$
 $R_{DS(ON)} < 8m\Omega @ V_{GS}=10V$ (Typ: $6.5m\Omega$)
- Special process technology for high ESD capability
- Special designed for Convertors and power controls
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



TO-247



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM80N07-T7	VSM80N07	TO-247	-	-	-

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	75	V
Gate-Source Voltage	V_{GS}	± 25	V
Drain Current-Continuous	I_D	80	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D(100^\circ C)$	60	A
Pulsed Drain Current	I_{DM}	320	A
Maximum Power Dissipation	P_D	180	W
Peak diode recovery voltage	dv/dt	30	V/ns
Derating factor		1.2	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	600	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to- Case ^(Note 2)	$R_{\theta Jc}$	0.83	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

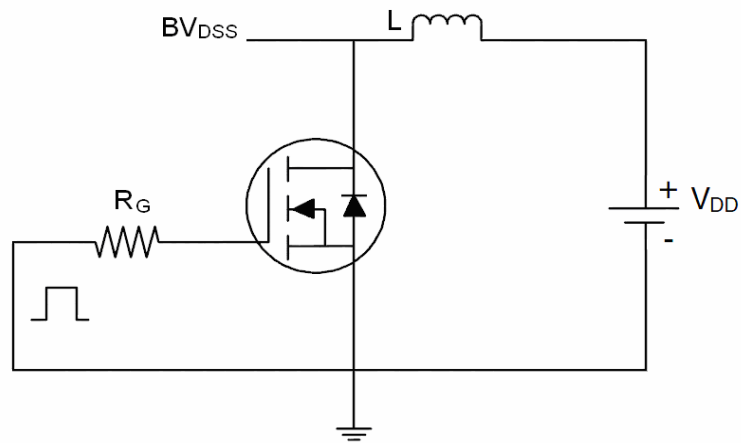
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	75	84	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±25V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	2.85	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =30A	-	6.5	8	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =30A	-	66	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, F=1.0MHz	-	4400	-	PF
Output Capacitance	C _{OSS}		-	340	-	PF
Reverse Transfer Capacitance	C _{RSS}		-	260	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, I _D =2A, R _L =15Ω V _{GS} =10V, R _G =2.5Ω	-	17.8	-	nS
Turn-on Rise Time	t _r		-	11.8	-	nS
Turn-Off Delay Time	t _{d(off)}		-	56	-	nS
Turn-Off Fall Time	t _f		-	14.6	-	nS
Total Gate Charge	Q _g	V _{DS} =24V, I _D =40A, V _{GS} =10V	-	100	-	nC
Gate-Source Charge	Q _{GS}		-	20	-	nC
Gate-Drain Charge	Q _{gd}		-	30	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =40A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	80	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 75A di/dt = 100A/μs ^(Note3)	-	35.6	50	nS
Reverse Recovery Charge	Q _{rr}		-	-	56	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

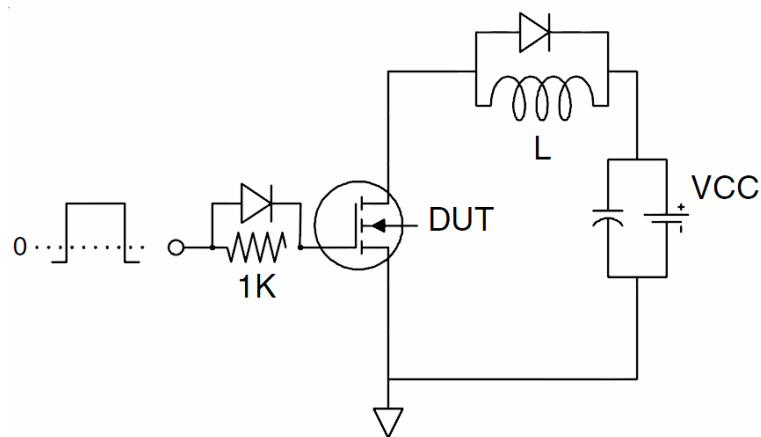
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.3mH, I_D=62A$

Test circuit

1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (curves)

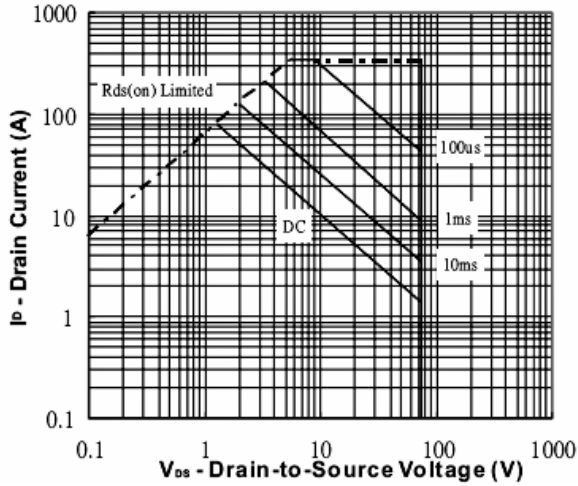
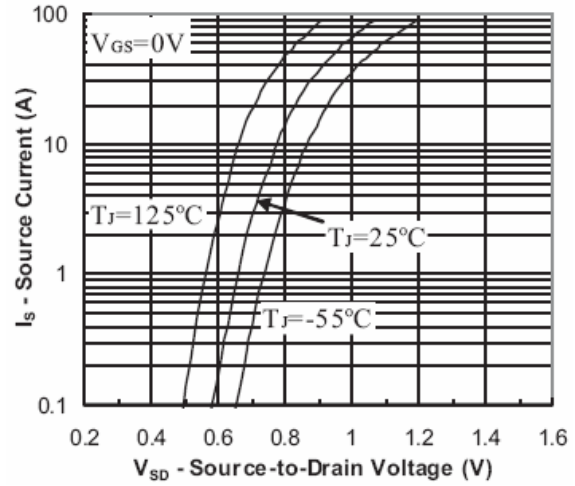
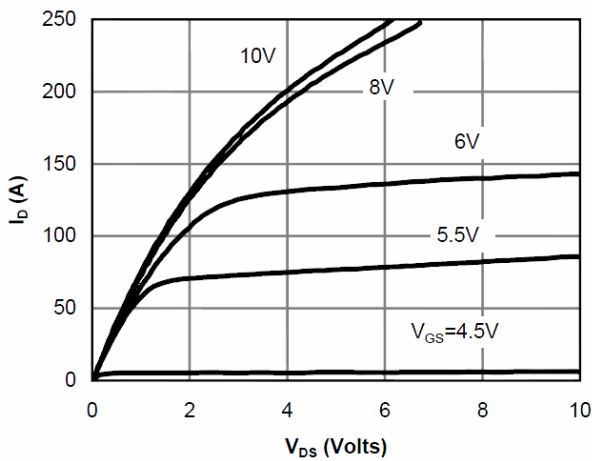
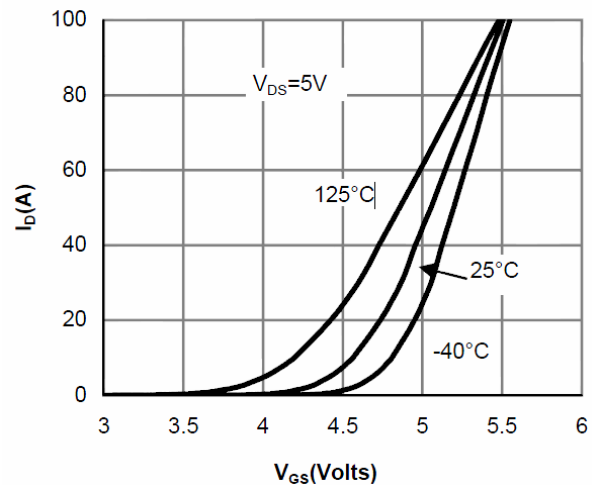
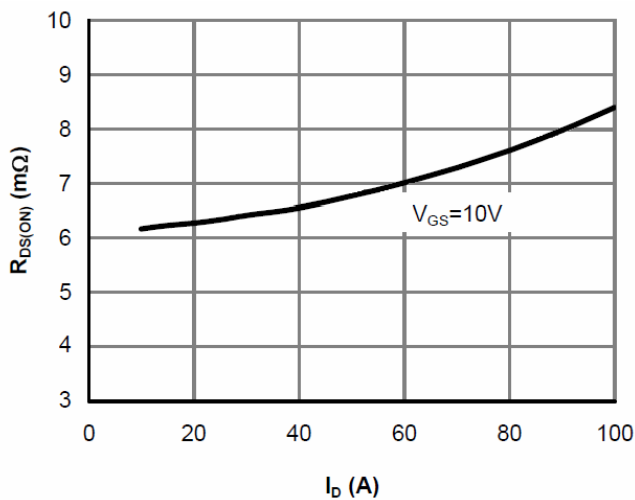
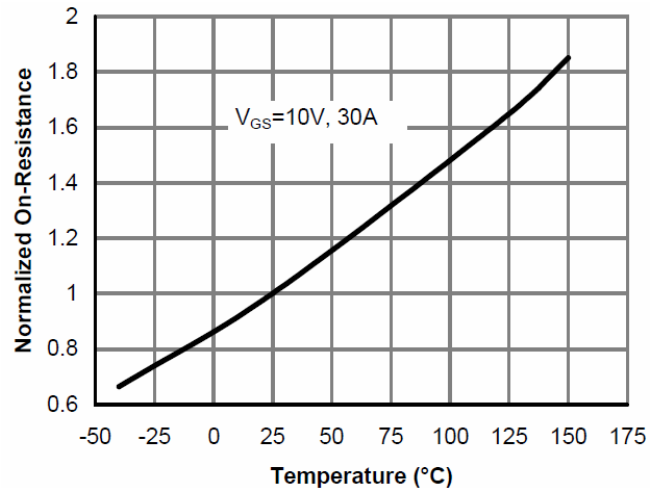
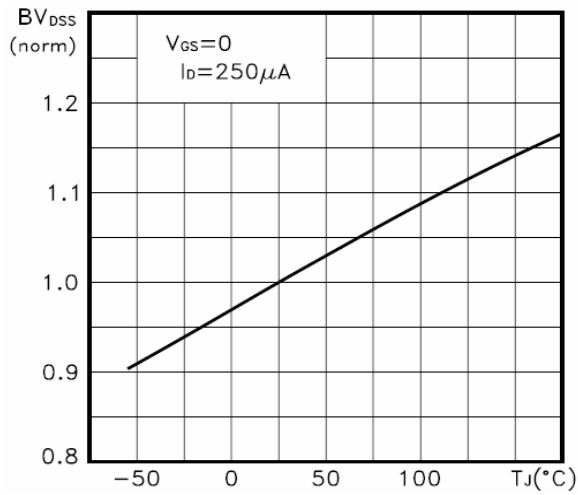
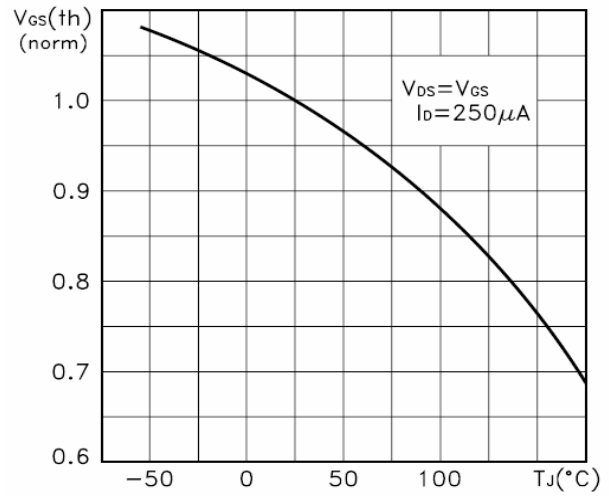
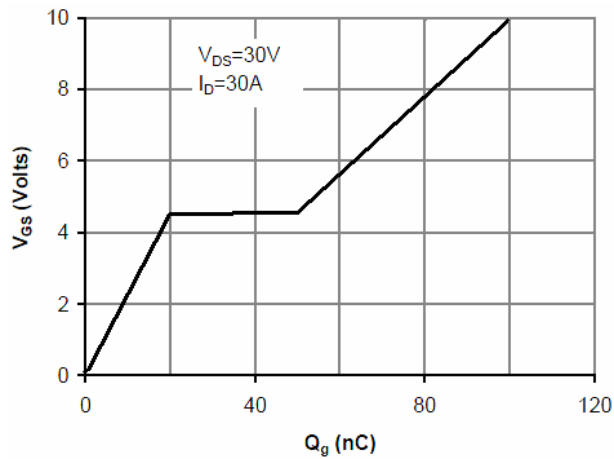
Figure1. Safe operating area

Figure2. Source-Drain Diode Forward Voltage

Figure3. Output characteristics

Figure4. Transfer characteristics

Figure5. Static drain-source on resistance

Figure6. $R_{DS(ON)}$ vs Junction Temperature


Figure7. BV_{DSS} vs Junction Temperature

Figure8. $V_{GS(th)}$ vs Junction Temperature

Figure9. Gate charge waveforms

Figure10. Capacitance
