

Description

The VSM15N04 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

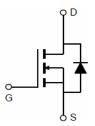
General Features

- V_{DS} =40V,I_D =15A
 - $R_{DS(ON)}$ <8.2m Ω @ V_{GS} =10V (Typ. 6.1 m $\Omega)$
 - $R_{DS(ON)}$ <25m Ω @ V_{GS} =4.5V (Typ. 11.4 m $\Omega)$
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply





SOP-8

Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM15N04-S8	VSM15N04	SOP-8	Ø330mm	12mm	2500 units

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	40	V	
Gate-Source Voltage	V _G s	±20	V	
Drain Current-Continuous	I _D	15	А	
Drain Current-Continuous(T _C =100 °C)	I _D (100℃)	10.6	А	
Pulsed Drain Current	I _{DM}	70	А	
Maximum Power Dissipation	P _D	3.1	W	
Operating Junction and Storage Temperature Range	T_{J}, T_{STG}	-55 To 150	$^{\circ}$	

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	R _{0JA}	40	°C/W
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Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics			•			
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	40	45	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V,V _{GS} =0V	-	-	1	μΑ
Gate-Body Leakage Current	I _{GSS}	V_{GS} =±20 V , V_{DS} =0 V	-	-	±100	nA
On Characteristics (Note 3)			•			
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS},I_{D}=250\mu A$	1.2	1.8	2.5	V
Drain-Source On-State Resistance	В	V _{GS} =10V, I _D =10A	-	6.1	8.2	mΩ
Diam-Source On-State Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D =8A	-	11.4	25	mΩ
Forward Transconductance	ward Transconductance g _{FS} V _{DS} =5V,I _D =10A			80	-	S
Dynamic Characteristics (Note4)				•		
Input Capacitance	C _{lss}	V 00V/V 0V	-	3090	-	PF
Output Capacitance	C _{oss}	V_{DS} =20V, V_{GS} =0V, F=1.0MHz	-	328	-	PF
Reverse Transfer Capacitance	C _{rss}	r-1.0IVInz	-	273	-	PF
Switching Characteristics (Note 4)	·					
Turn-on Delay Time	t _{d(on)}		-	7	-	nS
Turn-on Rise Time	t _r	V_{DD} =20V, R_L =2 Ω	-	20	-	nS
Turn-Off Delay Time	t _{d(off)}	V_{GS} =10 V , R_{G} =3 Ω	-	34	-	nS
Turn-Off Fall Time	t _f		-	19	-	nS
Total Gate Charge	Qg	\/ -20\/ L -40A	-	60		nC
Gate-Source Charge	Q _{gs}	$V_{DS}=20V, I_{D}=10A,$	-	8.1		nC
Gate-Drain Charge	Q_{gd}	V _{GS} =10V	-	16.9		nC
Drain-Source Diode Characteristics			•			
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =10A	-		1.2	V
Diode Forward Current (Note 2)	Is		-	-	15	Α
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF = 10A	-	31	-	nS
Reverse Recovery Charge	Qrr	$di/dt = 100A/\mu s^{(Note3)}$	-	33	-	nC

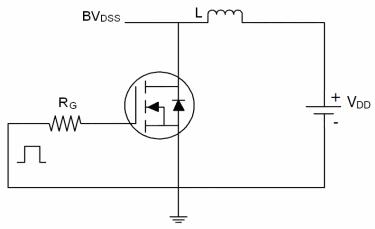
Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- **2.** Surface Mounted on FR4 Board, $t \le 10$ sec.
- **3.** Pulse Test: Pulse Width ≤ 300μ s, Duty Cycle ≤ 2%.
- 4. Guaranteed by design, not subject to production

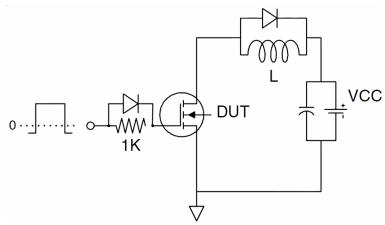


Test circuit

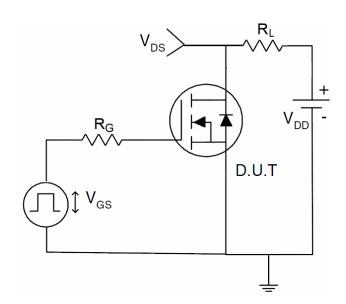
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit





Typical Electrical and Thermal Characteristics (Curves)

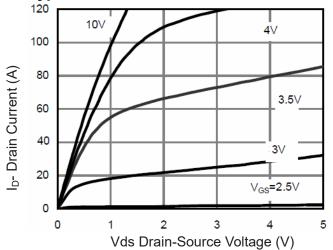


Figure 1 Output Characteristics

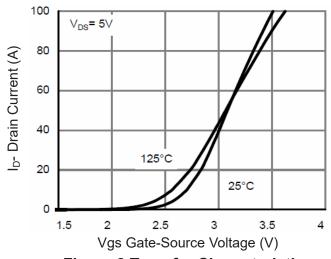


Figure 2 Transfer Characteristics

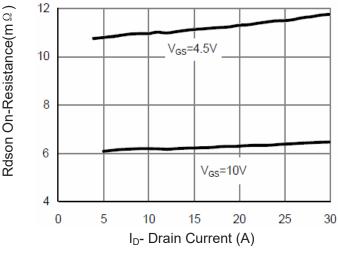


Figure 3 Rdson-Drain Current

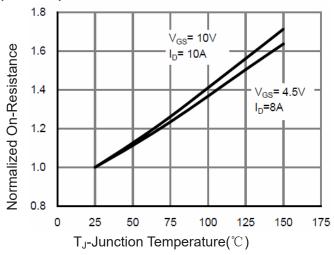


Figure 4 Rdson-JunctionTemperature

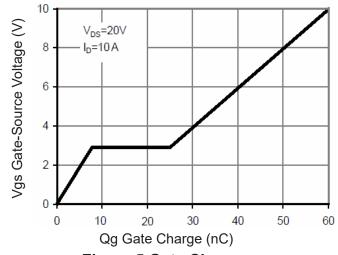


Figure 5 Gate Charge

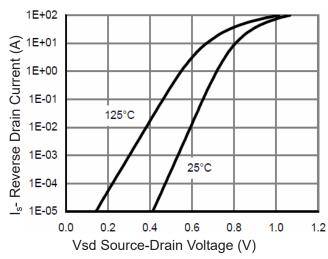
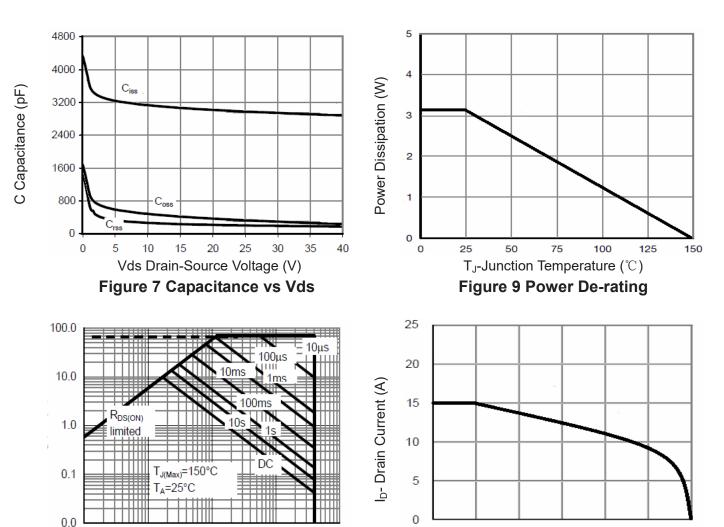


Figure 6 Source- Drain Diode Forward

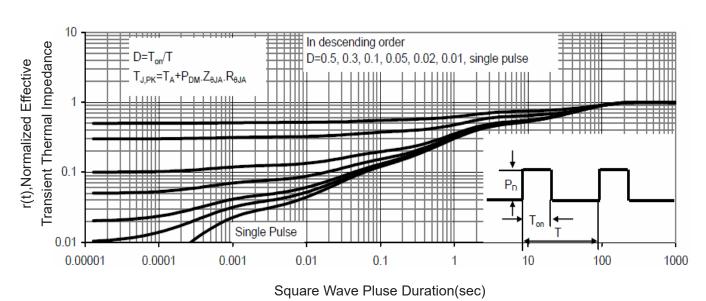




100

Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area

0.01



25

0

50

75

T_J-Junction Temperature(°C)

Figure 10 Current De-rating

100

125

150

Figure 11 Normalized Maximum Transient Thermal Impedance