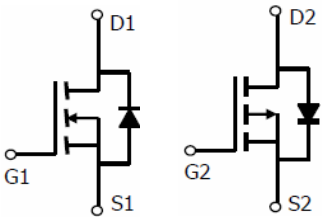
Description

The VSM2003 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge . The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

General Features

- **N-Channel**
  V_{DS} = 20V,I_D =3A
  $R_{DS(ON)}$ < 45mΩ @ V_{GS}=4.5V
  $R_{DS(ON)}$ < 60mΩ @ V_{GS}=2.5V
- **P-Channel**
  V_{DS} = -20V,I_D = -3A
  $R_{DS(ON)}$ < 110mΩ @ V_{GS}=-4.5V
  $R_{DS(ON)}$ < 140mΩ @ V_{GS}=-2.5V
- High power and current handing capability
- Lead free product is acquired
- Surface mount package

SOT-23-6



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM2003-S6	VSM2003	SOT-23-6	Ø180mm	8mm	3000 units

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	20	-20	V
Gate-Source Voltage		V_{GS}	±12	±12	V
Continuous Drain Current	T_A=25℃	I_D	3	-3	A
	T_A=70℃		2.4	-2.4	
Pulsed Drain Current (Note 1)		I_{DM}	13	-13	A
Maximum Power Dissipation	T_A=25℃	P_D	0.8	0.8	W
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note2)	$R_{\theta JA}$	N-Ch	156	℃/W
Thermal Resistance,Junction-to-Ambient (Note2)	$R_{\theta JA}$	P-Ch	156	℃/W

N-CH Electrical Characteristics (T_A=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	20	22	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±12V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	0.5	0.75	1.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=2.5V, I_D=3A	-	35	60	mΩ
		V_{GS}=4.5V, I_D=3A	-	29	45	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=3A	-	8	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=10V,V_{GS}=0V, F=1.0MHz	-	260	-	PF
Output Capacitance	C_{oss}		-	48	-	PF
Reverse Transfer Capacitance	C_{rss}		-	27	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=10V, R_L=3.3Ω V_{GS}=4.5V,R_{GEN}=6Ω	-	2.5	-	nS
Turn-on Rise Time	t_r		-	3.2	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	21	-	nS
Turn-Off Fall Time	t_f		-	3	-	nS
Total Gate Charge	Q_g	V_{DS}=10V,I_D=3A, V_{GS}=4.5V	-	2.9	5	nC
Gate-Source Charge	Q_{gs}		-	0.4	-	nC
Gate-Drain Charge	Q_{gd}		-	0.6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=3 A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	3	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

P-CH Electrical Characteristics (TA=25℃unless otherwise noted

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-20		-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±12V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-0.4	-0.7	-1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-3A	-	78	110	mΩ
		V_{GS}=-2.5V, I_D=-2A	-	102	140	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-3A	-	9.5	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-10V,V_{GS}=0V, F=1.0MHz	-	325	-	PF
Output Capacitance	C_{oss}		-	63	-	PF
Reverse Transfer Capacitance	C_{rss}		-	37	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-10V, R_L=5Ω V_{GS}=-4.5V,R_{GEN}=3Ω	-	11	-	nS
Turn-on Rise Time	t_r		-	5.5	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	22	-	nS
Turn-Off Fall Time	t_f		-	8	-	nS
Total Gate Charge	Q_g	V_{DS}=-10V,I_D=-3A, V_{GS}=-4.5V	-	3.2	-	nC
Gate-Source Charge	Q_{gs}		-	0.6	-	nC
Gate-Drain Charge	Q_{gd}		-	0.9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-3A	-	-	-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	-3	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

N- Channel Typical Electrical and Thermal Characteristics (Curves)

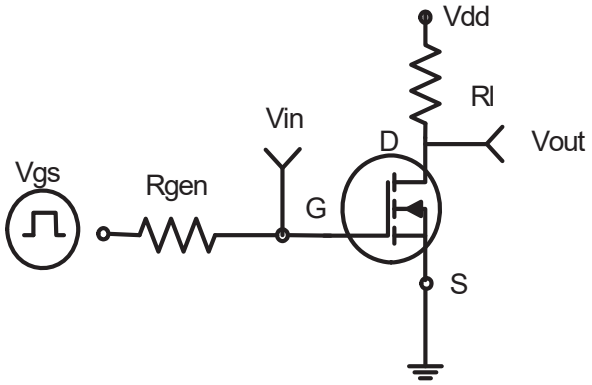


Figure 1:Switching Test Circuit

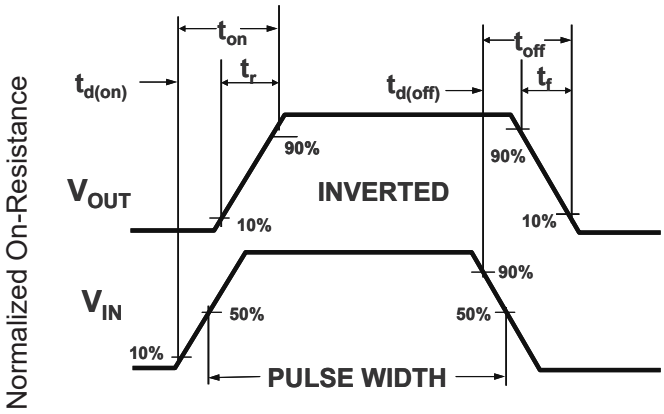


Figure 2:Switching Waveforms

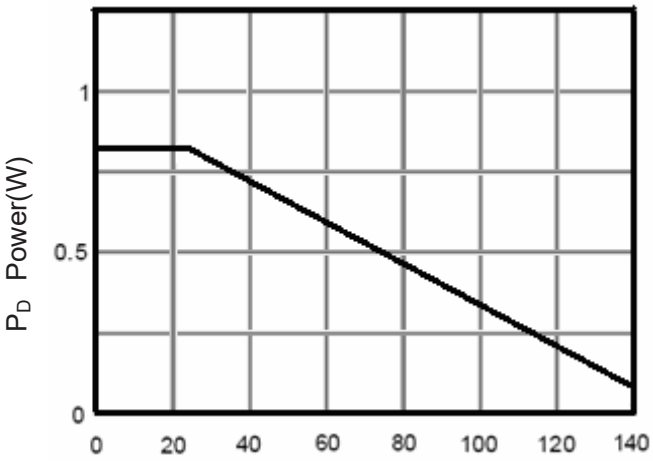


Figure 3 Power Dissipation

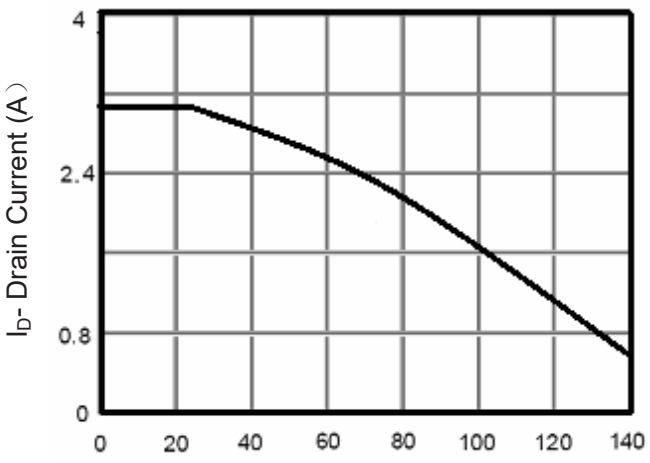


Figure 4 Drain Current

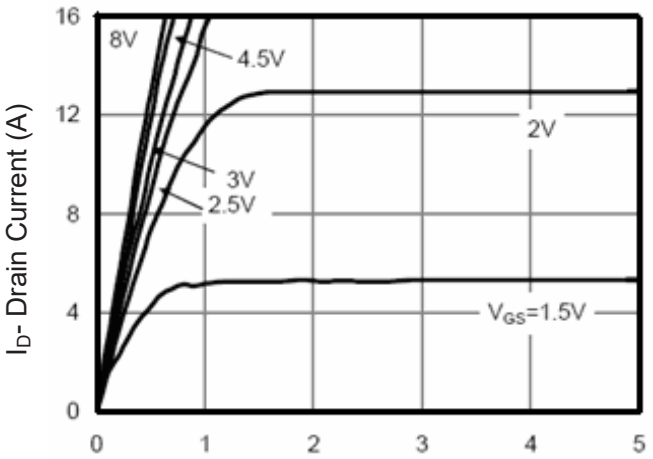


Figure 5 Output Characteristics

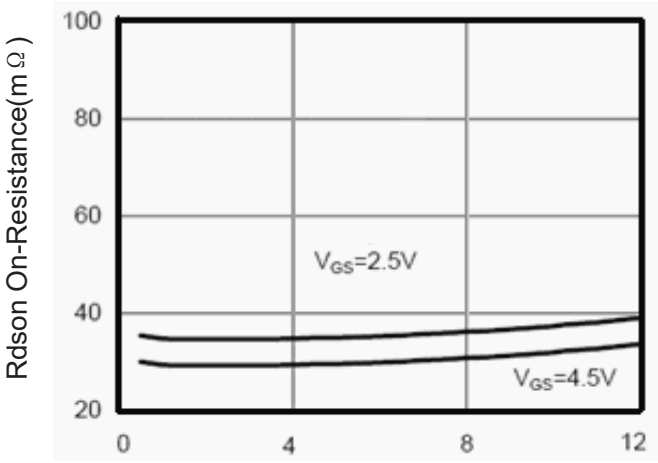


Figure 6 Drain-Source On-Resistance

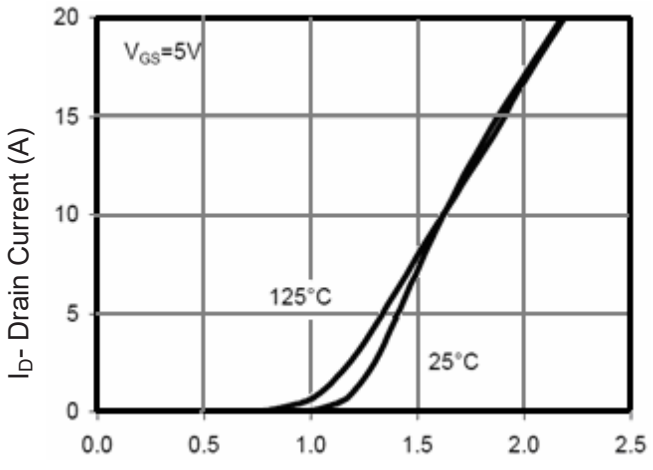


Figure 7 Transfer Characteristics

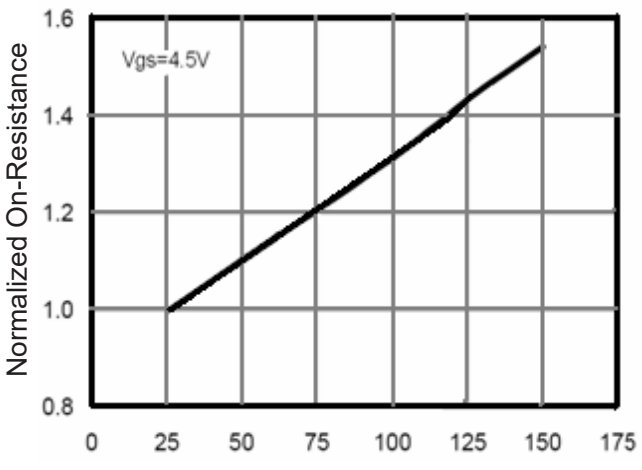


Figure 8 Drain-Source On-Resistance

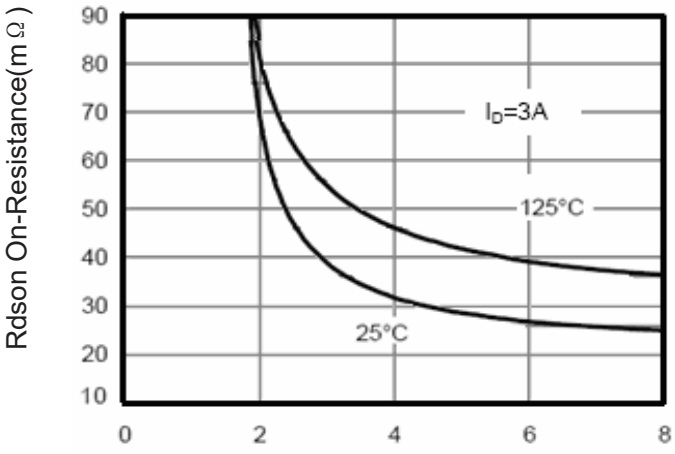


Figure 9 Rdson vs Vgs

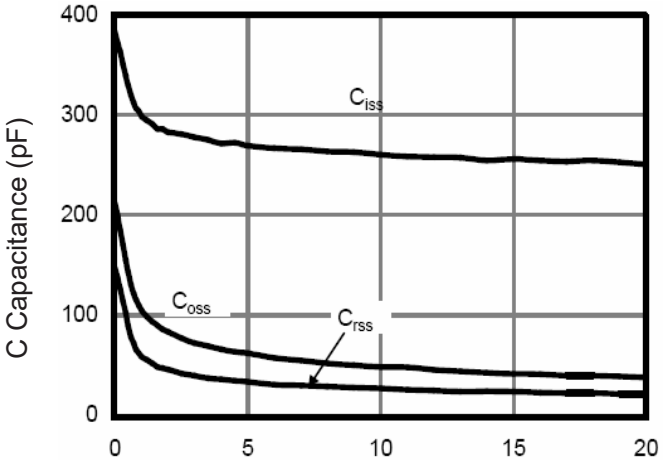


Figure 10 Capacitance vs Vds

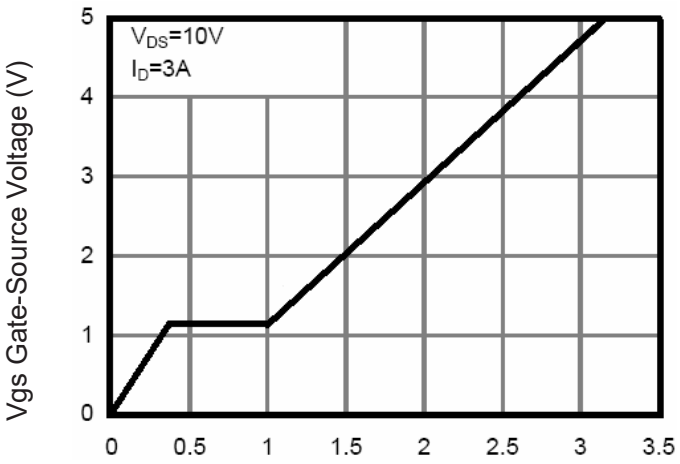


Figure 11 Gate Charge

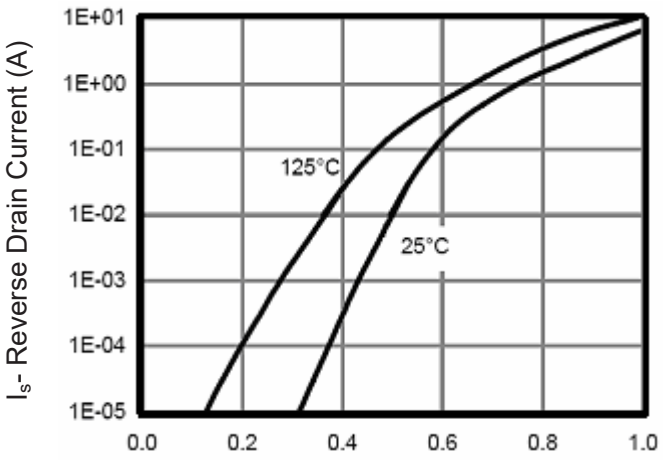


Figure 12 Source- Drain Diode Forward

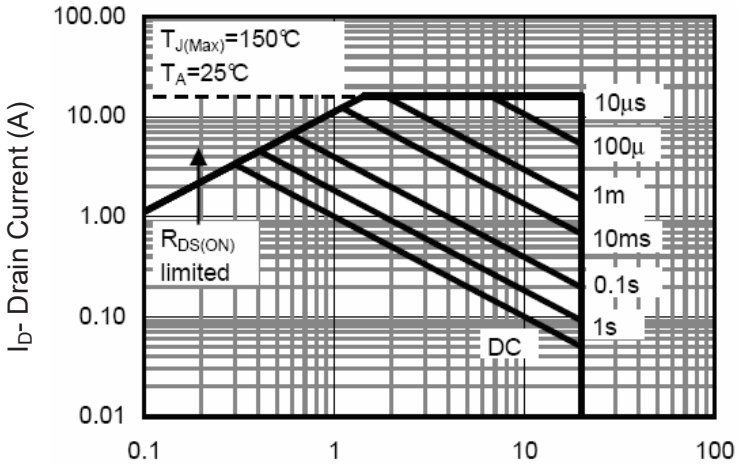


Figure 13 Safe Operation Area

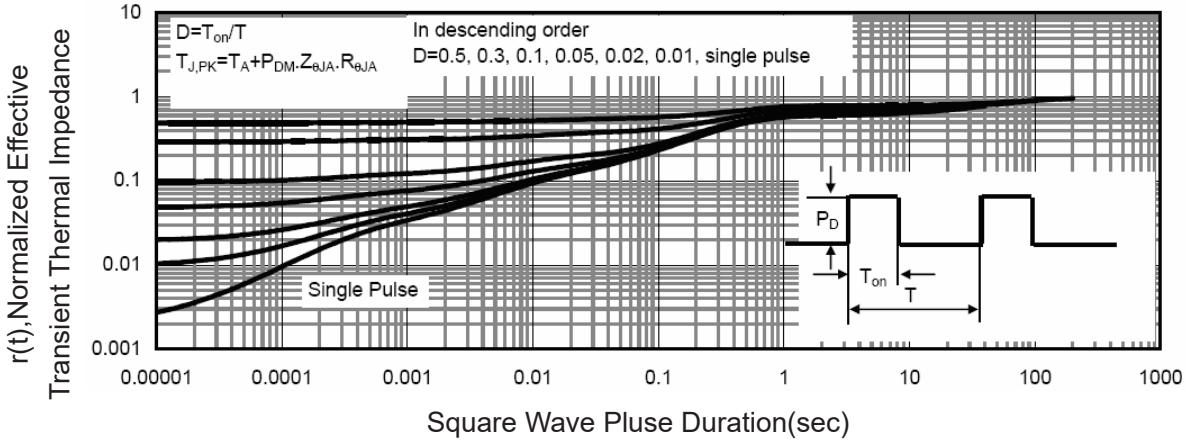


Figure 14 Normalized Maximum Transient Thermal Impedance

P- Channel Typical Electrical and Thermal Characteristics (Curves)

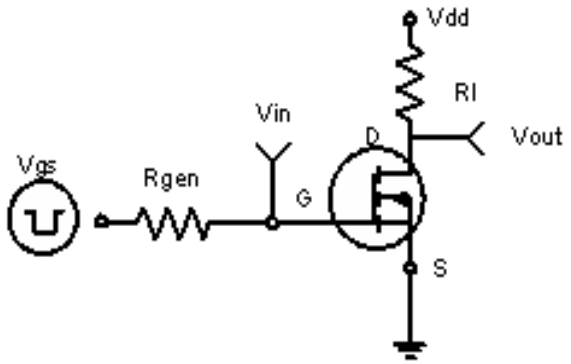


Figure 1:Switching Test Circuit

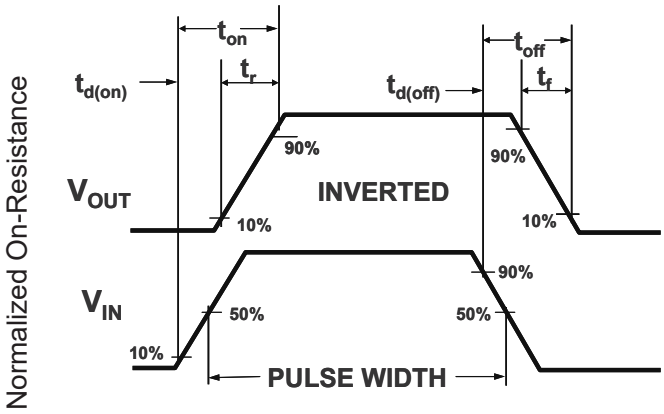
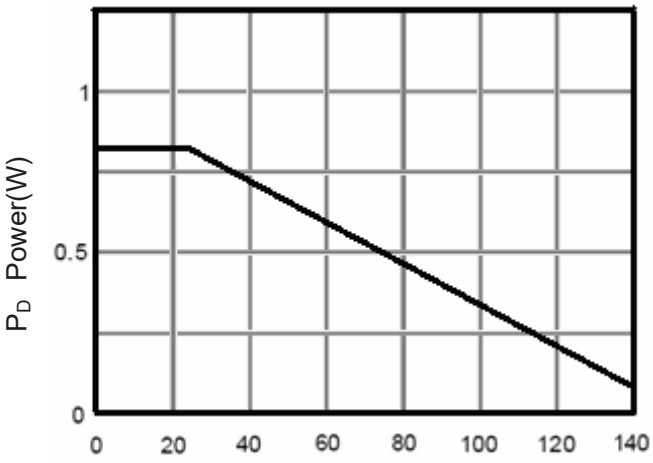
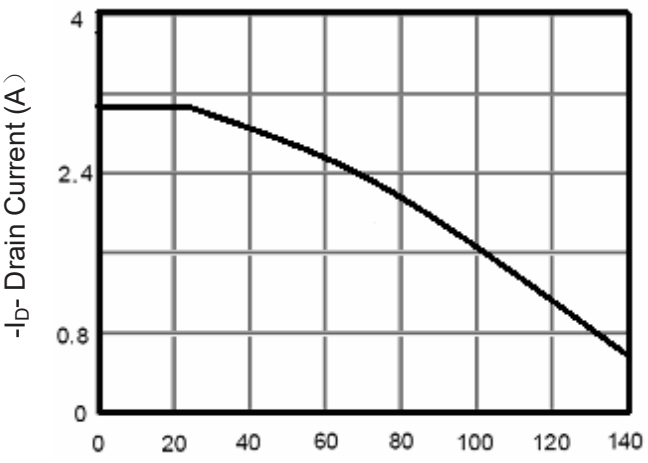


Figure 2:Switching Waveforms



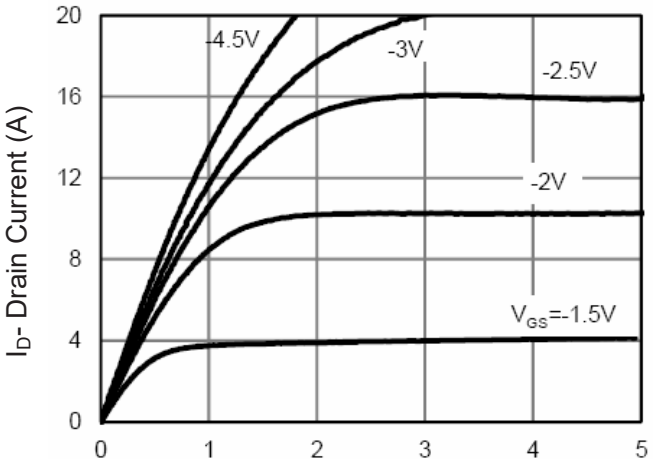
T_J-Junction Temperature(℃)

Figure 3 Power Dissipation



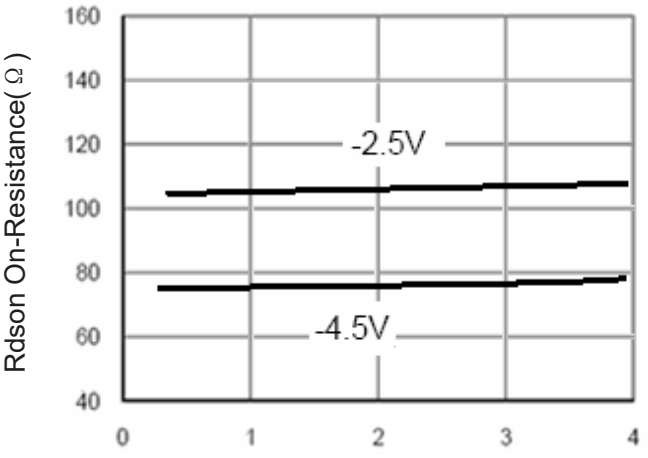
T_J-Junction Temperature(℃)

Figure 4 Drain Current



-Vds Drain-Source Voltage (V)

Figure 5 Output Characteristics



$-I_D$- Drain Current (A)

Figure 6 Drain-Source On-Resistance

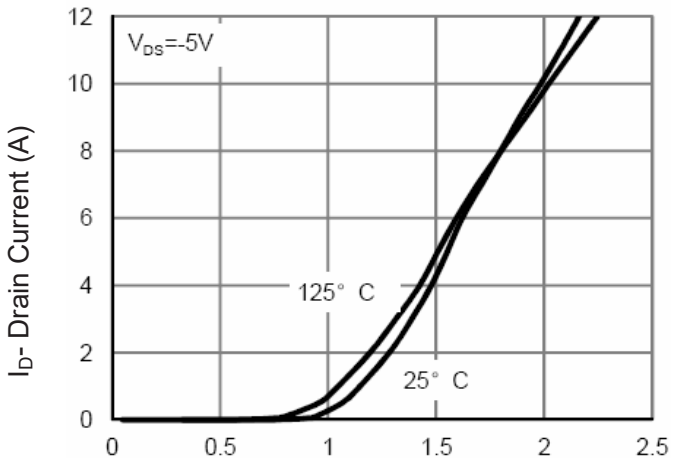


Figure 7 Transfer Characteristics

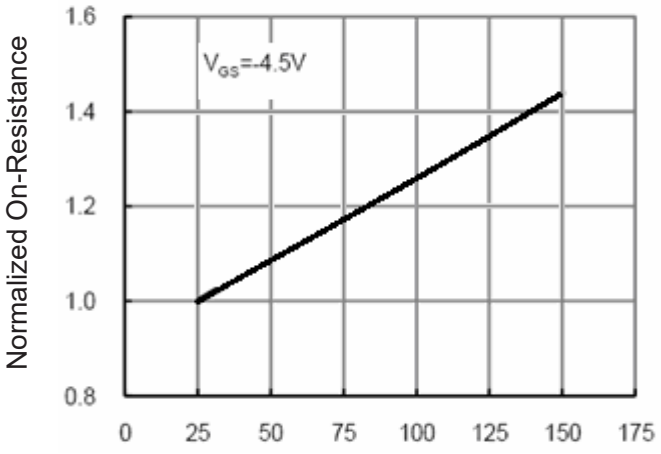


Figure 8 Drain-Source On-Resistance

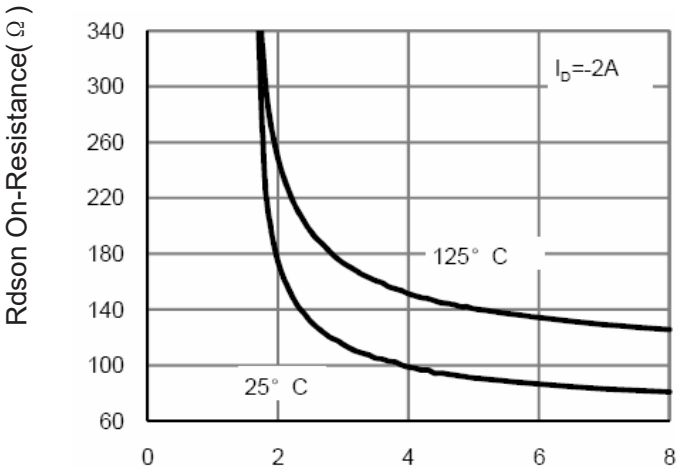


Figure 9 Rdson vs Vgs

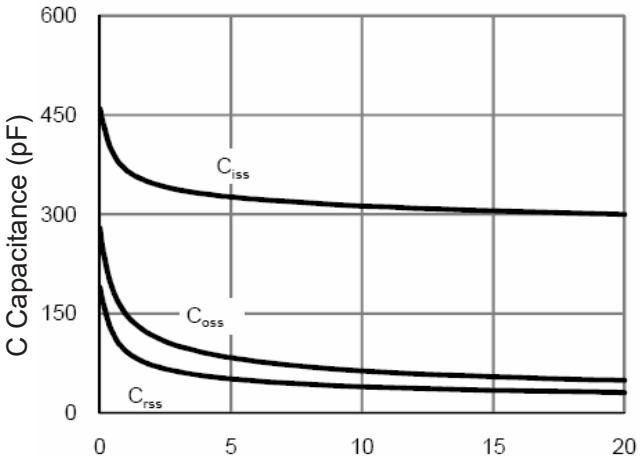


Figure 10 Capacitance vs Vds

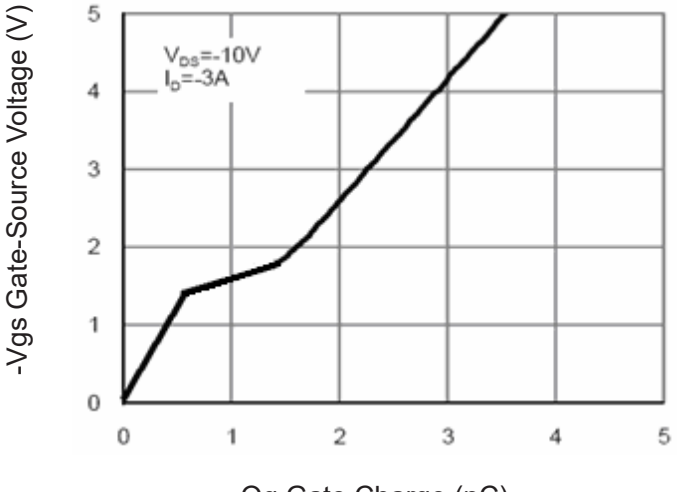


Figure 11 Gate Charge

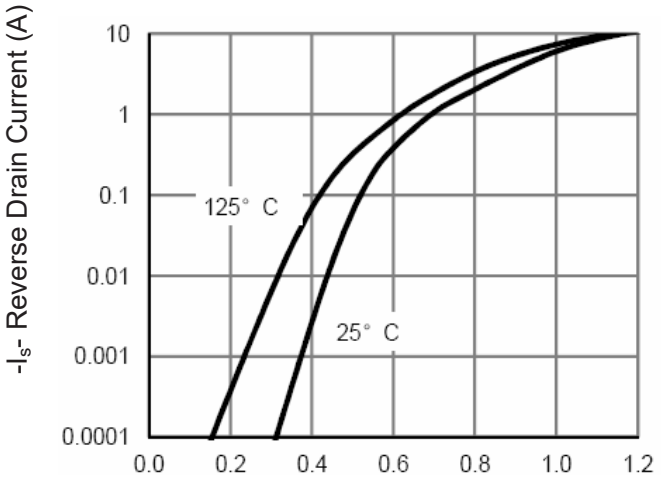


Figure 12 Source- Drain Diode Forward

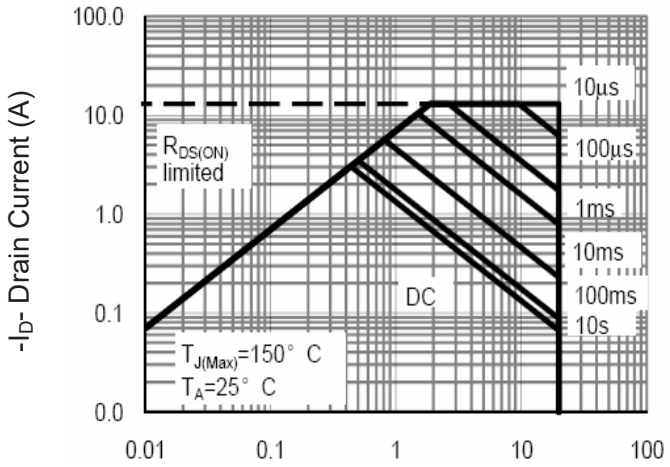


Figure 13 Safe Operation Area

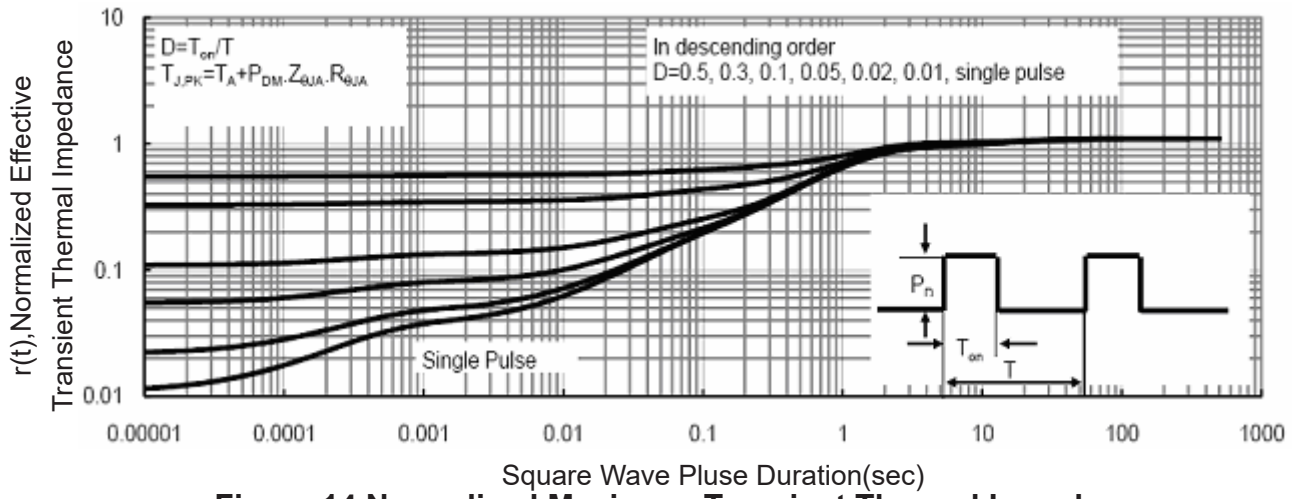


Figure 14 Normalized Maximum Transient Thermal Impedance