General Description

TheVSM80N07uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

Features

- V_{DS}=75V；I_D=80A@ V_{GS}=10V；
  $R_{DS(ON)}$<8mΩ @ V_{GS}=10V
- Special process technology for high ESD capability
- Special designed for convertors and power controls
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

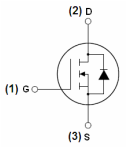
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

TO-220C

Product Summary

BV_{DSS}	typ.	84	V
$R_{DS(ON)}$	typ.	6.5	mΩ
	max.	8.0	mΩ
I_D		80	A

TO-220-3L top view



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM80N07-TC	VSM80N07	TO-220C	-	-	-

Table 1. Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Value	Unit
Drain-Source Voltage (V_{GS}=0V)	V_{DS}	75	V
Gate-Source Voltage (V_{DS}=0V)	V_{GS}	±25	V
Drain Current (DC) at Tc=25℃	$I_{D\ (DC)}$	80	A
Drain Current (DC) at Tc=100℃	$I_{D\ (DC)}$	60	A
Drain Current-Continuous@ Current-Pulsed (Note 1)	$I_{DM\ (pluse)}$	320	A
Peak diode recovery voltage	dv/dt	30	V/ns
Maximum Power Dissipation(Tc=25℃)	P_D	170	W
Derating factor		1.13	W/℃
Single pulse avalanche energy (Note 2)	E_{AS}	580	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition : Tj=25℃,V_{DD}=50V,VG=10V,L=0.3mH ,I_D=62A;

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance，Junction-to-Case（Maximum）	R_{thJC}	0.88	℃/W
Thermal Resistance，Junction-to-Ambient （Maximum）	R_{thJA}	63	℃/W

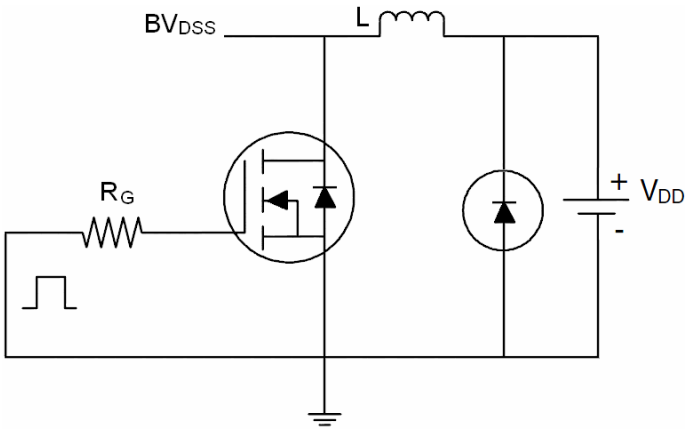
Table 3. Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	75	84		V
Zero Gate Voltage Drain Current(Tc=25℃)	I_{DSS}	V_{DS}=75V,V_{GS}=0V			1	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I_{DSS}	V_{DS}=75V,V_{GS}=0V			10	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	2.85	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=40A		6.5	8	mΩ
Dynamic Characteristics						
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=40A	20	-	-	S
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz		4400		PF
Output Capacitance	C_{oss}			340		PF
Reverse Transfer Capacitance	C_{rss}			260		PF
Total Gate Charge	Q_g	V_{DS}=30V,I_D=30A, V_{GS}=10V		100		nC
Gate-Source Charge	Q_{gs}			20		nC
Gate-Drain Charge	Q_{gd}			30		nC
Switching times						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V,I_D=2A,R_L=15Ω V_{GS}=10V,R_G=2.5Ω		17.8		nS
Turn-on Rise Time	t_r			11.8		nS
Turn-Off Delay Time	$t_{d(off)}$			56		nS
Turn-Off Fall Time	t_f			14.6		nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I_{SD}				80	A
Pulsed Source-drain current(Body Diode)	I_{SDM}				320	A
Forward on voltage(Note 1)	V_{SD}	Tj=25℃,I_{SD}=40A,V_{GS}=0V			1.2	V
Reverse Recovery Time(Note 1)	t_{rr}	Tj=25℃,I_F=75A,di/dt=100A/μs			36	nS
Reverse Recovery Charge(Note 1)	Q_{rr}				56	nC
Forward Turn-on Time	t_{on}	Intrinsic turn-on time is negligible(turn-on is dominated by L_S+L_D)				

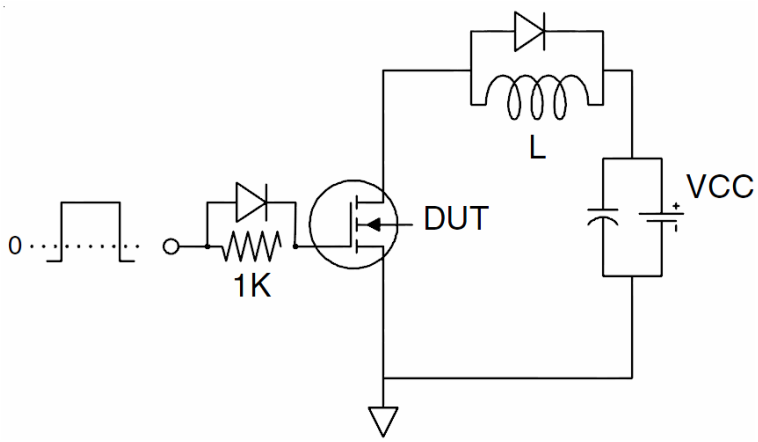
Notes 1.Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 1.5%, R_G=25Ω, Starting Tj=25℃

Test Circuit

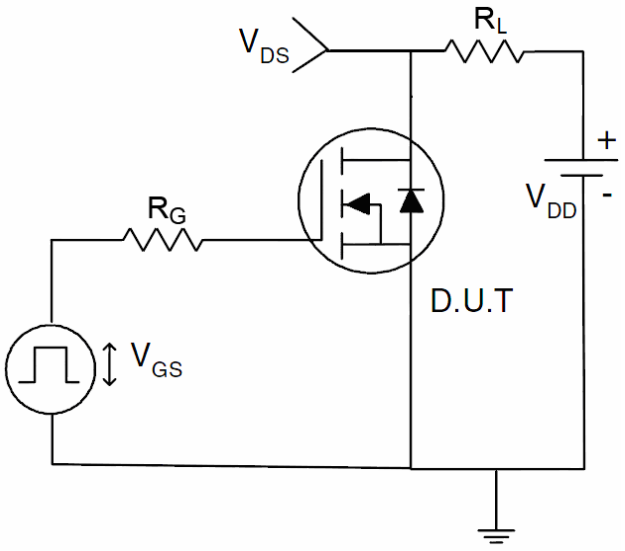
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (curves)

Figure1. Safe operating area

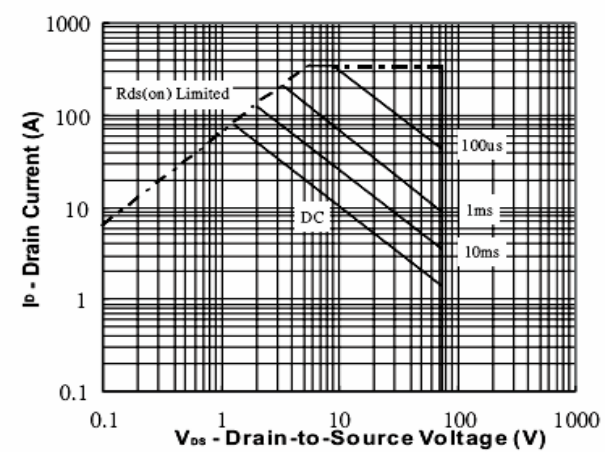


Figure2. Source-Drain Diode Forward Voltage

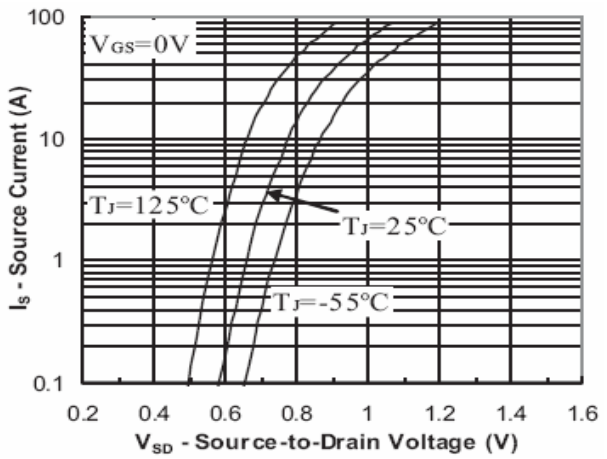


Figure3. Output characteristics

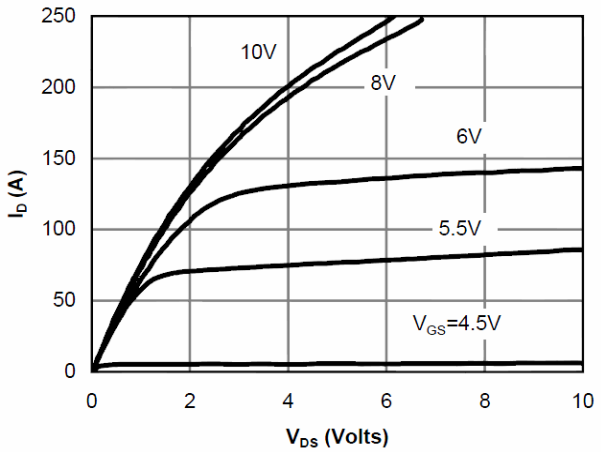


Figure4. Transfer characteristics

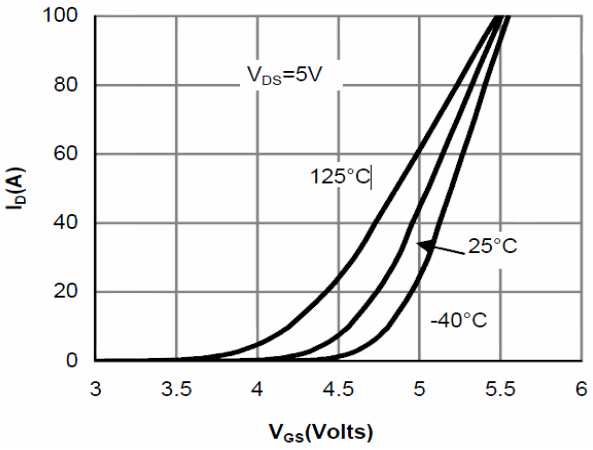


Figure5. Static drain-source on resistance

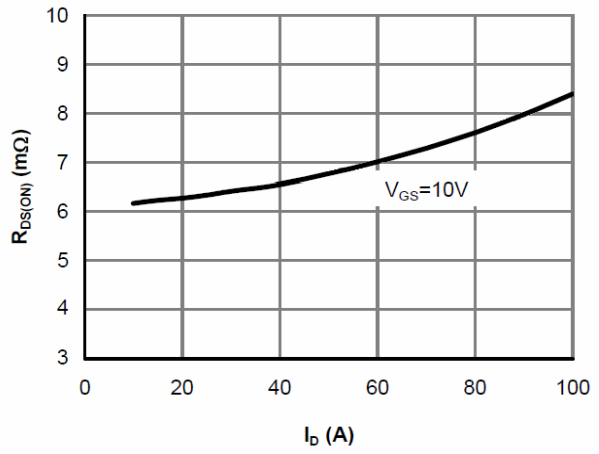


Figure6. $R_{DS(ON)}$ vs Junction Temperature

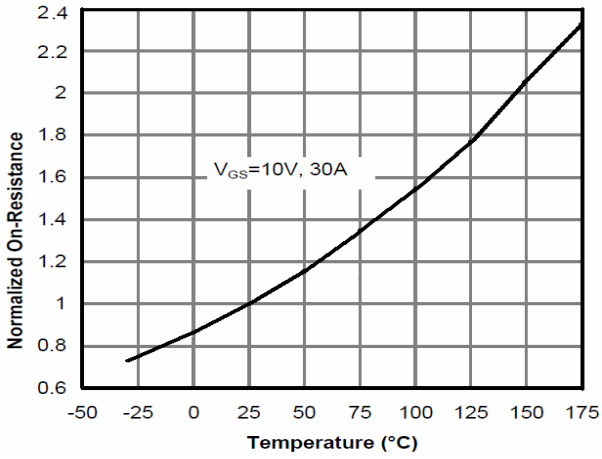


Figure7. BV_{DSS} vs Junction Temperature

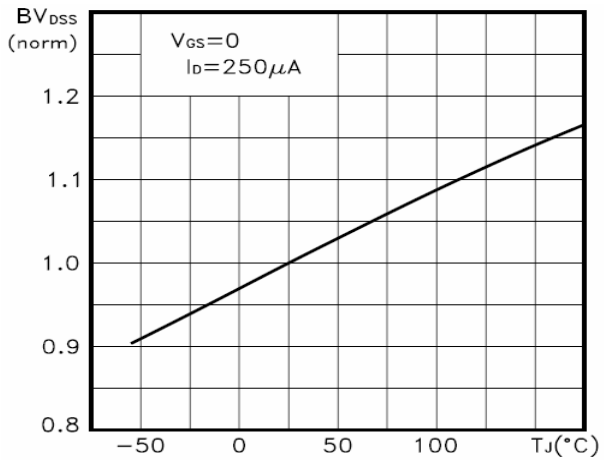


Figure8. $V_{GS(th)}$ vs Junction Temperature

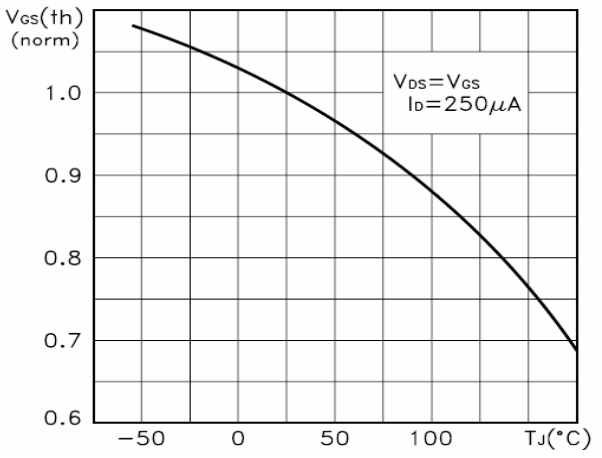


Figure9. Gate charge waveforms

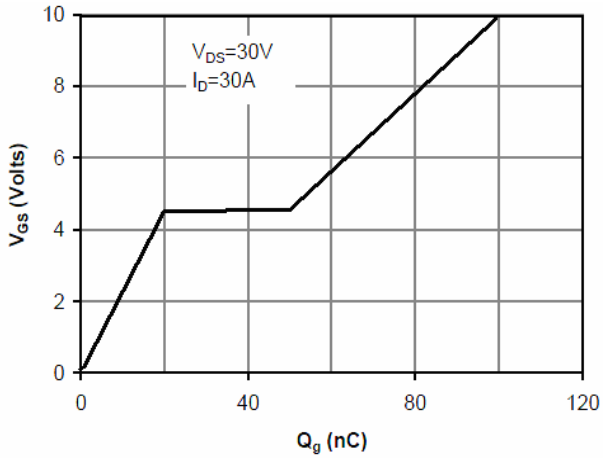


Figure10. Capacitance