

Description

The VST15N590 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{\text{DS(ON)}}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

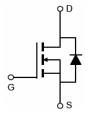
General Features

- V_{DS} =150V, I_D =20A $R_{DS(ON)}$ =59m Ω (typical) @ V_{GS} =10V
- Excellent gate charge x R_{DS(on)} product(FOM)
- Very low on-resistance R_{DS(on)}
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- LED backlighting
- Ideal for high-frequency switching and synchronous rectification





TO-220C

Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VST15N590-TC	VST15N590	TO-220C	-	-	-

Absolute Maximum Ratings (T_A=25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	150	V	
Gate-Source Voltage	V_{GS}	±20	V	
Drain Current-Continuous	I _D	20	А	
Drain Current-Continuous(T _C =100 °C)	I _D (100℃)	14	А	
Pulsed Drain Current	I _{DM}	80	Α	
Maximum Power Dissipation	P _D	68	W	
Derating factor		0.45	W/℃	
Single pulse avalanche energy (Note 5)	E _{AS}	65	mJ	
Drain Source voltage slope, V⊳s ≤120 V,	dv/dt	50	V/ns	
Drain Source voltage slope, V _{DS} ≤120 V, I _{SD} <i<sub>D</i<sub>	dv/dt	50	V/ns	
Operating Junction and Storage Temperature Range	T_{J} , T_{STG}	-55 To 175	$^{\circ}$	





Thermal Characteristic

TI (Note 2)	Б	0.0	°C /\ \
Thermal Resistance, Junction-to-Case (1885)	I Raic	2.2	l °C/W ∣

Electrical Characteristics (T_A=25°Cunless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics			•			
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	150	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =150V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)			•			•
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS}$, $I_{D}=250\mu A$	2.5	3.3	4.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =10A	-	59	65	mΩ
Gate resistance	R _G		-	4.5	-	Ω
Forward Transconductance	G FS	V _{DS} =5V,I _D =10A	15	-	-	S
Dynamic Characteristics (Note4)	·					
Input Capacitance	C _{lss}	V _{DS} =75V,V _{GS} =0V,	-	600		PF
Output Capacitance	C _{oss}		-	74.7		PF
Reverse Transfer Capacitance	C _{rss}	F=1.0MHz	-	10.8		PF
Switching Characteristics (Note 4)			•			•
Turn-on Delay Time	t _{d(on)}	V _{DD} =75V, R _L =7.5Ω	-	9.5	-	nS
Turn-on Rise Time	t _r		-	5.5	-	nS
Turn-Off Delay Time	t _{d(off)}	V_{GS} =10 V , R_{G} =3 Ω	-	12.5	-	nS
Turn-Off Fall Time	t _f		-	3	-	nS
Total Gate Charge	Qg	V _{DS} =75V,I _D =10A,	-	12	-	nC
Gate-Source Charge	Q _{gs}		-	2.8	-	nC
Gate-Drain Charge	Q _{gd}	V _{GS} =10V	-	1.8	-	nC
Drain-Source Diode Characteristics	·					
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =10A	-	-	1.2	V
Diode Forward Current (Note 2)	Is		-	-	20	Α
Reverse Recovery Time	t _{rr}	$T_J = 25^{\circ}C, I_F = I_S$	-	29	-	nS
Reverse Recovery Charge	Qrr	$di/dt = 100A/\mu s^{(Note3)}$	-	130	-	nC

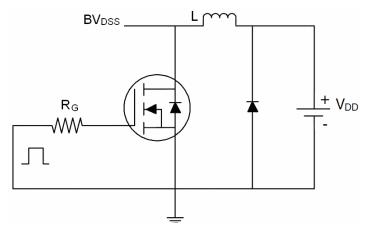
Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- 3. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.
- 4. Guaranteed by design, not subject to production
- 5. EAS condition : Tj=25 $^{\circ}\text{C}$,V_DD=50V,V_G=10V,L=0.5mH,Rg=25 Ω

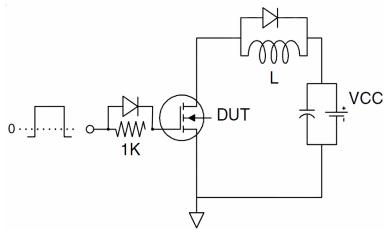


Test Circuit

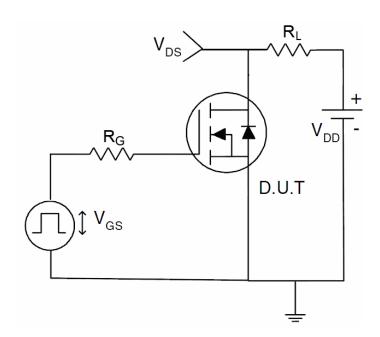
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit







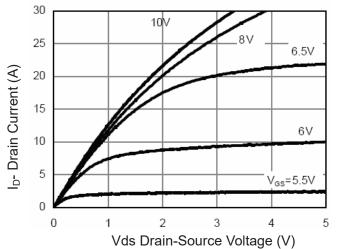


Figure 1 Output Characteristics

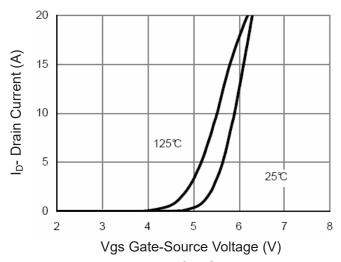


Figure 2 Transfer Characteristics

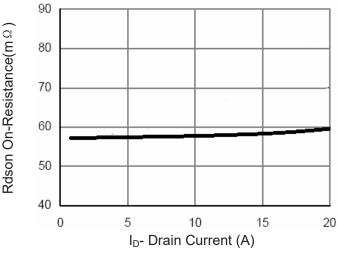


Figure 3 Rdson- Drain Current

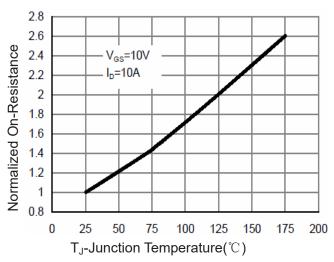


Figure 4 Rdson-Junction Temperature

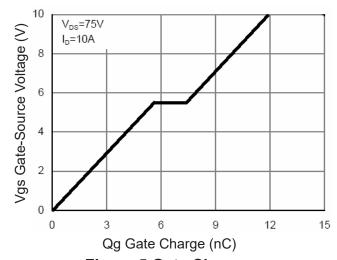


Figure 5 Gate Charge

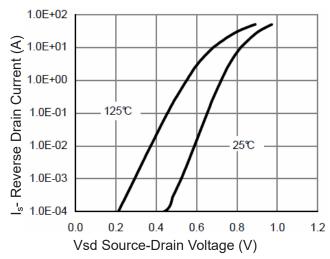
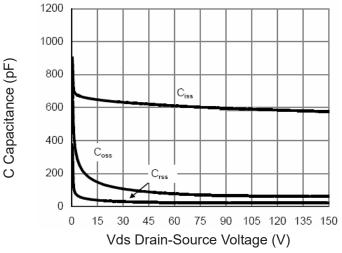


Figure 6 Source- Drain Diode Forward



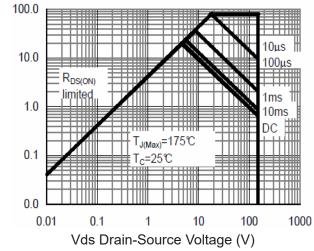
_{lo-} Drain Current (A)



120 100 Power Dissipation (W) 80 60 40 20 0 0 75 100 125 150 25 175 T_J-Junction Temperature(°C)

Figure 7 Capacitance vs Vds

Figure 9 Power De-rating



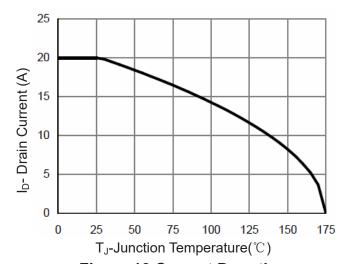
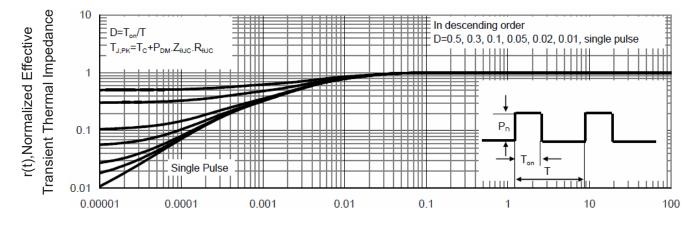


Figure 8 Safe Operation Area

Figure 10 Current De-rating



Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance