

## Description

The VSM60P04AY uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is well suited for use as a load switch or in PWM applications.

## General Features

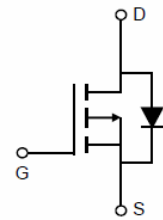
- $V_{DS} = -60V, I_D = -4.6A$   
 $R_{DS(ON)} < 75m\Omega @ V_{GS} = -10V$   
 $R_{DS(ON)} < 96m\Omega @ V_{GS} = -4.5V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

## Application

- Load switch
- PWM application



SOT-23-3



Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM60P04AY-S2	VSM60P04AY	SOT-23-3	Ø180mm	8 mm	3000 units

## Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-4.6	A
Pulsed Drain Current	$I_{DM}$	-17	A
Maximum Power Dissipation	$P_D$	1.5	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

## Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	83.3	$^\circ C/W$
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**Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)**

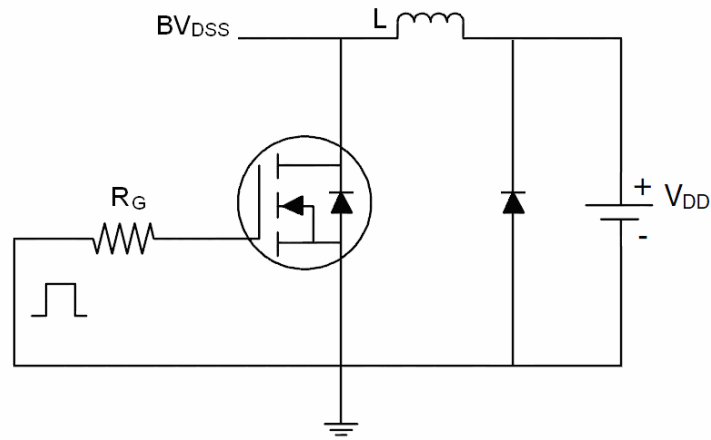
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-60V, V <sub>GS</sub> =0V	-	-	-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.0	-1.5	-2.0	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-4A	-	63	75	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3A	-	74	96	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-5V, I <sub>D</sub> =-4A	-	10	-	S
Dynamic Characteristics <sup>(Note4)</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V, F=1.0MHz	-	930	-	PF
Output Capacitance	C <sub>oss</sub>		-	85	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	35	-	PF
Switching Characteristics <sup>(Note 4)</sup>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-30V, R <sub>L</sub> =7.5Ω, V <sub>GS</sub> =-10V, R <sub>G</sub> =3Ω	-	8	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	4	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	32	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	7	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-30, I <sub>D</sub> =-4A, V <sub>GS</sub> =-10V	-	25	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	3	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-4A	-		-1.2	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>S</sub>		-	-	-4.6	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> =- 4A	-	25		nS
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = -100A/μs <sup>(Note3)</sup>	-	31		nC

**Notes:**

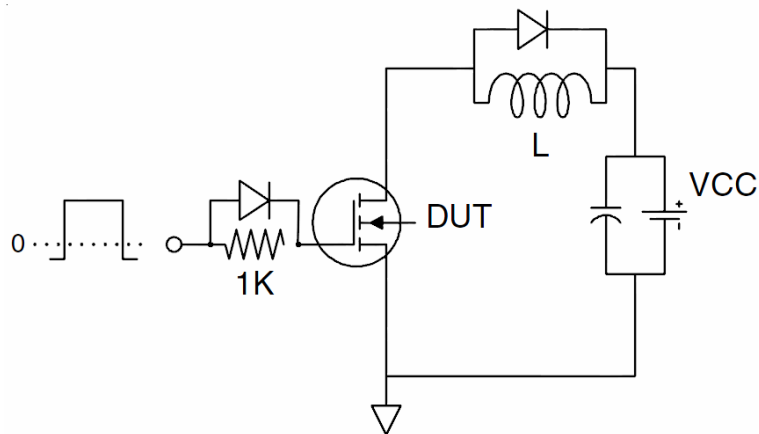
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

## Test Circuit

### 1) $E_{AS}$ test Circuit



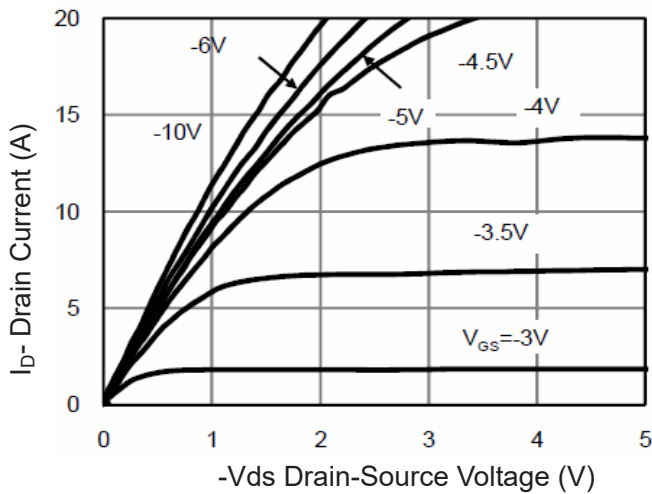
### 2) Gate charge test Circuit



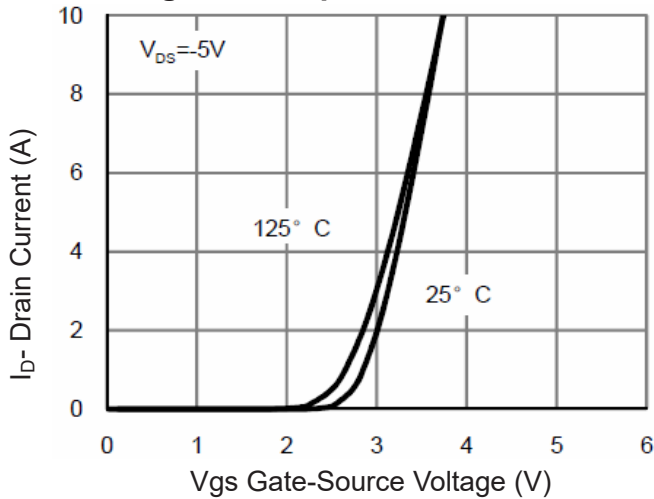
### 3) Switch Time Test Circuit



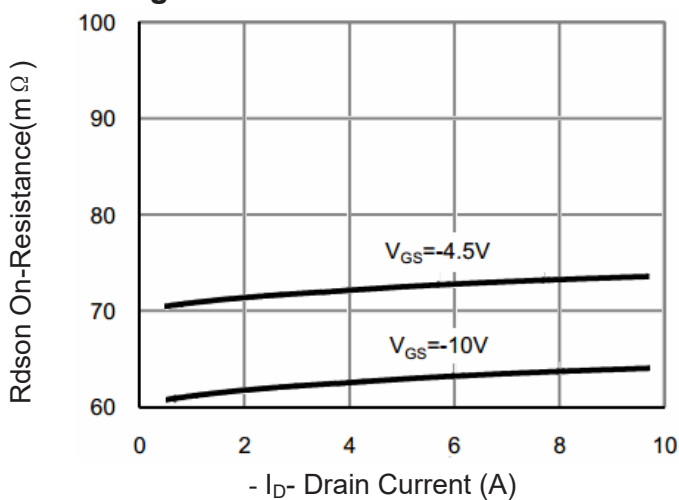
## Typical Electrical and Thermal Characteristics (Curves)



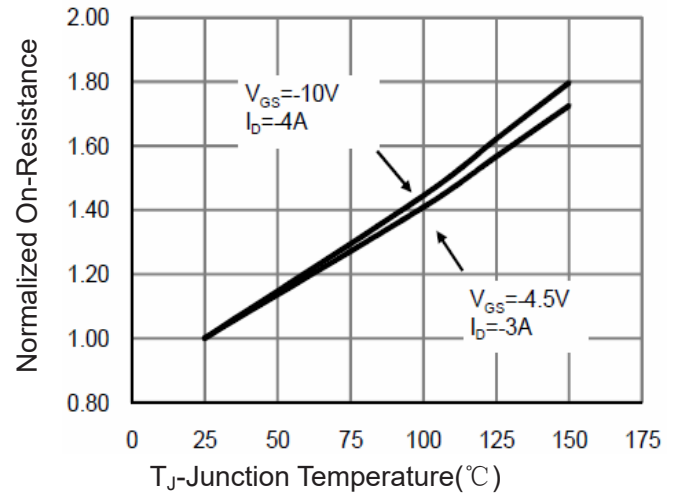
**Figure 1 Output Characteristics**



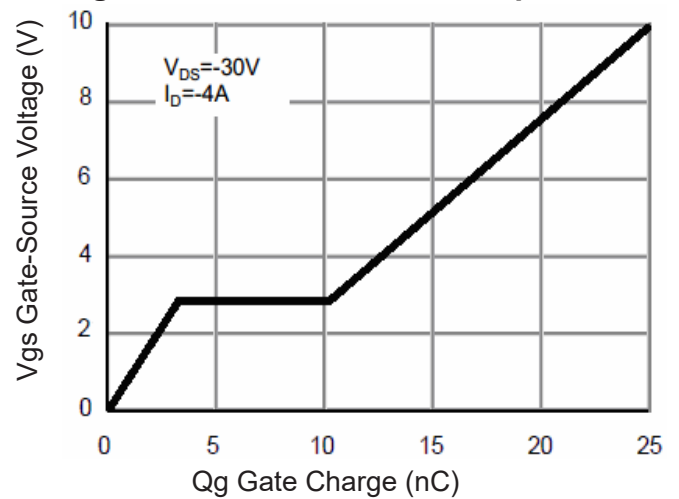
**Figure 2 Transfer Characteristics**



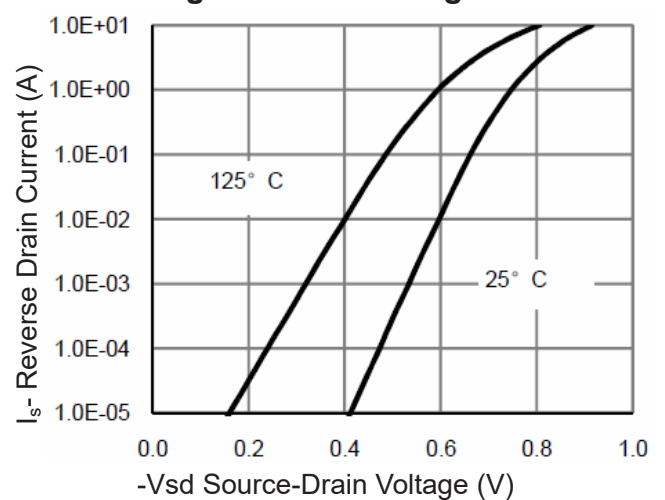
**Figure 3 Rdson- Drain Current**



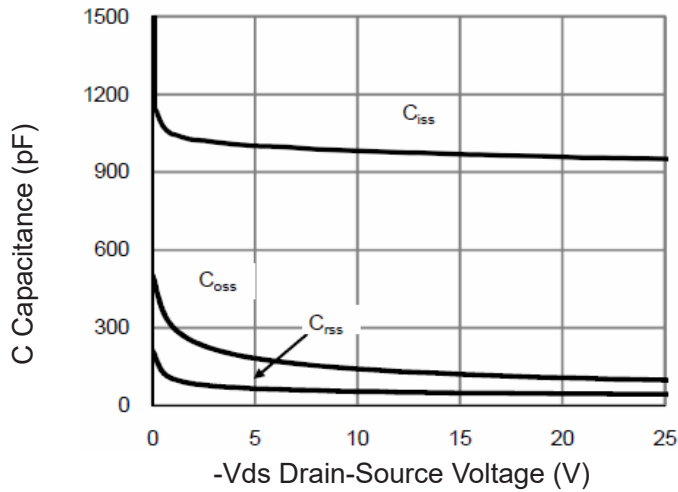
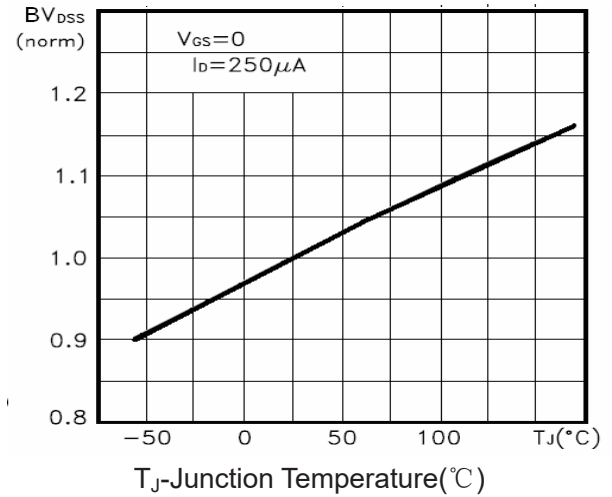
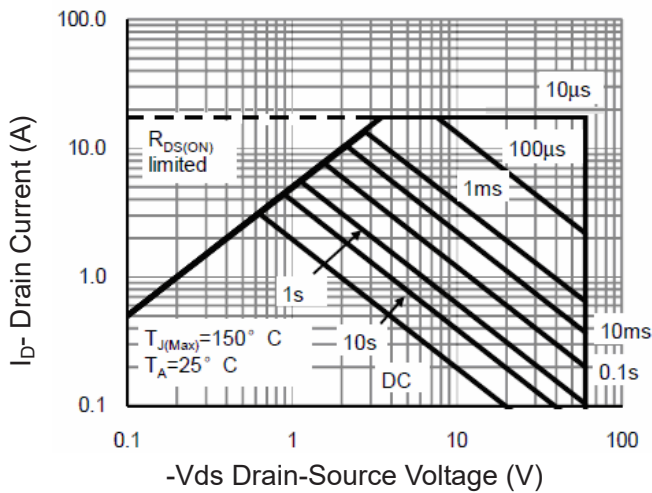
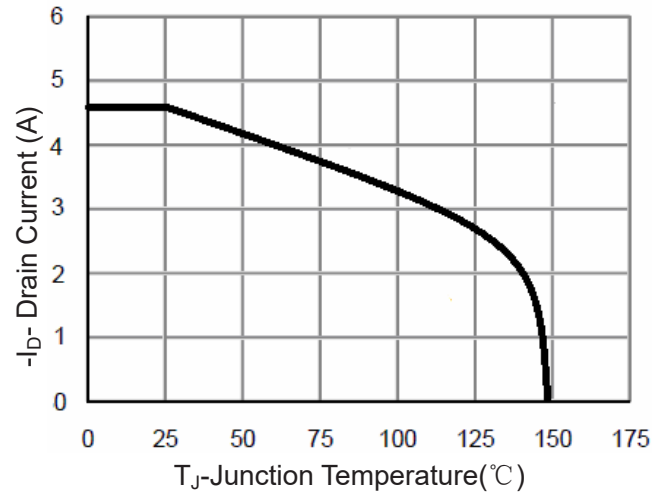
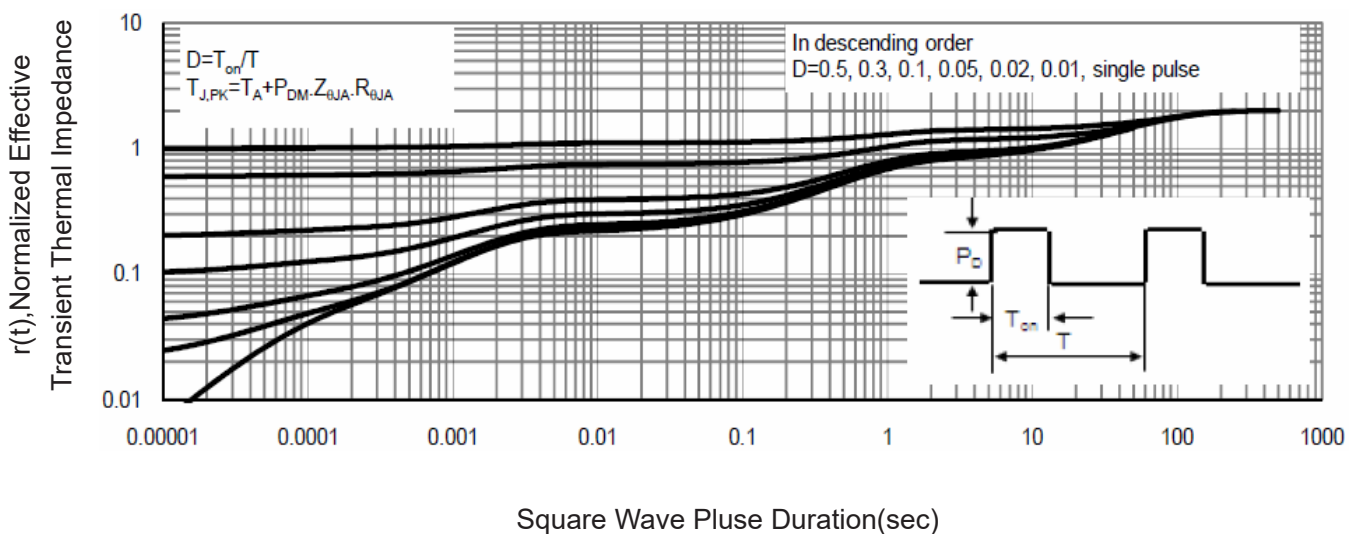
**Figure 4 Rdson-Junction Temperature**



**Figure 5 Gate Charge**



**Figure 6 Source- Drain Diode Forward**


**Figure 7 Capacitance vs Vds**

**Figure 9  $BV_{DSS}$  vs Junction Temperature**

**Figure 8 Safe Operation Area**

**Figure 10  $I_D$  Current De-rating**

**Figure 11 Normalized Maximum Transient Thermal Impedance**