Description

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and with stand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

- -30V,-4.0A,$R_{DS(ON).max}$=50mΩ@V_{GS}=-10V
- Improved dv/dt capability
- Fast switching
- Green device available

Applications

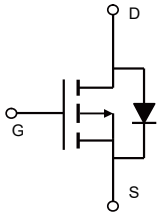
- PWM applications
- Load switch
- Portable Equipment

Product Summary

V_{DSS}	-30V
$R_{DS(on).max}$@ V_{GS}=-10V	50mΩ
I_D	-4.0A

Pin Configuration

SOT-23-3



Schematic

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-30	V
Continuous drain current (T_A = 25°C)	I_D	-4.0	A
Continuous drain current (T_A= 100°C)		-2.5	A
Pulsed drain current[1)]	I_{DM}	-16.0	A
Gate-Source voltage	V_{GSS}	±12	V
Power Dissipation (T_A = 25°C)	P_D	1.2	W
Storage Temperature Range	T_{STG}	-55 to +150	°C
Operating Junction Temperature Range	T_J	-55 to +150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JA}$	104	°C/W

Package Marking and Ordering Information

Device	Device Package	Marking
VSM3481-S2	SOT-23-3	VSM3481-S2

Electrical Characteristics

T_J = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0 V, I_D=-250uA	-30	---	---	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250uA	-0.6	-0.95	-1.3	V
Drain-source leakage current	I_{DSS}	V_{DS}=-30 V, V_{GS}=0 V, T_J = 25°C	---	---	-1	μA
		V_{DS}=-24V, V_{GS}=0 V, T_J = 125°C	---	---	-10	μA
Gate leakage current, Forward	I_{GSSF}	V_{GS}=12 V, V_{DS}=0 V	---	---	100	nA
Gate leakage current, Reverse	I_{GSSR}	V_{GS}=-12 V, V_{DS}=0 V	---	---	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=-10 V, I_D=-4 A	---	41	50	mΩ
		V_{GS}=-4.5 V, I_D=-3.5A	---	47	60	mΩ
		V_{GS}=-2.5 V, I_D=-2.5A		60	85	mΩ
Forward transconductance	g_{fs}	V_{DS} =-5 V , I_D=-4.0A	---	15	---	S
Dynamic characteristics						
Input capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, F = 1MHz	---	1180	---	pF
Output capacitance	C_{oss}		---	80	---	
Reverse transfer capacitance	C_{rss}		---	68	---	
Turn-on delay time	$t_{d(on)}$	V_{DD} = -15V,V_{GS}=-10V, I_D =-4A Rg=3Ω	---	1.8	---	ns
Rise time	t_r		---	30.2	---	
Turn-off delay time	$t_{d(off)}$		---	52.5	---	
Fall time	t_f		---	7.3	---	
Gate resistance	R_g	V_{GS}=0V,V_{DS}=0V,f=1MHz	---	11.5	---	Ω
Gate charge characteristics						
Gate to source charge	Q_{gs}	V_{DS}=-15 V, I_D=-4.0A, V_{GS}=-10 V	---	2.1	---	nC
Gate to drain charge	Q_{gd}		---	2.3	---	
Gate charge total	Q_g		---	19.3	---	
Drain-Source diode characteristics and Maximum Ratings						
Continuous Source Current	I_S		---	---	-4.0	A
Pulsed Source Current[2)]	I_{SM}		---	---	-16.0	A
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=-2A, T_J=25℃	---	---	-1.2	V

Notes:

1: Repetitive Rating: Pulse width limited by maximum junction temperature.

2: Pulse Test：Pulse Width ≤300 μs, Duty Cycle≤2%.

Electrical Characteristics Diagrams

Figure 1. Typ. Output Characteristics

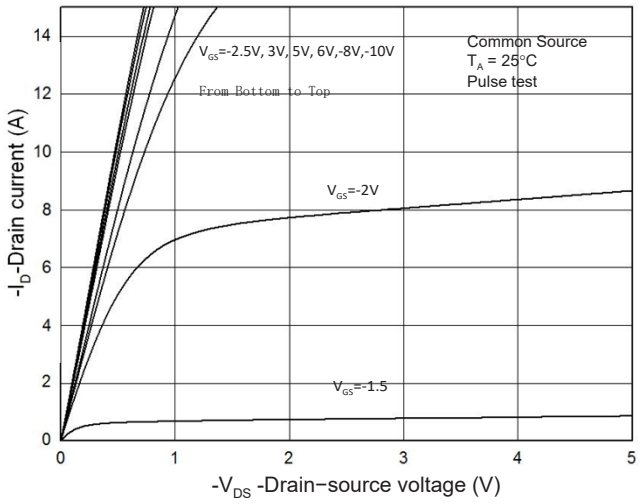


Figure 2. Transfer Characteristics

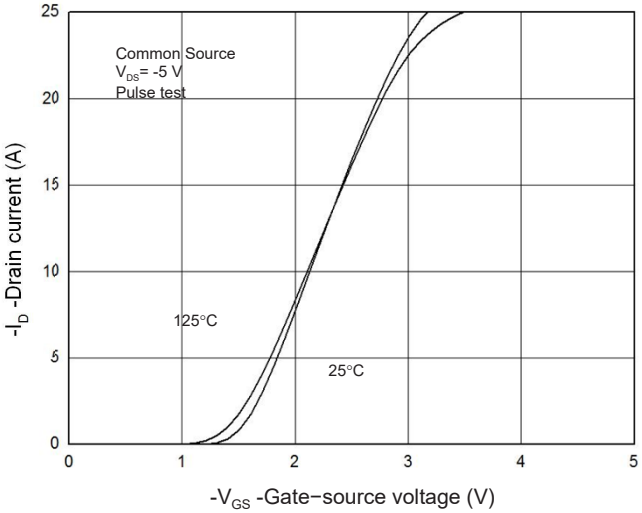


Figure 3. Capacitance Characteristics

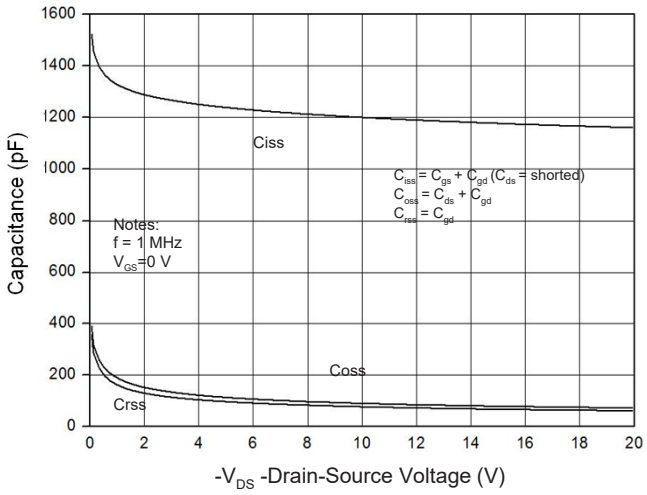


Figure 4. Gate Charge Waveform

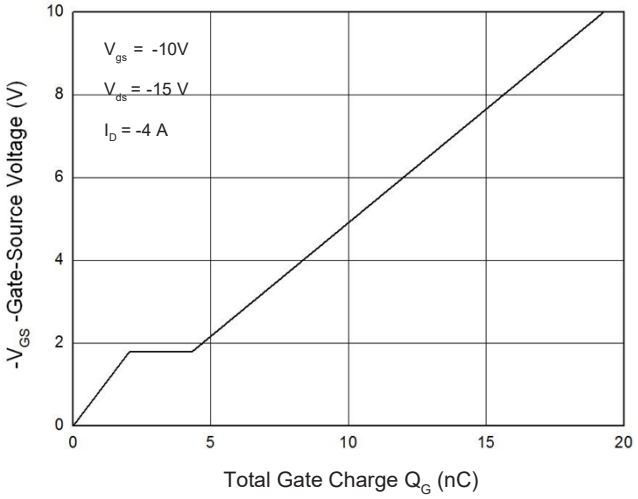


Figure 5. Body-Diode Characteristics

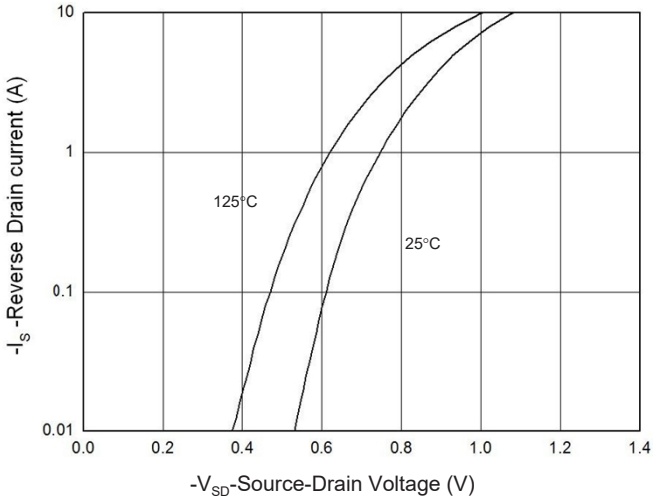


Figure 6. Rdson-Drain Current

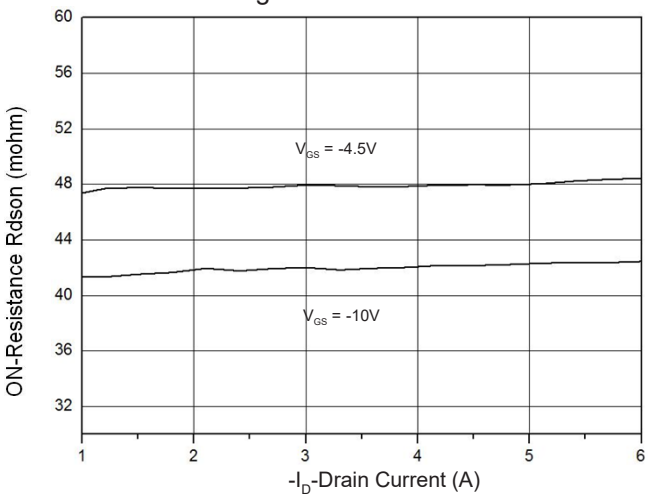


Figure 7. Rdson-Junction Temperature(℃)

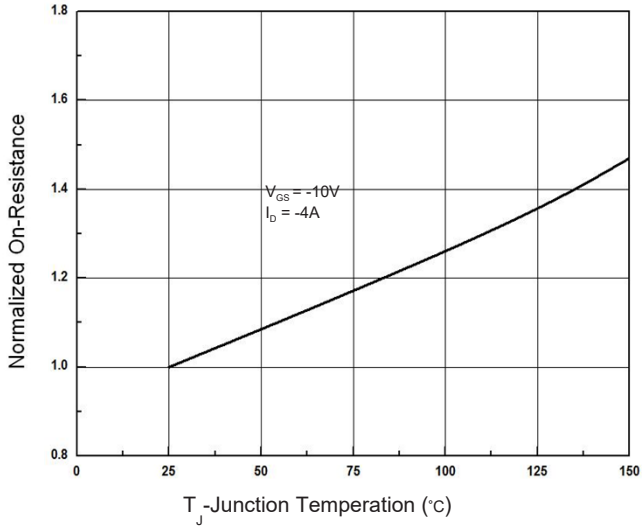


Figure 8. Rds(on) vs Gate Voltage

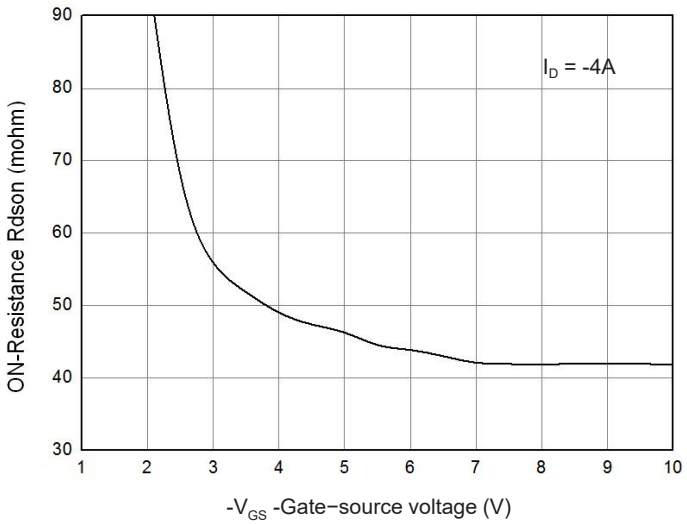


Figure 9. BVdss vs. Junction temperature(℃)

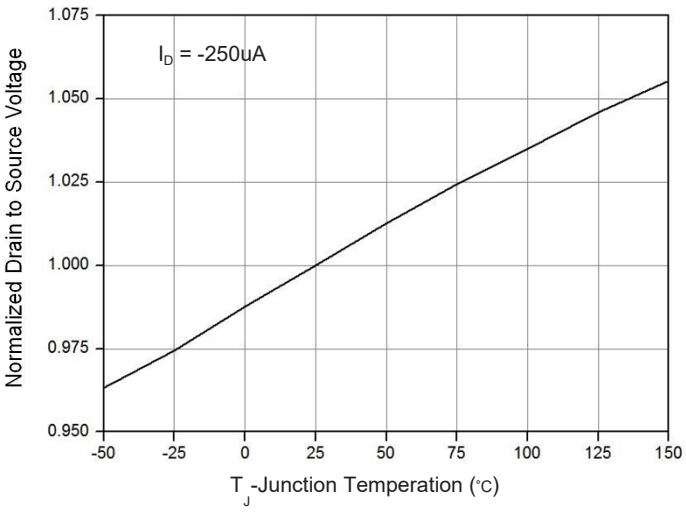


Figure 10. Maximum Safe Operating Area

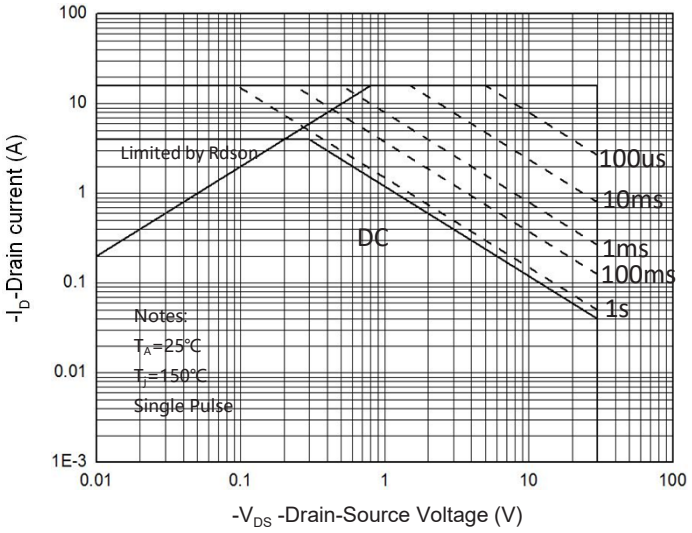
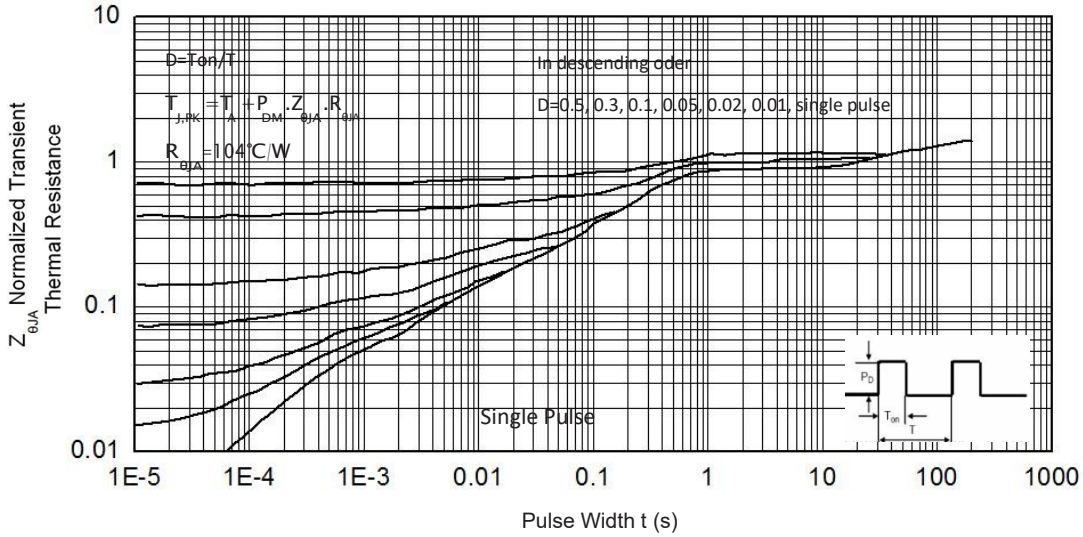


Figure 11. Normalized Maximum Transient Thermal Impedance (RthJA)



Test Circuit & Waveform

Figure 8. Gate Charge Test Circuit & Waveform

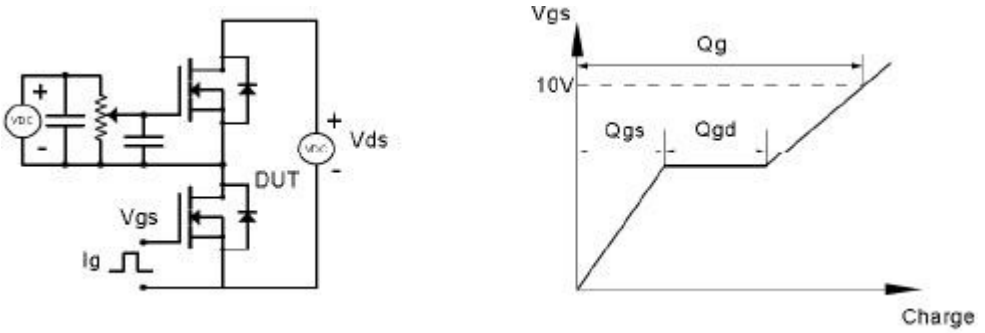


Figure 9. Resistive Switching Test Circuit & Waveforms

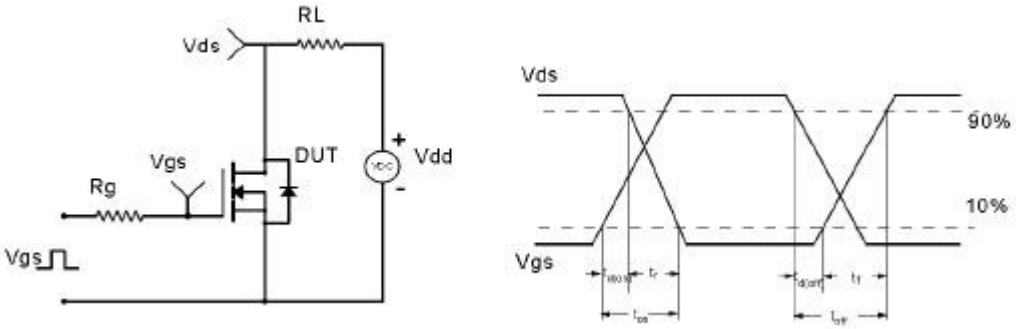


Figure 10. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

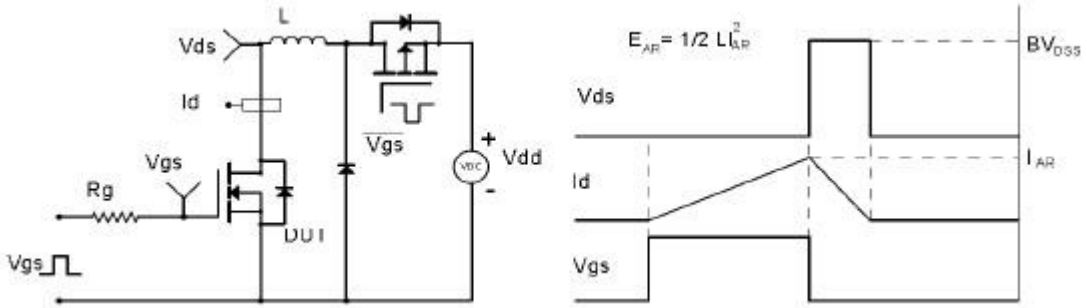


Figure 11. Diode Recovery Circuit & Waveform