

Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and with stand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

- ◆ 40V, 12A, $R_{DS(ON).max}=12m\Omega@V_{GS}=10V$
- ◆ Improved dv/dt capability
- ◆ Fast switching
- ◆ Green device available

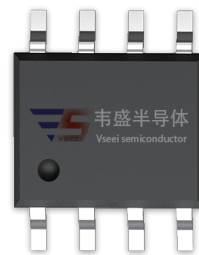
Applications

- ◆ Motor Drives
- ◆ UPS
- ◆ DC-DC Converter

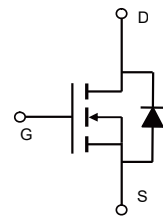
Product Summary

V_{DSS}	40V
$R_{DS(on).max}@V_{GS}=10V$	12m Ω
I_D	12A

Pin Configuration



SOP-8



Schematic

Absolute Maximum Ratings T_A= 25°C unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	40	V
Continuous drain current ($T_A = 25^\circ C$)	I_D	12	A
Continuous drain current ($T_A = 100^\circ C$)		7.6	A
Pulsed drain current ¹⁾	I_{DM}	48	A
Gate-Source voltage	V_{GSS}	± 20	V
Power Dissipation ($T_A = 25^\circ C$)	P_D	2.1	W
Storage Temperature Range	T_{STG}	-55 to +150	°C
Operating Junction Temperature Range	T_J	-55 to +150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	59.5	°C/W

Package Marking and Ordering Information

Device	Device Package	Marking
VSM12N04-S8	SOP-8	VSM12N04-S8

Electrical Characteristics

 $T_J = 25^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0 V, I _D =250uA	40	---	---	V
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1.0	---	2.0	V
Drain-source leakage current	I _{DSS}	V _{DS} =40 V, V _{GS} =0 V, T _J = 25°C	---	---	1	μA
		V _{DS} =32 V, V _{GS} =0 V, T _J = 125°C	---	---	10	μA
Gate leakage current, Forward	I _{GSSF}	V _{GS} =20 V, V _{DS} =0 V	---	---	100	nA
Gate leakage current, Reverse	I _{GSSR}	V _{GS} =-20 V, V _{DS} =0 V	---	---	-100	nA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} =10 V, I _D =12 A	---	9.2	12	mΩ
		V _{GS} =4.5 V, I _D =8 A	---	11.8	16	mΩ
Forward transconductance	g _{fs}	V _{DS} =5 V , I _D =20A	---	35	---	S
Dynamic characteristics						
Input capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, F = 1MHz	---	1370	---	pF
Output capacitance	C _{oss}		---	158	---	
Reverse transfer capacitance	C _{rss}		---	125	---	
Turn-on delay time	t _{d(on)}	V _{DD} = 20V,V _{GS} =10V, I _D =12 A	---	14.5	---	ns
Rise time	t _r		---	19.2	---	
Turn-off delay time	t _{d(off)}		---	61	---	
Fall time	t _f		---	27	---	
Gate resistance	R _g	V _{GS} =0V, V _{DS} =0V, F=1MHz	---	3.5	---	Ω
Gate charge characteristics						
Gate to source charge	Q _{gs}	V _{DS} =20V, I _D =12A, V _{GS} = 10V	---	7.1	---	nC
Gate to drain charge	Q _{gd}		---	2.9	---	
Gate charge total	Q _g		---	27.5	---	
Drain-Source diode characteristics and Maximum Ratings						
Continuous Source Current	I _S		---	---	12	A
Pulsed Source Current ⁽³⁾	I _{SM}		---	---	48	A
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =10A, T _J =25°C	---	---	1.2	V
Reverse Recovery Time	t _{rr}	I _S =12A,di/dt=100A/us, T _J =25°C	---	21	---	ns
Reverse Recovery Charge	Q _{rr}		---	7.8	---	nC

Notes:

1: Repetitive Rating: Pulse width limited by maximum junction temperature.

2: Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

Electrical Characteristics Diagrams

Figure 1. Typ. Output Characteristics

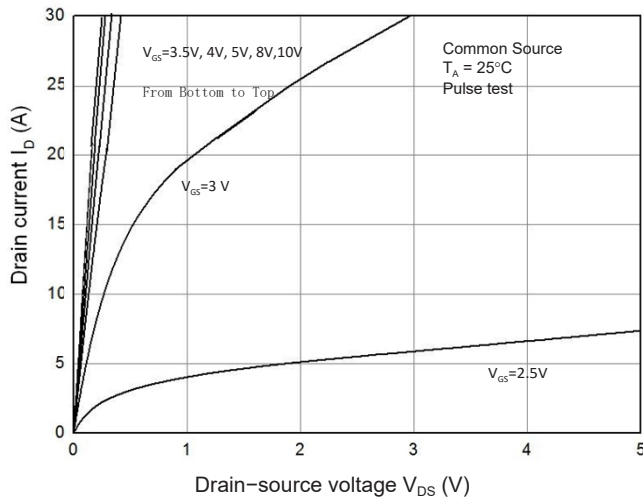


Figure 2. Transfer Characteristics

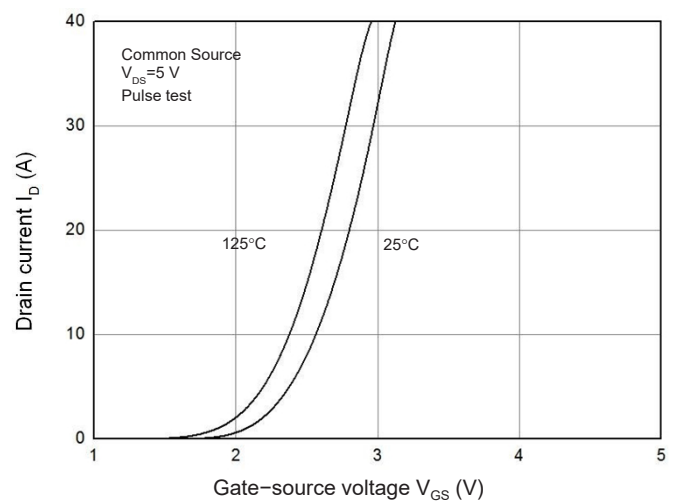


Figure 3. Capacitance Characteristics

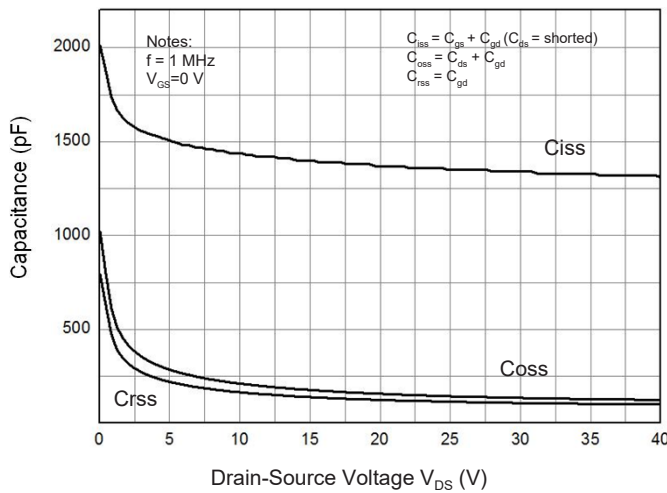


Figure 4. Gate Charge Waveform

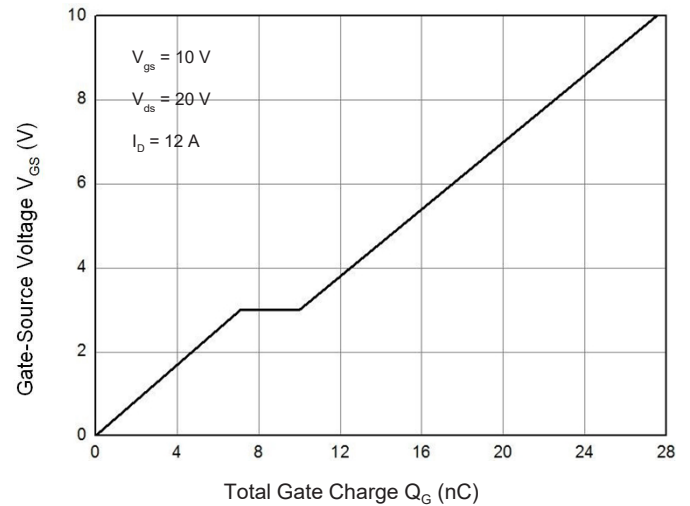


Figure 5. Body-Diode Characteristics

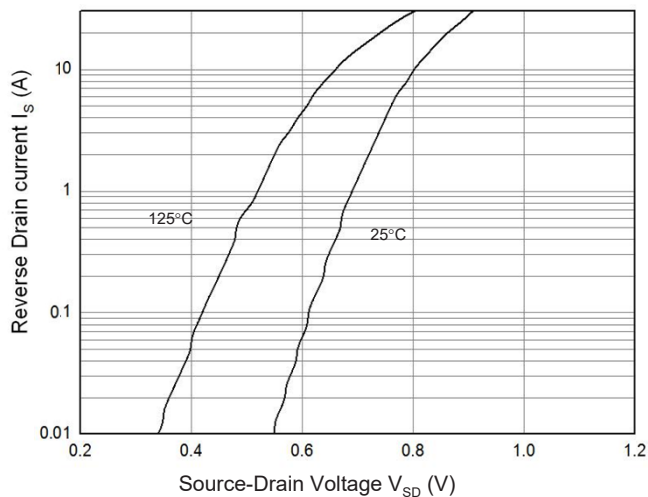


Figure 6. Rdson-Drain Current

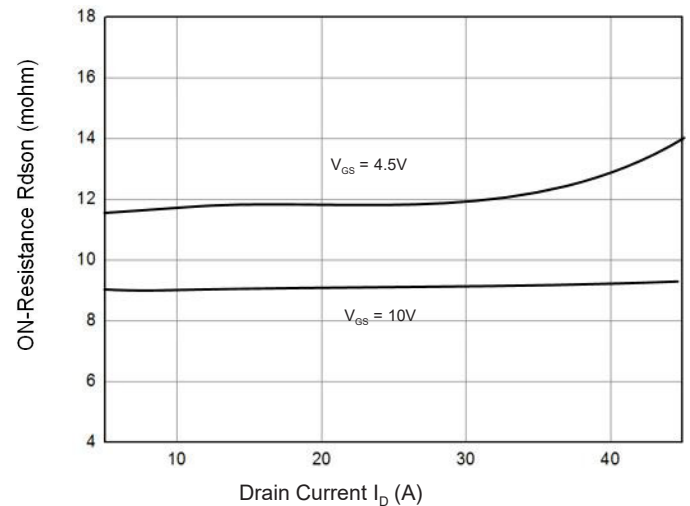


Figure 7. Rdson-Junction Temperature(°C)

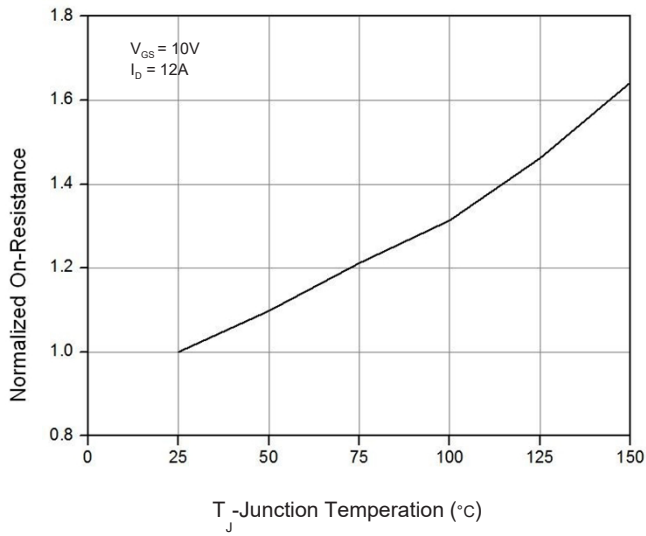


Figure 8. Maximum Safe Operating Area

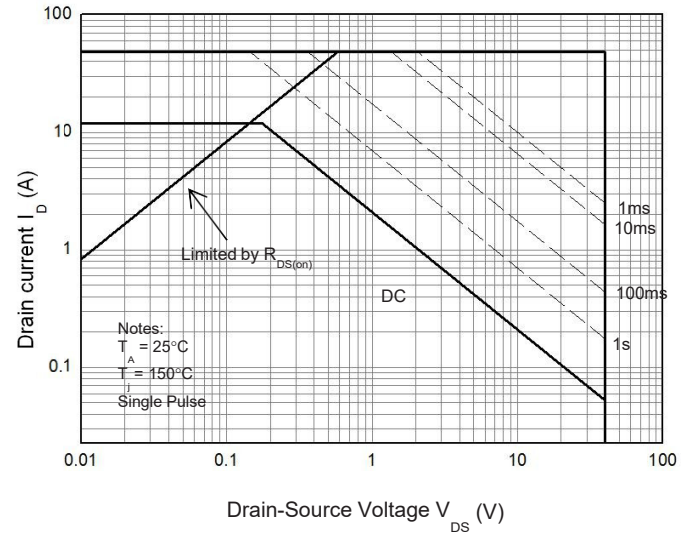
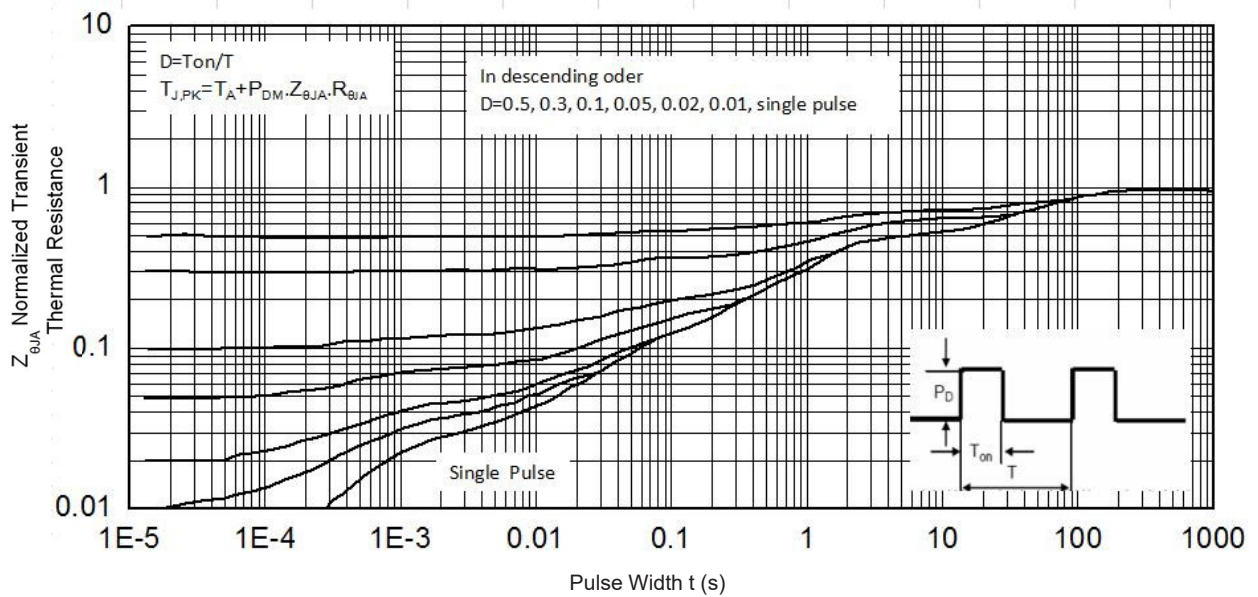


Figure 9. Normalized Maximum Transient Thermal Impedance (RthJA)



Test Circuit & Waveform

Figure 8. Gate Charge Test Circuit & Waveform

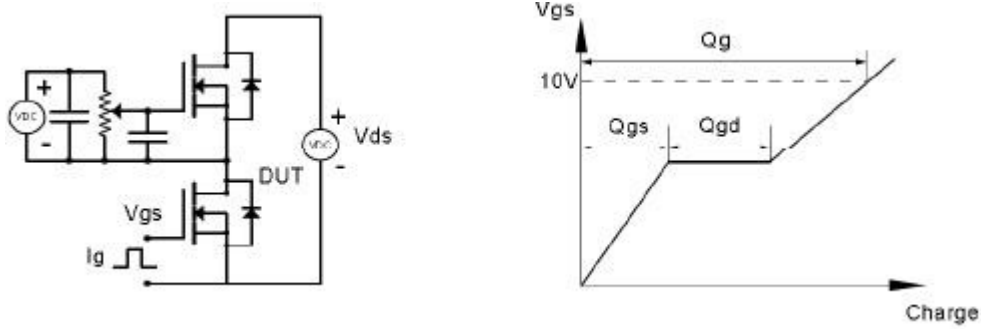


Figure 9. Resistive Switching Test Circuit & Waveforms

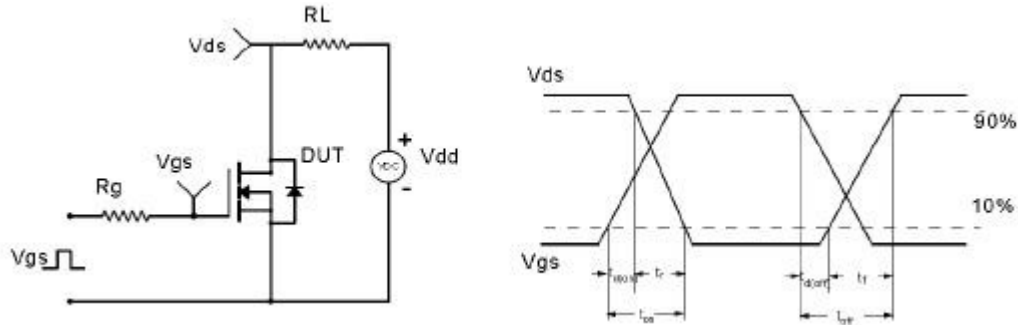


Figure 10. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

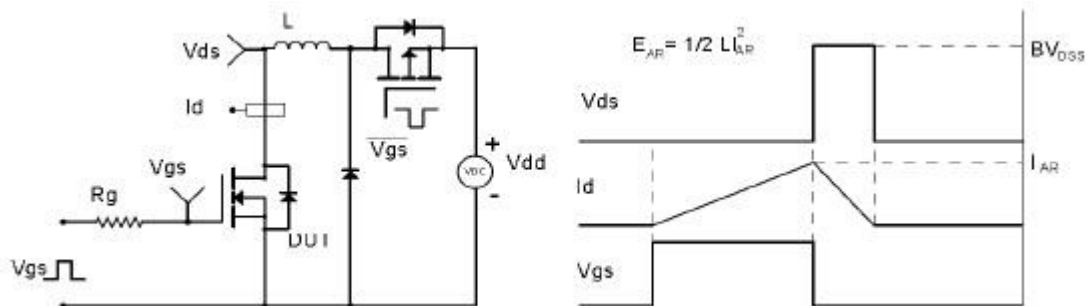


Figure 11. Diode Recovery Circuit & Waveform

