

Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and with stand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

- ◆ 30V,5.8A, $R_{DS(ON).max}=26m\Omega@V_{GS}=10V$
- ◆ Improved dv/dt capability
- ◆ Fast switching
- ◆ Green device available

Applications

- ◆ PWM application
- ◆ Load switch
- ◆ Power management

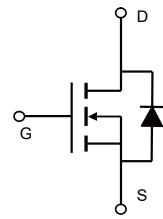
Product Summary

V_{DSS}	30V
$R_{DS(on).max}@V_{GS}=10V$	26m Ω
I_D	5.8A

Pin Configuration



SOT-23-3



Schematic

Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	30	V
Continuous drain current ($T_A = 25^\circ\text{C}$)	I_D	5.8	A
Continuous drain current ($T_A = 100^\circ\text{C}$)		3.7	A
Pulsed drain current ¹⁾	I_{DM}	23.2	A
Gate-Source voltage	V_{GSS}	± 12	V
Power Dissipation ($T_A = 25^\circ\text{C}$)	P_D	1.4	W
Storage Temperature Range	T_{STG}	-55 to +150	$^\circ\text{C}$
Operating Junction Temperature Range	T_J	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	89	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device	Device Package	Marking
VSM3400-S2	SOT-23-3	VSM3400-S2

Electrical Characteristics

 $T_J = 25^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0 V, I _D =250uA	30	---	---	V
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	0.65	1.0	1.35	V
Drain-source leakage current	I _{DSS}	V _{DS} =30 V, V _{GS} =0 V, T _J = 25°C	---	---	1	μA
		V _{DS} =24 V, V _{GS} =0 V, T _J = 125°C	---	---	10	μA
Gate leakage current, Forward	I _{GSSF}	V _{GS} =12 V, V _{DS} =0 V	---	---	100	nA
Gate leakage current, Reverse	I _{GSSR}	V _{GS} =-12 V, V _{DS} =0 V	---	---	-100	nA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} =10 V, I _D =5.8 A	---	18	26	mΩ
		V _{GS} =4.5 V, I _D =5 A	---	20	32	mΩ
		V _{GS} =2.5V, I _D =4A	---	31	52	mΩ
Forward transconductance	g _{fs}	V _{DS} =5 V , I _D =5.8A	---	30	---	S
Dynamic characteristics						
Input capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, F = 1MHz	---	494	---	pF
Output capacitance	C _{oss}		---	62.4	---	
Reverse transfer capacitance	C _{rss}		---	53.7	---	
Gate resistance	R _g	V _{GS} =0V,V _{DS} =0V,f=1MHz	---	4.2	---	mΩ
Turn-on delay time	t _{d(on)}	V _{DD} = 15V,V _{GS} =10V, I _D =5.8 A, R _g =10Ω	---	7.6	---	ns
Rise time	t _r		---	113.2	---	
Turn-off delay time	t _{d(off)}		---	44.4	---	
Fall time	t _f		---	13.6	---	
Gate charge characteristics						
Gate to source charge	Q _{gs}	V _{DS} =15V, I _D =5.8A, V _{GS} = 10V	---	3.3	---	nC
Gate to drain charge	Q _{gd}		---	2.1	---	
Gate charge total	Q _g		---	13.6	---	
Drain-Source diode characteristics and Maximum Ratings						
Continuous Source Current	I _s		---	---	5.8	A
Pulsed Source Current ²⁾	I _{SM}		---	---	23.2	A
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _s =5.8A, T _J =25°C	---	---	1.2	V

Notes:

1: Repetitive Rating: Pulse width limited by maximum junction temperature.

2: Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

Electrical Characteristics Diagrams

Figure 1. Typ. Output Characteristics

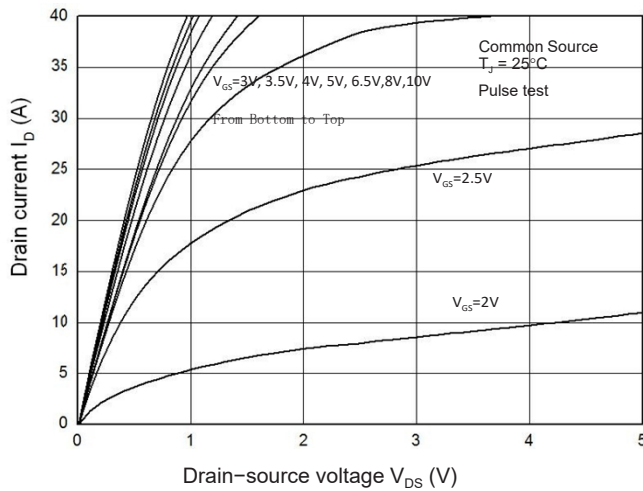


Figure 2. Transfer Characteristics

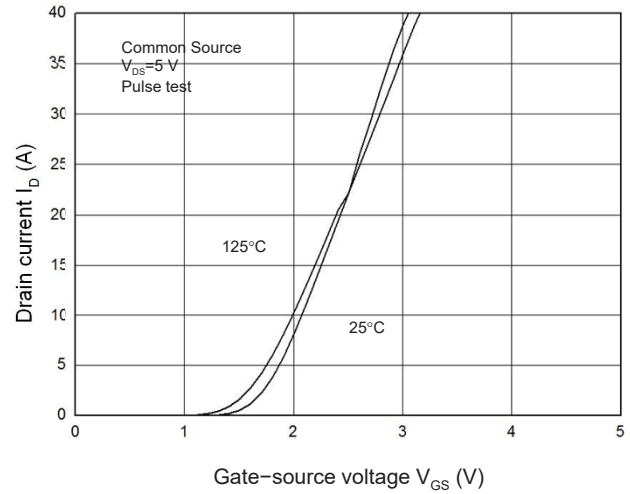


Figure 3. Capacitance Characteristics

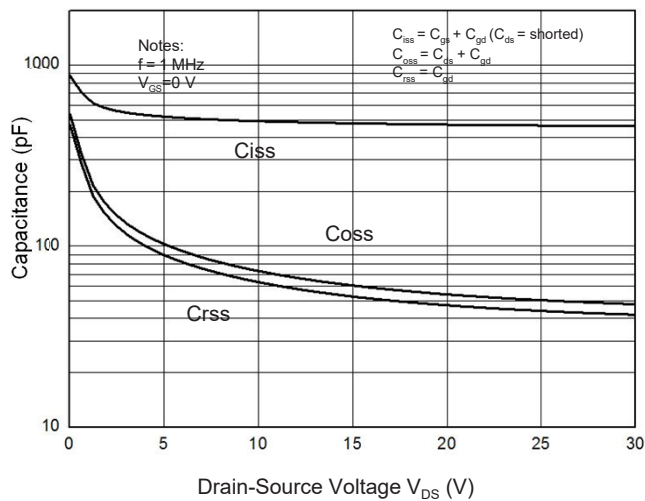


Figure 4. Gate Charge Waveform

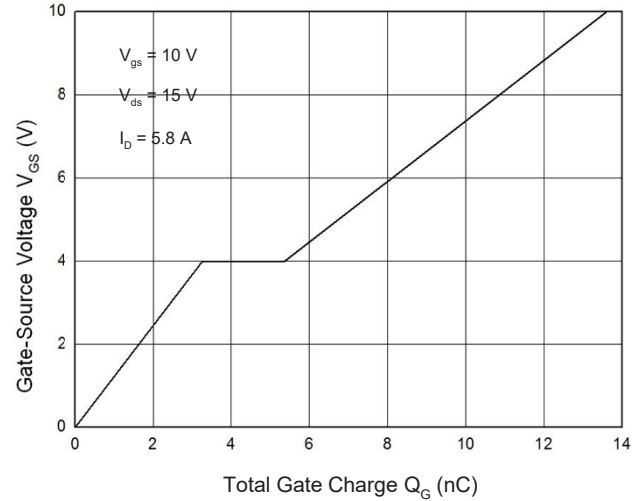


Figure 5. Body-Diode Characteristics

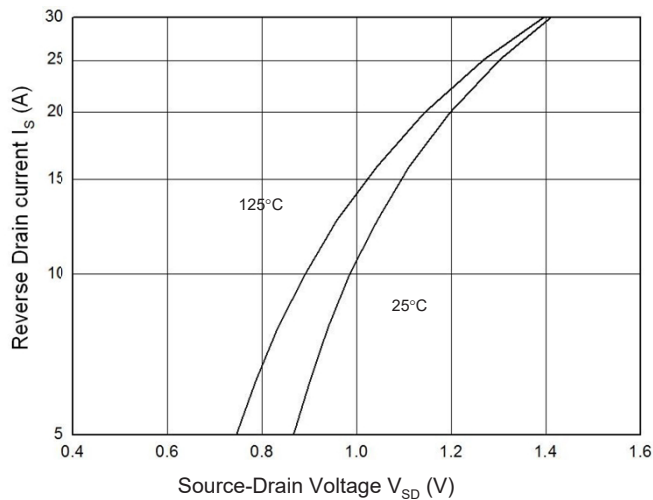


Figure 6. Rdson-Drain Current

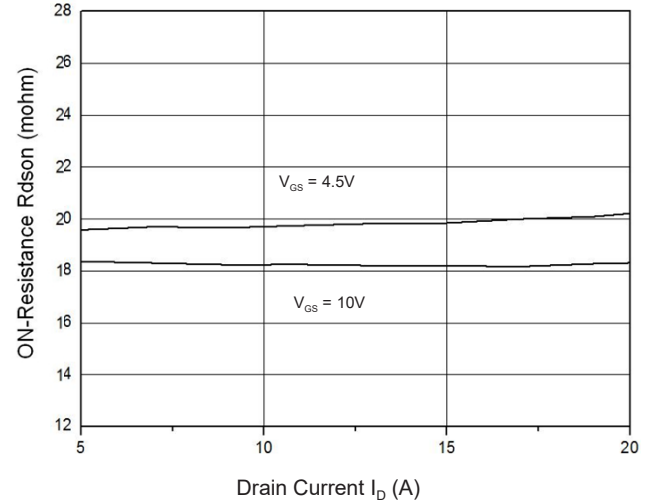


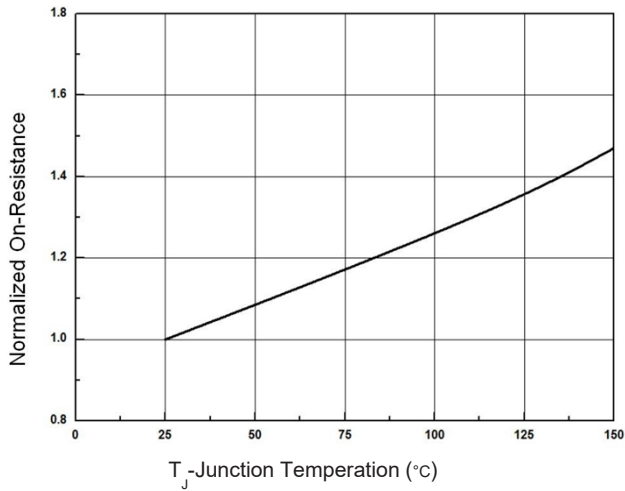
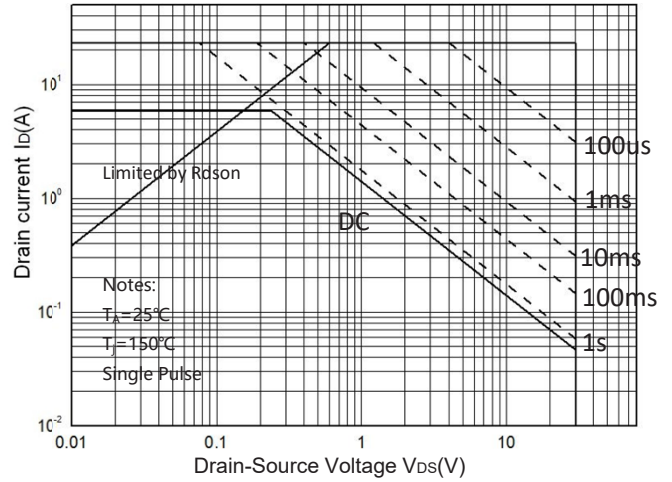
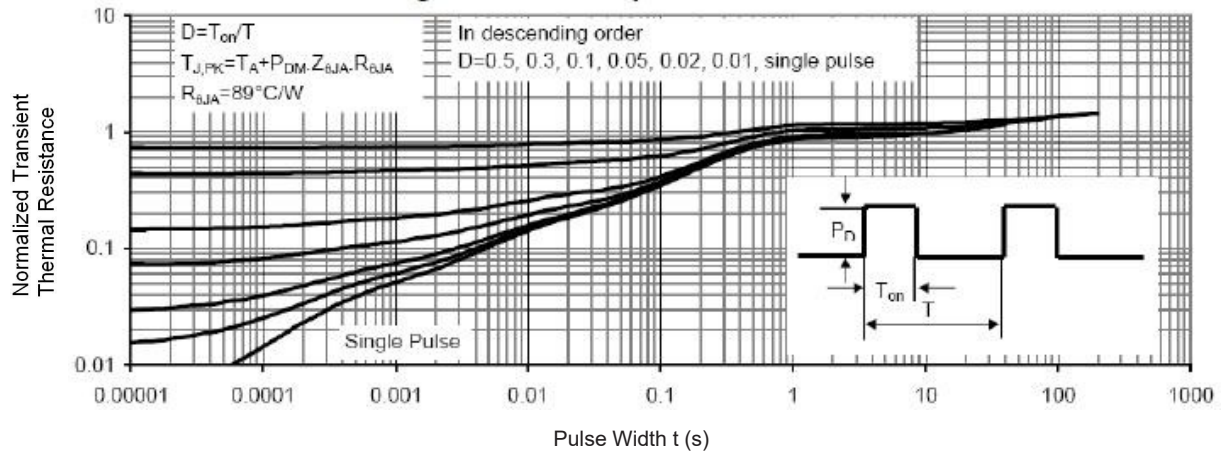
Figure 7. $R_{DS(on)}$ -Junction Temperature($^{\circ}\text{C}$)


Figure 8. Maximum Safe Operating Area


 Figure 9. Normalized Maximum Transient Thermal Impedance (R_{thJA})


Test Circuit & Waveform

Figure 8. Gate Charge Test Circuit & Waveform

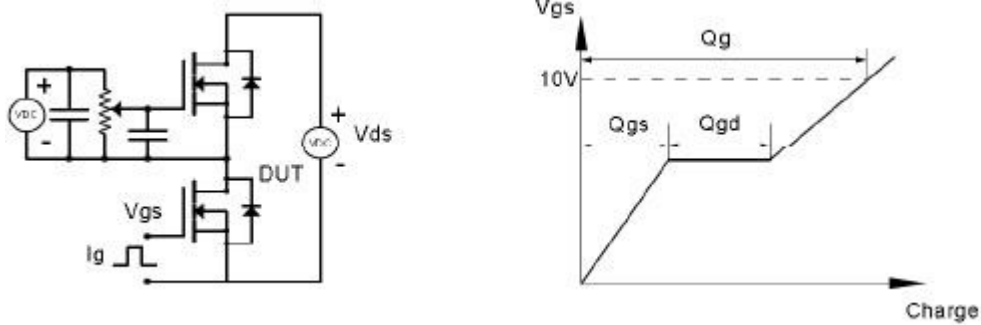


Figure 9. Resistive Switching Test Circuit & Waveforms

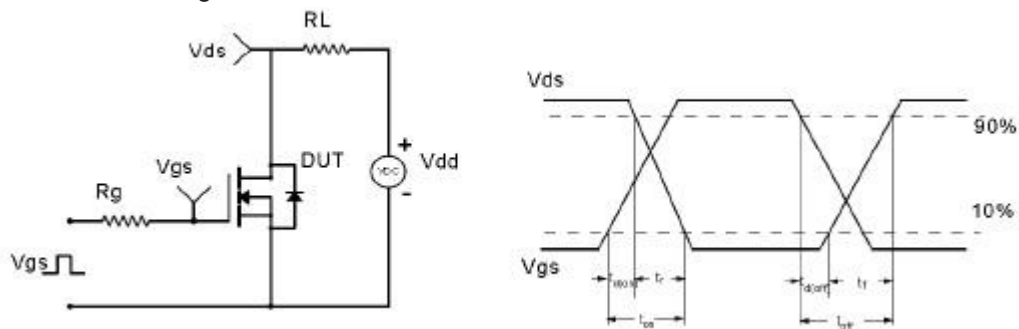


Figure 10. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

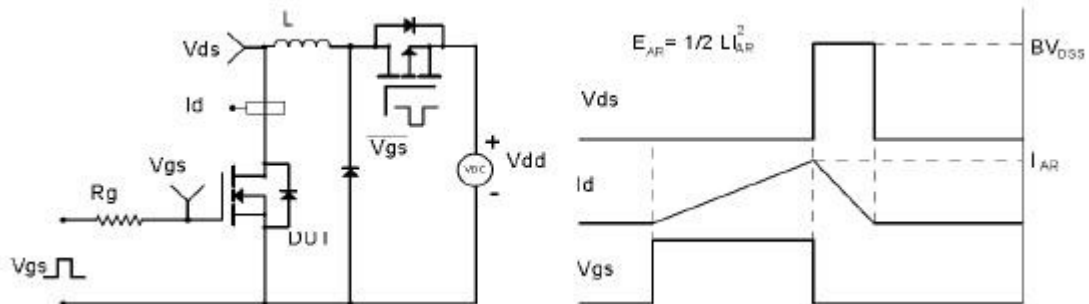


Figure 11. Diode Recovery Circuit & Waveform

