

Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and with stand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

- $40V,120A,R_{DS(on).max}=3.5m\Omega@V_{GS}=10V$
- Improved dv/dt capability
- Fast switching
- 100% EAS Guaranteed
- Green device available

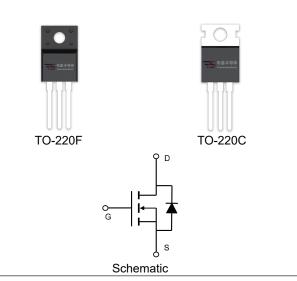
Applications

- Motor Drives
- UPS
- ◆ DC-DC Converter

Product Summary

 $\begin{array}{ll} V_{DSS} & 40V \\ R_{DS(on).max} @\ V_{GS} {=} 10V & 3.5 m\Omega \\ I_D & 120A \end{array}$

Pin Configuration



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	40	V
Continuous drain current (T _C = 25°C) ¹⁾		120	А
Continuous drain current (T _C = 100°C) ¹⁾	I _D	82	А
Pulsed drain current ²⁾	I _{DM}	480	А
Gate-Source voltage	V _{GSS}	±20	V
Avalanche energy ³⁾	Eas	1040	mJ
Power Dissipation (T _C = 25000 C C TO-220	D.	150	W
Power Dissipation (T _C = 25000) C C TO-220F	P _D	48	W
Storage Temperature Range	T _{STG}	-55 to +150	°C
Operating Junction Temperature Range	TJ	-55 to +150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Oase C C TO-220	ם	0.83	°C/W
Thermal Resistance, Junction-to-Oase C C TO-220F	Rejc	2.6	°C/W
Thermal Resistance, Junction-to-Amb@@CCCTO-220		62	°C/W
Thermal Resistance, Junction-to-Amb@ct C C TO-220	R _{0JA}	80	°C/W



Package Marking and Ordering Information

Device	Device Package	Marking
VSM120N04-TF	TO-220F	VSM120N04-TF
VSM120N04-TC	TO-220C	VSM120N04-TC

Electrical Characteristics T_J = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Static characteristics	1				ı	
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0 V, I _D =250uA	40			V
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1.3		2.5	V
Drain-source leakage current		V _{DS} =40 V, V _{GS} =0 V, T _J = 25°C			1	μΑ
	I _{DSS}	V _{DS} =40 V, V _{GS} =0 V, T _J = 125°C			10	μΑ
Gate leakage current, Forward	I _{GSSF}	V _{GS} =20 V, V _{DS} =0 V			100	nA
Gate leakage current, Reverse	I _{GSSR}	V _{GS} =-20 V, V _{DS} =0 V			-100	nA
Duning and the seriet and		V _{GS} =10 V, I _D =20 A		2.7	3.5	mΩ
Drain-source on-state resistance	R _{DS(on)}	V _{GS} =4.5 V, I _D =10 A		3.8	6.0	mΩ
Forward transconductance	g fs	V _{DS} =5 V , I _D =50A	26			S
Dynamic characteristics						
Input capacitance	Ciss	V 00 V V 0 V		7810		pF
Output capacitance	Coss	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V},$		677		
Reverse transfer capacitance	C _{rss}	- F = 1MHz		370		
Turn-on delay time	t _{d(on)}			15		- ns
Rise time	t _r	$V_{DD} = 20V, V_{GS} = 10V, I_D = 20 A$		17		
Turn-off delay time	t _{d(off)}	- VDD - 20V, VGS-10V, ID -20 A		52		
Fall time	t _f			23		
Gate resistance	Rg	V _{GS} =0V, V _{DS} =0V, F=1MHz		2.12		Ω
Gate charge characteristics	•					
Gate to source charge	Q _{gs}	V 00 V 1 400A		36.4		nC
Gate to drain charge	Q _{gd}	V _{DS} =20 V, I _D =100A,		37.3		
Gate charge total	Qg	- V _{GS} = 10 V		139		
Drain-Source diode characteris	tics and Maxi	mum Ratings			,	
Continuous Source Current	Is				120	А
Pulsed Source Current ⁴⁾	I _{SM}				480	А
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =50A, T _J =25℃			1.2	V
Reverse Recovery Time	t _{rr}	I _S =100A, di/dt=100A/us,		42		ns
Reverse Recovery Charge	Q _{rr}			120		nC

Notes:

- 1: The maximum junction current rating is package limited.
- 2: Repetitive Rating: Pulse width limited by maximum junction temperature.
- 3: V_{DD} =20V, V_{GS} =10V, L=1mH, I_{AS} =45.6A, R_{G} =25 Ω , Starting T_{J} =25 $^{\circ}$ C.
- 4: Pulse Test: Pulse Width $\leq 300~\mu$ s, Duty Cycle $\leq 2\%$.



Electrical Characteristics Diagrams

Figure 1. Typ. Output Characteristics

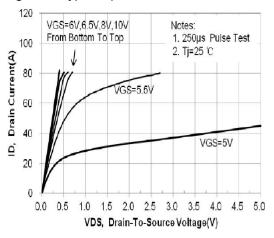


Figure 3. Capacitance Characteristics

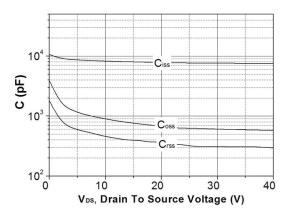


Figure 5. Body-Diode Characteristics

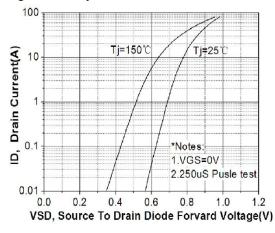


Figure 2. Transfer Characteristics

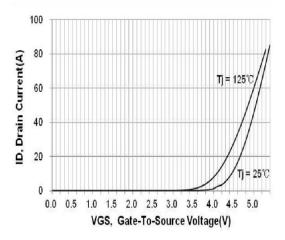


Figure 4. Gate Charge Waveform

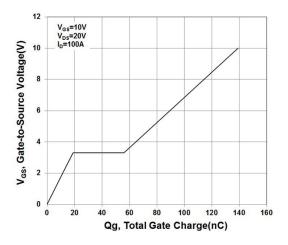


Figure 6. Maximum Safe Operating Area

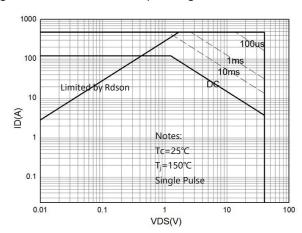




Figure 6. Normalized Maximum Transient Thermal Impedance (RthJC)

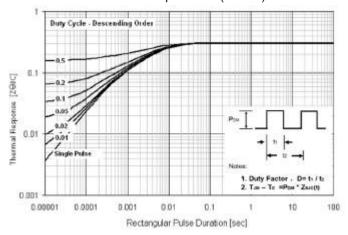
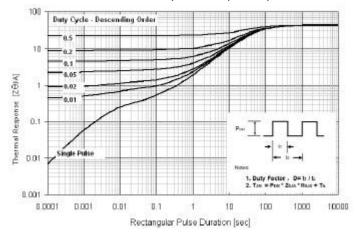


Figure 7. Normalized Maximum Transient Thermal Impedance (RthJA)

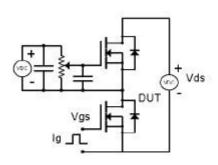


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Test Circuit & Waveform

Figure 8. Gate Charge Test Circuit & Waveform



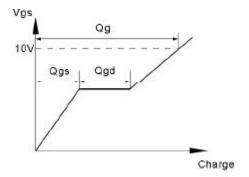
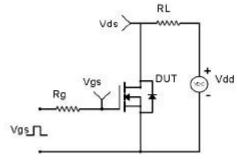


Figure 9. Resistive Switching Test Circuit & Waveforms



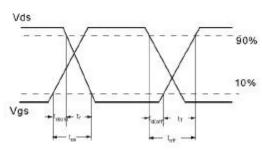
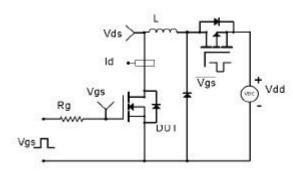


Figure 10. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



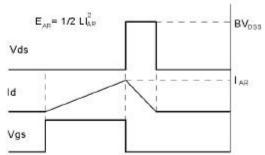


Figure 11. Diode Recovery Circuit & Waveform

