

#### **Description**

#### **Features**

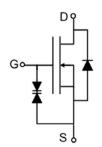
- 20V, 0.75A
  - $R_{DS(ON)}$ < 380m $\Omega$  @  $V_{GS}$  =4.5V  $R_{DS(ON)}$ < 450m $\Omega$  @  $V_{GS}$  =2.5V
- Advanced Trench Technology
- Excellent R<sub>DS(ON)</sub> and Low Gate Charge
- Lead free product is acquired
- ESD Protected: 2KV

#### **Application**

- Load Switch
- PWM Application
- Power management







Schematic Diagram

### **Package Marking and Ordering Information**

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
VSM2002KT2-S2	VSM2002KT2	TAPING	SOT-23-3	-	-	-

### **Absolute Maximum Ratings** ( $T_A$ =25 $^{\circ}$ C unless otherwise specified)

Symbol	Parameter		Max.	Units
V <sub>DSS</sub>	Drain-Source Voltage		20	V
V <sub>GSS</sub>	Gate-Source Voltage		±10	V
I <sub>D</sub>	Continuous Brain Comment	T <sub>A</sub> = 25℃	0.75	Α
	Continuous Drain Current	T <sub>A</sub> = 100°C	0.5	Α
I <sub>DM</sub>	Pulsed Drain Current note1		3	Α
P <sub>D</sub>	Power Dissipation	T <sub>A</sub> = 25°C	0.35	W
R <sub>0JA</sub>	Thermal Resistance, Junction to Case		417	°C/W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	$^{\circ}$



# **Electrical Characteristics** (TJ=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units		
Off Characteristic								
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	20	-	-	V		
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =16V, V <sub>GS</sub> =0V,	-	-	1	μΑ		
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±10V	-	-	±10	uA		
On Characteristics								
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250µA	0.3	0.65	1	V		
	Static Drain-Source on-Resistance	V <sub>GS</sub> =4.5V, I <sub>D</sub> =0.5A	-	250	380	mΩ		
R <sub>DS(on)</sub>	note2	V <sub>GS</sub> =2.5V, I <sub>D</sub> =0.3A	-	350	450			
Dynamic C	Dynamic Characteristics							
C <sub>iss</sub>	Input Capacitance		-	79	-	рF		
Coss	Output Capacitance	$V_{DS}=10V, V_{GS}=0V,$	-	13	-	pF		
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	9	-	pF		
Qg	Total Gate Charge	\/ -10\/   -0.24	-	5	-	nC		
Qgs	Gate-Source Charge	V <sub>DS</sub> =10V, I <sub>D</sub> =0.3A, V <sub>GS</sub> =4.5V	-	0.8	-	nC		
$Q_{gd}$	Gate-Drain("Miller") Charge	VGS-4.3V	-	1.2	-	nC		
Switching	Switching Characteristics							
t <sub>d(on)</sub>	Turn-on Delay Time	\/ 40\/	-	6.7	-	ns		
t <sub>r</sub>	Turn-on Rise Time	V <sub>DS</sub> =10V,	-	4.8	-	ns		
t <sub>d(off)</sub>	Turn-off Delay Time	$I_D$ =0.5A, $R_{GEN}$ =3Ω,	-	17.3	-	ns		
t <sub>f</sub>	Turn-off Fall Time	- V <sub>GS</sub> =4.5V	-	7.4	-	ns		
Drain-Soul	rce Diode Characteristics and Maxim	um Ratings						
Is	Maximum Continuous Drain to Source Diode Forward Current		-	-	0.75	Α		
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current			-	3	Α		
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =0.75A	-	-	1.2	V		

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

<sup>2.</sup> Pulse Test: Pulse Width≤300µs, Duty Cycle≤0.5%



## **Typical Performance Characteristics**

Figure1: Output Characteristics

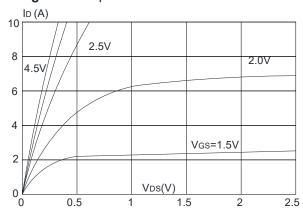


Figure 3:On-resistance vs. Drain Current

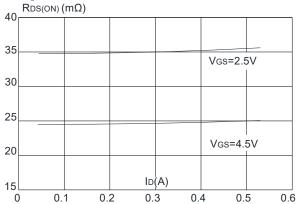


Figure 5: Gate Charge Characteristics

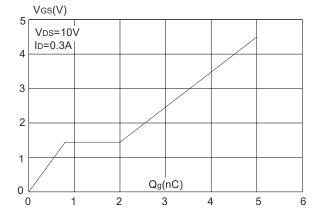


Figure 2: Typical Transfer Characteristics

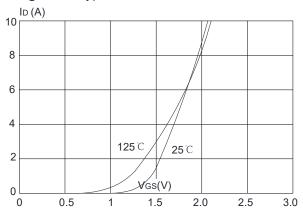


Figure 4: Body Diode Characteristics

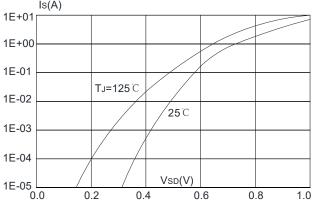
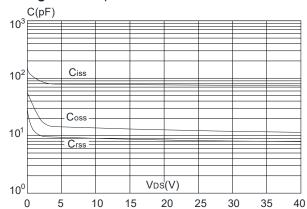


Figure 6: Capacitance Characteristics





**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature

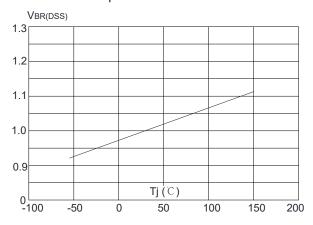
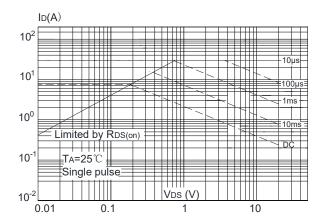
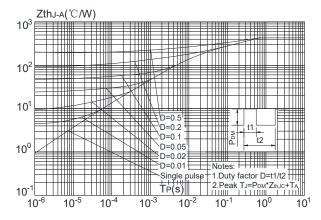


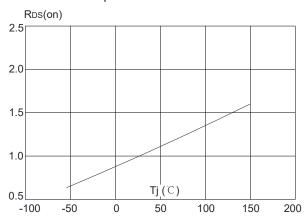
Figure 9: Maximum Safe Operating Area



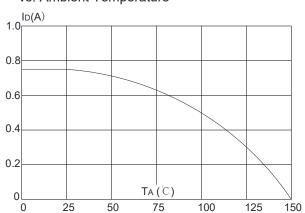
**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



**Figure 8:** Normalized on Resistance vs. Junction Temperature



**Figure 10:** Maximum Continuous Drain Current vs. Ambient Temperature





#### **Test Circuit**

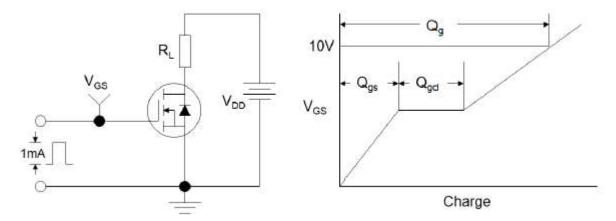


Figure1:Gate Charge Test Circuit & Waveform

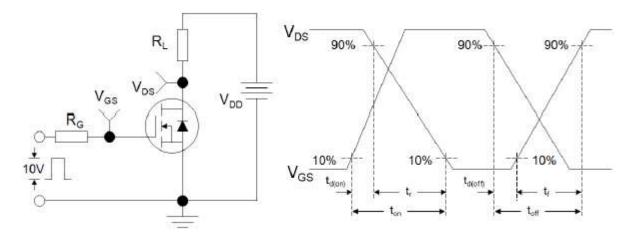


Figure 2: Resistive Switching Test Circuit & Waveforms

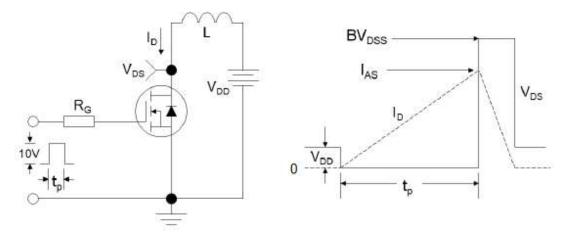


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms