

### **Description**

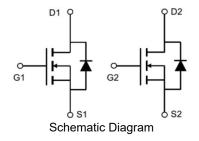
#### **Features**

- 30V, 3.8A
  - $R_{DS(ON)}$ <38m $\Omega$  @  $V_{GS}$ =10V
  - $R_{DS(ON)}$ <65m $\Omega$  @  $V_{GS}$  =4.5V
- Advanced Trench Technology
- Provide Excellent R<sub>DS(ON)</sub> and Low Gate Charge
- Lead free product is acquired

#### **Application**

- Load Switch
- PWM Application
- Power management





### **Package Marking and Ordering Information**

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
VSM3406D-S6	VSM3406D	TAPING	SOT-23-6	7inch	3000	180000

## **Absolute Maximum Ratings** (T<sub>A</sub>=25 ℃ unless otherwise specified)

Symbol	Parameter		Max.	Units
V <sub>DSS</sub>	Drain-Source Voltage		20	V
V <sub>GSS</sub>	Gate-Source Voltage		±20	V
I <sub>D</sub>	Continuous Drain Current	T <sub>A</sub> = 25℃	3.8	Α
		T <sub>A</sub> = 100°C	2.5	Α
I <sub>DM</sub>	Pulsed Drain Current note1		15.2	Α
P <sub>D</sub>	Power Dissipation	T <sub>A</sub> = 25℃	1	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		125	°C/W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	$^{\circ}\mathbb{C}$



# **Electrical Characteristics** (T<sub>J</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units		
Off Characteristic								
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250µA	30	-	-	V		
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V,	-	-	1.0	μA		
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V	-	-	±100	nA		
On Charac	teristics							
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_{D}=250\mu A$	1.0	1.5	2.5	V		
П	Static Drain-Source on-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =3A	-	29	38	mΩ		
$R_{DS(on)}$	note2	V <sub>GS</sub> =4.5V, I <sub>D</sub> =2A	-	46	65			
Dynamic C	Characteristics	•						
C <sub>iss</sub>	Input Capacitance	\\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	-	233	_	pF		
Coss	Output Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V,	-	44	-	pF		
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	33	-	pF		
Qg	Total Gate Charge	\/ -15\/   -24	-	3	-	nC		
$Q_{gs}$	Gate-Source Charge	V <sub>DS</sub> =15V, I <sub>D</sub> =2A, V <sub>GS</sub> =10V	-	0.5	-	nC		
$Q_{gd}$	Gate-Drain("Miller") Charge	VGS-10V	-	0.8	-	nC		
Switching	Characteristics							
t <sub>d(on)</sub>	Turn-on Delay Time	\	-	4	-	ns		
t <sub>r</sub>	Turn-on Rise Time	V <sub>DS</sub> =15V,	-	2.1	-	ns		
t <sub>d(off)</sub>	Turn-off Delay Time	$I_D$ =3A, $R_{GEN}$ =3 $\Omega$ , $V_{GS}$ =10V	-	15	-	ns		
t <sub>f</sub>	Turn-off Fall Time	VGS-10V	-	3.2	-	ns		
Drain-Sou	rce Diode Characteristics and Maxim	um Ratings						
Maximum Continuous Drain to Source Di		e Diode Forward	_	_	3.8	Α		
Is	Current			_	5.0			
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current			-	15.2	Α		
$V_{SD}$	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =3.8A	-	-	1.2	V		

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

<sup>2.</sup> Pulse Test: Pulse Width≤300µs, Duty Cycle≤0.5%



# **Typical Performance Characteristics**

Figure1: Output Characteristics

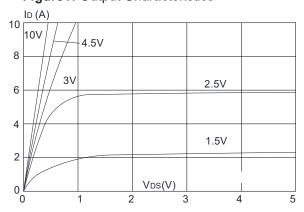


Figure 3:On-resistance vs. Drain Current

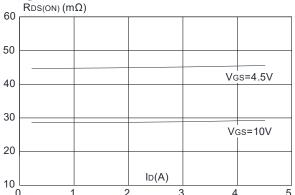


Figure 5: Gate Charge Characteristics

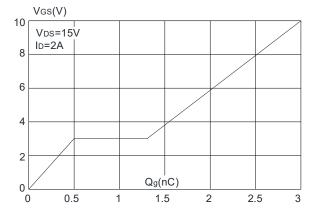


Figure 2: Typical Transfer Characteristics

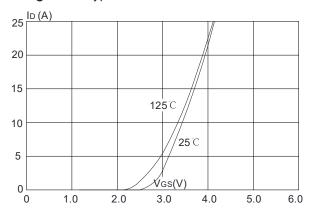


Figure 4: Body Diode Characteristics

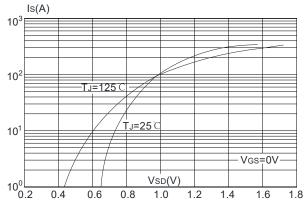
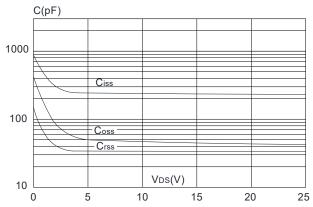


Figure 6: Capacitance Characteristics





**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature

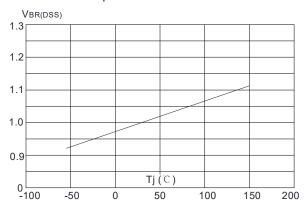
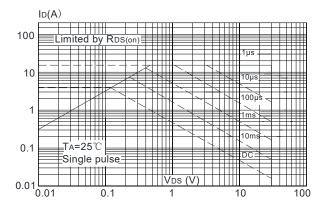
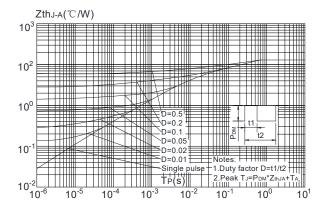


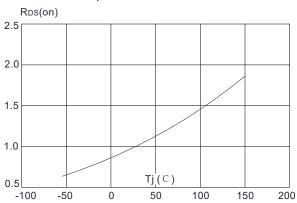
Figure 9: Maximum Safe Operating Area



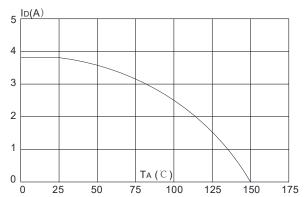
**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



**Figure 8:** Normalized on Resistance vs. Junction Temperature



**Figure 10:** Maximum Continuous Drain Current vs. Ambient Temperature





## **Test Circuit**

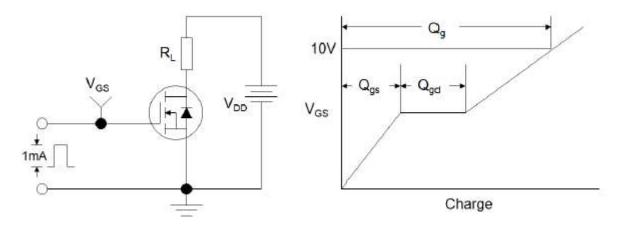


Figure1:Gate Charge Test Circuit & Waveform

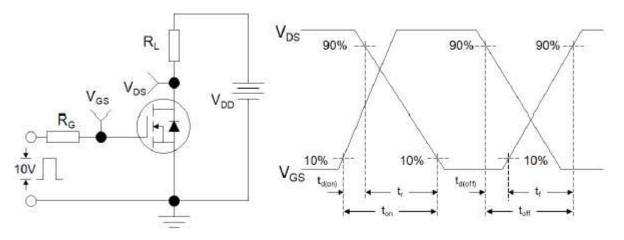


Figure 2: Resistive Switching Test Circuit & Waveforms

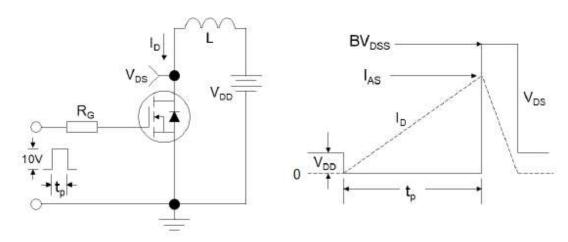


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms