

#### **Description**

#### **Features**

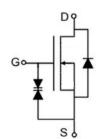
- 150V, 0.2A
  - $R_{DS(ON)}$ < 10 $\Omega$  @  $V_{GS}$  =10V
  - $R_{DS(ON)}$ < 15 $\Omega$  @  $V_{GS}$ =0V
- Self-aligned planner technology
- Pb-free lead plating
- Halogen free
- ESD improved capability

#### **Application**

- Load Switch
- PWM Application
- Power management







Schematic Diagram

## **Package Marking and Ordering Information**

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
VSM1515A-S2	VSM1515A	TAPING	SOT-23-3	7inch	3000	180000

#### **Absolute Maximum Ratings** (T<sub>A</sub>=25 ℃ unless otherwise specified)

Symbol	Parameter	Max.	Units	
$V_{DSS}$	Drain-Source Voltage		150	٧
V <sub>GSS</sub>	Gate-Source Voltage	±20	V	
I <sub>D</sub>	Continuous Drain Current	T <sub>A</sub> = 25℃	0.2	Α
	Continuous Diain Current	T <sub>A</sub> = 100℃	0.13	Α
I <sub>DM</sub>	Pulsed Drain Current note1		0.8	Α
dv/dt	Peak Diode Recovery dv/dt		5.0	V/ns
P <sub>D</sub>	Power Dissipation	T <sub>A</sub> = 25℃	0.5	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		250	°C/W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	$^{\circ}$



# **Electrical Characteristics** (T<sub>J</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units	
Off Characteristic							
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = -15V, I <sub>D</sub> =250μA	150	-	-	V	
I <sub>D(off)</sub>	Off-state Drain to Source Current	V <sub>DS</sub> =150V, V <sub>GS</sub> = -15V, T <sub>J</sub> =25°C	-	-	0.1	μΑ	
		V <sub>DS</sub> =120V, V <sub>GS</sub> =-15V, T <sub>J</sub> =125°C	-	-	10	μΑ	
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	1	-	±100	nA	
On Charac	teristics			•	•		
I <sub>DSS</sub>	On-state drain current	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V	0.2	-	-	Α	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =3V, I <sub>D</sub> =8µA	-8.0	-6.5	-5.0	V	
	Static Drain-Source on-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =0.2A	-	7.3	10	Ω	
$R_{DS(on)}$	note2	V <sub>GS</sub> =0V, I <sub>D</sub> =0.2A	1	9.5	15		
Dynamic C	Characteristics	•					
C <sub>iss</sub>	Input Capacitance	V 05VV 45V	-	12	-	pF	
Coss	Output Capacitance	$V_{DS} = 25V, V_{GS} = -15V,$ - f = 1.0MHz	-	5.5	-	pF	
C <sub>rss</sub>	Reverse Transfer Capacitance		1	2.1	-	pF	
Qg	Total Gate Charge	)/ 75\/ L 0.04	-	1.5	-	nC	
$Q_{gs}$	Gate-Source Charge	$V_{DS} = 75V$ , $I_{D} = 0.2A$ , $V_{GS} = -10V$ to $0V$	-	0.8	-	nC	
$Q_{gd}$	Gate-Drain("Miller") Charge	VGS =- 10V to 0V	-	0.55	-	nC	
Switching	Characteristics	•					
t <sub>d(on)</sub>	Turn-on Delay Time	75)	-	9.5	-	ns	
t <sub>r</sub>	Turn-on Rise Time	$V_{DS}$ =75V, $I_{D}$ =0.2A, $R_{GEN}$ =20 $\Omega$ ,	-	21	-	ns	
t <sub>d(off)</sub>	Turn-off Delay Time		-	9	-	ns	
t <sub>f</sub>	Turn-off Fall Time	V <sub>GS</sub> =-10V to 0V	-	25	-	ns	
Drain-Sou	rce Diode Characteristics and Maxin	num Ratings					
Is	Maximum Continuous Drain to Source Diode Forward Current		-	-	0.2	Α	
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current			-	0.8	Α	
V <sub>SD</sub>	Diode Forward Voltage	I <sub>F</sub> =0.2A, VGS=-15V	-	-	1.2	V	
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> =-15V, I <sub>F</sub> =0.01A,	-	260	-	ns	
Qrr	Reverse Recovery Charge di/dt=100A/µs		ı	650	-	nC	

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

<sup>2.</sup> Pulse Test: Pulse Width≤300µs, Duty Cycle≤0.5%



Figure1: Output Characteristics

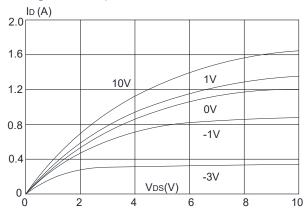


Figure 3:On-resistance vs. Drain Current

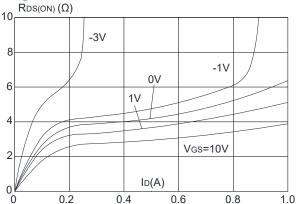


Figure 5: Gate Charge Characteristics

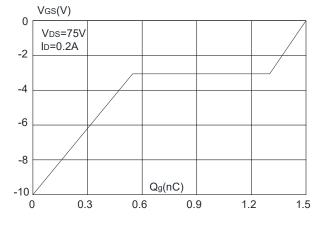


Figure 2: Typical Transfer Characteristics

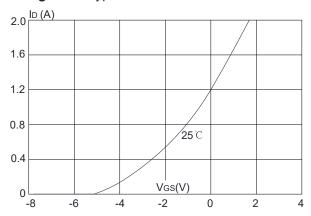


Figure 4: Body Diode Characteristics

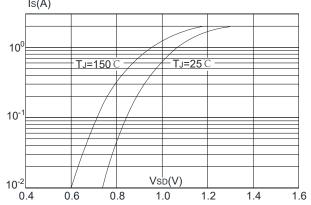
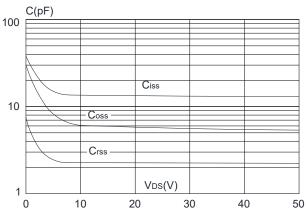


Figure 6: Capacitance Characteristics





**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature

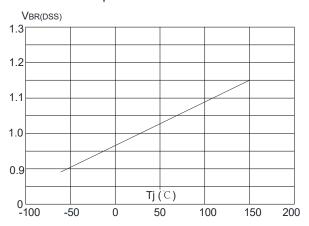
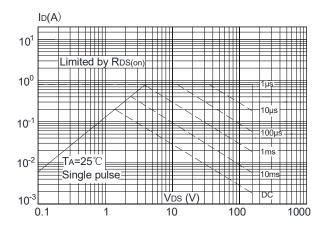
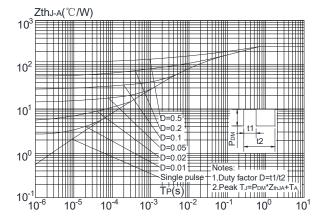


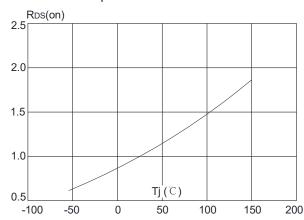
Figure 9: Maximum Safe Operating Area



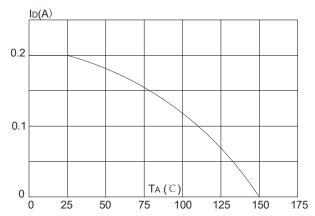
**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



**Figure 8:** Normalized on Resistance vs. Junction Temperature



**Figure 10:** Maximum Continuous Drain Current vs. Ambient Temperature





## **Test Circuit**

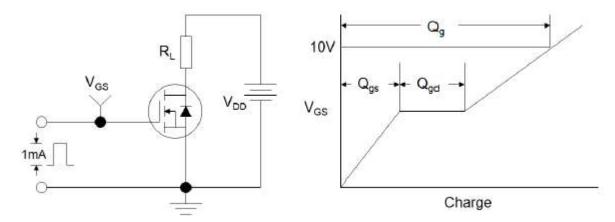


Figure1:Gate Charge Test Circuit & Waveform

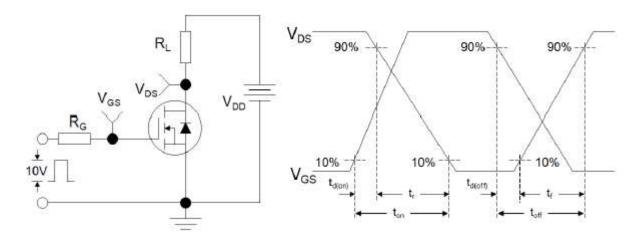


Figure 2: Resistive Switching Test Circuit & Waveforms

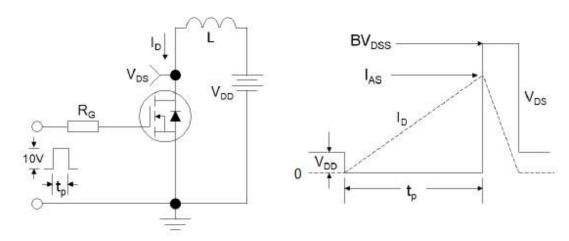


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms