

### **Description**

#### **Features**

- 650V,20A
- $R_{DS(ON)} = 0.35\Omega$  (Typ.) @  $V_{GS} = 10V$ ,  $I_D = 10A$
- Fast Switching
- Improved dv/dt Capability
- 100% Avalanche Tested

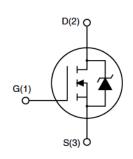
#### **Application**

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- Power Factor Correction (PFC)









247 TO-3P

-220F Schematic Diagram

### **Absolute Maximum Ratings** (Tc=25℃ unless otherwise specified)

Symbol	Parameter		Ma	Heite	
			TO-220F	TO-247/TO-3P	Units
V <sub>DSS</sub>	Drain-Source Voltage		65	V	
Vgss	Gate-Source Voltage		±3	V	
l <sub>D</sub>	Continuous Drain Current	T <sub>C</sub> = 25℃	2	Α	
		T <sub>C</sub> = 100 °C	1	13	
$I_{DM}$	Pulsed Drain Current note1		8	Α	
E <sub>AS</sub>	Single Pulsed Avalanche Energy note2		13	mJ	
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25°C	167	416	W
Rejc	Thermal Resistance, Junction to Case		0.75	0.3	°C/W
Reja	Thermal Resistance, Junction to Ambient		60	60 60	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to	$^{\circ}$ C	



# **Electrical Characteristics** ( $T_C=25^{\circ}C$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units			
Off Characteristic									
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V,I <sub>D</sub> =250µA	650	-	-	V			
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 650V, V_{GS} = 0V,$ $T_{J} = 25^{\circ}C$	-	-	1	μA			
Igss	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±30V	-	-	±100	nA			
On Charac	cteristics								
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS}$ = $V_{GS}$ , $I_D$ =250 $\mu$ A	2	3	4	V			
R <sub>DS(on)</sub>	Static Drain-Source on-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	-	0.35	0.45	Ω			
Dynamic (	Characteristics		•	•	•				
Ciss	Input Capacitance	05)/// 07//	-	2978	-	pF			
Coss	Output Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$	-	291	-	pF			
Crss	Reverse Transfer Capacitance	f = 1.0MHz	-	40	-	pF			
Qg	Total Gate Charge	V <sub>DD</sub> = 520V, I <sub>D</sub> = 20A, V <sub>GS</sub> = 10V	-	80	-	nC			
Qgs	Gate-Source Charge		-	12	-	nC			
$Q_{gd}$	Gate-Drain("Miller") Charge	VGS - 10V	-	34	-	nC			
Switching	Characteristics								
t <sub>d(on)</sub>	Turn-on Delay Time		-	37	-	ns			
tr	Turn-on Rise Time	$V_{DD} = 325V$ , $I_D = 20A$ ,	-	66	-	ns			
t <sub>d(off)</sub>	Turn-off Delay Time	$R_G = 25\Omega$	-	175	-	ns			
<b>t</b> f	Turn-off Fall Time		-	84	-	ns			
Drain-Sou	rce Diode Characteristics and Maxim	num Ratings							
ls	Maximum Continuous Drain to Source Diode Forward Current		-	-	20	Α			
Ism	Maximum Pulsed Drain to Source Diode Forward Current			-	80	Α			
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	te Diode Forward $V_{GS} = 0V$ , $I_{SD} = 20A$		-	1.4	V			
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> =0V, I <sub>S</sub> =20A,	-	450	-	ns			
Qrr	Reverse Recovery Charge	di/dt=100A/µs	-	7.1	-	μC			

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

- 2. I<sub>AS</sub> =16A,  $V_{DD}$  = 50V,  $R_G$  = 25  $\Omega$ , Starting  $T_J$  = 25°C
- 3. Pulse Test: Pulse Width≤350µs, Duty Cycle≤1%



## **Typical Performance Characteristics**

Figure1: Output Characteristics

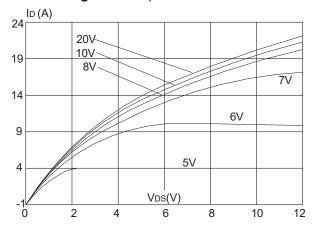


Figure 3:On-resistance vs. Drain Current

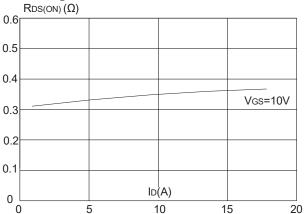


Figure 5: Gate Charge Characteristics

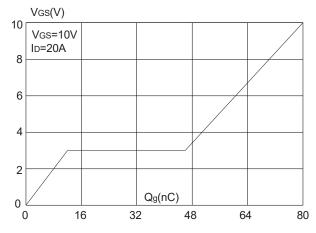


Figure 2: Typical Transfer Characteristics

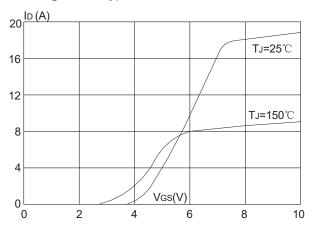


Figure 4: Body Diode Characteristics

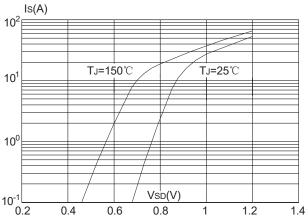
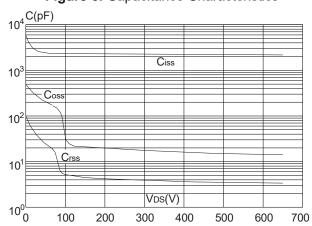


Figure 6: Capacitance Characteristics





**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature

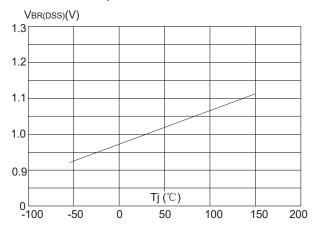


Figure 9: Maximum Safe Operating Area

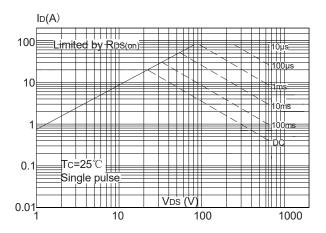
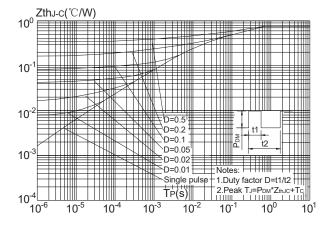
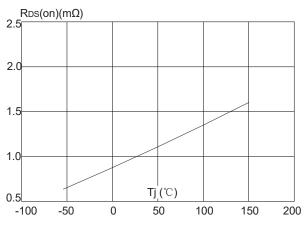


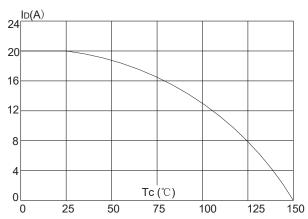
Figure.11: Maximum Effective
Transient Thermal Impedance, Junction-to-Case
(TO-220F)



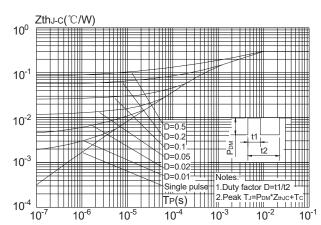
**Figure 8:** Normalized on Resistance vs. Junction Temperature



**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature



**Figure.12:** Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-247,TO-3P)





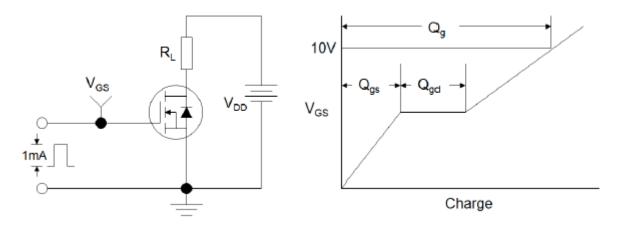


Figure1:Gate Charge Test Circuit & Waveform

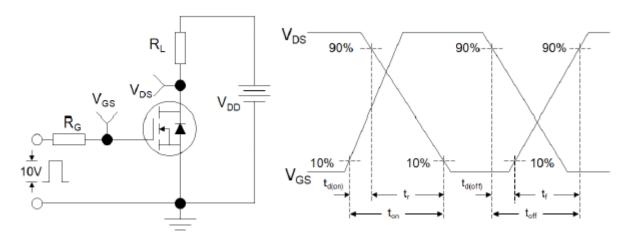


Figure 2: Resistive Switching Test Circuit & Waveforms

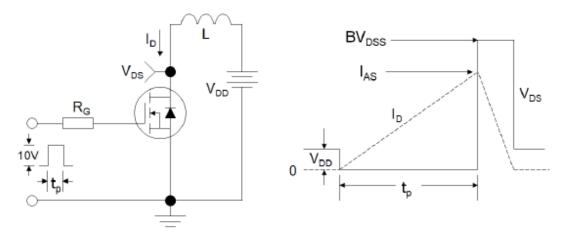
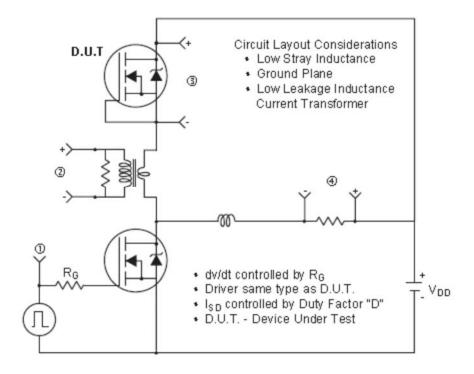
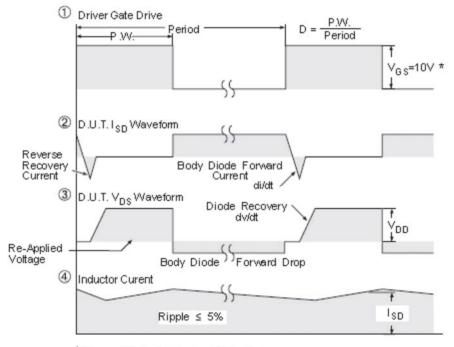


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms







\* VGS = 5V for Logic Level Devices

Figure 4:Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)