
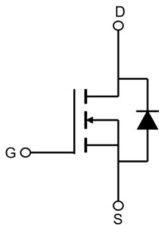


## Description

<b>Features</b> <ul style="list-style-type: none"> <li>● 650V, 9A  <math>R_{DS(ON)} &lt; 1.08\Omega @ V_{GS} = 10V</math></li> <li>● Fast Switching</li> <li>● Improved dv/dt Capability</li> </ul>	<b>Application</b> <ul style="list-style-type: none"> <li>● Load Switch</li> <li>● PWM Application</li> <li>● Power management</li> </ul> <p>100% UIS 100% <math>\Delta V_{ds}</math></p>
 <p>TO-252</p>	 <p>Schematic Diagram</p>

## Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
VSM9N65-T2	VSM9N65	TAPING	TO-252	13inch	2500	25000

## Absolute Maximum Ratings (T<sub>C</sub>=25°C unless otherwise specified)

Symbol	Parameter	Max.	Units
V <sub>DSS</sub>	Drain-Source Voltage	650	V
V <sub>GSS</sub>	Gate-Source Voltage	±30	V
I <sub>D</sub>	Continuous Drain Current	T <sub>C</sub> = 25°C	9
		T <sub>C</sub> = 100°C	5.8
I <sub>DM</sub>	Pulsed Drain Current <sup>note1</sup>	36	A
E <sub>AS</sub>	Single Pulsed Avalanche Energy <sup>note2</sup>	211	mJ
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25°C	31
R <sub>θJC</sub>	Thermal Resistance, Junction to Case	4	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient	62.5	°C/W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C

**Electrical Characteristics** ( $T_J=25^{\circ}\text{C}$  unless otherwise specified)

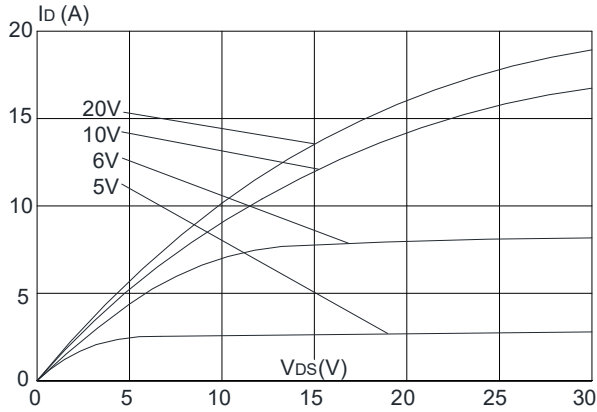
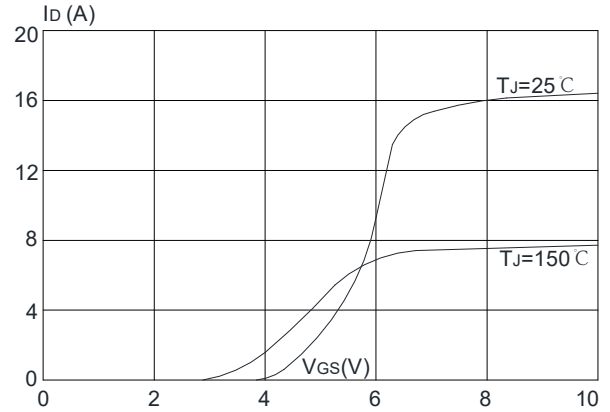
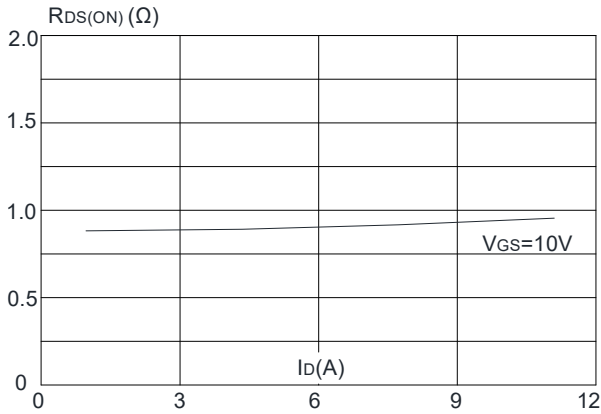
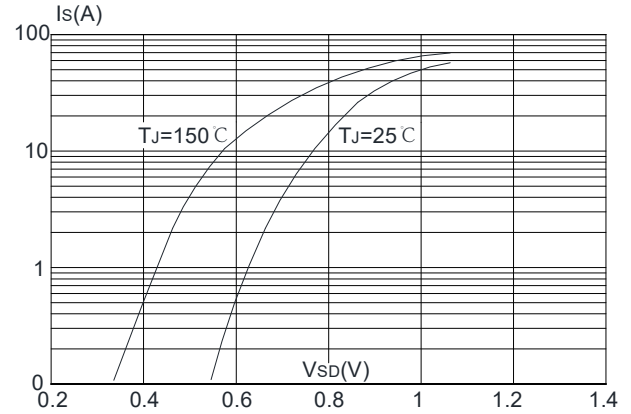
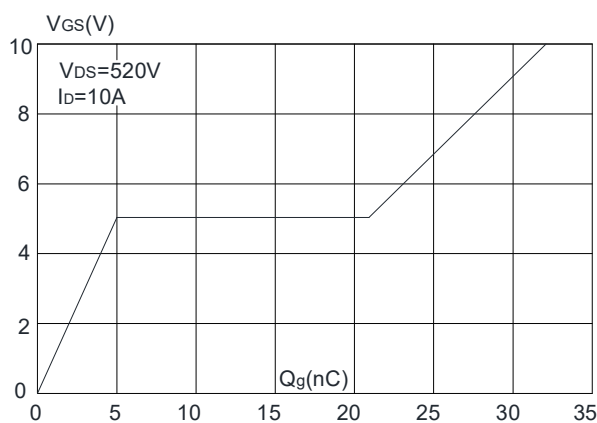
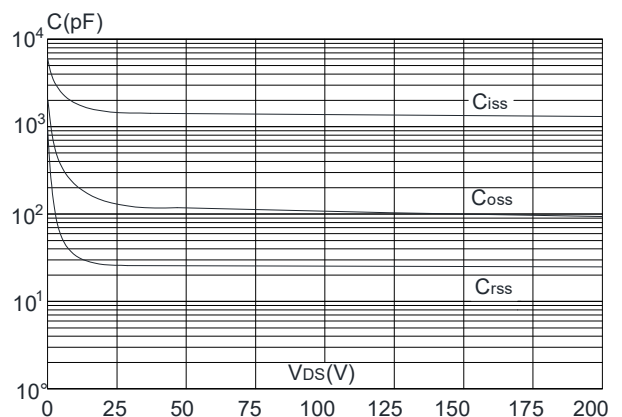
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	650	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =650V, V <sub>GS</sub> =0V, T <sub>J</sub> =25℃	-	-	1	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±30V	-	-	±100	nA
On Characteristics						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2	3	4	V
R <sub>DS(on)</sub>	Static Drain-Source on-Resistance note3	V <sub>GS</sub> =10V, I <sub>D</sub> =4.5A	-	0.9	1.08	Ω
Dynamic Characteristics						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1.0MHz	-	1400	-	pF
C <sub>oss</sub>	Output Capacitance		-	114	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	26	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DD</sub> =520V, I <sub>D</sub> =9A, V <sub>GS</sub> =10V	-	32	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	5	-	nC
Q <sub>gd</sub>	Gate-Drain(“Miller”) Charge		-	16	-	nC
Switching Characteristics						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =325V, I <sub>D</sub> =9A, R <sub>G</sub> =25Ω	-	23	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	15	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time		-	90	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	30	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	9	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	36	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>SD</sub> =9A	-	-	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> =0V, I <sub>S</sub> =9A, di/dt=100A/μs	-	310	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	4.1	-	μC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

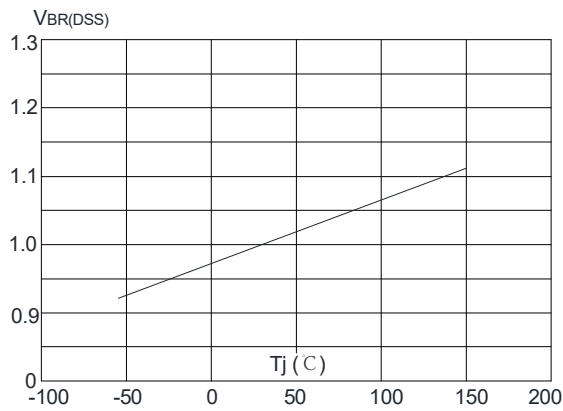
2. EAS condition:  $T_J=25^{\circ}\text{C}$ ,  $V_{DD}=50V$ ,  $V_G=10V$ ,  $L=10mH$ ,  $I_{AS}=6.5A$ 

3. Pulse Test: Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 1\%$

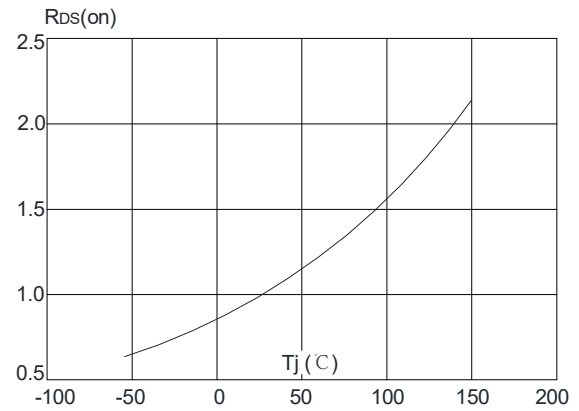
## Typical Performance Characteristics

**Figure1: Output Characteristics**

**Figure 2: Typical Transfer Characteristics**

**Figure 3: On-resistance vs. Drain Current**

**Figure 4: Body Diode Characteristics**

**Figure 5: Gate Charge Characteristics**

**Figure 6: Capacitance Characteristics**


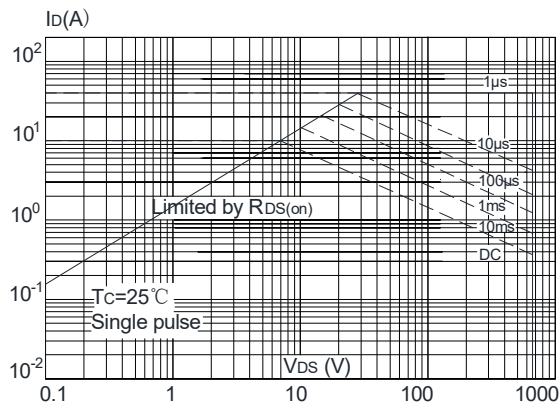
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



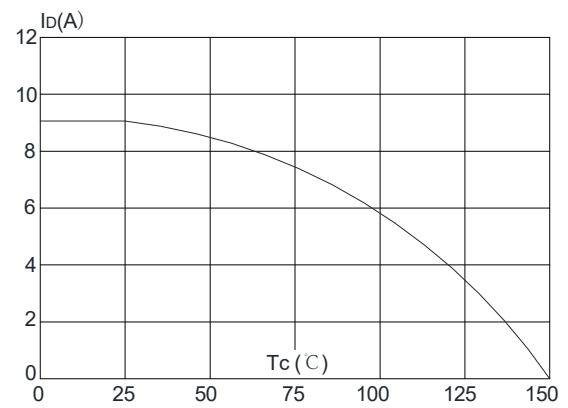
**Figure 8:** Normalized on Resistance vs. Junction Temperature



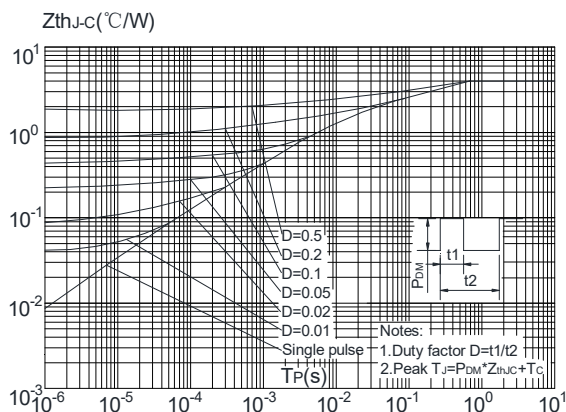
**Figure 9:** Maximum Safe Operating Area



**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature



**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case



## Test Circuit

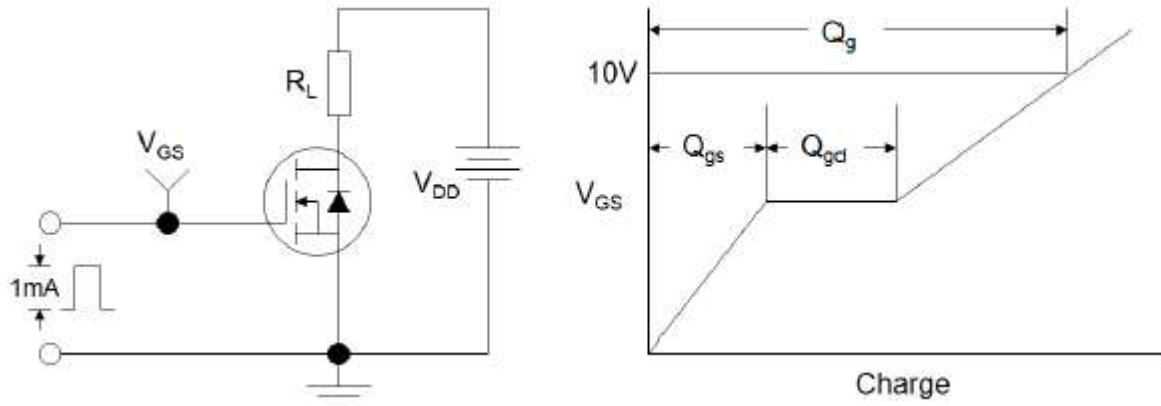


Figure1:Gate Charge Test Circuit & Waveform

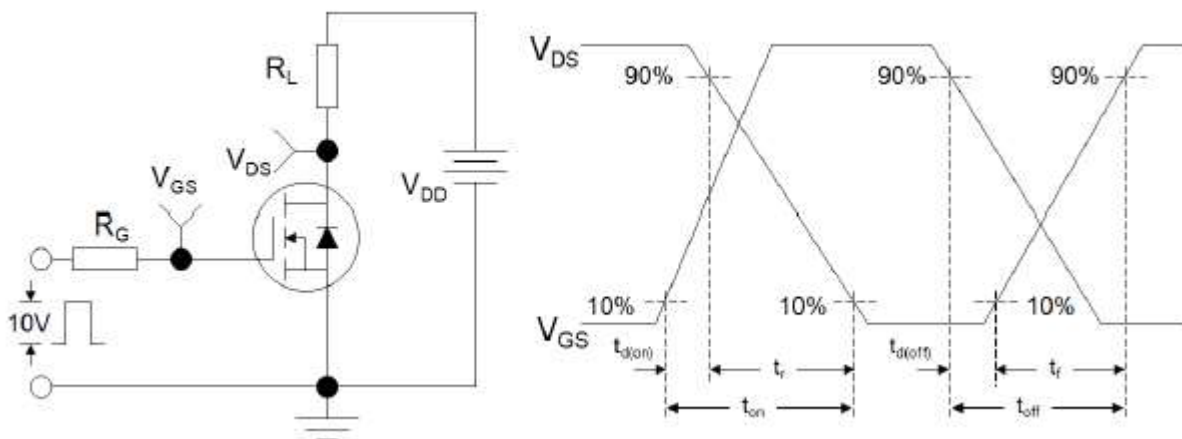


Figure 2: Resistive Switching Test Circuit & Waveforms

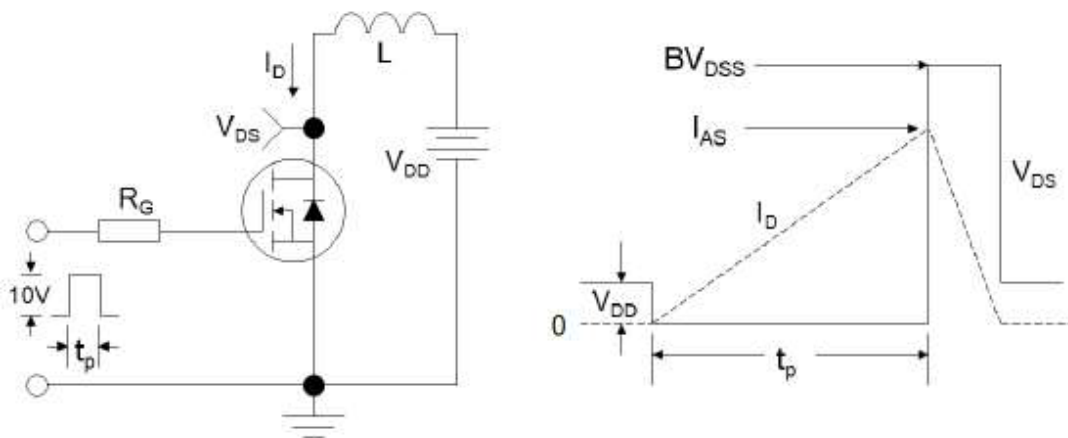


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms