

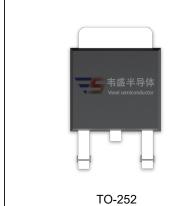
Description

Features

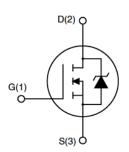
- 600V, 1.3A
- $R_{DS(ON)}$ = 8.5Ω (Typ.) @ V_{GS} = 10V, I_D =0.65A
- Fast Switching
- Improved dv/dt Capability
- 100% Avalanche Tested

Application

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- Power Factor Correction(PFC)







Schematic Diagram

Absolute Maximum Ratings (T_c=25℃ unless otherwise specified)

Symbol	Parameter		Max.	Units
V _{DSS}	Drain-Source Voltage		600	V
V _{GSS}	Gate-Source Voltage		±30	V
I _D	Continuous Drain Current	T _C = 25 °C	1.3	Α
		T _C = 100℃	0.8	Α
I _{DM}	Pulsed Drain Current note1		4	Α
E _{AS}	Single Pulsed Avalanche Energy note2		20	mJ
dv/dt	Peak Diode Recovery Energy		5	V/ns
P _D	Power Dissipation	T _C = 25 °C	45	W
R _{0JC}	Thermal Resistance, Junction to Case		2.8	°C/W
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C

^{*}Drain current limited by maximum junction temperature



Electrical Characteristics (T_C =25 $^{\circ}$ C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units
Off Charac	teristic		•	•	•	•
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V,I _D =250µA	600	-	-	V
$\triangle V_{(BR)DSS}$ $/ \triangle T_J$	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =250µA	-	0.6	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600V, V_{GS} = 0V,$ $T_{J} = 25^{\circ}C$	-	-	1	μA
		V_{DS} =480V, V_{GS} = 0V, T_{J} = 125°C	-	-	10	μΑ
I_{GSS}	Gate to Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 30V$	-	-	±100	nA
On Charac	teristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	2.0	3.0	4.0	V
R _{DS(on)}	Static Drain-Source on-Resistance	V _{GS} =10V, I _D =0.65A	-	8.5	10	Ω
9 FS	Forward Transconductance	V _{DS} =40V, I _D =0.65A	-	0.9	-	S
Dynamic C	Characteristics					
C _{iss}	Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ f = 1.0MHz	105	-	160	pF
C _{oss}	Output Capacitance		18.8	-	28.2	pF
C_{rss}	Reverse Transfer Capacitance		2.8	-	4.5	pF
Q_g	Total Gate Charge	$V_{DS} = 480V, I_{D} = 1A,$ $V_{GS} = 10V$	-	6.1	8	nC
Q_gs	Gate-Source Charge		-	1.3	2	nC
Q_gd	Gate-Drain("Miller") Charge	V _{GS} - 10V	-	3.1	4	nC
Switching	Characteristics					
t _{d(on)}	Turn-on Delay Time		-	10	13	ns
t _r	Turn-on Rise Time	$V_{DS} = 300V, I_{D} = 1A,$	-	10	18	ns
t _{d(off)}	Turn-off Delay Time	$R_G = 25\Omega$	-	20	26	ns
t _f	Turn-off Fall Time		-	11.5	23	ns
Drain-Soul	rce Diode Characteristics and Maxin	num Ratings				
	Maximum Continuous Drain to Source Diode Forward				4	Δ.
I_S	Current		-	-	1	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current			-	4	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _{SD} = 1A	-	0.82	1	V
t _{rr}	Reverse Recovery Time	V _{DS} =100V, I _F =1.3A,	-	114	137	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/µs	-	0.63	0.76	μC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

^{2.} L=60mH,I $_{AS}$ = 1A, V $_{DD}$ = 150V, R $_{G}$ = 10 Ω , starting T $_{J}$ = 25°C

^{3.} Pulse Test: Pulse Width≤300µs, Duty Cycle≤1%



Typical Performance Characteristics

Figure1: Output Characteristics

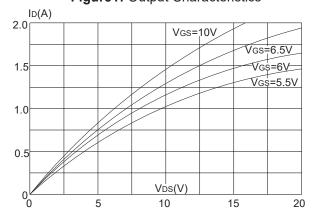


Figure 3: On-resistance vs Drain Current

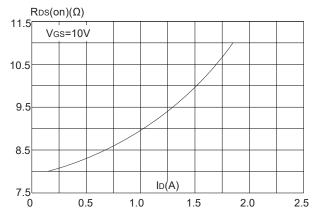


Figure 5: Gate Charge Characteristics

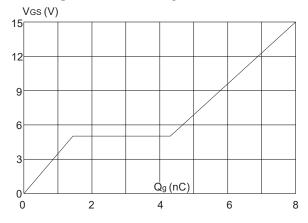


Figure 2: Typical Transfer Characteristics

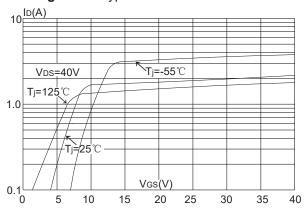


Figure 4: Body-Diode Characteristics

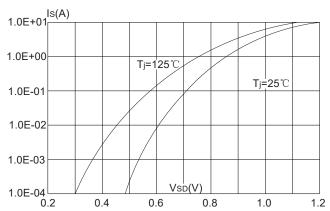


Figure 6: Capacitance Characteristics

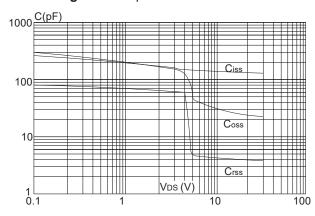




Figure 7: Breakdown Voltage vs Junction Temperature

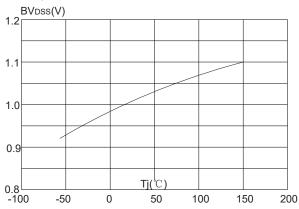


Figure 9: Maximum Safe Operating Area

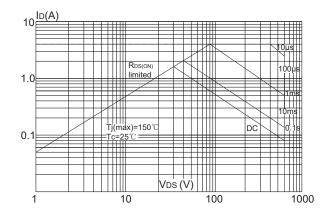


Figure 8: On-Resistance vs Junction Temperature

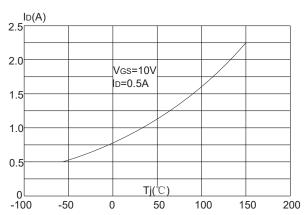


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

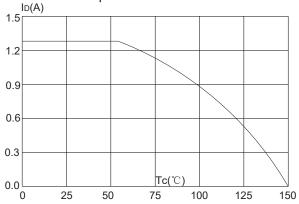
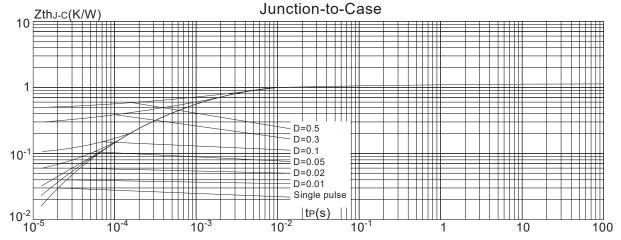


Figure.11: Maximum Effective Transient Thermal Impedance,





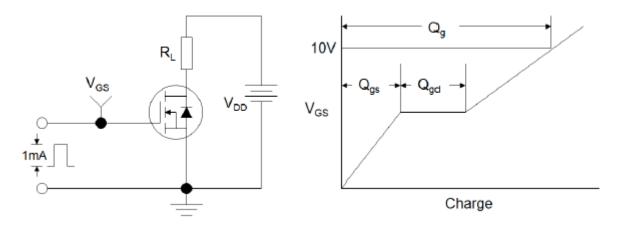


Figure12:Gate Charge Test Circuit & Waveform

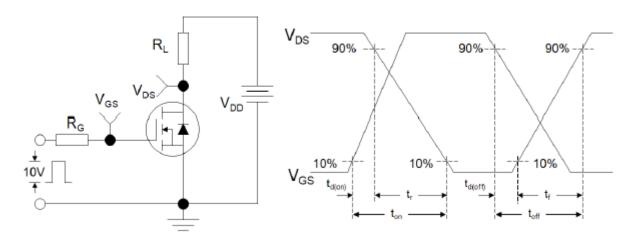


Figure 13: Resistive Switching Test Circuit & Waveforms

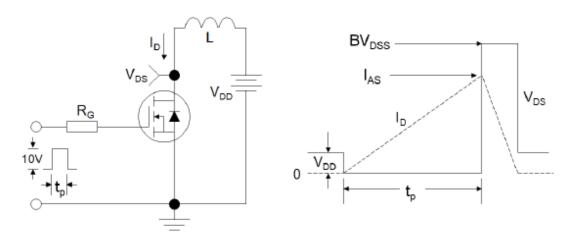
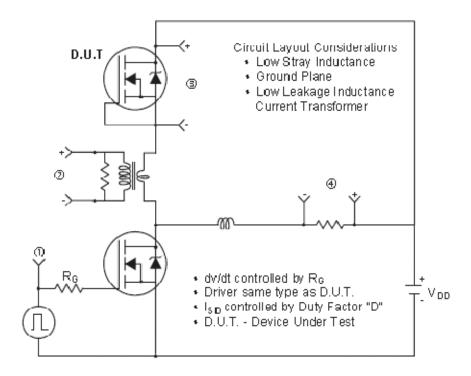
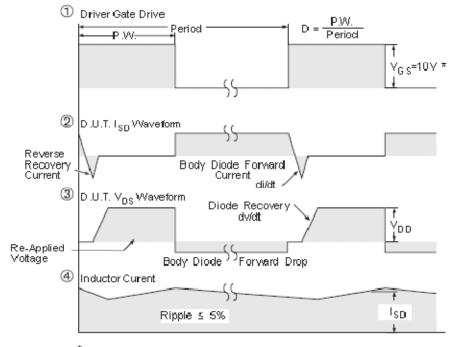


Figure 14:Unclamped Inductive Switching Test Circuit & Waveforms







* V_{GS} = 5V for Logic Level Devices

Figure 15:Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)