

#### **Description**

#### **Features**

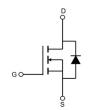
- $V_{DS}$ =600V,  $I_{D}$ =20A  $R_{DS(ON)}$  <0.19Ω @  $V_{GS}$  =10V
- Multi-Epi process SJ-MOSFET
- Smart design in high voltage technology
- Ultra lower on-resistance
- Ultra low gate charge
- Low reverse recovery charge
- Fast switching

#### **Application**

- Power factor correction ( PFC)
- Switched mode power supplies (SMPS)
- Uninterruptible power supply (UPS)

100% UIS 100% ΔVds





Schematic Diagram

# **Package Marking and Ordering Information**

Device Marking	Device	OUTLINE	Device Package	TUBE (PCS)	Inner Box (PCS)	Per Carton (PCS)
VSM20N60-TF	VSM20N60	TUBE	TO-220F	50	1,000	8,000

#### **Absolute Maximum Ratings** (Tc=25°C unless otherwise specified)

Symbol	pol Parameter		Max.	Units	
V <sub>DSS</sub>	Drain-Source Voltage		600	V	
$V_{GSS}$	Gate-Source Voltage		±30	V	
I <sub>D</sub>	Continuous Drain Current	T <sub>C</sub> = 25 °C	20	Α	
		T <sub>C</sub> = 100℃	13		
$I_{DM}$	Pulsed Drain Current note1		80	Α	
E <sub>AS</sub>	Single Pulsed Avalanche Energy note2		238	mJ	
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25 °C	34	W	
$R_{ heta JC}$	Thermal Resistance, Junction to Case		3.67	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		80	°C/W	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	$^{\circ}$	



## **Electrical Characteristics** (Tc=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units		
Off Characteristic								
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V,I <sub>D</sub> =250µA	600	_	_	V		
I <sub>DSS</sub>	Zana Cata Valtana Duain Commant	$V_{DS} = 600V, V_{GS} = 0V,$ $T_{C} = 25^{\circ}C$	-	0.05	1	μA		
	Zero Gate Voltage Drain Current	$V_{DS}$ =600V, $V_{GS}$ = 0V, $T_{C}$ = 125°C	-	-	100	μA		
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 30V$	-	-	±100	nA		
On Charac	teristics							
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS}$ = $V_{GS}$ , $I_D$ =250 $\mu$ A	2.0	-	4.0	V		
R <sub>DS(on)</sub>	Static Drain-Source on-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	-	0.15	0.19	Ω		
Dynamic C	Characteristics							
C <sub>iss</sub>	Input Capacitance	./ 50/// 0//	-	1950	-	pF		
Coss	Output Capacitance	$V_{DS} = 50V, V_{GS} = 0V,$	-	150	-	pF		
Crss	Reverse Transfer Capacitance	f = 1.0MHz	-	5	-	pF		
Qg	Total Gate Charge	\/ -400\/   -204	-	45	70	nC		
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =480V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	-	9	-	nC		
$Q_{gd}$	Gate-Drain("Miller") Charge	VGS - 10 V	ı	18	-	nC		
Switching	Characteristics							
t <sub>d(on)</sub>	Turn-on Delay Time		-	11	-	ns		
t <sub>r</sub>	Turn-on Rise Time	$V_{DS} = 380V, I_{D} = 10A,$	-	6	-	ns		
t <sub>d(off)</sub>	Turn-off Delay Time	$V_{GS}$ =10V, $R_{G}$ =4 $\Omega$	-	61	100	ns		
t <sub>f</sub>	Turn-off Fall Time		-	4.5	12	ns		
Drain-Soul	rce Diode Characteristics and Maxim	um Ratings						
Is	Maximum Continuous Drain to Source Diode Forward Current			-	20	А		
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current			-	80	Α		
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	-	0.9	1.2	V		
trr	Reverse Recovery Time	V <sub>GS</sub> =0V, I <sub>S</sub> =20A,	-	310	-	ns		
Qrr	Reverse Recovery Charge	di/dt=100A/μs	•	5	-	μC		

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

<sup>2.</sup> Ias = 6.9A,  $V_{DD}$  = 50V,  $R_G$  = 25 $\Omega$ , H=10mH, Starting  $T_J$  = 25 $^{\circ}$ C

<sup>3.</sup> Pulse Test: Pulse Width≤300µs, Duty Cycle≤2%



## **Typical Performance Characteristics**

Figure1: Output Characteristics

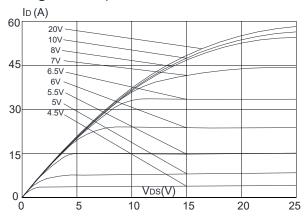


Figure 3:On-resistance vs. Drain Current

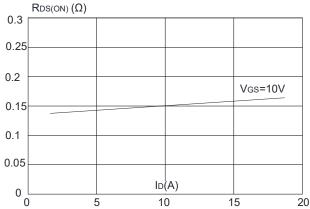


Figure 5: Gate Charge Characteristics

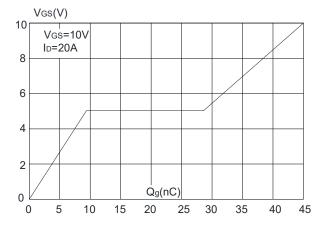


Figure 2: Typical Transfer Characteristics

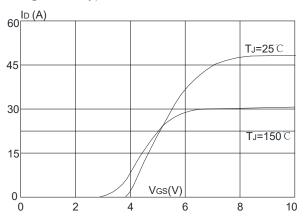


Figure 4: Body Diode Characteristics

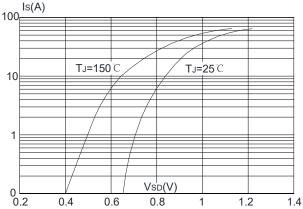
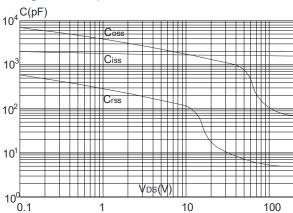


Figure 6: Capacitance Characteristics





**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature

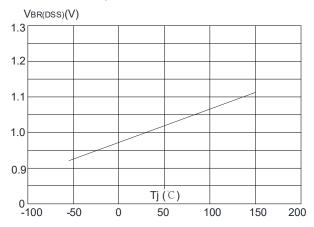
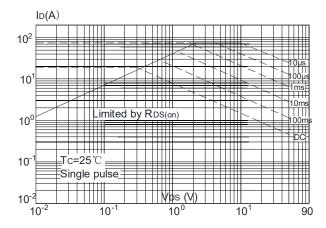
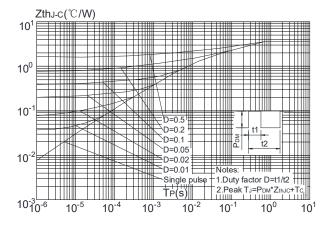


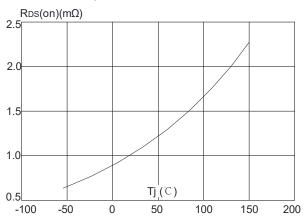
Figure 9: Maximum Safe Operating Area



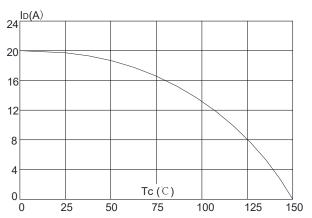
**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case



**Figure 8:** Normalized on Resistance vs. Junction Temperature



**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature





## **Test Circuit**

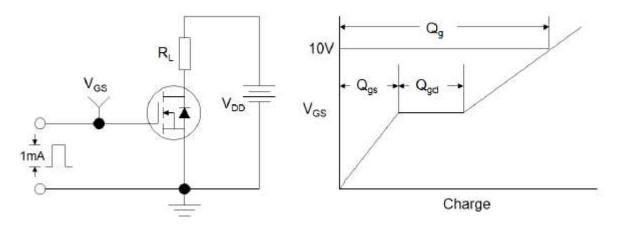


Figure1:Gate Charge Test Circuit & Waveform

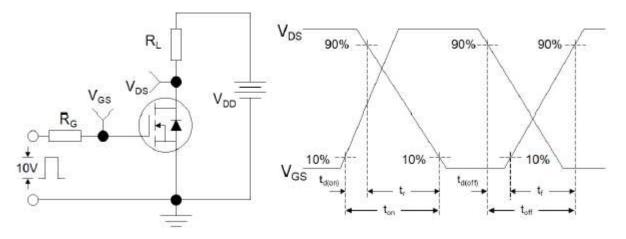


Figure 2: Resistive Switching Test Circuit & Waveforms

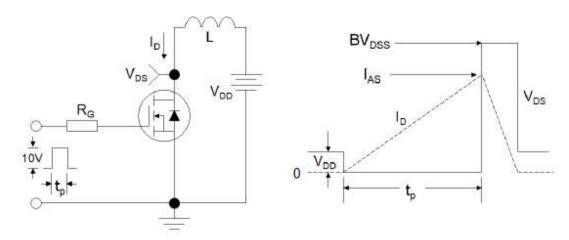


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms