CPU ISA Green Card

Registers

Code	Name	Notes
00	A	General purpose
01	B	General purpose
10	C	General purpose
11	IX	Index register

Memory

- **IMEM:** 16 instructions (PC = 4 bits)
- **DMEM:** 8 bytes, byte-addressable (3-bit address)

Instruction Format

Opcode [15:12]	Clarifier/AddrMode/R2 [11:10]	R(1) [9:8]	Imm8 / Addr / ShiftAmt [7:0]

Addressing Modes

Code	Meaning
00	Immediate (Imm8)
01	Direct (DMEM[addr3])
10	Indirect (DMEM[DMEM[addr3]])
11	Indexed (DMEM[IX+addr3])

Flags

Flag	Meaning
Z	Zero
C	Carry
N	Negative (sign bit)
O	Overflow

Instruction Set

Opcode	Clarifier	Mnemonic	Description	Instruction Format
0000	00	NOOP	Do nothing	NOOP
0000	01	IN	R ← Input	IN R
0000	10	OUT	Output R (ASCII)	OUT R
0000	11	END	Terminate program	END
0001	00	LDM	Load operand into R	LDM R, imm8
0001	01	LDD	Load operand into R	LDD R, addr3
0001	10	LDI	Load operand into R	LDI R, addr3
0001	11	LDX	Load operand into R	LDX R, addr3
0010	00	SWAP	Swap registers	SWAP R1, R2
0010	01	STO	Store R → operand	STO R, imm8
0010	10	STI	Store R → operand	STI R, addr3
0010	11	STX	Store R → operand	STX R, addr3
0011	00–11	ADDM/D/I/X	R ← R + operand	ADDM/D/I/X R, n
0100	00–11	SUBM/D/I/X	R ← R - operand	SUBM/D/I/X R, n
0101	00	INC	R ← R + 1	INC R
0101	01	DEC	R ← R - 1	DEC R
0101	10	LSL	Logical shift left by n	LSL R, shift3
0101	11	LSR	Logical shift right by n	LSR R, shift3
0110	–	ADDR	R1 ← R1 + R2	ADDR R1, R2
0111	–	SUBR	R1 ← R1 - R2	SUBR R1, R2
1000	–	MOV	R1 ← R2	MOV R1, R2
1001	00–11	CMP/D/I/X	Compare, set flags	CMP/D/I/X R, n
1010	00	SWAPR	Swap registers	SWAPR R1, R2
1010	01	JMP	PC ← addr4	JMP addr4
1011	00	JPN	Jump if Z=1	JPN addr4
1011	01	JPE	Jump if Z=0	JPE addr4
1011	10	JGT	Jump if greater (signed)	JGT addr4
1011	11	JGE	Jump if ≥ (signed)	JGE addr4
1100	00–11	ANDM/D/I/X	Bitwise AND	ANDM/D/I/X R, n
1101	00–11	ORM/D/I/X	Bitwise OR	ORM/D/I/X R, n
1110	00–11	XORM/D/I/X	Bitwise XOR	XORM/D/I/X R, n
1111	00	ASL	Arithmetic shift left	ASL R, shift3
1111	01	ASR	Arithmetic shift right	ASR R, shift3
1111	10	CSL	Circular shift left	CSL R, shift3
1111	11	CSR	Circular shift right	CSR R, shift3