ELECTRONIC SWITCHING SYSTEMS
(Elective- I)

OBJECTIVES :

The student will

- Understand the means of measuring traffic.
- Understand the implication of the traffic level on system design.

UNIT -I:

Introduction: Evolution of Telecommunications, Simple Telephone Communication, Basics of Switching System, Manual Switching System, Major Telecommunication Networks.

Crossbar Switching: Principles of Common Control, Touch Tone Dial Telephone, Principles of Crossbar Switching, Crossbar Switch Configurations, Cross point Technology, Crossbar Exchange Organization.

UNIT -II:

Electronic Space Division Switching: Stored Program Control, Centralized SPC: Stand by mode, Synchronous duplex mode, Distributed SPC, Software Architecture, Application Software, Enhanced Services, Two-Stage Networks, Three-Stage Networks, n- Stage Networks.

UNIT -III

Time Division Switching: Basic Time Division Space Switching, Basic Time Division Time Switching, Generalised time division Space switch, Basic Time division time switching: modes of operation, simple problems, Time Multiplexed Space Switching, Time Multiplexed Time division space Switch, Time Multiplexed Time Switching, Combination Switching: Time Space (TS) Switching, Space-time (ST) Switching, Three-Stage Combination Switching, n- Stage Combination Switching.

UNIT IV

Telephone Networks: Subscriber Loop System, Switching Hierarchy and Routing, Transmission Plan, Transmission Systems, Numbering Plan, Charging Plan, Signaling Techniques, In-channel Signaling, Common Channel Signaling, CCITT Signaling System no.6, CCITT Signaling System no.7, **Packet Switching:** Statistical Multiplexing, Local- Area and Wide- Area Networks, Large-scale Networks, Broadband Networks.

UNIT -V:

Switching Networks: Single- Stage Networks, Grading, Link Systems, Grades of service of link systems, Application of Graph Theory to link Systems, Use of Expansion, Call Packing,
Rearrange-able Networks, Strict- Sense non-blocking Networks, Sectionalized Switching Networks

Telecommunications Traffic: The Unit of Traffic, Congestion, Traffic Measurement, A Mathematical Model, Lost-call Systems, Queuing Systems. Problems

UNIT -VI:

Integrated Services Digital Network: Motivation for ISDN, New Services, Network and Protocol Architecture, Transmission Channels, User- Network Interfaces, Signaling, Numbering and Addressing, Service Characterization, Interworking, ISDN Standards, Expert Systems in ISDN, Broadband ISDN, Voice Data Integration.

TEXT BOOKS:

1. Telecommunication Switching Systems and Networks- Thiagarajan Viswanathan, 2000, PHI.
2. Telecommunications Switching, Traffic and Networks- J. E. Flood, 2006, Pearson Education.

REFERENCES:

1. Digital Telephony- J. Bellamy, 2nd Edition, 2001, John Wiley.
2. Data Communications and Networks- Achyut S. Godbole, 2004, TMH.
3. Principles of Communication Ststems- H. Taub & D. Schilling, 2nd Edition, 2003, TMH.
4. Data Communication & Networking- B. A. Forouzan, 3rd Edition, 2004, TMH.
5. Telecommunication System Engineering – Roger L. Freeman, 4th Ed., Wiley-Inter Science,John Wiley & Sons, 2004.

Outcomes

The student will be able to

- Evaluate the time and space parameters of a switched signal
- Establish the digital signal path in time and space, between two terminals
- Evaluate the inherent facilities within the system to test some of the SLIC, CODEC and digital switch functions.
- Investigate the traffic capacity of the system.
- Evaluate methods of collecting traffic data.
- Evaluate the method of interconnecting two separate digital switches.

SYSTEM DESIGN THROUGH VERILOG
(Elective- I)

UNIT-I

INTRODUCTION TO VERILOG:

Verilog as HDL, Levels of design description, concurrency, simulation and synthesis, functional verification, system tasks, programming language interface(PLI), module, simulation and synthesis tools, test benches.

LANGUAGE CONSTRUCTS AND CONVENTIONS:

Introduction, keywords, identifiers, whitespace characters, comments, numbers, strings, logic values, data types, scalars and vectors, parameters, memory, operators, system tasks.

UNIT-II

GATE LEVEL MODELLING:

Introduction, AND gate primitive, module structure, other gate primitives, illustrative examples, tristate gates, array of instances of primitives, design of Flip flops with gate primitives, delays, strengths and contention resolution, net types, design of basic circuits.

UNIT-III

BEHAVIORAL MODELLING:

Introduction, operations and assignments, functional Bifurcation, initial construct, always construct, examples, assignments with delays, wait construct, multiple always blocks, designs at behavioral level, blocking and non-blocking assignments, the case statement, simulation flow, if and if else constructs, assign-De assign construct, repeat construct, FOR loop, the disable construct, While loop, Forever loop, parallel blocks, force-release construct, event.

UNIT-IV

DATAFLOW LEVEL AND SWITCH LEVEL MODELLING:

Introduction, continuous assignment structures, delays and continuous assignments, assignment to vectors, basic transistor switches, CMOS switch, Bidirectional gates and time delays with switch primitives, instantiations with strengths and delays, strength contention with trireg nets.

UNIT-V

SYNTHSIS OF COMBINATIONAL AND SEQUENTIAL LOGIC USING VERILOG: Synthesis of combinational logic: Net list of structured primitives, a set of continuous assignment statements and level sensitive cyclic behavior with examples, Synthesis of priority structures, Exploiting logic don't care conditions. Synthesis of sequential logic with latches: Accidental synthesis of latches and Intentional synthesis of latches, Synthesis of sequential logic with flip-flops, Synthesis of explicit state machines.

UNIT-VI

VERILOG MODELS:

Static RAM Memory, A simplified 486 Bus Model, Interfacing Memory to a Microprocessor Bus, UART Design and Design of Microcontroller CPU.

TEXT BOOKS:

1. Design through Verilog HDL – T.R. Padmanabhan and B. Bala Tripura Sundari, WSE, IEEE Press, 2004.
2. Advanced Digital Design with Verilog HDL – Michael D. Ciletti, PHI, 2005.

REFERENCES:

1. Fundamentals of Logic Design with Verilog – Stephen. Brown and Zvonko Vranesic, TMH, 2005.
2. A Verilog Primier – J. Bhasker, BSP, 2003.

IV Year - I Semester

L	T	P	C
4	0	0	3

EMBEDDED SYSTEMS
ELECTIVE - II

OBJECTIVES:

The main objectives of this course are given below:

- The basic concepts of an embedded system are introduced.
- The various elements of embedded hardware and their design principles are explained.
- Different steps involved in the design and development of firmware for embedded systems is elaborated.
- Internals of Real-Time operating system and the fundamentals of RTOS based embedded firmware design is discussed.
- Fundamental issues in hardware software co-design were presented and explained.
- Familiarise with the different IDEs for firmware development for different family of processors/controllers and embedded operating systems.
- Embedded system implementation and testing tools are introduced and discussed.

Outcomes:

At the end of this course the student can able to:

- Understand the basic concepts of an embedded system and able to know an embedded system design approach to perform a specific function.
- The hardware components required for an embedded system and the design approach of an embedded hardware.
- The various embedded firmware design approaches on embedded environment.
- Understand how to integrate hardware and firmware of an embedded system using real time operating system.

Syllabus

UNIT-I
INTRODUCTION: Embedded system-Definition, history of embedded systems, classification of embedded systems, major application areas of embedded systems, purpose of embedded systems, the typical embedded system-core of the embedded system, Memory, Sensors and Actuators, Communication Interface, Embedded firmware, Characteristics of an embedded system, Quality attributes of embedded systems, Application-specific and Domain-Specific examples of an embedded system.

UNIT-II
EMBEDDED HARDWARE DESIGN: Analog and digital electronic components, I/O types and examples, Serial communication devices, Parallel device ports, Wireless devices, Timer and counting devices, Watchdog timer, Real time clock.

UNIT-III

EMBEDDED FIRMWARE DESIGN: Embedded Firmware design approaches, Embedded Firmware development languages, ISR concept, Interrupt sources, Interrupt servicing mechanism, Multiple interrupts, DMA, Device driver programming, Concepts of C versus Embedded C and Compiler versus Cross-compiler.

UNIT-IV

REAL TIME OPERATING SYSTEM: Operating system basics, Types of operating systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling, Task communication, Task synchronisation, Device Drivers.

HARDWARE SOFTWARE CO-DESIGN: Fundamental Issues in Hardware Software Co-Design, Computational models in embedded design, Hardware software Trade-offs, Integration of Hardware and Firmware, ICE.

UNIT-V

EMBEDDED SYSTEM DEVELOPMENT: The integrated development environment, Types of files generated on cross-compilation, Deassembler/Decompiler, Simulators, Emulators and Debugging, Target hardware debugging, Boundary Scan, Embedded Software development process and tools.

UNIT-VI

EMBEDDED SYSTEM IMPLEMENTATION AND TESTING: The main software utility tool, CAD and the hardware, Translation tools-Pre-processors, Interpreters, Compilers and Linkers, Debugging tools, Quality assurance and testing of the design, Testing on host machine, Simulators, Laboratory Tools.

Text Books:

1. Embedded Systems Architecture- By Tammy Noergaard, Elsevier Publications, 2013.
2. Embedded Systems-By Shibu.K.V-Tata McGraw Hill Education Private Limited, 2013.

References:

1. Embedded System Design, Frank Vahid, Tony Givargis, John Wiley Publications, 2013.
2. Embedded Systems-Lyla B.Das-Pearson Publications, 2013.

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ANALOG IC DESIGN

ELECTIVE - II

OBJECTIVES

The student will be introduced to

- The student will be able to understand the behavior of MOS Devices and Small-Signal & Large-Signal Modeling of MOS Transistor and Analog Sub-Circuits.
- In this course, students can study CMOS Amplifiers like Differential Amplifiers, Cascode Amplifiers, Output Amplifiers, and Operational Amplifiers.
- Another main object of this course is to motivate the graduate students to design and to develop the Analog CMOS Circuits for different Analog operations.
- The concepts of Open-Loop Comparators and Different Types of Oscillators like Ring Oscillator, LC Oscillator etc.

UNIT -I:

MOS Devices and Modeling: The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II:

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III:

CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV:

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT -V:

Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

UNIT -VI:

Oscillators & Phase-Locked Loops: General Considerations, Ring Oscillators, LC Oscillators, Voltage Controlled Oscillators.

Simple PLL, Charge Pump PLLs, Non-Ideal Effects in PLLs, Delay Locked Loops, Applications.

Text Books:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

References:

1. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.
2. Analog Integrated Circuit Design- David A.Johns, Ken Martin, Wiley Student Edn, 2013.

OUTCOMES

After going through this course the student will be able to

- Understand the concepts of MOS Devices and Modeling.
- Design and analyze any Analog Circuits in real time applications.
- Extend the Analog Circuit Design to Different Applications in Real Time.
- Understand of Open-Loop Comparators and Different Types of Oscillators.

NETWORK SECURITY AND CRYPTOGRAPHY
ELECTIVE - II

OBJECTIVES:

- In this course the following principles and practice of cryptography and network security are covered:
- Classical systems, symmetric block ciphers (DES, AES, other contemporary symmetric ciphers)
- Public-key cryptography (RSA, discrete logarithms),
- Algorithms for factoring and discrete logarithms, cryptographic protocols,hash functions, authentication, key management, key exchange, signature schemes,
- Email and web security, viruses, firewalls, digital right management, and other topics.

UNIT- I:

Basic Principles

Security Goals, Cryptographic Attacks, Services and Mechanisms, Mathematics of Cryptography.

UNIT- II:

Symmetric Encryption

Mathematics of Symmetric Key Cryptography, Introduction to Modern Symmetric Key Ciphers, Data Encryption Standard, Advanced Encryption Standard.

UNIT- III:

Asymmetric Encryption

Mathematics of Asymmetric Key Cryptography, Asymmetric Key Cryptography

UNIT- IV:

Data Integrity, Digital Signature Schemes & Key Management

Message Integrity and Message Authentication, Cryptographic Hash Functions, Digital Signature, Key Management.

UNIT -V:

Network Security-I

Security at application layer: PGP and S/MIME, Security at the Transport Layer: SSL and TLS

UNIT -VI:

Network Security-II

Security at the Network Layer: IPSec, System Security

OUTCOMES:

- To be familiarity with information security awareness and a clear understanding of its importance.
- To master fundamentals of secret and public cryptography
- To master protocols for security services
- To be familiar with network security threats and countermeasures
- To be familiar with network security designs using available secure solutions (such asPGP,
- SSL, IPSec, etc)

TEXT BOOKS:

1. Cryptography and Network Security, Behrouz A Forouzan, DebdeepMukhopadhyay, (3e) Mc Graw Hill.
2. Cryptography and Network Security, William Stallings, (6e) Pearson.
3. Everyday Cryptography, Keith M.Martin, Oxford.

REFERENCE BOOKS:

1. Network Security and Cryptography, Bernard Meneges, Cengage Learning.

IV Year - I Semester

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MICROWAVE ENGINEERING & OPTICAL LAB

Minimum Twelve Experiments to be conducted:
Part – A (Any 7 Experiments (8 & 9 compulsory)) :
1. Reflex Klystron Characteristics.
2. Gunn Diode Characteristics.
3. Attenuation Measurement.
4. Directional Coupler Characteristics.
5. Impedance and Frequency Measurement.
6. Scattering parameters of Circulator.
7. Scattering parameters of Magic Tee.
8. Radiation Pattern of Horn and Parabolic Antennas.
9. Synthesis of Microstip antennas (Rectangular Structure) Using HFSS.

Part – B (Any 5 Experiments) :
10. Characterization of LED.
11. Characterization of Laser Diode.
12. Intensity modulation of Laser output through an optical fiber.
13. Measurement of Data rate for Digital Optical link.
14. Measurement of NA.
15. Measurement of losses for Analog Optical link.

Equipment required for Laboratories:
1. Regulated Klystron Power Supply, Klystron mount
2. VSWR Meter
3. Micro Ammeter
4. Multi meter
5. CRO
6. GUNN Power Supply, Pin Modulator
7. Crystal Diode detector
8. Micro wave components (Attenuation)
9. Frequency Meter
10. Slotted line carriage
11. Probe detector
12. Wave guide shorts
13. SS Tuner
14. Directional Coupler
15. E, H, Magic Tees
16. Circulators, Isolator
17. Matched Loads
18. Pyramidal Horn and Parabolic Antennas
19. Turntable for Antenna Measurements
20. HFSS Software
21. Fiber Optic Analog Trainer based LED
22. Fiber Optic Analog Trainer based laser
23. Fiber Optic Digital Trainer
24. Fiber cables - (Plastic, Glass)

IV Year - I Semester

L	T	P	C
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DIGITAL SIGNAL PROCESSING LABORATORY

List of the Experiments / programs

To Student has to perform at least FOUR Experiments in each part

PART-1(SIGNALS)

1) Generation of discrete time signals for discrete signals
2) To verify the Linear Convolution
   a) Using MATLAB
   b) Using Code Composer Studio(CCS)
3) To verify the Circular Convolution for discrete signals
   a) Using MATLAB
   b) Using Code Composer Studio(CCS)
4) To Find the addition of Sinusoidal Signals
5) To verify Discrete Fourier Transform(DFT) and Inverse Discrete Fourier Transform(IDFT)
   a) Using MATLAB
   b) Using Code Composer Studio(CCS)
6) Transfer Function Stability Analysis: using pole-zero plot, bode plot, Nyquist plot, z-plane plot.

PART-2 (FILTERS)

7) Frequency Response of IIR low pass Butterworth Filter
8) Frequency Response of IIR high pass Butterworth Filter
9) Frequency Response of IIR low pass Chebyshev Filter
10) Frequency Response of IIR high pass Chebyshev Filter
11) Frequency Response of FIR low pass Filter using Rectangle Window
12) Frequency Response of FIR low pass Filter using Triangle Window

PART – 3(IMAGE PROCESSING)

13) An image processing in a false contouring system
14) To generate the histogram equalization to the image
15) To verify the Normalized Cross Correlation to the addition of noise and removal of noise using filters to an image.
16) Compute the edge of an image using spatial filters.
17) Perform the image motion blur and calculate PSNR to the noise image and also noise free image.
18) To verify the PSNR to the Second order Decomposition of Discrete Wavelet transforms and to the reconstructed image using inverse Discrete Wavelet transform