ELectronics**E**ngineering **S**tudents' Association**(ELESA)**

Presents

ELECTROVERT 2018

The Performers' creed

Name of the Event**: Age of µ Tron**
Candidate's Code:

Date:8th sept 2018
Time:

Instructions

- All questions are compulsory and carries equal amount of marks.
- Use of calculators is allowed.
- Use of mobile is strictly prohibited.

1.The internal RAM memory of the 8051 is:
a.32 bytes b. 64 bytes
c. 128 bytes d. 256 bytes

2. When the microcontroller executes some arithmetic operations, then the flag bits of which register are affected?
a. PSW b. SP
c. DPTR d. PC

3. Which general purpose register holds eight-bit divisor and store the remainder especially after the execution of division operation?
a. A-Register
b. B-Register
c. Registers R0 through R7
d. All of the above

4. The 8051 can handle _____interrupt sources including reset.
a. 3 b. 4
c. 5 d. 6

5. Which operations are performed by stack pointer during its incremental phase?
a. Push b. Pop
c. Return d. All of the above

6. The I/O ports that are used as address and data for external memory are:
a. ports 1 and 2 b. ports 1 and 3
c. ports 0 and 2 d. ports 0 and 3

7. Which register bank is supposed to get selected if the values of register bank select bits RS1 & RS0 are detected to be '1' & '0' respectively?
a. Bank 0 b. Bank 1
c. Bank 2 d. Bank 3

8. Which of the following instructions will load the value 35H into the high byte of timer 0?
a. mov th0, #35h
b. mov th0, 35h
c. mov t0, #35h
d. mov t0, 35h

9. What happens when the pins of port 0 & port 2 are switched to internal ADDR and ADDR / DATA bus respectively while accessing an external memory?
a. Pots cannot be used as general-purpose Inputs/Outputs
b. Ports start sinking more current than sourcing
c. Ports cannot be further used as high impedance input
d. All of the above

10.The contents of the accumulator after this operation will be
MOV A, #0BH

ANL A, #2CH

a. 11010111 b. 11011010
c. 00001000 d. 00101000

11. What kind of instructions usually affect the program counter?

a. Call & Jump b. Call & Return
c. Push & Pop d. Return & Jump

12. Why are the resonators not preferred for an oscillator circuit of 8051?

a. Because they do not avail for 12 MHz higher order frequencies
b. Because they are unstable as compared to quartz crystals
c. Because cost reduction due to its utility is almost negligible in comparison to total cost of microcontroller board
d. All of the above

13. Which among the below stated registers does not belong to the category of special function registers?

a. TCON & TMOD b. TH0 & TL0
c. P0 & P1 d. SP & PC

14. Which location specify the storage/loading of vector address during the interrupt generation?

a. Stack Pointer b. Program Counter
c. Data Pointer d. All of the above

15. Which of the following commands will move the number 27H into the accumulator?

a. MOV A, P27 b. MOV A, #27H
c. MOV A, 27H d. MOV A, @27

16. What is the maximum delay generated by the 12 MHz clock frequency in accordance to an auto-reload mode (Mode 2) operation of the timer?

a. 125 µ s b. 250 µ s
c. 256 µ s d. 1200 µ s

17. Why is the speed accessibility of external data memory slower than internal on-chip RAM?

a. Due to multiplexing of lower order byte of address-data bus
b. Due to multiplexing of higher order byte of address-data bus
c. Due to demultiplexing of lower order byte of address-data bus
d. Due to demultiplexing of higher order byte of address-data bus

18. Which commands are used for addressing the off-chip data and associated codes respectively by data pointer?

a. MOVX & MOVC b. MOVY & MOVB
c. MOVZ & MOVA d. MOVC & MOVY

19. Where should the pin 19 (XTAL1), acting as an input of inverting amplifier as well as part of an oscillator circuit, be connected under the application of external clock?

a. to XTAL2 b. to Vcc
c. to GND d. to ALE

20. Match the following:

A. ISS - 1. Monitors the status of int pin
B. IER - 2. Allows the termination of ISS
C. RETI -3. MCS-51 Interrupts Initialization
D. INTO - 4. Occurrence of high to low transition level

a. A-1, B-2, C-3, D-4
b. A-3, B-2, C-4, D-1
c. A-1, B-3, C-2, D-4
d. A-4, B-3, C-2, D-1

21. Which data memory controls and handles the operation of several peripherals

by assigning them in the category of special function registers?

a. Internal on-chip RAM
b. External off-chip RAM
c. Both a & b
d. None of the above

22. The contents of the accumulator after this operation
MOV A,#2BH
ORL A,00H
will be:
a. 1b h b. 2b h
c. 3b h d. 4b h

23.What is the disadvantage of a level triggered pulse?
a. a constant pulse is to be maintained for a greater span of time
b. difficult to analyse its effects
c. it is difficult to produce
d. another interrupt may be caused, if the signal is still low before the completion of the last instruction

24. Baud rate is the reverse of the
a. baud time b. baud period
c. bit time d. bit period

25.In SAR ADC based conversions, each bit typically requires one clock cycle (sometimes two) to make a comparison and set up the new voltage.
a. true c. can't be said
b. false d. depends on the conditions

26.Usually a capacitor is inserted between an analog input and the ground because
a. it blocks the analog voltage
b. it suppresses the noise
c. it increases the gain
d. none of the mentioned

27. Device pins XTAL1 and XTAL2 for the 8051 are used for connections to an external oscillator or crystal.

a. True b. False

28. Identify the row and the column for the following case when for the row D3-D0= 1110 and for the column D3-D0= 1101
a. first row and second column
b. first row and third column
c. second row and first column
d. second row and second column

29.To latch in information at the data pins of the LCD, we send
a. H-L pulse at the E pin
b. L-H pulse at the E pin
c. A constant H pulse at the E pin
d. A constant L pulse at the E pin

30.What is the address of the second column and the second row of the 16*2 LCD?
a. 0xc2 b. 0x81
c. 0xc0 d. 0xc1

31.Which architecture is followed by general purpose microprocessors?
a. Harvard architecture
b. Von Neumann architecture
c. None of the mentioned
d. All of the mentioned

32. What is the file extension that is loaded in a micro controller for executing any instruction?
a) .doc b) .c
c) .txt d) .hex

33. Why are ULN2803 normally used between the micro controllers and the relays?
a) for switching purposes
b) for increasing the current capability required by a relay

c) for increasing the voltage capability required by a relay
d) all of the mentioned

34. Why are opto isolators normally used between the micro controllers and the ULN2803?
a) to optimise the current
b) to reduce the back emf
c) to increase the current
d) to increase the voltage

35.CJNE instruction makes
a) the pointer to jump if the values of the destination and the source address are equal
b) sets CY=1, if the contents of destination register are greater than that of the source register
c) sets CY=0, if the contents of destination register is smaller then that of the source register
d) none of the mentioned

36. A pull-up or pull-down resistor
a) removes the full output drive on the output pin
b) gives only a feeble current through the pull-up to resistor
c) both of the mentioned
d) none of the mentioned

37.input DAC has
a) 8 discrete voltage levels
b) 64 discrete voltage levels
c) 124 discrete voltage levels
d) 256 discrete voltage levels

38. How many bytes of bit addressable memory is present in 8051 based micro controllers?
a. 8 bytes b. 32 bytes
c. 16 bytes d. 128 bytes

39. Data transfer from I/O to external data memory can only be done with the MOVX command.

a. True b. False

40. Serial port interrupt is generated, if ____ bits are set
a) IE b) RI, IE
c) IP, TI d) RI, TI

41.What is the difference between UART and USART communication?
a) they are the names of the same particular thing, just the difference of A and S is there in it
b) one uses asynchronous means of communication and the other uses synchronous means of communication
c) one uses asynchronous means of communication and the other uses asynchronous and synchronous means of communication
d) one uses angular means of the communication and the other uses linear means of communication

42. Which of the following is the logic level understood by the micro-controller/micro-processor?
a. TTL logic level b. RS232 logic level
c. None of the above d. Both of the above

43.Why are solid relays advantageous over electromagnetic relays?
a) they need zero voltage circuit
b) they need less current to be energised
c) they need less voltage to be energised
d) none of the mentioned

44. How many rows and columns are present in a 16*2 alphanumeric LCD?
a) rows=2, columns=32
b) rows=16, columns=2
c) rows=16, columns=16
d) rows=2, columns=16