ELectronics **E**ngineering **S**tudents' **A**ssociation **(ELESA)**

Presents

ELESA Placement Cell (EPC)

Assessment test

Name of the Candidate : Mail ID:	Section (No of Questions): Duration: 35 mins

1. Which of the following is not the feature of modern control system?
   a) Quick response
   b) Accuracy
   c) Correct power level
   d) No oscillation

2. The output of the feedback control system must be a function of:
   a) Reference input
   b) Reference output
   c) Output and feedback signal
   d) Input and feedback signal

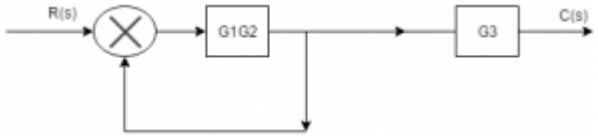
3. The principle of homogeneity and superposition are applied to:
   a) Linear time invariant systems
   b) Nonlinear time invariant systems
   c) Linear time variant systems
   d) Nonlinear time invariant systems

4. A linear system at rest is subject to an input signal $r(t)=1-e^{-t}$. The response of the system for $t>0$ is given by $c(t)=1-e^{-2t}$. The transfer function of the system is:
   a) (s+2)/(s+1)
   b) (s+1)/(s+2)
   c) 2(s+1)/(s+2)
   d) (s+1)/2(s+2)

5. In regenerating the feedback, the transfer function is given by
   a) C(s)/R(s)=G(s)/1+G(s)H(s)
   b) C(s)/R(s)=G(s)H(s)/1-G(s)H(s)

c) C(s)/R(s)=G(s)/1+G(s)H(s)
d) C(s)/R(s)=G(s)/1-G(s)H(s)

6. For the block diagram given in the following figure, the expression of C/R is:



a) G1G2G3/1-G2G1
b) G1G2/1-G1G2G3
c) G1G2G3/1-G1G2G3
d) G1G2/G3(1-G1G2)

7. The overall transfer function of two blocks in parallel are :
a) Sum of individual gain
b) Product of individual gain
c) Difference of individual gain
d) Division of individual gain

8. Transfer function of the system is defined as the ratio of Laplace output to Laplace input considering initial conditions_____
a) 1
b) 2
c) 0
d) infinite

9. Oscillations in output response is due to :
a) Positive feedback
b) Negative feedback
c) No feedback
d) None of the mentioned

10. Signal flow graphs are reliable to find transfer function than block diagram reduction technique.
a) True
b) False

11. The collector of a transistor is ……. doped

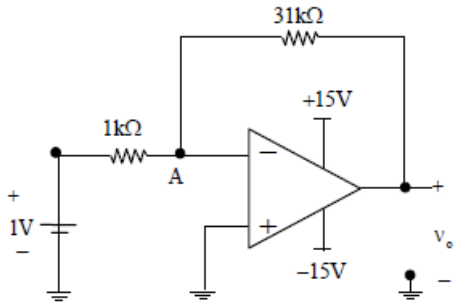
a) heavily
b) moderately
c) lightly

d) none of the above

12. The value of α of a transistor is …….

a) more than 1
b) less than 1
c) 1
d) none of the above

13. An op-amp based circuit is implemented as shown below.



In the above circuit, assume the op-amp to be ideal. The voltage (in volts, correct to one decimal place) at node A, connected to the negative input of the op-amp as indicated in the figure is____.

a) 15
b) -15
c) 0.5
d) -0.5

14. The input impedance of a transistor connected in …….. arrangement is the highest

a) common emitter
b) common collector
c) common base
d) none of the above

15. A JFET has ……. power gain

a) small
b) very high
c) very small
d) none of the above

16. The use of negative feedback ……

a) reduces the voltage gain of an Op-amp
b) makes the Op-amp oscillate
c) makes linear operation possible

d) answers (1) and (2)

17. If A_{DM} = 3500 and A_{CM} = 0.35, the CMRR is …….

a) 1225
b) 10,000
c) 80 dB
d) answers (1) and (3)

18. The Op-amp can amplify

a) a.c. signals only
b) d.c. signals only
c) both a.c. and d.c. signals
d) neither d.c. nor a.c. signals

19. The input stage of an Op-amp is usually a …….

a) differential amplifier
b) class B push-pull amplifier
c) CE amplifier
d) swamped amplifier

20. Current cannot flow to ground through ……

a) a mechanical ground
b) an a.c. ground
c) a virtual ground
d) an ordinary ground.

21. In a 4-stage ripple counter, the propagation delay of a flip flop is 30 ns. If the pulse width of the strobe is 30 ns, the maximum frequency at which the counter operates reliably is nearly

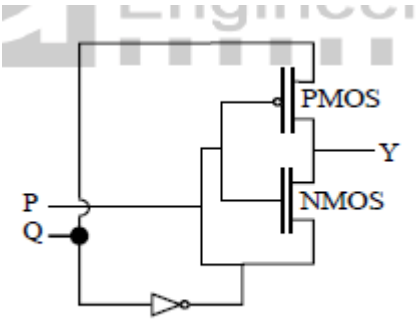
(a) 9.7 MHz (b) 8.4 MH (c) 6.7 MHz (d) 4.4 MHz

22. A product-of-sums (POS) expression leads to what kind of logic circuit?

(a) OR-AND circuit (b) NOR-NOR circuit (c) AND-OR-INVERT circuit (d) NAND-NAND

23. In a master slave JK flip-flop
(a) both master and slave are positive edge triggered
(b) both master and slave are negative edge triggered
(c) master is positive edge triggered and slave is negative edge triggered
(d) master is negative edge triggered and slave is positive edge triggered

24. For the circuit shown in the figure, P and Q are the inputs and Y is the output.



The logic implemented by the circuit is

(A) XNOR (B) XOR (C) NOR (D) OR

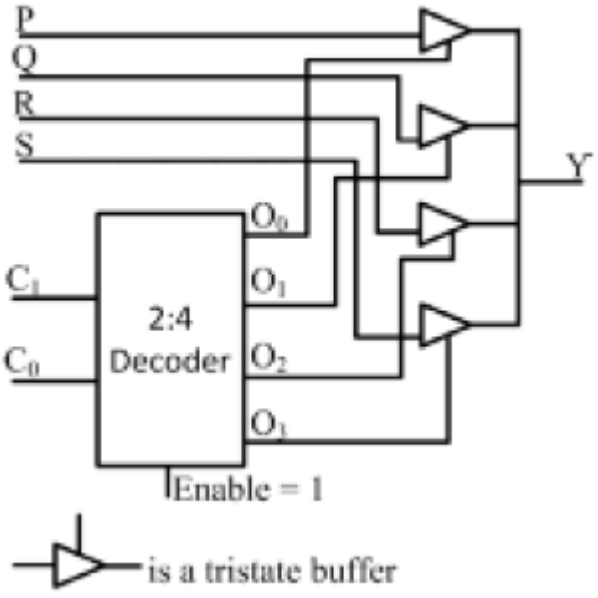
25. In a DRAM,
(A) periodic refreshing is not required
(B) information is stored in a capacitor
(C) information is stored in a latch
(D) both read and write operations can be performed simultaneously

26. A good transimpedance amplifier has
(A) low input impedance and high output impedance
(B) high input impedance and high output impedance
(C) high input impedance and low output impedance
(D) low input impedance and low output impedance

27. Red (R), Green (G) and Blue (B) Light Emitting Diodes (LEDs) were fabricated using p-n junctions of three different inorganic semiconductors having different band-gaps. The built-in voltage of red, green and blue diodes are respectively. Assume donor and acceptor doping to be the same (NA and ND, respectively) in the p and n sides of all the three diodes. Which one of the following relationships about the built-in voltages in TRUE? R G B V , V and V

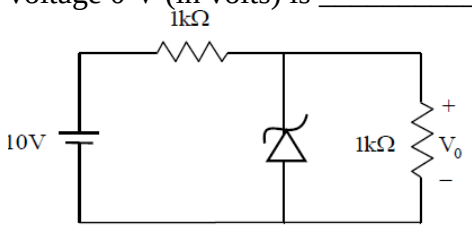
A) Vr > Vg> Vb B) Vr < Vg < Vb C) Vr = Vg = Vb D) Vr > Vg < Vb

28. The functionality implemented by the circuit below is

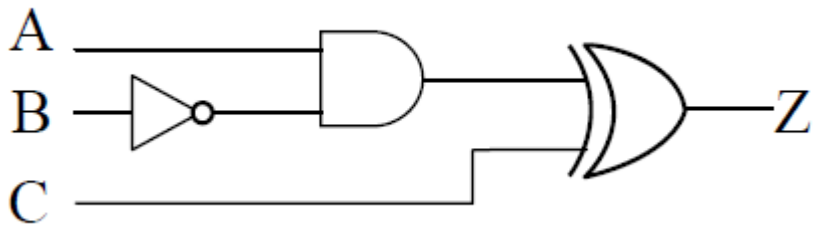


(A) 2-to-1 multiplexer (B) 4-to-1 multiplexer (C) 7-to-1 multiplexer (D) 6-to-1 multiplexer

29. In the circuit shown below, the Zener diode is ideal and the Zener voltage is 6V. The output voltage 0 V (in volts) is _____.



30. All the logic gates shown in the figure have a propagation delay of 20 ns. Let A=C=0 and B=1 until time t=0. At t= 0, all the inputs flip (i.e., A = C = 1 and B = 0) and remain in that state. For t > 0, output Z = 1 for a duration (in ns) of.



A) 20 B) 40 C) 60 D) infinity