

# **Progress Presentation-I**

## **e-Yantra Summer Internship-2019**

### **Robot Designing using FPGA**

#### **Interns:**

Vishal Narkhede  
Karthik K Bhat

#### **Mentors:**

Simranjeet Singh  
Lohit Penubaku

IIT Bombay

June 14, 2019

# Overview of Project

Progress  
Presentation-I

Interns:  
Vishal Narkhede  
Karthik K Bhat

Mentors:  
Simranjeet Singh  
Lohit Penubaku

Overview of  
Project

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DE0-Nano Board

Robot Block  
Diagram

Tasks  
Accomplished

RTL Design

RTL Design

Resource  
Utilization

Tasks Remaining

Challenges Faced

- Project Name:  
Robot Designing using Field Programmable Gate Array (FPGA)
- Objective:  
To interface the basic building blocks of robot with FPGA, that performs simple robotic functions like line following.
- Deliverables:
  - Display the line sensor readings on the LCD
  - A robot that is able to follow black line
  - Interface camera with FPGA

# Overview of Tasks

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Challenges Faced

#	Task	Deadline
1	Understand the DE0-Nano board and NIOS Processor in the FPGA	5 days
2	Interface an analog sensor with FPGA	3 days
3	Interface 16x2 LCD with FPGA	3 days
4	Combine the display and analog sensors	2 days
5	Interface motor driver and motor encoders	3 days
6	Design a power management circuit	1 day
7	Combine all the building blocks together	2 days
8	Line following code, testing and debugging	4 days
9	Interface camera with the FPGA	3 days
10	Develop the robot using NIOS processor	5 days
11	Compare the performances	3 days
12	Documentation and creating user manual	3 days

# DEO-Nano Board Features

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Challenges Faced

- 22,320 Logic Elements
- 32 MB SDRAM
- 2Kb I2C EEPROM
- 64 Mb Serial configuration memory device
- 153 Input/Output Ports
- 8 channel 12-bit ADC (ADC128S022)  
Sampling rate: 50 Ksps to 200 Ksps
- 13 bit, 3-axis Accelerometer (ADXL345)

# Robot Block Diagram

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Challenges Faced

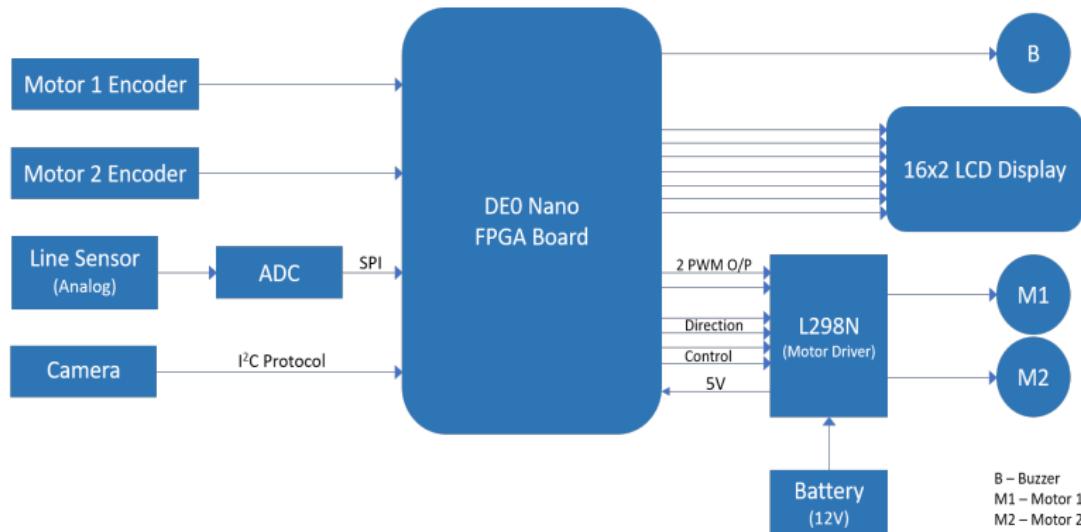


Figure: Block diagram of the robot

# Tasks Accomplished

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Challenges Faced

#	Tasks	Remarks
1	Understand the given board	Referred the datasheets and videos for better understanding
2	Interfacing analog sensors	Support for Analog to Digital Converters (SPI Communication)
3	Interfacing 16x2 LCD	Used 4-bit datalines with time constraints as per datasheet
4	Analog sensor readings on LCD	Used the Firebird's Line sensor. <b>Hardware testing yet to be done.</b>
5	Motor Control	Interfacing motor driver, quadrature encoder and PWM generation. <b>Hardware testing yet to be done.</b>
6	Analysis of Power Consumption	Total power consumption and runtime of the robot

# RTL Design - ADC Interface

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Challenges Faced

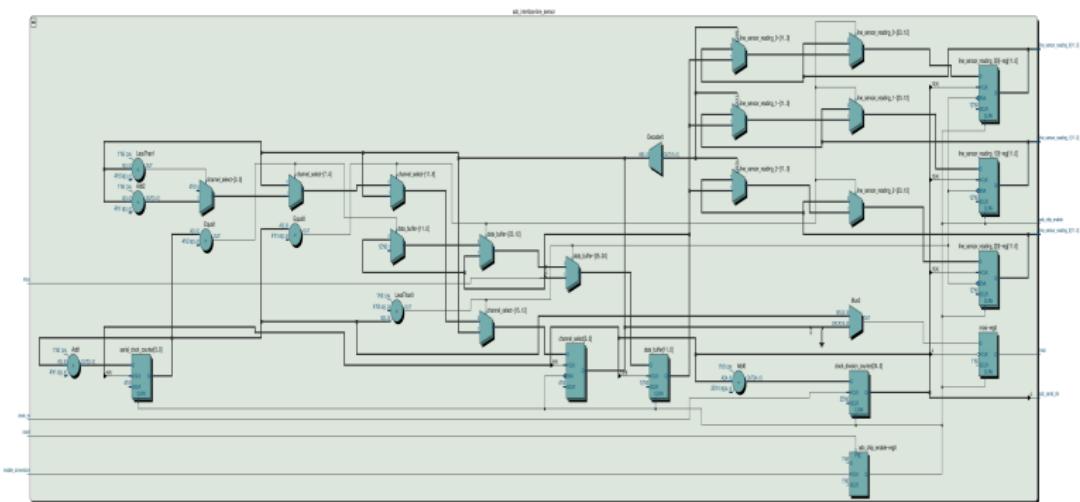


Figure: RTL Design of Analog to Digital Converter interface

# RTL Design - LCD & ADC Interface

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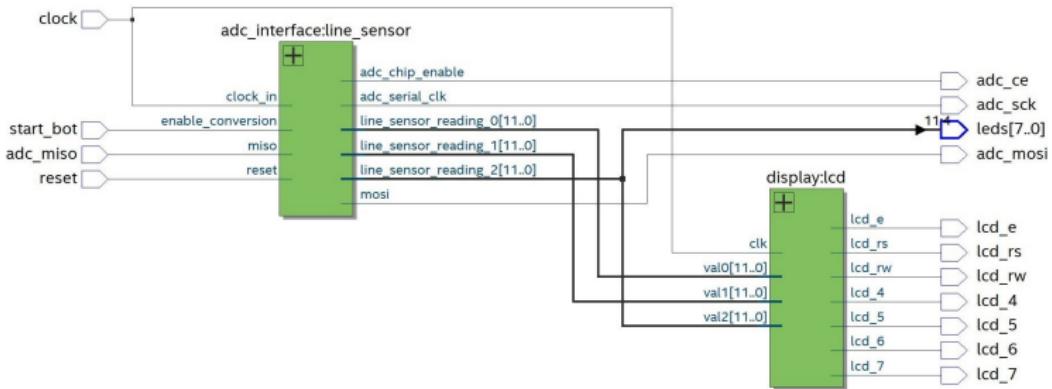


Figure: RTL Design of LCD & ADC Interface

# Resource Utilization

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Challenges Faced

- Logic elements: 1,678/22,320
- Registers: 99
  - ADC Interface: 61
  - LCD Interface: 38
- Look-up Tables: 1634
  - ADC Interface: 32
  - LCD Interface: 1602
- I/O Pins: 22/153

# Tasks Remaining

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Challenges Faced

#	Tasks	Remarks
1	Combining all building blocks	Building the robot with compact structure and precise power management
2	Line Following Algorithm	Novel left-hand rule approach
3	Camera on FPGA	Using I <sup>2</sup> C Protocol
4	Realizing robot using NIOS processor	For performance comparison with FPGA
5	Compare the performances	Need to find the evaluation parameter
6	Documentation	With user manual

# Challenges Faced

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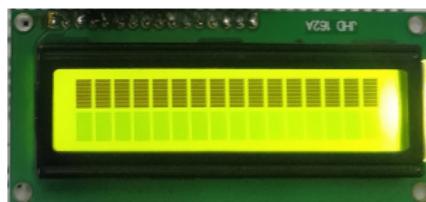
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Challenges Faced

- Difficulty in interfacing the LCD with 8-bit datalines.
- Timing constraint in sending commands and data to LCD.



(a) LCD initialization error



(b) LCD Working with 4  
datalines

# Future Plans

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Future Plans

- A Line Following Robot using FPGA
- Camera interfaced with the FPGA on the robot
- Develop the robot with NIOS Processor in the FPGA

# Thank You

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Feedback

# Thank You!

Any Queries