

# Progress Presentation-I

## e-Yantra Summer Internship-2019

### Robot Designing using FPGA

#### **Interns:**

Vishal Narkhede

Karthik K Bhat

#### **Mentors:**

Simranjeet Singh

Lohit Penubaku

IIT Bombay

June 28, 2019

# Overview of Project

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Interns:  
Vishal Narkhede  
Karthik K Bhat

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## Overview of Project

## Overview of Tasks

## Tasks Remaining

## Design Block Diagram

## Challenges Faced

## Thank You

- **Project Name:**  
Robot Designing using Field Programmable Gate Array (FPGA)
- **Objective:**  
To interface the basic building blocks of robot with FPGA, that performs simple robotic functions like line following.
- **Deliverables:**
  - Display the line sensor readings on the LCD
  - A robot that is able to follow black line

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Tasks

Tasks Remaining

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Challenges Faced

Thank You

#	Tasks
1	Understand the DE0-Nano board and NIOS Processor in the FPGA
2	Interface an analog sensor with FPGA
3	Interface 16x2 LCD with FPGA
4	Combine the display and analog sensors
5	Interface motor driver and motor encoders
6	Design a power management circuit
7	Combine all the building blocks together
9	Line following algorithm and coding
8	Motor encoder based movements
10	Testing and Debugging
11	Documentation and creating user manual

# Tasks Remaining

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- Switch for robot movements - Encoder based and Line sensor based movements.
- Documentation and User Manual.
- Optimize the code

# Design Block Diagram

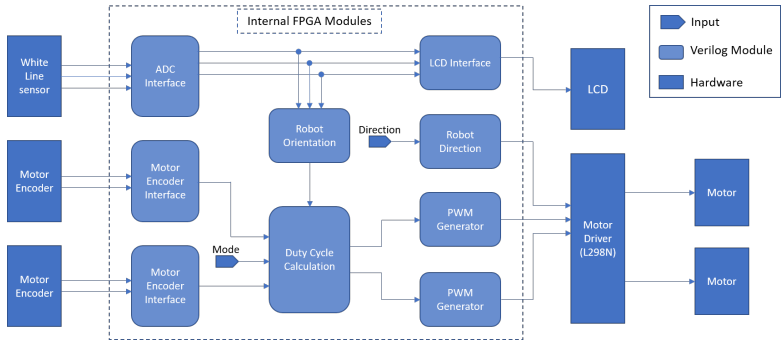


Figure: Verilog Design Block Diagram

# Challenges Faced

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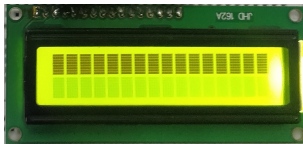
Tasks Remaining

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Challenges Faced

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- Difficulty in interfacing the LCD with 8-bit datalines.  
Timing constraint in sending commands and data to LCD.



(a) LCD initialization error



(b) LCD Working with 4 datalines

- Calculation of motor speed with the motor encoder pulses.

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Thank You

# Thank You!

## Any Queries