Avie Vasantlal

860-936-2159 | adv5201@psu.edu | | | Suffield, CT (open to relocation)

Education

The Pennsylvania State University — University Park, PA

B.S. ***Computer Engineering****, Minor* ***Computer Science****; GPA: 3.53* — *August 2022 – May 2026*

Relevant Coursework

Embedded/Electronics: Embedded Systems | Analog Integrated Circuit Design | VLSI Circuits | Discrete Time Signals | Computer Organization & Design

Systems: Computer Architecture | Operating Systems | Concurrent Programming | Data Structures & Algorithms | Computer Vision

Technical Skills

Hardware/Embedded: KiCad | Ultiboard | FMEA | PCB layout & stackup | oscilloscopes | logic analyzers | multimeters | power supplies | bench testing

Languages: C | C++ | Python | Matlab | Shell | Perl | RISC-V | Java | HTML/CSS | Typescript

Tools: Linux/Unix | Docker | AWS | GitHub Actions CI/CD | Valgrind | Tensorflow

Experience

Embedded Systems Engineer Intern — August 2023 – May 2024

Nittany Motorsports — *State College, PA*

- Designed & validated 4-layer control PCB with power distribution, sensor/actuator interfaces, HV-LV conversion; improved reliability 20%, cut BOM cost 12% via FMEA.
- Led full PCB lifecycle: requirements, KiCad schematic/layout, prototyping, board bring-up, system integration & troubleshooting.
- Performed bench validation & in-vehicle testing using oscilloscopes/multimeters to debug signal integrity, noise, & grounding issues.
- Designed cable/harness interfaces simplifying vehicle electrical architecture & improving serviceability.
- Authored test reports & documentation for QA/manufacturing; conducted design reviews improving robustness.

Software Engineer (AI RLHF) — May 2025 – August 2025

Outlier — *San Francisco, CA*

- Built GitHub Actions CI/CD pipelines for C/C++/Python code verification, increasing test reliability & reducing triage time by 25%.
- Engineered reproducible test harnesses cutting flaky tests 30%; applicable to embedded firmware validation.
- Converted 80+ GitHub issues to minimal reproducible tests, improving failure signal-to-noise by 30%.

Director of Entertainment — December 2023 – December 2025

HackPSU — *University Park, PA*

- Led 15-person ops team managing $1K+ budget for 500+ attendee hackathon, boosting satisfaction 18% YoY.
- Built structured hiring/onboarding improving team ramp time & cohesion.
- Coordinated multi-venue logistics ensuring on-time execution.

Projects

Dynamically Scheduled Processor | *C++, Shell* — April 2025 – May 2025

- C++ framework exploring 18D CPU microarchitecture space across SimpleScalar benchmarks; analyzed pipeline widths, scheduling, memory hierarchies.
- Identified Pareto-optimal designs developing timing/throughput intuition relevant to FPGA/digital logic.

Dynamic Memory Allocator | *C, Perl* — February 2025 – March 2025

- malloc/free/realloc with 16-byte alignment & coalescing; iterated allocator strategies for utilization/throughput.
- Built heap consistency checker validating invariants; similar to embedded firmware diagnostics.

5-Stage Harvard Pipelined Processor | *Verilog* — October 2024 – December 2024

- Designed and implemented a Harvard-style, RISC-like 5-stage pipelined processor in Verilog with separate instruction/data memories and supporting testbenches and scripts for simulation and verification.
- Explored computer architecture concepts such as instruction fetch/decode, execute, memory, write-back stages and pipeline hazard handling by modularizing each stage to enable experimentation and extension of the CPU design.