CECS341_Lab1

Twan Tran, Brian Thi, Jae Bum Jang

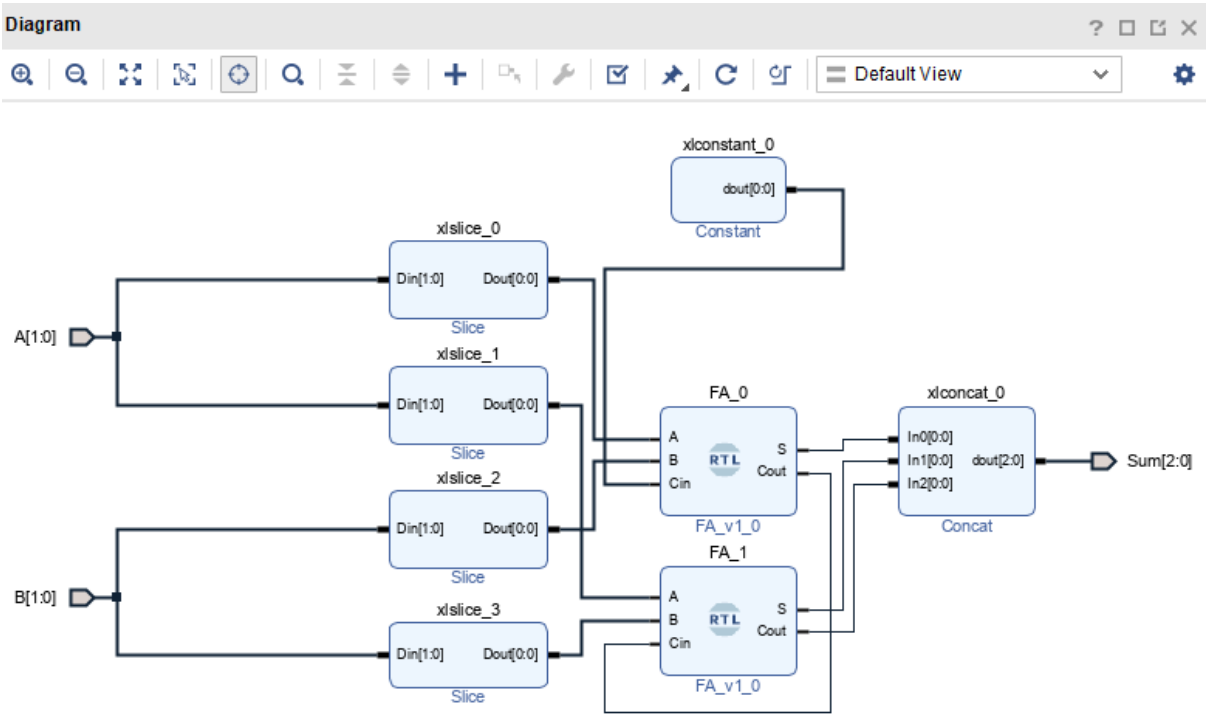
Group# 22

CECS 341

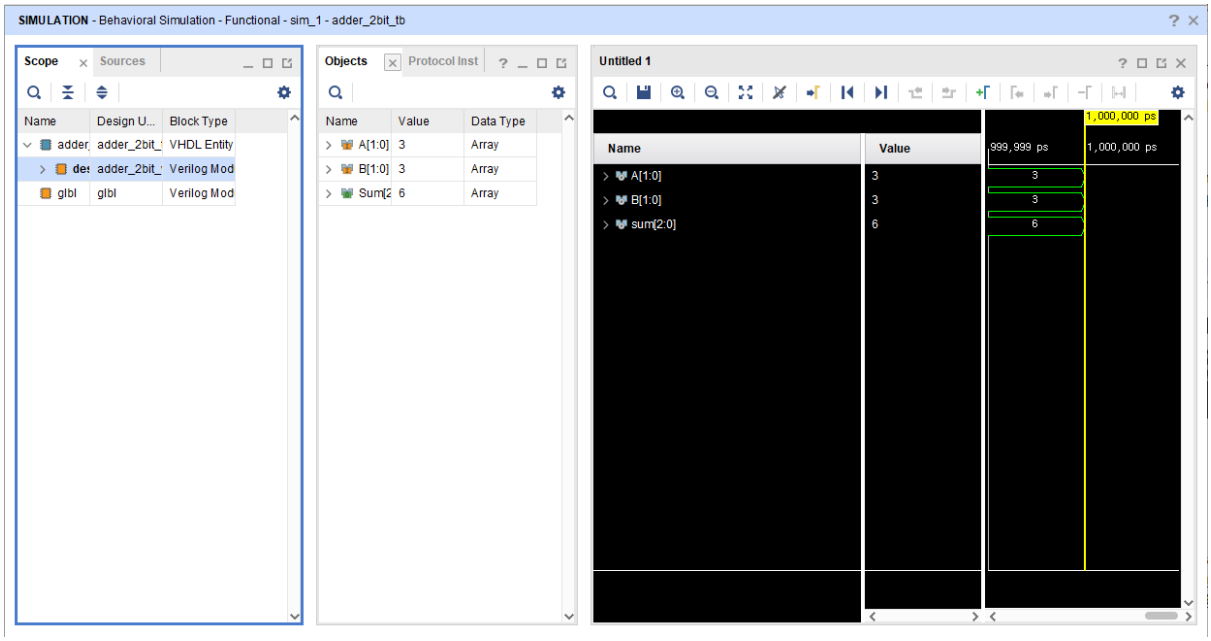
Lab 1 - Introduction to Xilinx Vivado IP Integrator

Our team gained knowledge about installing Xilinx Vivado and using IP Integrator functionalities. By building a VHDL module, we were able to add capabilities like instances, ports for input and output, slices, constants, and concat to block designs. During the process, the parts that make up these characteristics' modified properties such as setting the number of bits became clearer to us. Our diagram was finished by connecting the features, and we could then see the pipelining design. As a result, we have two "Blocks" of an array with a value of 3, and we added 2 arrays together in the concat block to get an output of 3+3 = 6, which perfectly matches the example model.

<Design>



<Waveform>


SIMULATION - Behavioral Simulation - Functional - sim_1 - adder_2bit_tb
Scope
Sources
Name
Design U...
Block Type
adder_
adder_2bit_
VHDL Entity
des
adder_2bit_
Verilog Mod
glbl
glbl
Verilog Mod
Objects
Protocol Inst
Name
Value
Data Type
A[1:0]
3
Array
B[1:0]
3
Array
Sum[2
6
Array
Untitled 1
Name
Value
A[1:0]
3
B[1:0]
3
sum[2:0]
6
999,999 ps
1,000,000 ps
1,000,000 ps
3
3
6