## AIM OF THE EXPERIMENT: 8

To study the functions of basic logic gates : AND, OR, NAND, NOT, NOR & EX-OR.

## APPARATUS. REQUIRED:

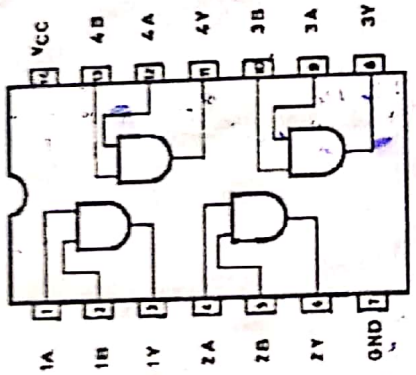
1. Multimeter 1no.
2. Logic I.C. Trainer

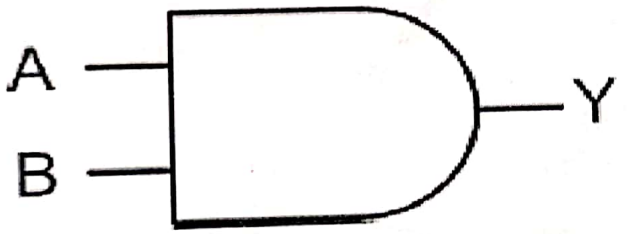
## PROCEDURE:

i. **AND gate**

Identify the terminals of the 7408 quada, 2- input IC AND gate.Switch on the +5 Volt d.c from digital IC trainer i.e. IC power ON. (Ref. Trainer Block No.-5)

Use +3 volt for logic '1' and 0 Volt for logic '0'. A section of the IC shown in Fig .




$Y = A \cdot B$

Ten different switches are available 1 to 10 known as logic input switches. Choose any two input switch for two input signal voltage. Fed the signal voltage to any input pin of the IC and measure output voltage for the various combinations of the input voltage given in Table- 2 and verify the results with the truth table of the And gate given in Table-1.

**TABLE 1**

| Gate | Logic Diagram | Function | Truth Table | | |
|---|---|---|---|---|---|
| AND | | Y = A AND B | INPUT | | OUTPUT |
| | | = A. B | A | B | Y |
| | | = A^B | 0 | 0 | 0 |
| | | = AB | 0 | 1 | 0 |
| | | | 1 | 0 | 0 |
| | | | 1 | 1 | 1 |

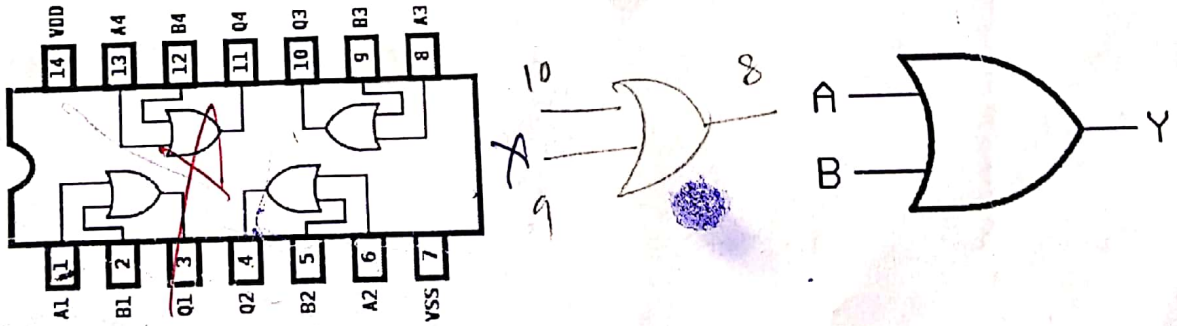
**TABLE 2**

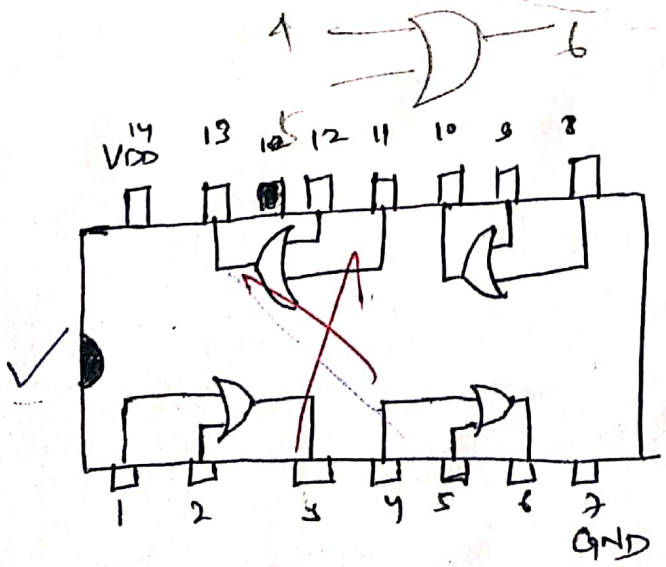
| A | B |
|---|---|
| 0 V | 0 V |
| 0 V | 5 V |
| 5 V | 0 V |
| 5 V | 5 V |

Check if the output voltages for the logic levels '1' and '0' correspond to the values given in table- 1.

ii. **OR gate**

Repeat (i) for a 7432 quad, 2- input IC OR gate, a section of which is shown in fig



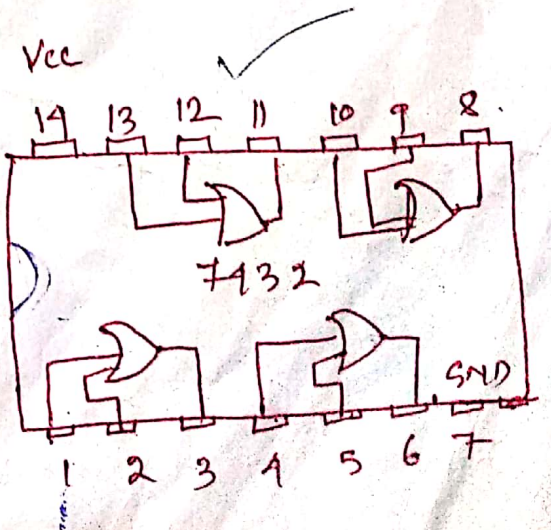
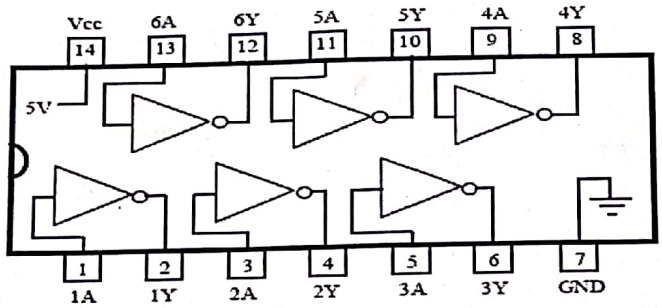



**TABLE 3**

| Gate | Logic Diagram | Function | Truth Table | | |
|---|---|---|---|---|---|
| OR | | Y= A OR B | A | B | Y |
| | | = A + B | 0 | 0 | 0 |
| | | | 0 | 1 | 1 |
| | | | 1 | 0 | 1 |
| | | | 1 | 1 | 1 |

iii. **NOT gate**

Repeat (i) for a 7404 hex IC inverter, a section of which is shown in fig.



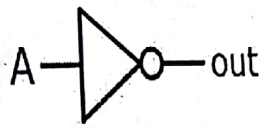
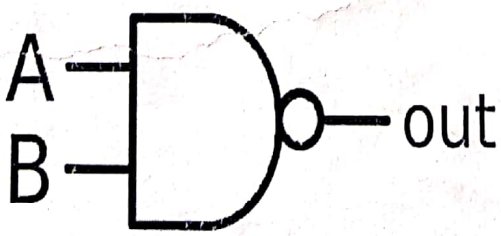



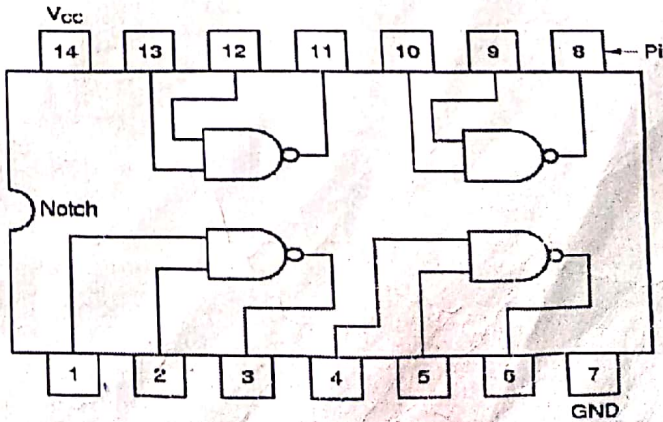

**TABLE 4**

| Gate | Logic Diagram | Function | Truth Table | |
|---|---|---|---|---|
| NOT | | Y= NOT A | A | Y |
| | | = $\bar{A}$ | 0 | 1 |
| | | | 1 | 0 |

iv. **NAND gate**

Repeat (i) for a 7400 quad, 2- input IC NAND gate, a section of which is shown in fig



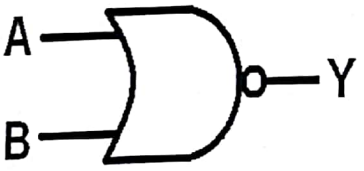



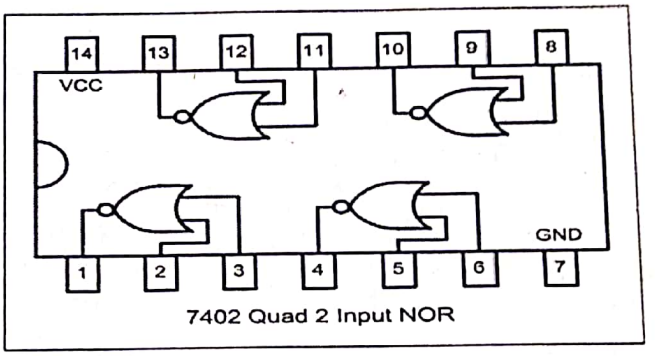
## TABLE 5

| Gate | Logic Diagram | Function | Truth Table | | |
|---|---|---|---|---|---|
| NAND | | Y= A NOT AND B | A | B | Y |
| | | = A NAND B | 0 | 0 | 1 |
| | | = A. B | 0 | 1 | 1 |
| | | =A ↑B | 1 | 0 | 1 |
| | | $= \widehat{AB}$ | 1 | 1 | 0 |

v. **NOR gate**

Repeat (i) for a 7402 quad, 2- input IC NOR gate, a section of which is shown in fig .



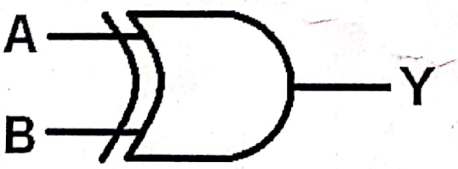




## TABLE 6

| Gate | Logic Diagram | Function | Truth Table | | |
|---|---|---|---|---|---|
| NOR | | Y= A NOT OR B | A | B | Y |
| | | = A NOR B | 0 | 0 | 1 |
| | | $= \overline{A + B}$ | 0 | 1 | 0 |
| | | | 1 | 0 | 0 |
| | | | 1 | 1 | 0 |

vi. **EX-OR gate**

Repeat (i) for a 7486 quad, IC EX-OR gate, a section of which is shown in fig .



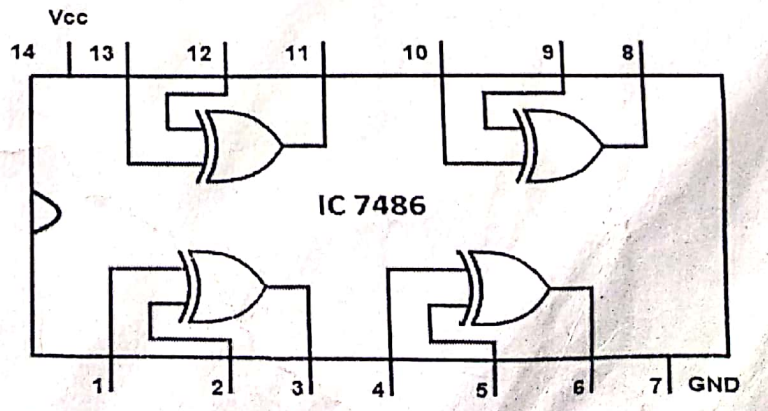



**TABLE 7**

| Gate | Logic Diagram | Function | Truth Table | | |
|---|---|---|---|---|---|
| EX-OR | | Y= A EX-OR B | A | B | Y |
| | | | 0 | 0 | 0 |
| | | = A(+) B | 0 | 1 | 1 |
| | | $=A\bar{B}+\bar{A}B$ | 1 | 0 | 1 |
| | | | 1 | 1 | 0 |

** WRITE THEORY (FROM BOOK) BEFORE PROCEDURE
** WRITE CONCLUSION (AT LAST).