SG2002
Preliminary Datasheet

Version: 1.0-alpha
Release date: 2023-12-15

© 2023 SOPHGO

Revision History

Revision	Date	Description
1.0	2023/12/15	Preliminary release 1.0-alpha

Contents

List of Figures

List of Tables

1 Product Overview

1.1 Overview

SG2002 is a high-performance, low-power chip for edge intelligent surveillance IP cameras, smart cat-eye door locks, visual doorbells, home intelligence and many other product areas, integrating H.264 video compression codec, H.265 video compression encoder and ISP; support for HDR Wide Dynamics, 3D noise reduction, demisting, lens aberration correction, and other image enhancement and correction algorithms, providing customers with professional-grade video image quality. customers with professional-grade video image quality.

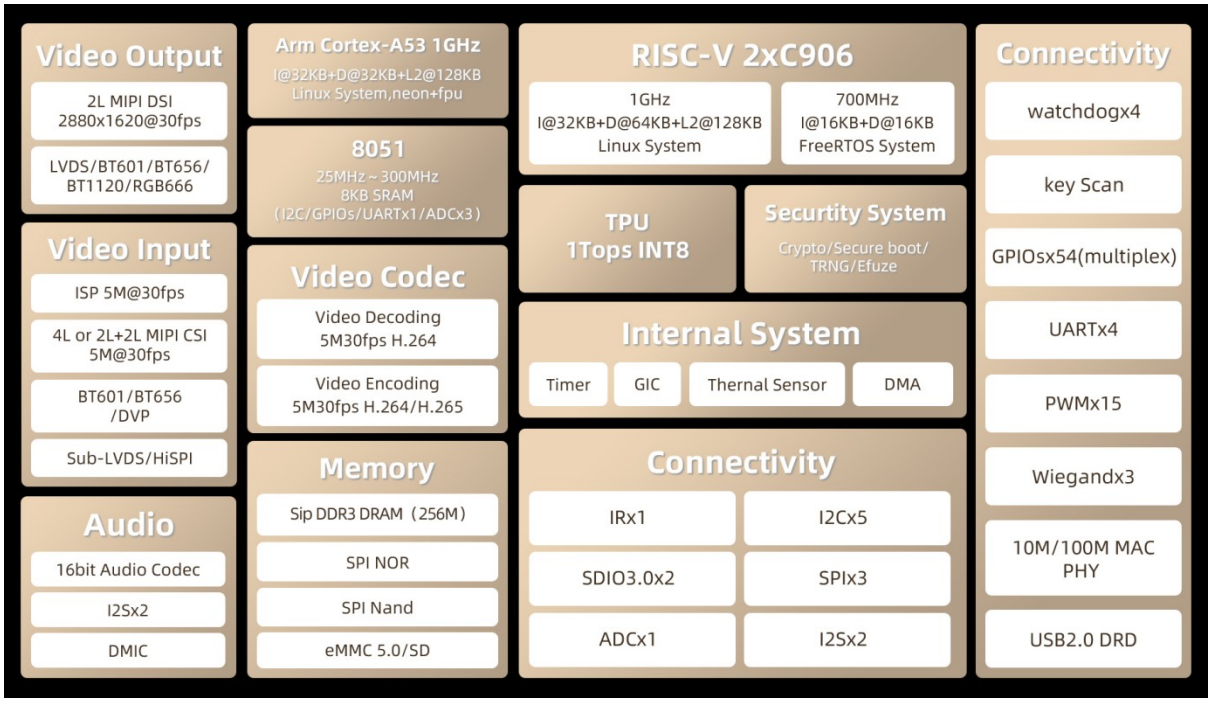
The chip also integrates a self-developed TPU that provides 1.0 TOPS of arithmetic power at 8-bit integer operations. The specially designed TPU scheduling engine efficiently provides extremely high bandwidth data streams to all tensor processor cores. A powerful deep learning model compiler and software SDK development kit are also provided for users. Mainstream deep learning frameworks, such as Caffe and Tensorflow, can be easily ported to its platform.

In addition, it also provides secure boot, secure update, secure encryption, etc. It provides a series of security solutions for users from development, mass production, and product application.

The chip integrates an 8-bit MCU subsystem, which can replace the general external MCU to achieve the purpose of saving BOM cost and power consumption.

1.2 Architecture

1.2.1 Overview



FigureError: Reference source not found-1 SG2002 architecture diagram

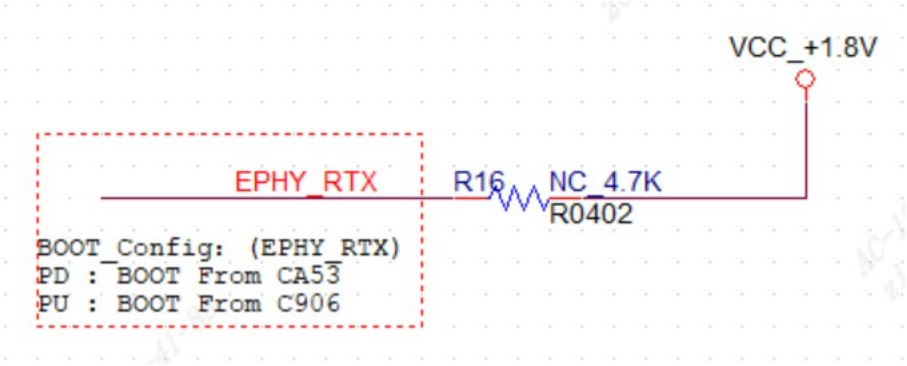
1.2.2 Processor Core

- Main Processor RISCV C906 @ 1.0Ghz
  - 32KB I-cache, 64KB D-Cache
  - Integrated Vector and floating-point unit (FPU)
- Main Processor ARM Cortex-A53 @ 1.0GHz
  - 32KB I-cache, 32KB D-Cache
  - 128KB L2 cache
  - Support for Neon and floating-point unit (FPU)
- Coprocessor RISCV C906 @ 700Mhz
  - Integrated floating-point unit (FPU)

The main processor RISCV C906 @ 1.0Ghz and the main processor ARM Cortex-A53 @ 1.0GHz can be switched via pin GPIO_RTX__EPHY_RTX (as shown below) with the switching logic:

Low-------ARM Cortex-A53 @ 1.0GHz

High------RISCV C906 @ 1.0Ghz



1.2.3 TPU

- Built-in TPU, with ~1.0TOPS INT8
- Support for major neural network architectures: Caffe, Pytorch, TensorFlow (Lite), ONNX and MXNet
- It can realize Pedestrian Detection, Face Detection, Face recognition, Face anti-spoofing and other video structuring applications.

1.2.4 Video Codec

- H.264 Baseline/Main/High profile
- H.265 Main profile
- H.264/H.265 both support I-frame and P-frame
- MJPEG/JPEG baseline
- H.264 codec maximum resolution: 2880×1620 (5M)
- H.265 encoding maximum resolution: 2880×1620 (5M)
- H.264 codec performance
  - 2880×1620@30fps+720×576@30fps
  - 1920×1080@30fps encoding + 1920×1080@30fps Decoding
- H.265 Encoding Performance
  - 2880×1620@30fps+720×576@30fps
- JPEG maximum codec performance
  - 2880×1620@30fps
- Supports multiple bit rate control modes such as CBR/VBR/FIXQP.
- Support Region of Interest (ROI) coding

1.2.5 Video Interface (SG2002)

- Input
  - Supports two simultaneous video inputs (mipi 2L+1L)
  - Support MIPI, Sub-LVDS, HiSPI and other serial interfaces
  - Support 8/10/12 bit RGB Bayer video input
  - Support BT.656
  - Support AHD Multi-Mix BT format
  - Support SONY, OnSemi, OmniVision and other HD CMOS sensors
  - Provides a programmable frequency output for the sensor as a reference clock
  - Support a maximum width of 2880 and a maximum resolution of 5M (2688×1944, 2880×1620)

- Output
  - Support a wide range of serial and parallel display specifications
  - Support serial interfaces such as MIPI
  - Support BT656, BT601(8bit), BT1120, 8080 and other parallel interfaces
  - Support SPI output interface

1.2.6 ISP and Image Processing

- Support image or video rotation by 90, 180, or 270 degrees
- Support horizontal (Flip) or vertical (Mirror) flipping of image or video
- Support overlaying two layers of OSD (On-Screen Display) on the video
- Support video scaling down to 1/32 or up to 32 times
- Support 3A algorithm: automatic exposure (AE), automatic white balance (AWB), and automatic autofocus (AF)
- Support fixed-mode noise reduction and bad pixel correction
- Support correction of lens shading, distortion, and purple fringing
- Support direction-adaptive demosaic algorithm that selects the best demosaic algorithm based on the image orientation
- Support Gamma correction, dynamic contrast enhancement, and color management algorithms
- Support regional adaptive defogging
- Support Bayer denoising, 3D denoising, detail enhancement, and

sharpening enhancement
- Support local Tone mapping
- Support sensor with wide dynamic range and 2-frame wide dynamic range
- Support two-axis digital image stabilization
- Support lens distortion correction
- Provide PC-side ISP tuning tools

1.2.7 CV Hardware Acceleration Engine

- Hardware/software mixed mode support for some OpenCV libraries
- Hardware/Software Mixed Mode support for some IVE libraries

1.2.8 Audio Codec (SG2002)

- Integrated Audio CODEC, supports 16-bit audio/voice input and output
- Integrated mono microphone input
- Integrated mono output. (Requires external amplifier to drive speakers)
- An internal microphone is integrated for direct connection to the output channel, making it easy to implement AEC
- Software audio codec protocols (G.711, G.726, ADPCM)
- The software supports Audio 3A (AEC, ANR, AGC) functions

1.2.9 Network Interface

- The Ethernet module provides one Ethernet MAC for receiving and sending network data
- Ethernet MAC with built-in 10/100Mbps Fast Ethernet Transceiver can work in 10/100Mbps full duplex or half duplex mode

1.2.10 Security System Module

- Hardware implementation of multiple encryption and decryption algorithms such as AES/DES/SM4
- Hardware implementation of HASH (SHA1/SHA256) hash algorithm

- Hardware implementation of a random number generator
- Internally integrated 2Kbit eFuse logical space

1.2.11 Intelligent Secure Operating Environment

- Support the establishment of a trust chain: provide the basis for a secure environment, which is the foundation of a trusted environment, such as hardware security settings, root of trust, etc.
- Support secure boot, provides secure hardware and software protection functions
- Support data encryption security: data encryption program, computing core encryption
- Support software and firmware validation process: confirms software trustworthiness and integrity, including boot and load the signature verification program
- Support secure storage and transmission: protects external data storage and exchange
- Support security updates

1.2.12 Peripheral Interface (SG2002)

- Integrated POR, Power sequence
- 4 single-ended ADCs (3 no die domain)
- 6 I2C (1 no die domain)
- 3 SPI
- 5 groups of UART (1 no die domain)
- 4 groups (15 channels) PWM
- 2 SDIO interfaces
  One supports 3V to connect to SD 3.0 Card (supporting a maximum capacity
  of SDXC 2TB, supported speed is UHS-I)
  One supports 1.8V/3.0V to connect other SDIO 3.0 devices. (Supported speed
  is UHS-I)
- 66 GPIO Interface (14 no die domain)
- Integrated keyscan and Wiegand

- Integrated MAC PHY supports 10/100Mbps full-duplex or half-duplex mode.
- One USB Host / device interface

1.2.13 External Memory Interface

- Built-in DRAM
  - SG2002 DDR3 16bitx1, maximum rate up to 1866Mbps, capacity 2Gbit (256MB)
- SPI NOR flash interface (1.8V/3.0V)
  - Support 1, 2, 4-wire modes
  - Maximum support for 256MByte
- SPI Nand flash interface (1.8V/3.0V)
  - Support 1KB/2KB/4KB page (corresponding maximum capacity 16GB/32GB/64GB)
  - Uses the built-in ECC module of the device
- eMMC 4.5 interface (1.8V/3.0V) SD0 EMMC co-power supply. Because of SD card default 3V, it is not suitable to connect 1.8V eMMC with SD card
  - 4-bit interface
  - Support HS200
  - Maximum Supported Capacity 2TB

1.2.14 SDK

- Linux-5.10-based SDK

1.2.15 Chip Physical Specifications

- Power Consumption
  - 1080P + Video encode + AI: ~ 500mW
  - Other Scenarios: TBD
- Operating voltage
  - Core voltage: 0.9V
  - IO voltage: 1.8V and 3.0V
  - The DDR voltage is shown in the table below.
    - SG2002 = 1.35V
- Package

- Using QFN package, the package size is 9mm×9mm×0.9mm. The pin pitch is 0.35mm, and the total number of pins is 88

1.3 Boot and Upgrade Modes

1.3.1 Overview

The chip is booted by the built-in ROM (BOOTROM). When the chip is reset, it detects whether there is a weak pull-up or weak pull-down on two pins (EMMC_DAT3, EMMC_DAT0) to determine the type of memory device currently in use.

Secure boot chips are signed during boot-up and chip upgrades to ensure that the software being executed or upgraded is secure.

1.3.2 Boot Mode and Corresponding Signal Latch Value Relationship

- Support booting from SPI Nor Flash (EMMC_DAT3 pull down, EMMC_DAT0 pull up)
- Support booting from SPI Nand Flash (EMMC_DAT3 pull down, EMMC_DAT0 pull down)
- Support booting from eMMC (EMMC_DAT3 pull up, EMMC_DAT0 pull up)

Notes: SG2002 does not support eMMC because SD0 and eMMC domain share IO power. Since the SD card defaults to 3.0V and eMMC is mostly 1.8V, it basically does not support eMMC unless SD0 does not connect to the SD card.

1.3.3 Image Burning Mode

- Supports burning image through SD card
- Supports burning image through USB device mode
- If the image already exists in flash, software supports upgrading through the network

1.3.4 Secure Boot

- Supports secure boot and upgrade
- AES/DES/SM4 hardware encryption and decryption
- SHA/TRNG/Secure eFuse security hardware

1.4 Address Space Mapping

Starting Address [31:0]	End Address [31:0]	Space Function	Space Size (Byte)
0x01000000	0x017FFFFF	reserve	8M
0x01800000	0x018FFFFF	reserve	
0x01900000	0x01900FFF	ap_mailbox	4K
0x01901000	0x01901FFF	ap_system_ctrl	4K
0x01902000	0x019EFFFF	reserve	
0x01F00000	0x01F0FFFF	reserve	64K
0x01F10000	0x01FFFFFF	reserve	
0x02000000	0x02FFFFFF	reserve	64K
0x03000000	0x03000FFF	TOP_MISC control register	4K
0x03001000	0x03001FFF	PINMUX control register	4K
0x03002000	0x03002FFF	CLKGEN/PLL control register	4K
0x03003000	0x03003FFF	RSTGEN control register	4K
0x03004000	0x03005FFF	reserve	
0x03006000	0x03006FFF	reserve	4K
0x03007000	0x03008FFF	reserve	
0x03009000	0x03009FFF	reserve	4K
0x0300A000	0x0300AFFF	reserve	4K
0x0300B000	0x0300FFFF	reserve	
0x03010000	0x03010FFF	WATCH DOG0 control register	4K
0x03011000	0x03011FFF	WATCH DOG1 control register	4K
0x03012000	0x03012FFF	WATCH DOG2 control register	4K
0x03020000	0x03020FFF	GPIO0 control register	4K
0x03021000	0x03021FFF	GPIO1 control register	4K
0x03022000	0x03022FFF	GPIO2 control register	4K
0x03023000	0x03023FFF	GPIO3 control register	4K
0x03024000	0x0302FFFF	reserve	
0x03030000	0x03030FFF	WGN0 control register	4K
0x03031000	0x03031FFF	WGN1 control register	4K
0x03032000	0x03032FFF	WGN2 control register	4K
0x03033000	0x0303FFFF	reserve	
0x03040000	0x0304FFFF	KEYSCAN control register	64K
0x03050000	0x0305FFFF	EFUSE control register	64K
0x03060000	0x03060FFF	PWM0 control register	4K
0x03061000	0x03061FFF	PWM1 control register	4K
0x03062000	0x03062FFF	PWM2 control register	4K
0x03063000	0x03063FFF	PWM3 control register	4K
0x03064000	0x0309FFFF	reserve	
0x030A0000	0x030AFFFF	TIMER control register	64K
0x030C0000	0x030CFFFF	reserve	
0x030D0000	0x030D0FFF	reserve	4K
0x030D1000	0x030D1FFF	reserve	4K
0x030D2000	0x030D2FFF	reserve	4K

0x030D3000	0x030DFFFF	reserve	
0x030E0000	0x030EFFFF	TEMPSEN control register	64K
0x030F0000	0x030FFFFF	SARADC control register	64K
0x04000000	0x0400FFFF	I2C0 control register	64K
0x04010000	0x0401FFFF	I2C1 control register	64K
0x04020000	0x0402FFFF	I2C2 control register	64K
0x04030000	0x0403FFFF	I2C3 control register	64K
0x04040000	0x0404FFFF	I2C4 control register	64K
0x04050000	0x0405FFFF	reserve	
0x04060000	0x0406FFFF	SPI_NAND control register	64K
0x04070000	0x0407FFFF	ETH0 control register	
0x04080000	0x040FFFFF	reserve	
0x04100000	0x04107FFF	I2S0 control register	64K
0x04108000	0x0410FFFF	I2S Global control register	64K
0x04110000	0x0411FFFF	I2S1 control register	64K
0x04120000	0x0412FFFF	I2S2 control register	64K
0x04130000	0x0413FFFF	I2S3 control register	64K
0x04140000	0x0414FFFF	UART0 control register	64K
0x04150000	0x0415FFFF	UART1 control register	64K
0x04160000	0x0416FFFF	UART2 control register	64K
0x04170000	0x0417FFFF	UART3 control register	64K
0x04180000	0x0418FFFF	SPI0 control register	64K
0x04190000	0x0419FFFF	SPI1 control register	64K
0x041A0000	0x041AFFFF	SPI2 control register	64K
0x041B0000	0x041BFFFF	SPI3 control register	64K
0x041C0000	0x041CFFFF	UART4 control register	64K
0x041D0000	0x041DFFFF	AUDSRC control register	64K
0x041E0000	0x042FFFFF	reserve	
0x04300000	0x0430FFFF	eMMC control register	64K
0x04310000	0x0431FFFF	SD0 control register	64K
0x04320000	0x0432FFFF	SD1 control register	
0x04330000	0x0433FFFF	DMA control register	64K
0x04340000	0x0434FFFF	USB control register	64K
0x04350000	0x043FFFFF	reserve	
0x04400000	0x0441FFFF	ROM memory space	128K
0x04420000	0x04FFFFFF	reserve	
0x05000000	0x05000FFF	reserve	4KB
0x05020000	0x05020FFF	RTCSYS_Timer control register	4KB
0x05021000	0x05021FFF	RTCSYS_GPIO control register	4KB
0x05022000	0x05022FFF	RTCSYS_UART control register	4KB
0x05023000	0x05023FFF	RTCSYS_INTR control register	4KB
0x05024000	0x05024FFF	RTCSYS_MBOX control register	4KB
0x05025000	0x05025FFF	RTCSYS_CTRL control register	4KB
0x05026000	0x05026FFF	RTCSYS_CORE	4KB
0x05027000	0x05027FFF	RTCSYS_IO control register	4KB

0x05028000	0x05028FFF	RTCSYS_OSC control register	4KB
0x05029000	0x05029FFF	reserve	4KB
0x0502A000	0x0502AFFF	RTCSYS_32kless control register	4KB
0x0502B000	0x0502BFFF	RTCSYS_I2C control register	4KB
0x0502C000	0x0502CFFF	RTCSYS_SAR control register	4KB
0x0502D000	0x0502DFFF	RTCSYS_WDT control register	4KB
0x0502E000	0x0502EFFF	RTCSYS_IRRX control register	4KB
0x05200000	0x053FFFFF	RTCSYS_SRAM	8KB
0x05400000	0x057FFFFF	RTCSYS_SPINOR	4MB
0x08000000	0x08001FFF	reserve	8K
0x08004000	0x08005FFF	DDR Controller control register	8K
0x08006000	0x08007FFF	reserve	8K
0x08008000	0x08009FFF	DDR AXI Monitor control register	8K
0x0800A000	0x0800BFFF	DDR Global control register	8K
0x08010000	0x08011FFF	reserve	8K
0x08012000	0x08013FFF	reserve	8K
0x08014000	0x09FFFFFF	reserve	
0x0A000000	0x0A07FFFF	ISP control register	512K
0x0A080000	0x0A0803FF	sc_top control register	1K
0x0A080400	0x0A080BFF	reserve	2K
0x0A080C00	0x0A080CFF	osd enc control register	256B
0x0A080D00	0x0A080FFF	reserve	768B
0x0A081000	0x0A081FFF	reserve	4K
0x0A082000	0x0A082FFF	img_v control register	4K
0x0A083000	0x0A083FFF	img_d control register	4K
0x0A084000	0x0A084FFF	sc_d control register	4K
0x0A085000	0x0A085FFF	sc_v1 control register	4K
0x0A086000	0x0A086FFF	sc_v2 control register	4K
0x0A087000	0x0A087FFF	sc_v3 control register	4K
0x0A088000	0x0A088FFF	DISP control register	4K
0x0A089000	0x0A089FFF	reserve	4K
0x0A08A000	0x0A08AFFF	dsi_mac control register	4K
0x0A08B000	0x0A08BFFF	cmdq control register	4K
0x0A08C000	0x0A08CFFF	reserve	4K
0x0A08D000	0x0A08DFFF	reserve	4K
0x0A08E000	0x0A09FFFF	reserve	72K
0x0A0A0000	0x0A0AFFFF	IVE control register	64K
0x0A0A0000	0x0A0BFFFF	reserve	64K
0x0A0C0000	0x0A0C1FFF	ldc control register	8K
0x0A0C2000	0x0A0C3FFF	VI0/MIPI_RX0 control register	8K
0x0A0C4000	0x0A0C5FFF	VI1/MIPI_RX1 control register	8K
0x0A0C6000	0x0A0C7FFF	VI2/MIPI_RX2 control register	8K
0x0A0C8000	0x0A0C9FFF	VIPSYS control register	8K
0x0A0CA000	0x0A0CFFFF	reserve	24K
0x0A0D0000	0x0A0D0FFF	CSI_PHY control register	4K

0x0A0D1000	0x0A0D1FFF	DSI_PHY control register	4K
0x0A0D2000	0x0AFFFFFF	reserve	
0x0B000000	0x0B00FFFF	JPEG codec control register	64K
0x0B010000	0x0B01FFFF	H.264 codec control register	64K
0x0B020000	0x0B02FFFF	H.265 codec control register	64K
0x0B030000	0x0BFFFFFF	reserve	
0x0C000000	0x0FFFFFFFF	reserve	
0x10000000	0x1FFFFFFFF	SPI_NOR memory space	256M
0x30000000	0x7FFFFFFFF	reserve	
0x80000000	0xFFFFFFFF	DDR memory space	2G

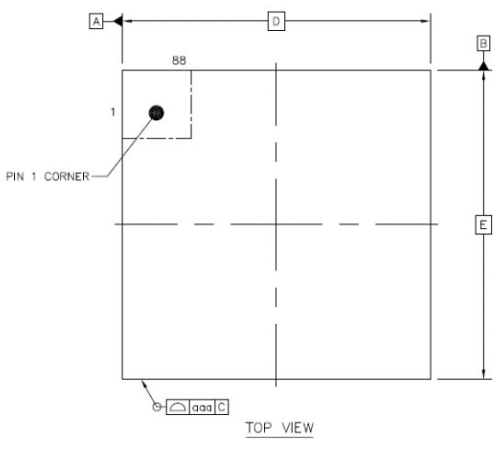
*Read and write operations to reserved address space may produce unintended results.

2 Hardware Characteristics

2.1 Package and Pin Distribution

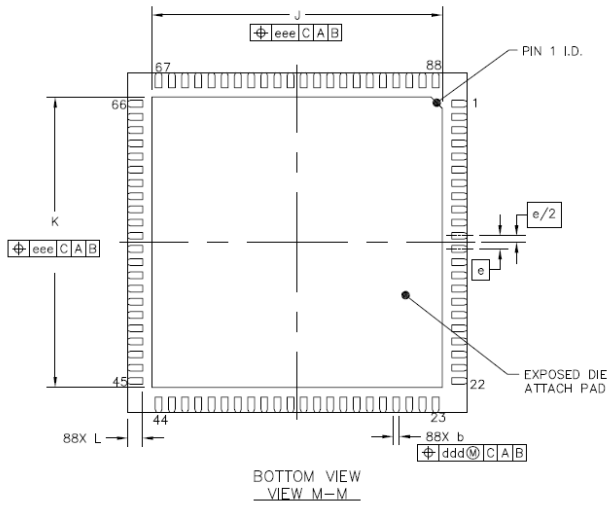
2.1.1 Package SG2002

SG2002 uses QFN package with dimensions of 9mm×9mm×0.9mm. The pin pitch is 0.35mm. The total number of pins is 88. Please refer to the figure below for more detailed package dimensions.



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.7	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.13	0.18	0.23
BODY SIZE	X	D		9 BSC	
	Y	E		9 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	J	7.6	7.7	7.8
	Y	K	7.6	7.7	7.8
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure Error: Reference source not found-2 SG2002 package dimensions, top view



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.7	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.13	0.18	0.23
BODY SIZE	X	D		9 BSC	
	Y	E		9 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	J	7.6	7.7	7.8
	Y	K	7.6	7.7	7.8
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure Error: Reference source not found-3 SG2002 Package external dimensions, bottom view

2.1.2 Pin Distribution SG2002

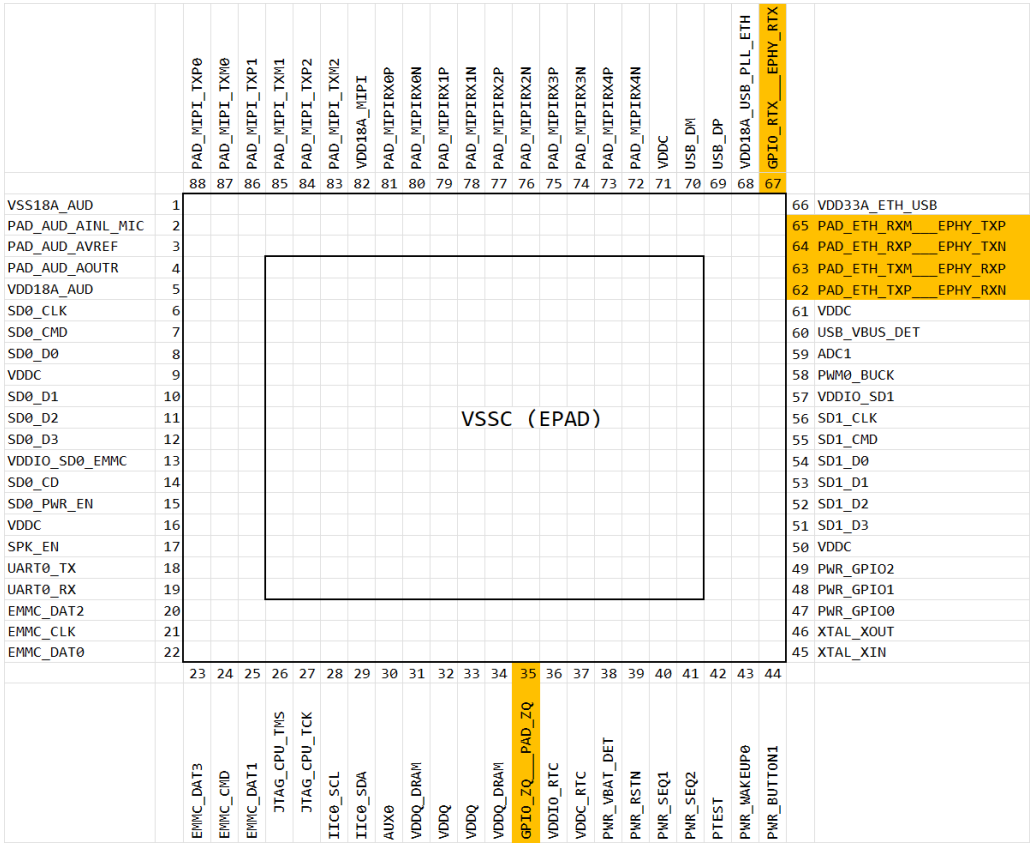


Figure Error: Reference source not found-4 SG2002 pin distribution

2.2 Pin Information Description

Please refer to SG2002_PINOUT_CN.xlsx

2.3 Welding Process Suggestions

Please refer toFigure Error: Reference source not found-5 for the lead-free reflow soldering process curve.
SG2002 Please refer to Pure Sn.

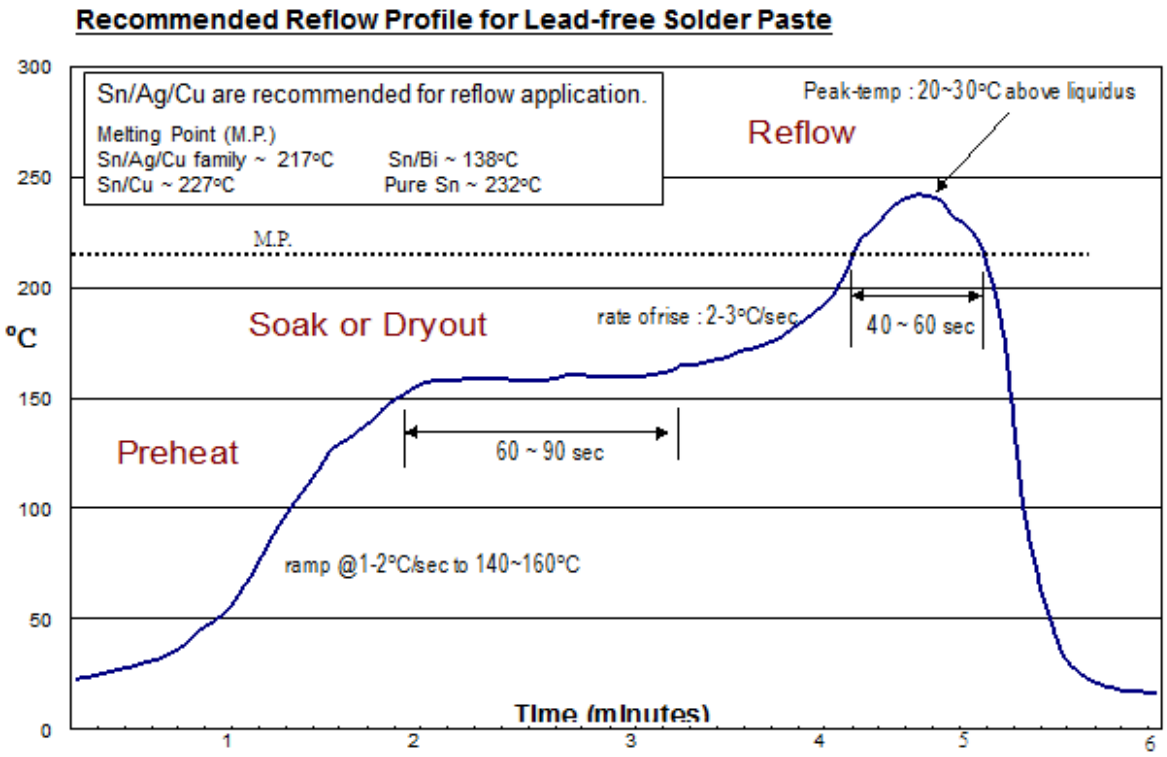


Figure Error: Reference source not found-5 Lead-free reflow soldering process curve

Please refer to Table Error: Reference source not found-1 for the parameters of lead-free reflow soldering process.

The following parameters are only recommended values for reference. Clients need to make relative adjustments according to the actual production conditions.

Table Error: Reference source not found-1 Lead-free reflow soldering cover parameters

Area	Time	Heating Rate	Peak Temperature	Cooling Rate
preheat zone (40~150°C)	60~120sec	1~2°C/sec		
Soak zone (150~200°C)	60~90sec	< 1°C/sec		
reflow zone (>melting point 20~30°C)	40~60sec	2~3°C/sec	Sn/Ag/Cu 237~247°C Sn/Cu 247~257°C Pure Sn 252~262°C	
cooling Zone (Tmax~Tamb)				1~4°C/sec

Due to environmental protection considerations, the parameters for leaded reflow soldering are not provided currently.

2.4 Moisture Sensitivity Parameters

2.4.1 Moisture Barrier Packaging for SOPHGO Products

This section establishes the principles for the storage and use of chips (moisture sensitive products) during welding. The relevant terms are as follows:

- Floor life: refers to the maximum allowable time between opening the moisture barrier packaging and reflow, in an environment with temperature < 30°C/60% RH.
- Shelf life: refers to the normal storage time after the moisture barrier packaging has been sealed.

2.4.1.1 Packaging Information

The moisture-proof vacuum bag containing (1) chip and tray. (2) desiccant Pack (3) Humidity Indicator Card (HIC)

Figure Error: Reference source not found-6 Vacuum drying packaging information

Figure Error: Reference source not found-7 Desiccant packs, humidity indicator card, chip and tray

2.4.1.2 Moisture-Sensitive Product Incoming Inspection

After opening the vacuum moisture-proof bag before SMT, inspect the humidity indicator card. There are many different styles of humidity indicator cards, but if it shows that it has been exposed to moisture, it must be baked before SMT use. The relevant time and temperature parameters for baking are

shown in TableError: Reference source not found-2.

If re-packaging after opening, and it has not been exposed for more than 2 hours in an environment of <30°C/60% RH, it can be vacuum dried and packaged by only replacing the drying bag. If it exceeds 2 hours, it is recommended to re-bake, replace the drying bag, and then reseal the package.

2.4.1.3 Storage and Use (Refer to JEDEC J-STD-033)

- Shelf life:
  The sealed vacuum moisture-proof bag can be stored for at least 12 months in an environment of 40°C/90% RH.

- Floor life:
  Before SMT, if the humidity card indicates that the components have not been exposed to moisture after opening in an environment of 30°C/60% RH, it can be used directly without baking. The time for Level 3 (the floor life classification of this chip is Level 3) is shown in.

TableError: Reference source not found-1 Humidity classification and floor life

Moisture classification level and floor life

Level	Floor Life (out of bag) at factory ambient ≤ 30 °C/60% RH or as stated
1	Unlimited at ≤ 30 °C/85%RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

2.4.1.4 Rebaking

If found to have been exposed to moisture after opening, before SMT or before being resealed in vacuum packaging, they should be baked first. Baking temperature and time can be referred to inTableError: Reference source not found-2 .

After baking, shelf life can be recalculated after being sealed in moisture-proof packaging.

If not sealed in moisture-proof packaging after baking, the storage time should refer to the floor life.

TableError: Reference source not found-2 Baking temperature and time table

Package Thickness	Level	Bake @ 125 °C	Bake @ 40 °C ≤ 5% RH
≤ 1.4 mm	2a	4 h.	5 days
	3	7 h.	11 days
	4	9 h.	13 days
	5	10 h.	14 days
	5a	14 h.	19 days
≤ 2.0 mm	2a	18 h.	21 days
	3	24 h.	33 days
	4	31 h.	43 days
	5	37 h.	52 days
	5a	48 h.	68 days
≤ 4.0 mm	2a	48 h.	67 days
	3	48 h.	67 days
	4	48 h.	68 days
	5	48 h.	68 days
	5a	48 h.	68 days

2.5 Electrical Performance Parameters

2.5.1 Power Consumption Parameters

Typical scenario: 1080P + Video Encode + AI ~500mW
Other scenarios: TBD

2.5.2 Temperature and Thermal Resistance Parameters (SG2002)

Thermal resistance values ThetaJA, JB, JC of the chip. The results of the actual test conducted on the JEDEC 2s2p PCB are shown inTable Error: Reference source not found-3.

Table Error: Reference source not found-3 Thermal resistance parameters for SG2002

PCB Condition	Package Size(mm)	Theta JA (C/W)			Psi Jt (C/W)	Theta JC (C/W)	Theta JB (C/W)
		0 m/s	1 m/s	2 m/s			
JEDEC 2s2p PCB	9×9	20.3	15.9	14.8	0.17	6.9	5.32

The temperature-related parameters of the chip are shown inTable Error: Reference source not found-4.

Table Error: Reference source not found-4 Temperature-related parameters

	Min	Max	Note
Working environment temperature Tamb	-30°C	70°C	1
Recommended value for the junction temperature	-30°C	85°C ~ 105°C	2

	Min	Max	Note
(Tjunc) of chip			
Destructive junction temperature	-40°C	+125°C	3, 4

1. The maximum operating temperature in the working environment depends on the power consumption and heat dissipation conditions of the scenario, without violating the premise of junction temperature.
2. The recommended range of junction temperature is mainly considered to avoid thermal runaway caused by poor heat dissipation conditions at high temperatures, which may lead to uncontrolled temperature entering the destructive junction temperature range and damaging the chip. In addition, long-term operation at high temperatures may slightly accelerate chip aging and reduce its service life.
3. The DRAM used guarantees a junction temperature of only -40°C to 115°C. Content inside the DRAM cannot be guaranteed to remain intact beyond this range.
4. When the chip operates at the destructive junction temperature, it may cause irreversible physical damage to the chip.

2.5.3 Destructive Voltage

The destructive voltage parameters are shown inTableError: Reference source not found-5 . When working above destructive voltage, it may cause irreversible physical damage.

TableError: Reference source not found-5 Destructive voltage parameters (SG2002)

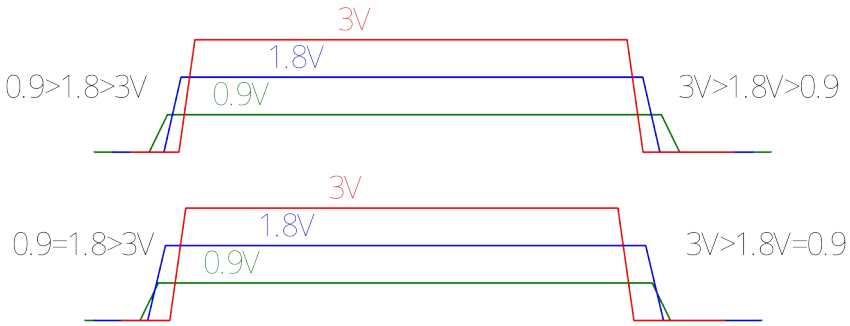
Parameter		Max	Unit
VDDC	Core power	1.05V	V
VDDC_RTC	Core power for RTC domain (comes with LDO)		
VDD18A_AUD	Analog power for Audio ADC/DAC	1.98	V
vdd18a_usb_pll_eth	Analog power for USB, PLL, ETH, eFuse	1.98	V
VDD18A_MIPI	Analog power for MIPI	1.98	V
VDD33A_ETH_USB	Analog power for Ethernet PHY, USB PHY	3.465	V
VDDIO_SD0_EMMC	IO power for EMMC & SD0 domain	3.465	V
VDDIO_SD1	IO power for SD1 domain	3.465	V
VDDIO_RTC	IO power for RTC domain (backup power)	1.98	V
VDDQ VDDQ_DRAM	IO & DRAM Power for DDR2/DDR3L/DDR3	1.65	V

2.5.4 Power Up/Down Sequence (SG2002)

In principle, chips can be divided into the following groups. The same group of power domains can be powered up/down at the same time. For different groups, the power up/down time is separated according to the following conditions.

- Always on domain
  - VDDIO_RTC (1.8V)
  - VDDC_RTC (0.9V) (built-in LDO)
  - VDDIO_SD1
- Core power domain
  - VDDC
- 1.8V IO domain
  - VDD18A_AUD (analog)
  - VDD18A_USB_PLL_ETH (analog)
  - VDD18A_MIPI (analog)
- 18OD33 IO domain (1.8V domain / 3V domain depending on voltage)
  - VDDIO_SD1 (also no die domain)
- 3V domain
  - VDDIO_SD0_EMMC
  - VDD33A_ETH__USB
- DDR IO & DRAM domain
  - VDDQ
  - VDDQ_DRAM

In principle, 0.9V power domain and 1.8V power domain can be powered up at the same time, or power-up the 0.9V power domain prior to 1.8V power domain. **However, the 3V power domain must be powered on after the establishment of 1.8V power domain. Violations may cause irreversible damage to the chip.** The power down sequence is the reverse of the power up sequence.



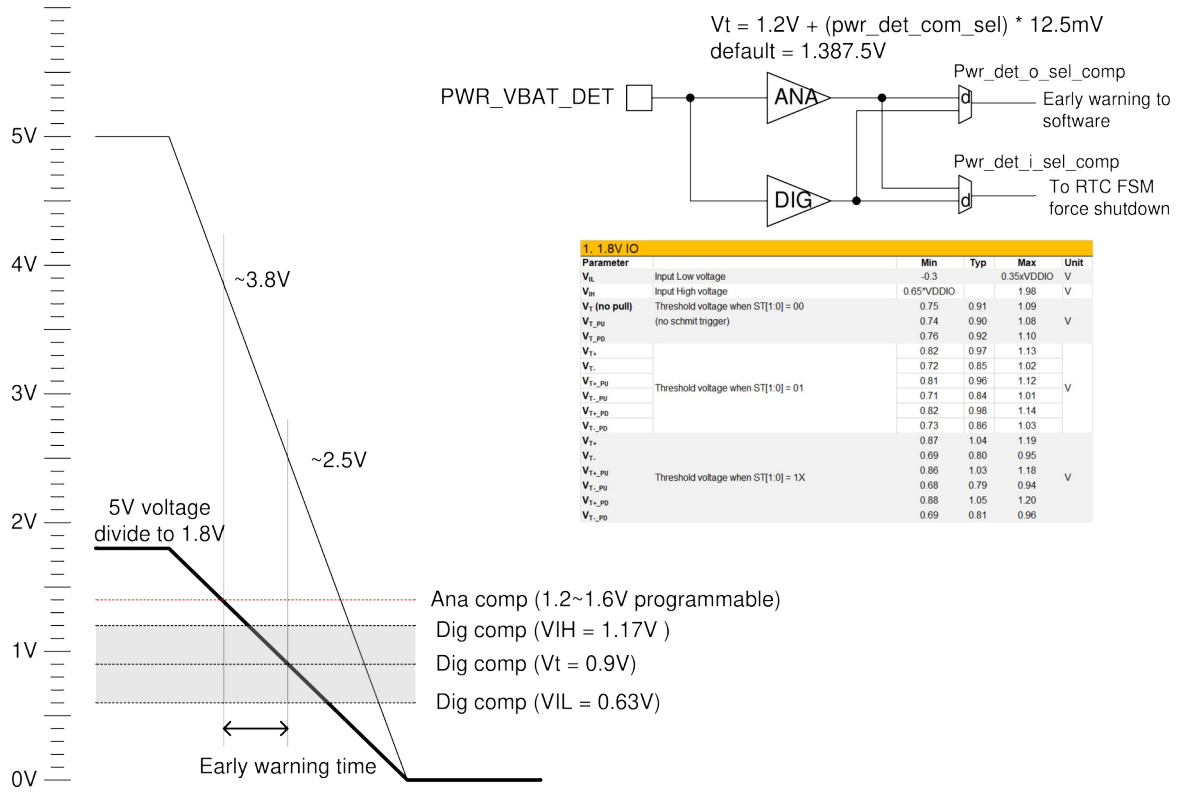
Possible risky power-up and power-down behaviors include:

1. During power-up, if VDD3 > 2V while VDD18 has not reached 1.8V-10%, it may damage the 3V circuit.
2. During power-down, if VDD3 < 2V while VDD18 has already dropped below 1.8V-10%.
3. During power-up, if VDD18 > 0.7V while VDD09 is still below 0.5V, it may cause eFuse misoperation.
4. During power-down, if VDD09 < 0.5V while VDD18 is still > 0.7V, it may also cause eFuse misoperation.

The chip provides two pins, PWR_SEQ1 and PWR_SEQ2, to co-control the power supply (VDDIO_RTC domain) switch. SEQ1 is preset to 0.9V and 1.8V, while SEQ2 controls 3V. Some plug-in systems may use RC to determine the switch for both 0.9V and 1.8V, but it is important that the chip's 3V still needs to be controlled by SEQ2 to prevent damage.

SEQ1 -> SEQ2 at power-up
SEQ2 -> SEQ1 on power off

PWR_VBAT_DET is used to detect the status of the main power supply. If the voltage is low, the software will receive an interrupt first (such as stopping writing flash to prevent damage to the file system). If the voltage continues to drop, the RTC module will actively start the power-down program. PWR_VBAT_DET also needs to be logic high to start up.



1. 1.8V IO

Parameter		Min	Typ	Max	Unit
V_{IL}	Input Low voltage	-0.3		0.35xVDDIO	V
V_{IH}	Input High voltage	0.65*VDDIO		1.98	V
V_T (no pull)	Threshold voltage when ST[1:0] = 00	0.75	0.91	1.09	
V_{T+_PU}	(no schmit trigger)	0.74	0.90	1.08	V
V_{T-_PD}		0.76	0.92	1.10	
V_{T+}	Threshold voltage when ST[1:0] = 01	0.82	0.97	1.13	V
V_{T-}		0.72	0.85	1.02	
V_{T+_PU}		0.81	0.96	1.12	
V_{T-_PU}		0.71	0.84	1.01	
V_{T+_PD}		0.82	0.98	1.14	
V_{T-_PD}		0.73	0.86	1.03	
V_{T+}	Threshold voltage when ST[1:0] = 1X	0.87	1.04	1.19	V
V_{T-}		0.69	0.80	0.95	
V_{T+_PU}		0.86	1.03	1.18	
V_{T-_PU}		0.68	0.79	0.94	
V_{T+_PD}		0.88	1.05	1.20	
V_{T-_PD}		0.69	0.81	0.96	

In practice. The following four conditions can be subdivided. The recommendations are as follows.

Power	Control	Plug-in Applications (1) Ext RTC/no RTC	Plug-in Applications (2) 32Kless
Main 0.9V	Always on	VDDC	VDDC
Main 1.8V	Always on	VDD18A_AUD vdd18a_usb_pll_eth VDD18A_MIPI VDDIO_SD1 VDDIO_RTC	VDD18A_AUD vdd18a_usb_pll_eth VDD18A_MIPI
Main 3.0V	SEQ2	VDD33A_ETH_USB VDDIO_SD0_EMMC VDDIO_SD1	VDD33A_ETH_USB VDDIO_SD0_EMMC
Main VDDQ	always on	VDDQ VDDQ_DRAM	VDDQ VDDQ_DRAM
VDDBACKUP	Coin Batt	For external RTC	
V18RTC (low iddq LDO)	Always on, from Coin batt	No need	VDDIO_RTC VDDIO_SD1

Power	Control	Battery Applications (3) Ext RTC/no RTC	Battery Applications (4) 32Kless
Main 0.9V	SEQ1	VDDC	VDDC
Main 1.8V	SEQ1	VDD18A_AUD vdd18a_usb_pll_eth VDD18A_MIPI	VDD18A_AUD vdd18a_usb_pll_eth VDD18A_MIPI
Main 3.0V	SEQ2	VDD33A_ETH_USB VDDIO_SD0_EMMC	VDD33A_ETH_USB VDDIO_SD0_EMMC
Main VDDQ	SEQ2 or 3	VDDQ	VDDQ

Power	Control	Battery Applications (3) Ext RTC/no RTC	Battery Applications (4) 32Kless
		VDDQ_DRAM	VDDQ_DRAM
VDDBACKUP	Coin Batt	For external RTC	
V18RTC (low iddq LDO)	Always on, from Coin batt	No need	VDDIO_RTC
VAO18	from Main batt	WIFI other AO device VDDIO_RTC VDDIO_SD1	WIFI other AO device VDDIO_SD1
VAO33	from Main batt	WIFI other AO device	WIFI other AO device

2.5.5 Power Supply DC/AC Electrical Parameters

Table Error: Reference source not found-6 The power supply electrical parameters of the SG2002 (Recommended OPERATING conditions)

Parameter		Min	Typ	Max	Unit
VDDC	Core power	0.81	0.9	0.99	V
VDDC_RTC	Core power for RTC domain (Internal LDO, Cap only)	0.81	0.9	0.99	V
VDD18A_AUD	Analog power for Audio ADC/DAC	1.62	1.8	1.98	V
vdd18a_usb_pll_eth	Analog power for Ethernet PHY, USB PHY, PLL	1.62	1.8	1.98	V
VDD18A_MIPI	Analog power for MIPI	1.62	1.8	1.98	V
VDD33A_ETH_USB	Analog power for Ethernet PHY, USB PHY	2.97	3.3	3.465	V
					V
VDDIO_SD0_EMMC	IO power for SD0 & EMMC domain	1.71 2.85	1.8 3.0/3.3	1.89 3.15/3.465	V
VDDIO_SD1	IO power for SD1 domain	1.71 2.85	1.8 3.0/3.3	1.89 3.465	V
VDDIO_RTC	IO power for RTC domain IO & LDO	1.3V	1.8	+10%	V
VDDQ **VDDQ_DRAM**	IO & DRAM Power for DDR3L IO & DRAM Power for DDR3 IO & DRAM Power for DDR2	1.283 1.425 1.425	1.35 1.50 1.50	1.417 1.575 1.575	V

Parameter		Min	Typ	Max	Unit
Tjunc	Junction Temperature (Max reduce from 125C due to DRAM)	-40	25	115 (note)	°C

Note: The operating junction temperature of the DRAM used is guaranteed to be only between -40°C to 115°C. Contents inside the DRAM cannot be guaranteed to be intact beyond this temperature range.

2.5.6 1.8V IO Electrical Parameters

For domain (VDDIO18_0, VDDIO18_1, VDDIO18_RM0, VDDIO_RTC)

Table Error: Reference source not found-7 1.8V IO Electrical Parameters

Parameter		Min	Typ	Max	Unit
V_{IL}	Input Low voltage	-0.3		0.35xVDDIO	V
V_{IH}	Input High voltage	0.65*VDDIO		1.98	V
V_T (no pull) V_{T_PU} V_{T_PD}	Threshold voltage when ST[1:0] = 00 (no schmit trigger)	0.75 0.74 0.76	0.91 0.90 0.92	1.09 1.08 1.10	V
V_{T+} V_{T-} V_{T+_PU} V_{T-_PU} V_{T+_PD} V_{T-_PD}	Threshold voltage when ST[1:0] = 01	0.82 0.72 0.81 0.71 0.82 0.73	0.97 0.85 0.96 0.84 0.98 0.86	1.13 1.02 1.12 1.01 1.14 1.03	V
V_{T+} V_{T-} V_{T+_PU} V_{T-_PU} V_{T+_PD} V_{T-_PD}	Threshold voltage when ST[1:0] = 1X	0.87 0.69 0.86 0.68 0.88 0.69	1.04 0.80 1.03 0.79 1.05 0.81	1.19 0.95 1.18 0.94 1.20 0.96	V
I_I	Input leakage (V_I = 1.8V or 0V)			+/-10u	A
I_{OZ}	Tri-state output leakage current (V_O =1.8V or 0V)			+/-10u	A
R_{PU}	Pull up resistor	55k	79k	121k	Ω
R_{PD}	Pull down resistor	51k	87k	169k	Ω
V_{OL}	Output low voltage			0.45	V
V_{OH}	Output high voltage	1.35			V
I_{OL}	Low level output current @ V_{OL} (max) DS[1:0] = 00 DS[1:0] = 01 DS[1:0] = 10 DS[1:0] = 11	 7.6 15.2 22.6 29.7	 12.8 25.3 37.4 49	 18.0 35.5 52.2 67.9	 mA mA mA mA
I_{OH}	High level output current @ V_{OH} (max) DS[1:0] = 00 DS[1:0] = 01 DS[1:0] = 10 DS[1:0] = 11	 4.8 9.5 14.3 18.9	 10.8 21.5 32.1 42.4	 18.9 37.4 55.9 73.9	 mA mA mA mA

2.5.7 18OD33 IO (VDDIO=1.8V) Electrical Parameters

For domain (VDDIO_EMMC, VDDIO_SD0)

Table Error: Reference source not found-8 18OD33 IO (VDDIO=1.8V) Electrical Parameters

Parameter		Min	Typ	Max	Unit
V_{IL}	Input Low voltage	-0.3		0.58	V
V_{IH}	Input High voltage	1.27		2.00	V
V_T (no pull) V_{T_PU} V_{T_PD}	Threshold voltage when ST = 0 (no schmit trigger)	0.91 0.90 0.91	0.97 0.96 0.97	1.03 1.02 1.06	V
V_{T+} (no pull) **V_{T-} (no pull)** V_{T+_PU} V_{T-_PU} V_{T+_PD} V_{T-_PD}	Threshold voltage when ST = 1	1.03 0.75 1.02 0.74 1.03 0.75	1.07 0.83 1.06 0.82 1.08 0.83	1.12 0.91 1.11 0.90 1.13 0.92	V
I_I	Input leakage (V_I = 1.8V or 0V)			+/-10u	A
I_{OZ}	Tri-state output leakage current (V_O =1.8V or 0V)			+/-10u	A
R_{PU}	Pull up resistor	33k	60k	92k	Ω
R_{PD}	Pull down resistor	34k	61k	158k	Ω
V_{OL}	Output low voltage			0.45	V
V_{OH}	Output high voltage	1.40			V
I_{OL}	Low level output current @ V_{OL} (max) DS[2:0] = 000 DS[2:0] = 001 DS[2:0] = 010 DS[2:0] = 011 DS[2:0] = 100 DS[2:0] = 101 DS[2:0] = 110 DS[2:0] = 111	 4.9 7.4 9.8 12.2 14.6 17.0 19.4 21.7	 7.8 11.7 15.5 19.2 23.0 26.6 30.2 33.7	 11.1 16.4 21.7 26.7 31.9 36.8 41.6 46.2	 mA mA mA mA mA mA mA mA
I_{OH}	High level output current @ V_{OH} (max) DS[2:0] = 000 DS[2:0] = 001 DS[2:0] = 010 DS[2:0] = 011 DS[2:0] = 100 DS[2:0] = 101 DS[2:0] = 110 DS[2:0] = 111	 3.6 5.4 7.2 9.0 10.8 12.6 14.4 16.2	 6.2 9.3 12.4 15.4 18.5 21.6 24.6 27.7	 9.5 14.3 19.1 23.8 28.5 33.1 37.8 42.5	 mA mA mA mA mA mA mA mA

2.5.8 18OD33 IO (VDDIO=3.0V) Electrical Parameters

For domain (VDDIO_EMMC, VDDIO_SD0)

Table Error: Reference source not found-9 18OD33 IO (VDDIO=3.0V) Electrical Parameters

Parameter		Min	Typ	Max	Unit
V_{IL}	Input Low voltage	-0.3		0.25*VDDIO	V

Parameter		Min	Typ	Max	Unit
V_{IH}	Input High voltage	0.625*VDDIO		3.3	V
V_T (no pull) V_{T_PU} V_{T_PD}	Threshold voltage when ST = 0 (no schmit trigger)	0.82 0.81 0.83	0.95 0.93 0.96	1.11 1.09 1.13	V
V_{T+} (no pull) V_{T-} (no pull) V_{T+_PU} V_{T-_PU} V_{T+_PD} V_{T-_PD}	Threshold voltage when ST = 1	1.00 0.75 1.00 0.73 1.01 0.75	1.10 0.90 1.09 0.88 1.11 0.91	1.23 1.08 1.21 1.05 1.25 1.09	V
I_I	Input leakage (V_I = 3.0V or 0V)			+/-10u	A
I_{OZ}	Tri-state output leakage current (V_O =3.0V or 0V)			+/-10u	A
R_{PU}	Pull up resistor	33k	60k	93k	Ω
R_{PD}	Pull down resistor	34k	62k	285k	Ω
V_{OL}	Output low voltage			0.125*VDDIO	V
V_{OH}	Output high voltage	0.75*VDDIO			V
I_{OL}	Low level output current @ V_{OL} (max) DS[2:0] = 000 DS[2:0] = 001 DS[2:0] = 010 DS[2:0] = 011 DS[2:0] = 100 DS[2:0] = 101 DS[2:0] = 110 DS[2:0] = 111	 3.1 4.7 6.2 7.7 9.3 10.8 12.3 13.8	 5.5 8.2 10.8 13.4 16.1 18.7 21.2 23.7	 8.6 12.7 16.9 20.8 24.9 28.8 32.6 36.3	 mA mA mA mA mA mA mA mA
I_{OH}	High level output current @ V_{OH} (max) DS[2:0] = 000 DS[2:0] = 001 DS[2:0] = 010 DS[2:0] = 011 DS[2:0] = 100 DS[2:0] = 101 DS[2:0] = 110 DS[2:0] = 111	 5.0 7.5 10.1 12.6 15.1 17.6 20.1 22.6	 7.5 11.2 14.9 18.6 22.3 26.0 29.8 33.4	 10.5 15.7 21.0 26.2 31.4 36.5 41.8 46.9	 mA mA mA mA mA mA mA mA

2.5.9 Audio GPIO Electrical Parameters

Table Error: Reference source not found-10 Audio GPIO Electrical Parameters

Parameter		Min	Typ	Max	Unit
V_{IL}	Input Low voltage	-0.3		0.55	V
V_{IH}	Input High voltage	1.2		1.98	V
V_{T+} V_{T-}	Threshold voltage with schmitt trigger	0.8 0.65	0.95 0.82	1.1 0.99	V
I_I	Input leakage (V_I = 1.8V or 0V)			+/-4u	A
I_{OZ}	Tri-state output leakage current (V_O=1.8V or 0V)			+/-4u	A
V_{OL}	Output low voltage			0.4	V
V_{OH}	Output high voltage	1.4			V
I_{OL}	Low level output current @ V_{OL} (max)	4.9	9.9	18.4	mA
I_{OH}	High level output current @ V_{OH} (max)	11.3	17.1	26.1	mA

2.5.10 ETH GPIO Electrical Parameters

Table Error: Reference source not found11 ETH GPIO Electrical Parameters

Parameter		Min	Typ	Max	Unit
V_{IL}	Input Low voltage	-0.3		0.3*VDD18A	V
V_{IH}	Input High voltage	0.7*VDD18A		1.98	V
V_{T+} V_{T-}	Threshold voltage with schmitt trigger	0.84 0.66	0.99 0.83	1.14 1.01	V
I_I	Input leakage (V_I = 1.8V or 0V)			+/-1.3u	A
I_{OZ}	Tri-state output leakage current (V_O=1.8V or 0V)			+/-1.3u	A
V_{OL}	Output low voltage			0.4	V
V_{OH}	Output high voltage	VDD18A-0.4			V
I_{OL}	Low level output current @ V_{OL} (max) DS=0 Low level output current @ V_{OL} (max) DS=1	8.8 10.2	15.7 17.8	27.3 30.5	mA
I_{OH}	High level output current @ V_{OH} (max) DS=0 High level output current @ V_{OH} (max) DS=1	4.0 4.7	5.3 6.2	7.4 8.5	mA

2.5.11 MIPI Rx Electrical Parameters

MIPI D-PHY High Speed (MIHS) electrical parameters are shown in Table 2-13 andTable Error: Reference source not found-13 .

MIPI D-PHY Low Power (MILP) electrical parameters are shown inTableError: Reference source not found-14 andTable Error: Reference source not found-15.

Table Error: Reference source not found-12 MIPI D-PHY High Speed (MISH) Differential DC Electrical Parameters

Parameter	Symbol	Data Rate	Min	Typ	Max	Unit
Common Mode Voltage Range (VP+VM)/2	VCM(MIHS)	≤1.5Gbps	70	200	330	mV
		>1.5Gbps				
Internal Termination Resister Value	ZID(MIHS)	≤1.5Gbps	80	100	125	ohm
		>1.5Gbps				
Single-ended threshold for HS termination enable	VTERM-EN(MIHS)	≤1.5Gbps	--	--	450	mV
		>1.5Gbps				

Table Error: Reference source not found-13 MIPI D-PHY High Speed (MIHS) Differential AC Electrical Parameters

Parameter	Symbol	Data Rate	Min	Typ	Max	Unit
Differential Input Threshold Voltage (VP—VM)	VIDTH(MIHS)	≤1.5Gbps	-70	--	70	mV
		>1.5Gbps	-40	--	40	
Single-ended Input Voltage VP,VM	VIS(MIHS)	≤1.5Gbps	-40	--	460	mV
		>1.5Gbps				
Common-mode interface beyond 450MHz	ΔVCMRX	≤1.5Gbps	--	--	100	mV
		>1.5Gbps				
Common-mode interface 50MHz-450MHz	ΔVCMRX(LF)	≤1.5Gbps	-50	--	50	mV
		>1.5Gbps	-25	--	25	
Single-ended threshold for HS termination enable	VTERM-EN	≤1.5Gbps	--	--	450	mV
		>1.5Gbps				
Common-mode termination	CCM	≤1.5Gbps	--	--	60	pF
		>1.5Gbps				

TableError: Reference source not found-14 MIPI D-PHY Low Power (MILP) Differential DC Electrical Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Logic 1 input voltage	VIHLP	740	--	--	mV
Logic 0 input voltage	VILLP	--	--	550	mV
Input hysteresis	VHYST	25	--	--	mV

Table Error: Reference source not found-15 MIPI D-PHY Low Power (MILP) Differential AC Electrical Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Input pulse rejection	eSPIKE	--	--	300	V·ps
Minimum pulse width response	TMIN-RX	20	--	--	ns
Peak interference amplitude	VINT	--	--	200	mV
Interference frequency	fINT	450	--	--	MHz

2.5.12 Sub-LVDS Electrical Parameters

The electrical parameters are shown inTableError: Reference source not found-16 andTableError: Reference source not found-17.

TableError: Reference source not found-16 Sub-LVDS(SL) Differential DC Electrical Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Common Mode Voltage Range (VP+VM)/2	VCM(SL)	600	900	1200	mV
Internal Termination Resister Value	ZID(SL)	80	100	120	mV

TableError: Reference source not found-17 Sub-LVDS(SL) Differential AC Electrical Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Differential Input Threshold Voltage (VP—VM)	VIDTH(SL)	-70	--	70	mV
Single-ended Input Voltage VP,VM	VIS(SL)	400	--	1400	mV

2.5.13 HiSPi Electrical Parameters

HiSPi is divided into SLVS (HSSL) and HiVCM (HSHI). The electrical parameters are shown inTable Error: Reference source not found-18 and .

Table Error: Reference source not found-18 HiSPi Differential DC Electrical Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Common Mode Voltage Range (VP+VM)/2	VCM(HSSL)	50	200	350	mV
	VCM(HSHI)	660	900	1170	
Internal Termination Resister Value	ZID(HSSL)	80	100	125	mV
	ZID(HSHI)	80	100	125	

Table Error: Reference source not found19 HiSPi Differential AC Electrical Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Differential Input Threshold Voltage (VP—VM)	VIDTH(HSSL)	-70	--	70	mV
	VIDTH(HSHI)	-100	--	100	
Single-ended Input Voltage VP,VM	VIS(HSSL)	-40	--	490	mV
	VIS(HSHI)	550	--	1350	

2.5.14 MIPI /LVDS Tx Electrical Parameters

Table Error: Reference source not found20 MIPI HS Transmitter DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{CMTX}	HS transmit static common-mode voltage	150	200	250	mV	
$\lvert\Delta V_{CMTX(1,0)}\rvert$	VCMTX mismatch when output is Differential-1 or Differential-0	–	–	5	mV	
$\lvert V_{OD}\rvert$	HS transmit differential voltage	140	200	270	mV	
$\lvert\Delta V_{OD}\rvert$	VOD mismatch when output is Differential-1 or Differential-0	–	–	14	mV	
V_{OHHS}	HS output high voltage	–	–	360	mV	
Z_{OS}	Single ended output impedance	40	50	62.5	Ω	
ΔZ_{OS}	Single ended output impedance mismatch	–	–	20	%	

Table Error: Reference source not found21 MIPI HS Transmitter AC Specifications

Parameter	Description	Min	Typ	Max	Units	Notes
$\Delta V_{CMTX(HF)}$	Common-level variations above 450MHz	–	–	15	mV_{RMS}	
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450MHz	–	–	25	mV_{PEAK}	
t_R and t_F	20%-80% rise time and fall time	–	–	0.3	UI	1, 2
		–	–	0.35	UI	1, 3
		100	–	–	ps	4

Note:
1. UI is unit interval. Example: 1UI = 1ns for 1Gbps speed.
2. Applicable when supporting maximum HS bit rates ≤ 1 Gbps (UI ≥ 1 ns).
3. Applicable when supporting maximum HS bit rates > 1 Gbps (UI ≤ 1 ns) but ≤ 1.5 Gbps (UI ≥ 0.667 ns).
4. Applicable when supporting maximum HS bit rates ≤ 1.5 Gbps. However, to avoid excessive radiation, bit

rates < 1 Gbps (UI ≥ 1 ns), should not use values below 150 ps.

TableError: Reference source not found22 MIPI LP Transmitter DC Specifications

Parameter	Description	Min	Typ	Max	Units	Notes
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	1
		0.95	–	1.3	V	2
V_{OL}	Thevenin output low level	-50	–	50	mV	–
Z_{OLP}	Output impedance of LP transmitter	110	–	–	Ω	

Note:
1. Applicable in normal Low Power mode when the supported data rate ≤ 1.5 Gbps.
2. Applicable in normal Low Power mode when the supported data rate > 1.5 Gbps.

Table Error: Reference source not found23 MIPI LP Transmitter AC Specifications

Parameter	Description	Min	Typ	Max	Units	Notes
T_{RLP}/T_{FLP}	15%-85% rise time and fall time	–	–	25	ns	
T_{REOT}	30%-85% rise time and fall time	–	–	35	ns	
$T_{LP\text{-}PULSE\text{-}TX}$	Minimum pulse width	20	–	–	ns	
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	–	300	mV/ns	1
		25	–	300	mV/ns	2
C_{LOAD}	Load capacitance	0	–	70	pF	

Note:
1. Applicable in normal Low Power mode when the supported data rate ≤ 1.5 Gbps.
2. Applicable in normal Low Power mode when the supported data rate > 1.5 Gbps.

Table Error: Reference source not found24 LVDS Transmitter DC/AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OS}	LVDS common mode offset voltage	1.125	1.25	1.375	V	
$\lvert\Delta V_{OS(1,0)}\rvert$	VOS mismatch when output is Differential-1 or Differential-0	–			mV	
V_{OD}	LVDS transmit differential voltage	247	350	454	mV	
$\lvert\Delta V_{OD}\rvert$	VOD mismatch when output is Differential-1 or Differential-0	–	–	50	mV	
T_{RLP}/T_{FLP}	15%-85% rise time and fall time (DUT side)		–	0.3UI	ns	

2.5.15 SDIO Electrical Parameters

EMMC / SD0 / SD1 Refer to2.5.7 and2.5.8

2.5.16 VI RAW/BT.601/BT.656/BT.1120 Electrical Parameters

Please refer to2.5.7 and2.5.8 according to the domain of IO.

2.5.17 BT.601/BT.656/8080 Electrical Parameters in VO (Video Out)

Please refer to2.5.7 and2.5.8 according to the domain of IO.

2.5.18 AUDIO CODEC Electrical Parameters

Table Error: Reference source not found25 Audio CODEC Overall Indicator Table

Parameters	Min	Typ	Max	Unit	Description
Analog Power AVDD	1.62	1.8	1.98	V	
VREF		1.4/1.8 *VDD		V	

Table Error: Reference source not found26 Audio DAC Electrical Parameters

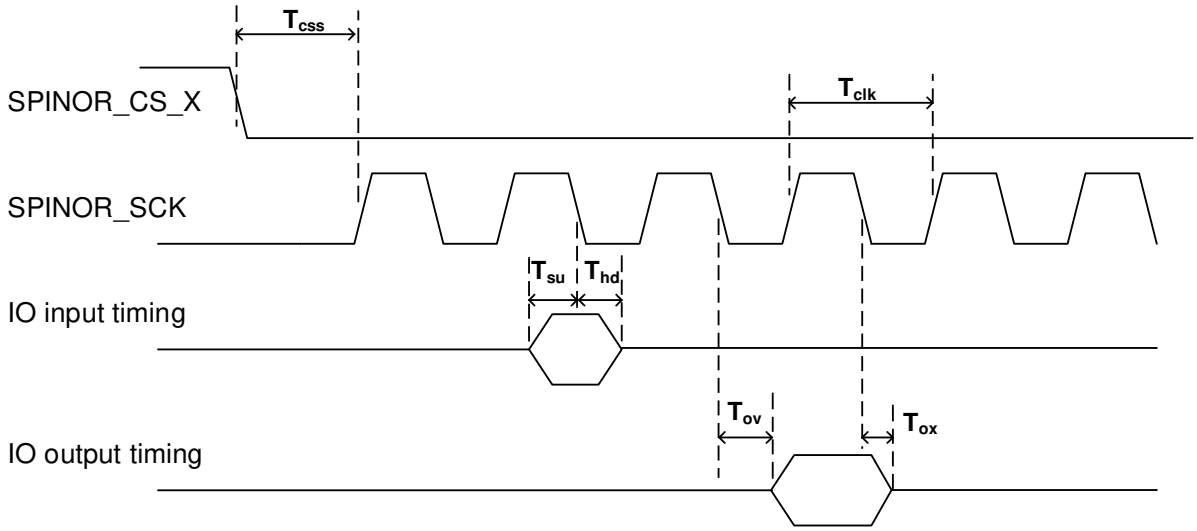
Parameters	Min	Typ	Max	Unit	Description
Full Output Amplitude		1.55		Vpp	Maximum output signal swing

Table Error: Reference source not found27 Audio ADC Electrical Parameters

Parameters	Min	Typ	Max	Unit	Description
Maximum Input Amplitude		1.75		Vpp	Maximum input signal swing

2.6 Timing

2.6.1 SPI NOR Timing



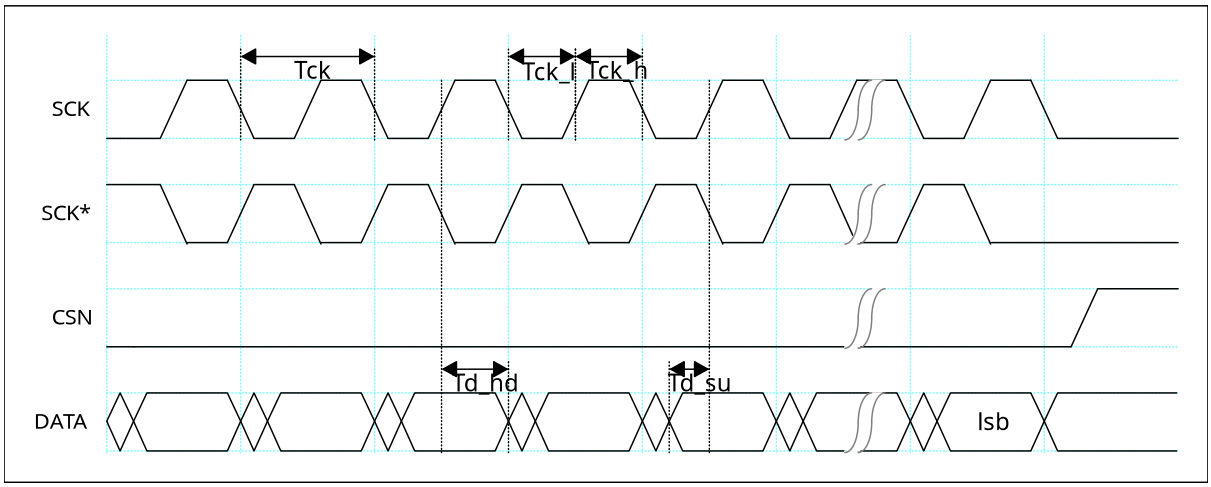
FigureError: Reference source not found-8 SPI NOR Timing Diagram

*IO input timing / IO output timing refers to the IO timing for SPI_NOR CMD/DATA transmission under 1xI/O, 2xI/O, 4xI/O, which includes SPINOR_SDI, SPINOR_SDO, SPINOR_HOLD_X, SPINOR_WP_X.

Table Error: Reference source not found28 SPI_NOR Timing Parameter Table

Symbol	Description	Min	Gen	Max	Unit
T_{css}	Time of CS negative edge to the first clock edge	13.4	-	-	ns
T_{clk}	Clock Cycle	13.4	-	-	ns
T_{su}	Input Signal Setup Time Requirements	3.5	-	-	ns
T_{hd}	Input Signal Hold Time Requirements	0	-	-	ns
T_{ov}	Output Signal Delay	-	-	2.6	ns
T_{ox}	Output Signal Hold Time	-1.5	-	-	ns

2.6.2 SPI NAND Timing



FigureError: Reference source not found-9 SPI NAND Input Timing Diagram

Table Error: Reference source not found-29 SPI NAND Input Timing

Parameters	Symbol	Min	Typ	Max	Unit
Clock Cycle	Tck	10.66		170.56	ns
Input Signal Setup Time Requirements	Td_su	2.00			ns
Input Signal Hold Time Requirements	Td_hd	1.20			ns

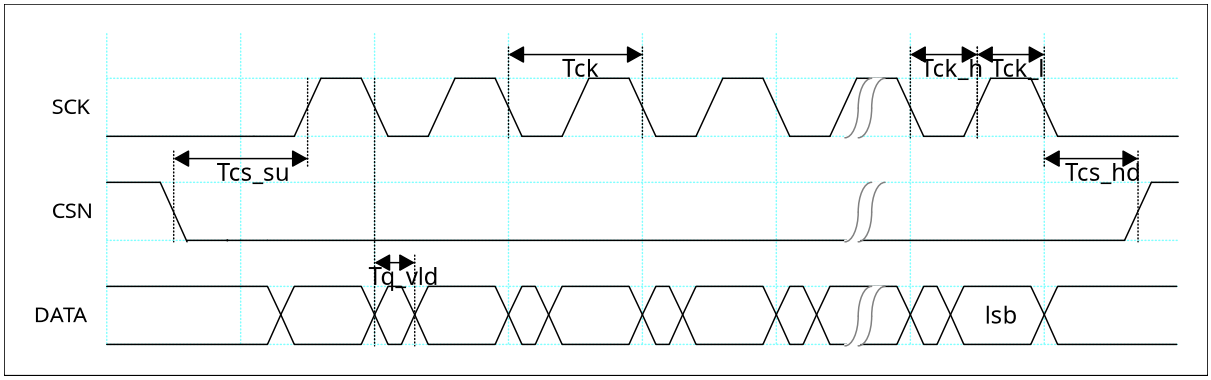


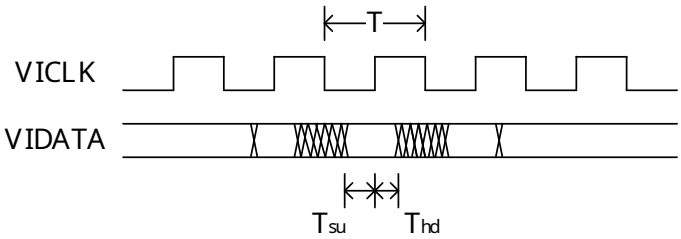
Figure Error: Reference source not found-10 SPI NAND Output Timing Diagram

Table Error: Reference source not found30 SPI NAND Output Timing

Parameters	Symbol	Min	Typ	Max	Unit
Clock Cycle	Tck	10.66		170.56	ns
Clock High Level Period	Tck_h	5.33		85.28	ns
Clock Low Level Period	Tck_l	5.33		85.28	ns
Output CS Setup time	Tcs_su	10.66			ns
Output CS Hold Time	Tcs_hd	10.66			ns
Output Signal Delay	Tq_vld	-1.00		2.00	ns

2.6.3 VI Timing

The VI timing is shown inFigureError: Reference source not found-11.



FigureError: Reference source not found-11 VI Timing Diagram

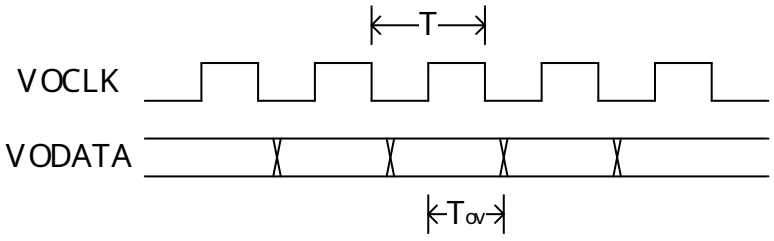
The VI timing parameters are shown inTable Error: Reference source not found-31.

Table Error: Reference source not found-31 VI Timing Parameter Table

	Symbol	Min	Typ	Max	Unit
VICLK clock cycle	T	6.73			ns
VIDATA setup time	T_{su}	1.9			ns
VIDATA hold time	T_{hd}	0.8			ns

2.6.4 VO Timing

The VO timing is shown inFigureError: Reference source not found-12.



FigureError: Reference source not found-12 VO Timing Diagram

The VO timing parameters are shown in.

Table Error: Reference source not found32 VO Timing Parameter Table

	Symbol	Min	Typ	Max	Unit
VOCLK clock cycle	T		6.73		ns
VODATA delay time	Tov	T/2-1.5		T/2+1.5	ns

Figure Error: Reference source not found-13 BT.656 Timing Diagram

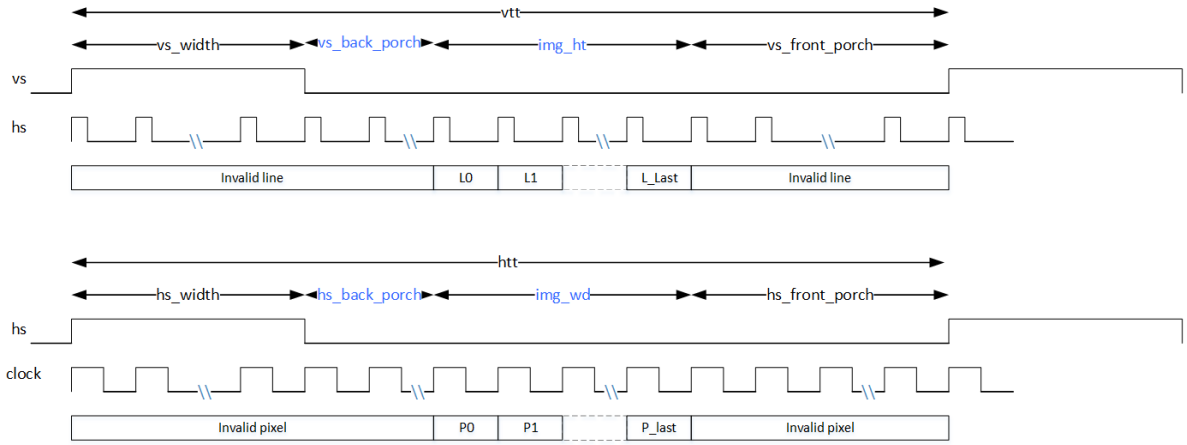
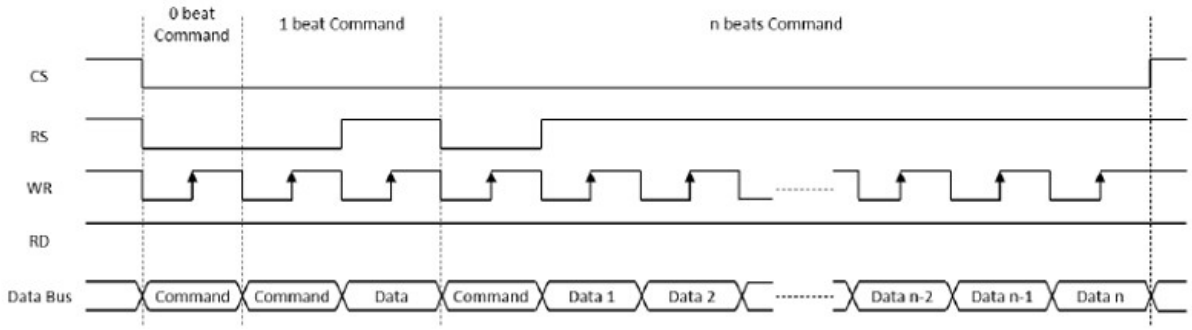


Figure Error: Reference source not found-14 BT.601 Timing Diagram

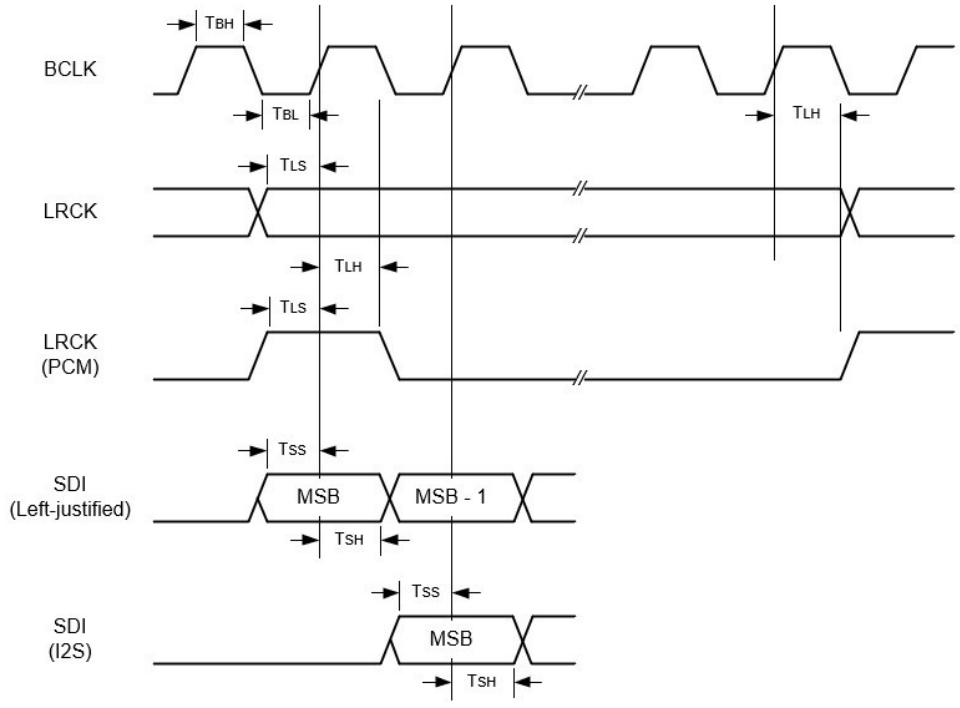
Figure Error: Reference source not found-15 BT.1120 Timing Diagram



FigureError: Reference source not found-16 8080 Timing Diagram

2.6.5 AIAO (I2S/PCM) Timing

The RX timing diagram of I2S and PCM modes for connecting with external Audio Codec is shown inFigureError: Reference source not found-17.



FigureError: Reference source not found-17 I2S & PCM Rx Timing Diagram

The Tx timing diagram of I2S and PCM modes is shown in Figure Error:

Reference source not found-18.

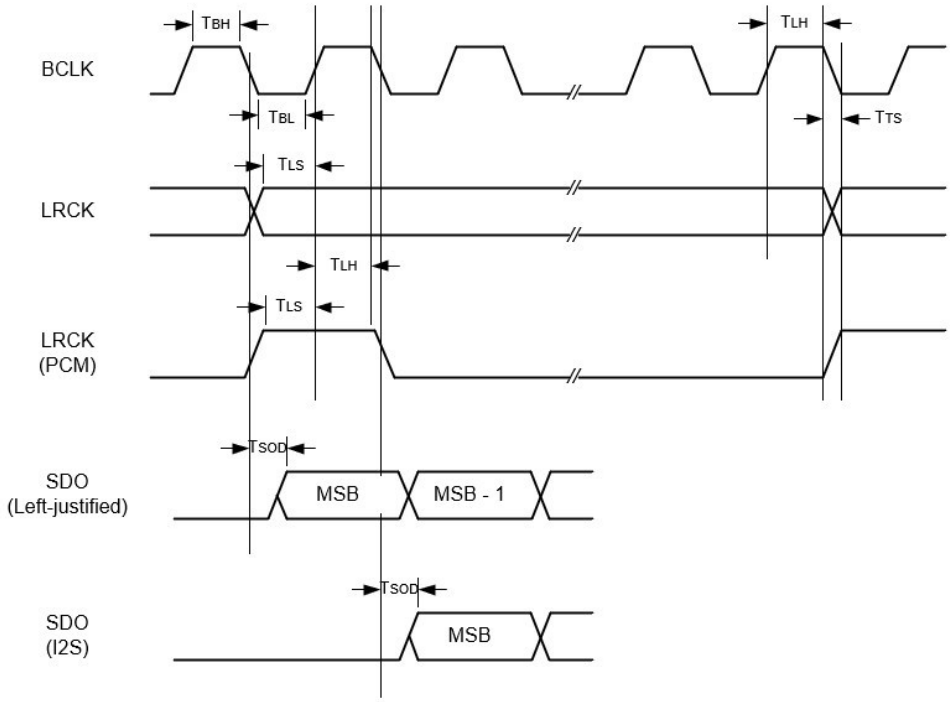


Figure Error: Reference source not found-18 I2S & PCM Tx Timing Diagram

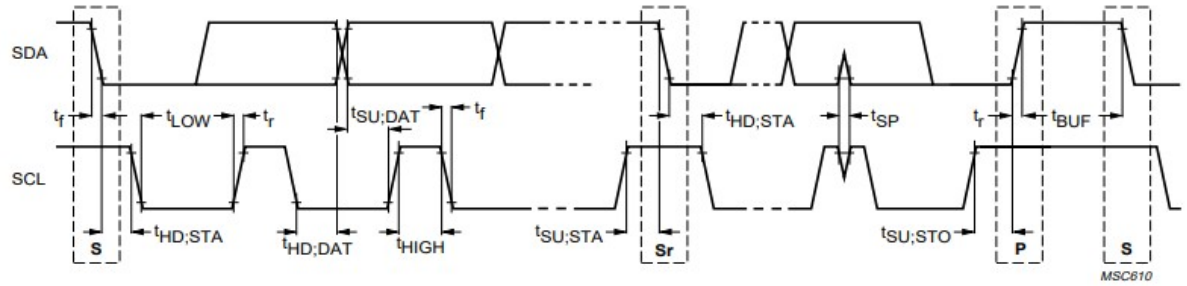
The timing parameters are shown inTable Error: Reference source not found-33.

Table Error: Reference source not found-33 I2S/PCM Timing Parameter Table

Symbol	Parameters	Min	Typ	Max	Unit
T_{BL}	BCLK low pulse width (master and slave modes)	40	-	-	ns
T_{BH}	BCLK high pulse width (master and slave modes)	40	-	-	ns
T_{LS}	LRCK setup time to BCLK rising (slave mode)	10	-	-	ns
T_{LH}	LRCK hold time from BCLK rising (slave mode)	10	-	-	ns
T_{SS}	SDI setup time to BCLK rising (master and slave modes)	10	-	-	ns
T_{SH}	SDI hold time from BCLK rising (master and slave modes)	10	-	-	ns
T_{TS}	BCLK falling to LRCK timing skew (master mode)	0	-	10	ns
T_{SOD}	SDO delay time from BCLK falling (master	0	-	10	ns

Symbol	Parameters	Min	Typ	Max	Unit
	and slave modes)				

2.6.6 I2C Timing

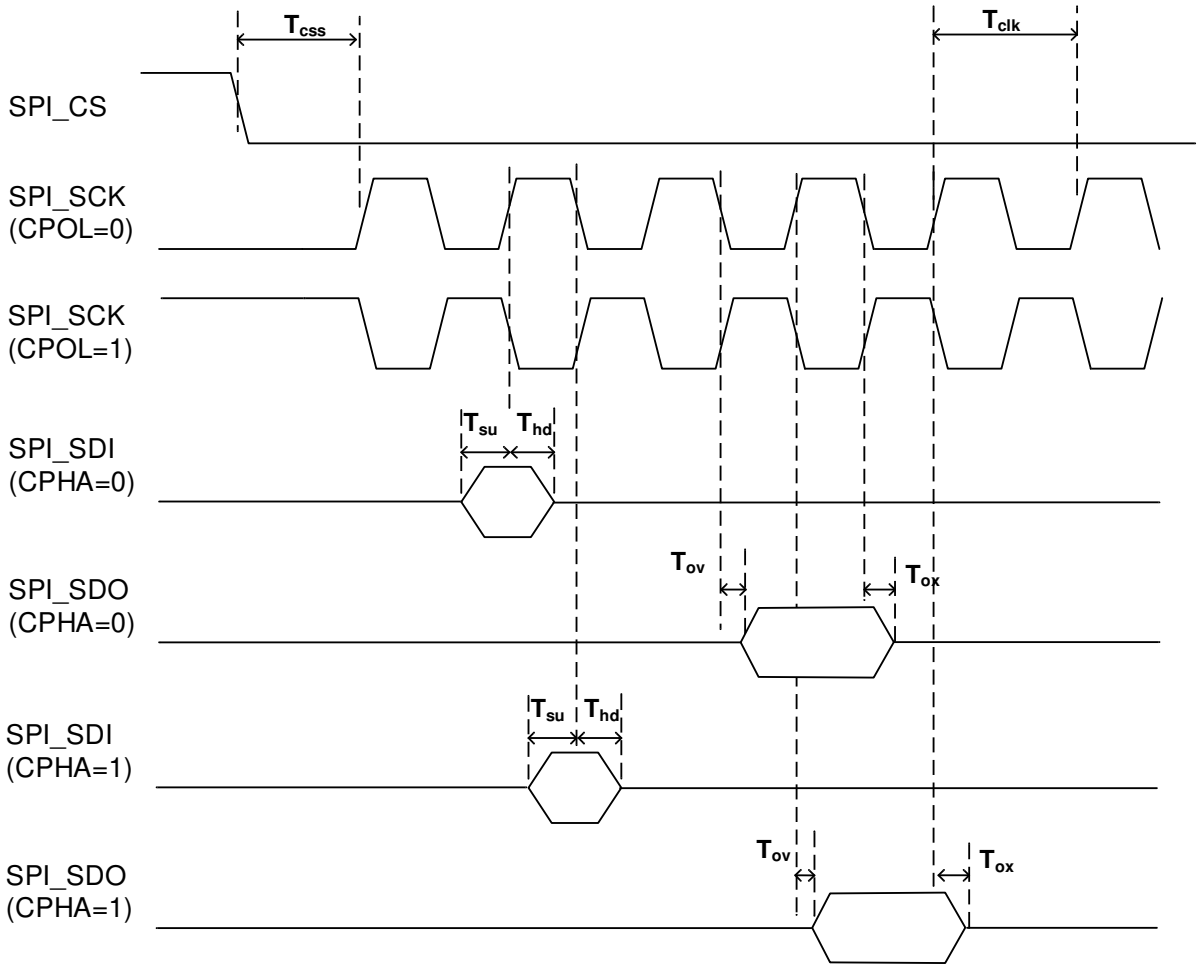


FigureError: Reference source not found-19 I2C Timing Diagram

Table Error: Reference source not found34 I2C Timing Parameter Table

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	µs
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	µs
Data hold time: for CBUS compatible masters (see NOTE, Section 10.1.3) for I²C-bus devices	$t_{HD;DAT}$	 5.0 0(2)	 – 3.45(3)	 – 0(2)	 – 0.9(3)	 µs µs
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	$20 + 0.1C_b$(5)	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	$20 + 0.1C_b$(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	µs
Capacitive load for each bus line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	–	$0.1V_{DD}$	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	–	$0.2V_{DD}$	–	V

2.6.7 SPI Timing



FigureError: Reference source not found-20 SPI Timing Diagram

TableError: Reference source not found35 SPI Timing Parameter Table

Symbol	Parameters	Min	Typ	Max	Unit
F_{clk}	SCK Frequency		-	46.8	MHz
T_{css}	Time of CS negative edge to the first clock edge	21.4	-	-	ns
T_{clk}	Clock cycle	21.4	-	-	ns
T_{su}	Input Signal Setup Time Requirements	9.5	-	-	ns
T_{hd}	Input Signal Hold Time Requirements	0	-	-	ns
T_{ov}	Output Signal delay	-	-	3	ns
T_{ox}	Output Signal hold time	-3	-	-	ns

2.6.8 MIPI Rx Timing

The speed range of MIPI Rx is: 0.08Gbps ≤ Data Rate ≤ 1.5Gbps

A.0.08Gbps ≤ Data Rate ≤ 1.5Gbps

The timing diagram is shown inFigure Error: Reference source not found-21 and the timing parameters are shown inTable Error: Reference source not found36.

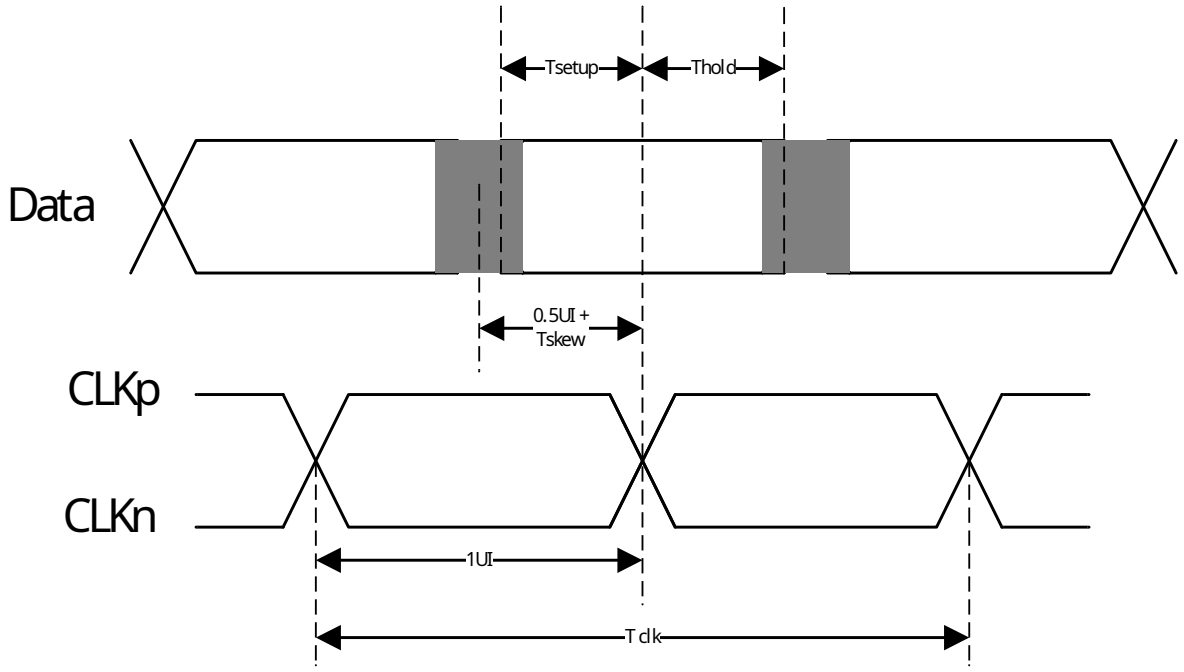


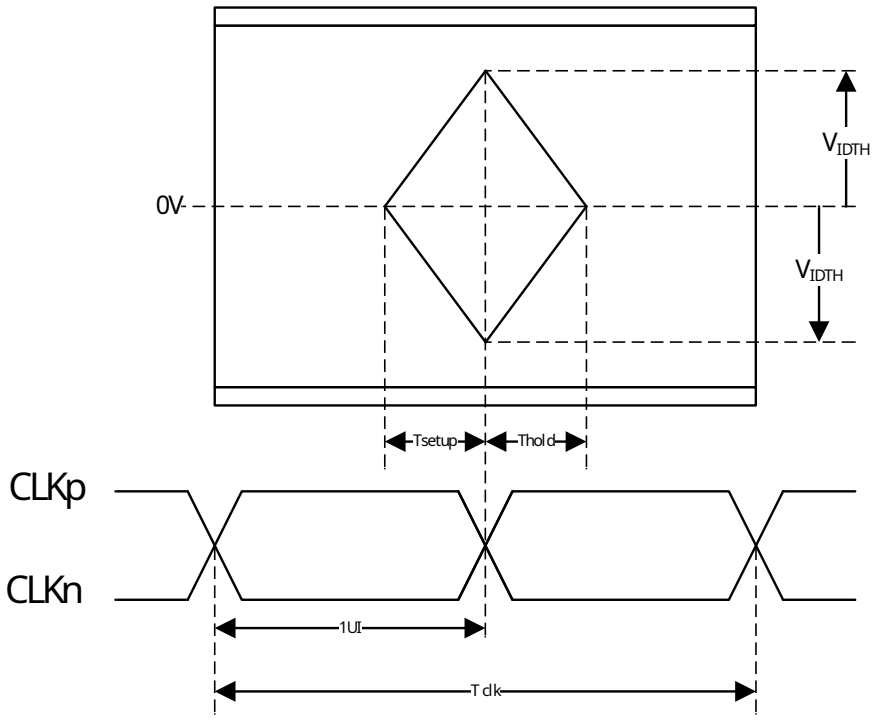
Figure Error: Reference source not found-21 Timing Diagram of MIPI Rx Clock when 0.08Gbps ≤ Data Rate ≤ 1.5Gbps

Table Error: Reference source not found36 Timing Parameter of MIPI Rx at 0.08Gbps ≤ Data Rate ≤ 1.5Gbps

Parameter	Symbol	Data Rate	Min	Typ	Max	Unit
Data Rate	Data Rate	0.08G≤Data Rate≤1G	0.08		1	Gbps
		1G<Data Rate≤1.5G	1		1.5	
Differential Clock Period	Tclk	0.08G≤Data Rate≤1G	2		25	ns
		1G<Data Rate≤1.5G	1.33		2	
TX Data to Clock Skew	T_{SKEW}	0.08G≤Data Rate≤1G	-0.15		0.15	UIHS *
		1G<Data Rate≤1.5G	-0.2		0.2	
RX Data to Clock Setup Time Tolerance	T_{SETUP}	0.08G≤Data Rate≤1G	0.15			UIHS
		1G<Data Rate≤1.5G	0.2			
RX Data to Clock Hold Time Tolerance	T_{HOLD}	0.08G≤Data Rate≤1G	0.15			UIHS
		1G<Data Rate≤1.5G	0.2			
* UIHS= 1/(Data Rate) = Tclk/2						

2.6.9 Sub-LVDS Timing

The Sub-LVDS clock data timing diagram is shown inFigureError: Reference source not found-22 and the timing parameters are shown inTable Error: Reference source not found37.



FigureError: Reference source not found-22 Sub-LVDS Clock Data Timing

Diagram

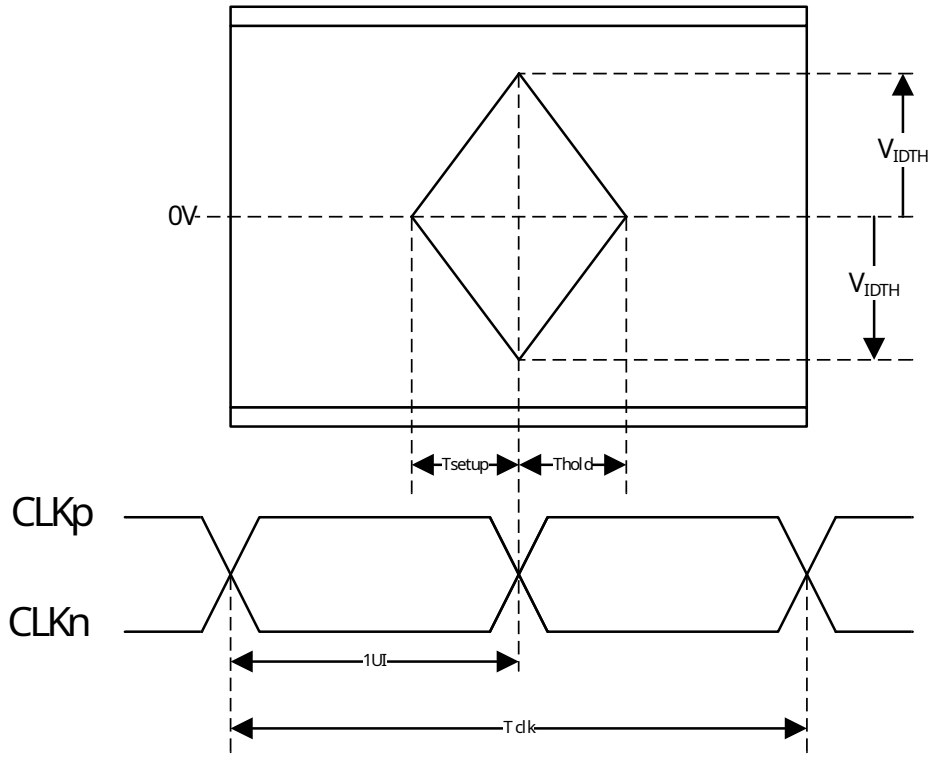
Table Error: Reference source not found37 Sub-LVDS Timing Parameter Table

Parameter	Symbol	Min	Typ	Max	Unit
Data Rate	Data Rate	--	--	1.5	Gbps
Unit Interval	UI	666.6	--	--	ns
Differential Clock Period	Tclk	1333.3	--	--	ns
RX Data to Clock Setup Time Tolerance	T_{SETUP}	0.15	--	--	UI
RX Data to Clock Hold Time Tolerance	T_{HOLD}	0.15	--	--	UI
Differential Input Threshold Voltage (VP-VM)	VIDTH(SL)	-70	--	70	mV

* UI= 1/(Data Rate) = Tclk/2

2.6.10 HiSPi Timing

The HiSPi clock data timing diagram is shown inFigureError: Reference source not found-23 and the timing parameters are shown inTable Error: Reference source not found38 .



FigureError: Reference source not found-23 HiSPi Clock Data Timing Diagram

Table Error: Reference source not found38 HiSPi Timing Parameters Table

Parameter	Symbol	Min	Typ	Max	Unit
Data Rate	Data Rate	--	--	1.5	Gbps
Unit Interval	UI	666.6	--	--	ns
Differential Clock Period	Tclk	1333.3	--	--	ns
RX Data to Clock Setup Time Tolerance	T_{SETUP}	0.15	--	--	UI
RX Data to Clock Hold Time Tolerance	T_{HOLD}	0.15	--	--	UI
Differential Input Threshold Voltage (VP-VM)	VIDTH(HSSL)	-70	--	70	mV
	VIDTH(HSHI)	-100	--	100	
* UI= 1/(Data Rate) = Tclk/2					

2.6.11 MIPI Tx Timing

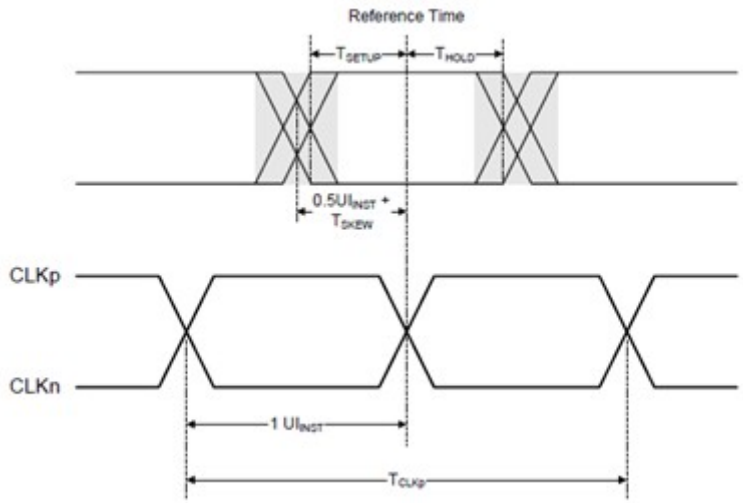


Figure Error: Reference source not found-24 MIPI TX Data-to-Clock Timing Diagram

TableError: Reference source not found-39 Data-Clock Timing Specifications for ≧ 0.08Gbps and ≦ 1 Gbps

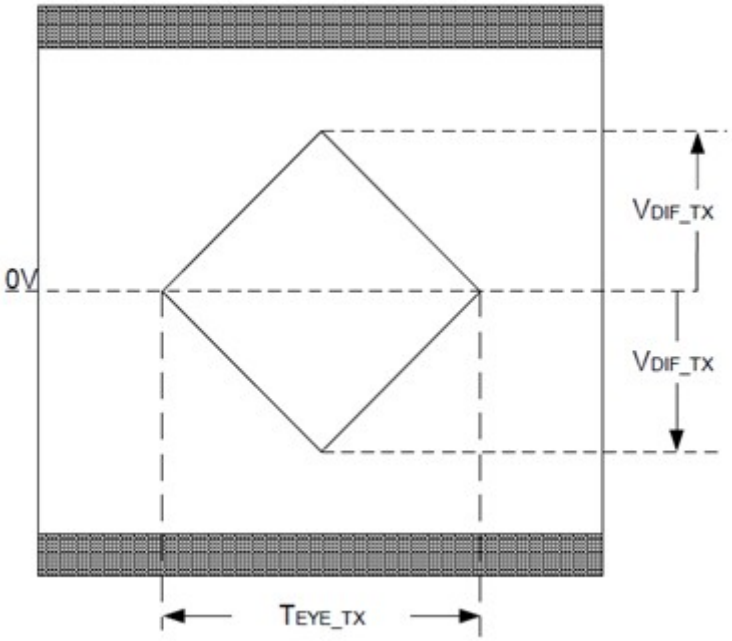
Symbol	Description	Min	Nom	Max	Units	Notes
$T_{SKEW[TX]}$	TX Data to Clock Skew	-0.15		0.15	UI_{HS}	

Table Error: Reference source not found40 Data-Clock Timing Specifications for > 1Gbps and ≦ 1.5 Gbps

Symbol	Description	Min	Nom	Max	Units	Notes
$T_{SKEW[TX]}$	TX Data to Clock Skew	-0.2		0.2	UI_{HS}	

TableError: Reference source not found-41 Data-Clock Timing Specifications for > 1.5Gbps and ≦ 2.5 Gbps

Symbol	Description	Min	Nom	Max	Units	Notes
$T_{SKEW[TX]}$	TX Data to Clock Skew	-0.2		0.2	UI_{HS}	
TJ_{TX}	TX Data to Clock Total Jitter			0.3	UI_{HS}	
DJ_{TX}	TX Data to Clock Deterministic Jitter			0.2	UI_{HS}	
RJ_{TX}	TX Data to Clock Random Jitter			0.1	UI_{HS}	



FigureError: Reference source not found-25 TX EYE Diagram Specification

Table Error: Reference source not found42 Transmitter Eye Diagram Specification

Bit Error Rate	TEYE_TX	VDIF_TX
10^{-12}	0.5UI	40mV
10^{-6} (Prorated for Validation)	0.53UI	47mV

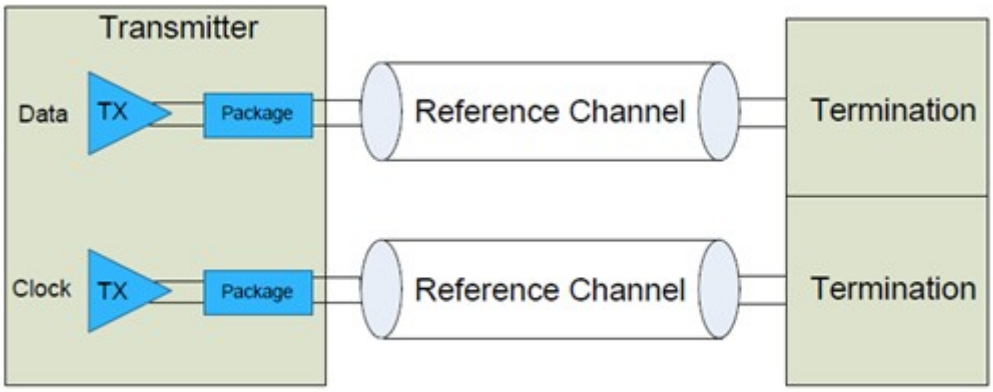
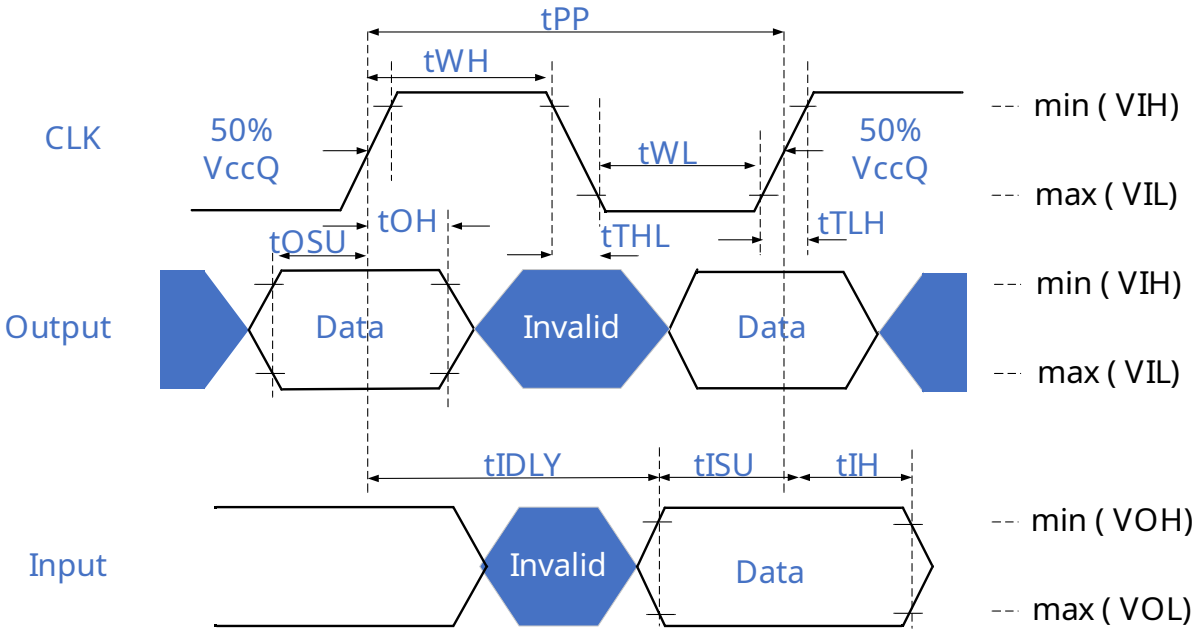


Figure Error: Reference source not found-26 Transmitter Eye Diagram Validation Setup

2.6.12 SDIO/MMC Timing

The data input/output timing for a single edge is shown inFigureError: Reference source not found-27.



FigureError: Reference source not found-27 SDIO/MMC single-edge (SDR) data input/output timing diagram

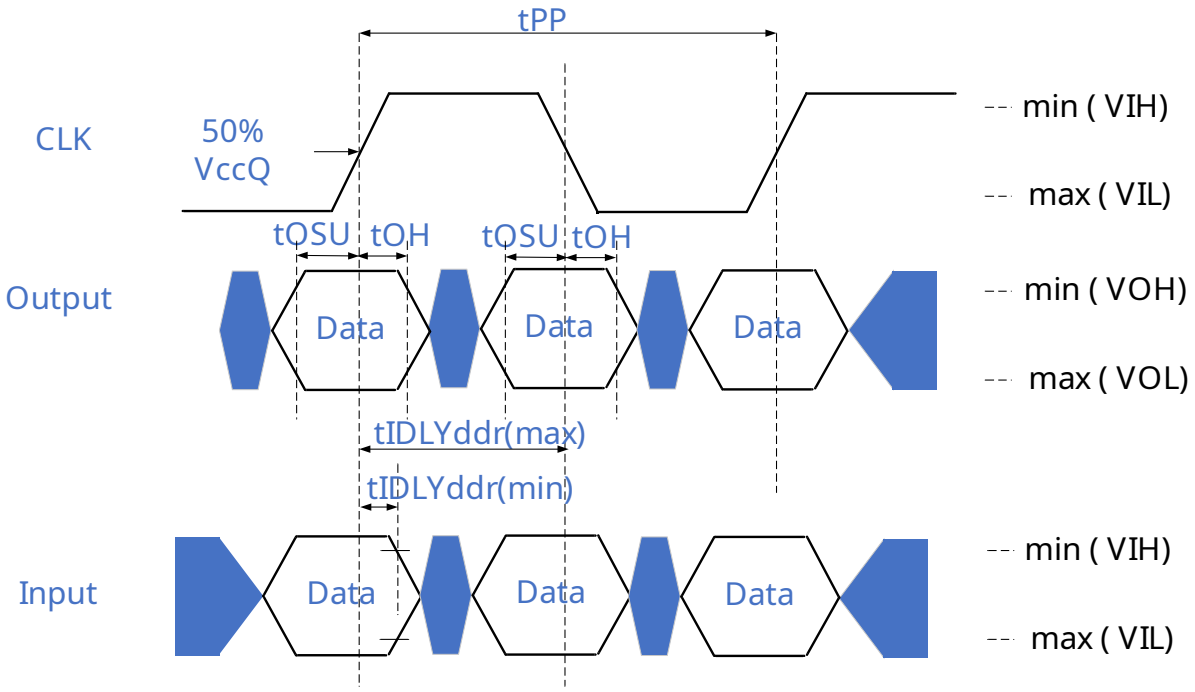
Table Error: Reference source not found-43 SDIO/MMC Single Edge DS (default speed) Mode Timing Parameter Table

Parameters	Symbol	Min	Typ	Max	Unit	Note
Clock CLK						
Clock frequency Data transfer Mode	fPP	0	-	26	MHz	fpp=1/tpp CL≤30pF
Clock frequency Identification Mode	fOD	0	-	400	KHz	CL≤30pF
Clock high time	tWH	10	-	-	ns	CL≤30pF
Clock low time	tWL	10	-	-	ns	CL≤30pF
Clock rise time	tTLH	-	-	10	ns	CL≤30pF
Clock fall time	tTHL	-	-	10	ns	CL≤30pF
Inputs CMD, DAT (referred to CLK)						
Input set-up time	tISU	6	-	-	ns	CL≤30pF
Input hold time	tIH	8.3	-	-	ns	CL≤30pF
Outputs CMD, DAT (referenced to CLK)						
Output set-up time	tOSU	5	-	-	ns	CL≤30pF
Output hold time	tOH	5	-	-	ns	CL≤30pF

TableError: Reference source not found-45 SDIO/MMC Single Edge HS (High speed) Mode Timing Parameter Table

Parameters	Symbol	Min	Typ	Max	Unit	Note
Clock CLK						
Clock frequency Data transfer Mode	fpp	0	-	52	MHz	fpp=1/tpp CL≤30pF
Clock high time	tWH	6.5	-	-	ns	CL≤30pF
Clock low time	tWL	6.5	-	-	ns	CL≤30pF
Clock rise time	tTLH	-	-	3	ns	CL≤30pF
Clock fall time	tTHL	-	-	3	ns	CL≤30pF
Inputs CMD, DAT (referred to CLK)						
Input set-up time	tISU	6	-	-	ns	CL≤30pF
Input hold time	tIH	2.5	-	-	ns	CL≤30pF
Outputs CMD, DAT (referenced to CLK)						
Output set-up time	tOSU	6	-	-	ns	CL≤30pF
Output hold time	tOH	3	-	-	ns	CL≤30pF

The timing of double edge data input/output is shown inFigureError: Reference source not found-28.

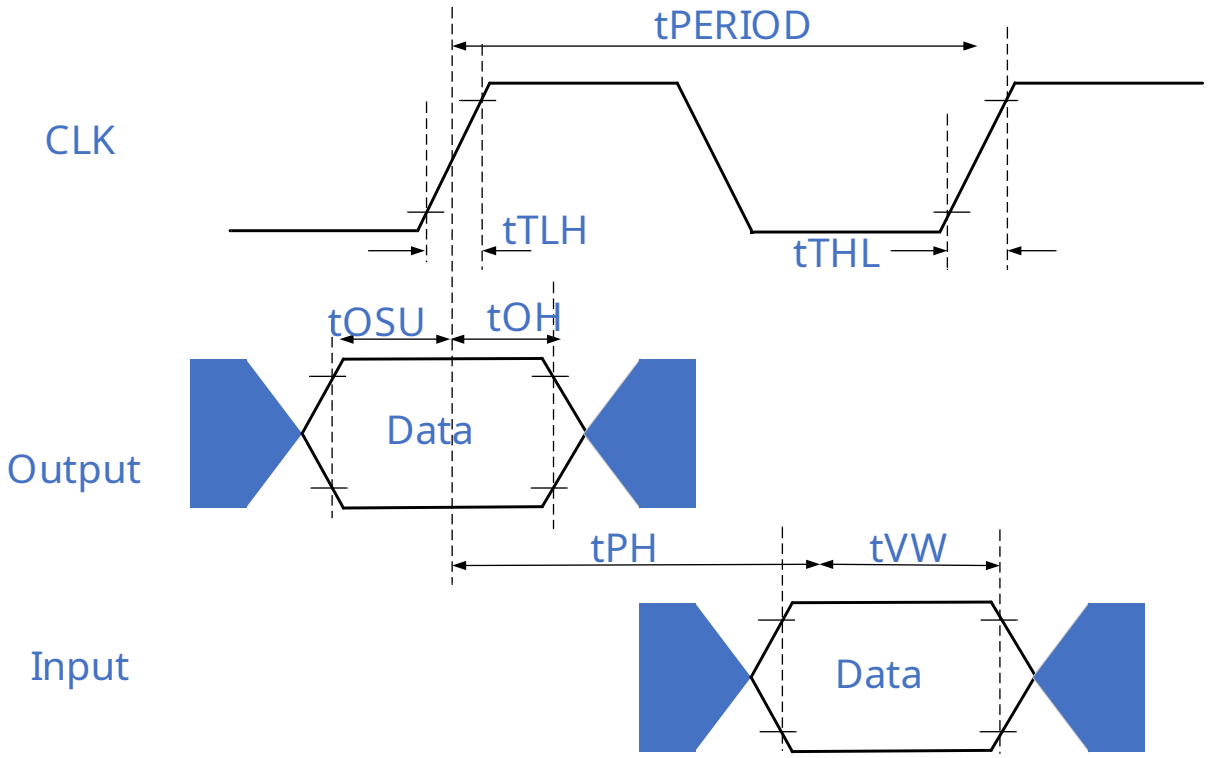


FigureError: Reference source not found-28 SDIO/MMC double edge DDR50 mode data input/output timing diagram

TableError: Reference source not found-44 SDIO/MMC Double Edge DDR50 Mode Timing Parameter Table

Parameters	Symbol	Min	Typ	Max	Unit	Note
Clock CLK						
Clock frequency Data transfer Mode	fP	0	-	52	MHz	fpp=1/tpp CL≤30pF
Inputs DAT (referenced to CLK)						
Input delay time during data transfer	tIDLYddr	1.5	-	7	ns	CL≤20pF
Outputs DAT (referenced to CLK)						
Output set-up time	tOSU	3	-	-	ns	CL≤20pF
Output hold time	tOH	2.5	-	-	ns	CL≤20pF

The timing diagram of HS200 and SDR104 data input/output is shown inFigureError: Reference source not found-29 .



FigureError: Reference source not found-29 SDIO/MMC HS200 and SDR104 mode data command input/output timing diagram

TableError: Reference source not found45 SDIO/MMC HS200 and SDR104 Mode Output Parameters Table

Parameters	Symbol	Min	Typ	Max	Unit	Note
Output set-up time	tOSU	1.4	-	-	ns	$C_{DEVICE} \leq 6pF$
Output hold time	tOH	0.8	-	-	ns	

Table Error: Reference source not found46 SDIO/MMC HS200 and SDR104 Mode Input Timing Parameter Table

Parameters	Symbol	Min	Typ	Max	Unit	Note
Phase difference between device TX CMD/DAT and RX CLK	tPH	0	-	2	UI	Unit Interval (UI) is one-bit nominal time. For 200Mhz, UI=5ns
Input valid data window	tVW	0.575	-	-	UI	TVW=2.88ns at 200MHz