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## PC Motherboard Technology

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By: J. Scott Gardner

### The Urge to Create; the Motherboard

As a kid, perhaps you enjoyed putting together model cars or airplanes. Some people grow up and still like the challenge of buying plastic airplane parts and trying to create something that resembles the picture on the front of the box. Some people move on to woodworking, risking life and limb in an attempt to turn harmless pieces of wood into furniture. Others end up covered in grease while restoring an old car, spending more money than they would on a shiny new model. It's the urge to create, and the instinct has been around since before our ancestors did cave paintings in France. Now some of us have a new hobby, buying a box of computer parts and bringing to life one of the most fascinating creations ever envisioned.

### A Fast Trip Through the Motherboard Landscape

These days, it's gotten much easier for a person to put together a new PC from a set of components, thanks to improvements in technology and the availability of helpful guides on the Internet. Bringing a new computer to life can still provide that same thrill and sense of accomplishment, since building your own PC is really an opportunity to do system design engineering. Choosing the right components and carefully configuring the system can create a perfectly balanced (and cost-effective) computer architecture.

While the latest, sexy CPU's receive all the attention, it's really the motherboard that brings it all together to turn a processor into a personal computer. Let's take a look at the way desktop motherboard and processor technologies have evolved these last few years, focusing on the system issues facing the designers of screaming-fast CPU's. We'll take a processor-neutral approach and try to give the reader some tools for making an objective evaluation of systems based on Cyrix, Intel, or AMD processors. We'll explain the various components on today's motherboards, including some new initiatives that have dramatically simplified the motherboard upgrade ritual.

It would take an entire article to properly cover the (somewhat controversial) overclocking methodology, but we'll touch briefly on this topic in the context of what we learned about motherboard parameters. We'll then test-drive this new system knowledge by making brief case studies of some motherboards that accommodate the newest processors. These motherboards were selected to highlight various architectural differences, and do not represent our endorsement of particular products. In [our last section](#), we'll talk about what the future holds for motherboard architectures.

Before we plunge into the intricacies of the motherboard itself, first we need to take a little time to understand general computer architecture. That will help us later as we describe some of the new motherboard technologies.

### Built for Speed, Designed for Balance

A modern PC is all about moving data--fast, really fast.

The CPU at the heart of the PC has been evolving rapidly through each processor generation, but there has also been a gradual evolution of the rest of the system. The first IBM PC microprocessor was the Intel 8088, running at 4.77 MHz with a 16-bit internal architecture and an 8-bit data bus. Now it's a 32-bit processor humming along at well over a GHz, hooked to a 64-bit data bus.

CPU designers have done a great job of pushing the clock rates, partly in response to the public's psychological need for a single, simple number for evaluating a computer purchase. But megahertz isn't the whole story by any means.

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a from a PC is more of a  
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rapidly wiggling a clock  
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Computers, like most things in life, are never that simple. Getting  
re of a holistic endeavor, and rapidly wiggling a clock signal doesn't  
am. Depending on the processor, the amount of work done during  
ables up to 9 different operations each clock cycle. The Pentium 4  
ceed on both edges of the clock, effectively doubling the amount of  
s of instructions. Billions of times per second, the compute hardware in  
these modern CPU's is looking for something new to work on.

The work we're finding for these CPU's has also changed dramatically over the years. While a CPU still must perform classic math, data movement, and comparison operations, the main performance-demanding application is now media processing (graphics, video, sound). These new media types require massive quantities of data to move rapidly throughout the system.

### **A Balanced Design**

Keeping these ravenous compute engines fed with data takes a lot of clever engineering. The goal of a system designer is to create a balanced design, one where the "compute bandwidth" matches the "memory bandwidth". If the memory system is dramatically slower than the CPU's need for instruction and data transfers, then that expensive processor is "memory starved", and a lot of performance potential is wasted. Likewise, it makes little sense to put a fast, expensive memory system on a slow processor. The bottleneck would shift to the CPU, resulting in a poor system design.

Interestingly enough, processor companies like Intel (through the Intel Architecture Labs) have put a lot of energy into getting the rest of the system components to run faster, even if other vendors provide these components. Unless the CPU continues to be the bottleneck, then CPU companies would have no place to sell those higher-priced processors.

While Intel and AMD both help design new system architectures to support faster processors, they also encourage more advanced application workloads that can be processed by the CPU instead of using external dedicated hardware, and Intel especially is criticized for this tactic by computer enthusiasts. As we'll show, the need to maintain a balanced design has led to dramatic improvements in the system architecture of today's motherboards, though much more needs to be done.

### **Cache: Power and Limitations**

#### **From Fast to Slow--A Hierarchical View of a Computer System**

Let's consider cache memory as part of our system architecture. A processor cache is fast memory for storing the information that a CPU is most likely to need. If the CPU finds the data it needs in the cache (a cache "hit"), then it will load from there. Otherwise, it must go get the data externally (a cache "miss"), sometimes looking in another cache level or retrieving from system DRAM.

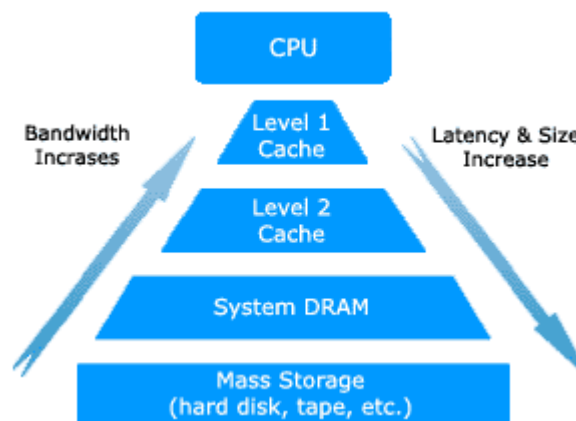


Figure 1: Memory Hierarchy

The best way to view cache memory is to consider these blocks of memory as part of the memory hierarchy in a system. Figure 1 illustrates the concept that data can live anywhere in the memory hierarchy, and the memory gets faster as you get closer to the CPU.

The key to performance lies in a well-designed memory system, and each stage of the memory hierarchy should be constructed to avoid overloading the other stages. Fortunately, a lot of the memory hierarchy is integrated in the processor chip, and designing a balanced PC system starts with choosing the appropriate CPU.

### **Tough Choices for Cache Designers**

Before the Pentium II or Athlon generations of motherboards, Level 2 cache memory was constructed with standard SRAM's on the motherboard. A few chipsets attempted to integrate this memory, but the inevitable march of Moore's law saw Level 2 cache sucked up into the CPU. There will likely be a generation of high-end PC's to use a Level 3 cache on the motherboard in the near future, but this approach has limitations.

Cache memories on-chip with a CPU are usually much more powerful and complex than a cache memory located on the motherboard. With a split cache (separate instruction and data caches, also called a "Harvard Architecture" for historical reasons), an instruction fetch can happen simultaneously with a data access.

With caches on-chip, the designers are also able to use much wider cache interfaces. For instance, even a Pentium fetches 256 bits (32 bytes) at a time from the instruction cache. The 256 bits is equal to one "cache line" in the Pentium, the smallest amount of the cache that must be replaced on a miss. Each line has a "cache tag", which is implemented in separate cache tag memory that is checked to determine if there is a cache hit.

With integrated caches, it's also much easier to include multiple cache tag memories for allowing higher cache associativity that leads to a lower cache miss rate. This concept can be a little confusing. More "sets" of tag memories lead to lower miss rates at the expense of design size and complexity. A cache with only a single set of tags is referred to as "1-way" or "direct-mapped". If you had 4 sets of tags, then it would be called a "4-way" set-associative cache. Computer architects can come close to blows in arguing about which is the best architectural trade-off, though bigger caches are almost always better.

The other advantage of being on-chip is that the cache can have multiple ports, giving a CPU core simultaneous read and write access (as well as access from multiple pipelines). Tag memories are also multi-ported in various CPUs. These extra ports add to the die area and power used by the caches, limiting the overall cache size.

Larger caches also tend to be slower, since it takes more time (and power) to drive a larger bank of

SRAM. These are the reasons why a Level 1 cache is often much smaller than would seem reasonable. For instance, in a throwback to the first Pentium, the Pentium 4 has only an 8 KB Level 1 data cache (plus 12K of pre-decoded micro-ops in an Execution Trace Cache, which is like an L1 instruction cache).

The Intel designers obviously wanted to have more, but limitations with the current process generation forced them to compromise for power and cost.

### **The Real Enemy is Memory Latency**

Understanding memory hierarchy is key to dealing with the nemesis of computer system architects. So far, we've only discussed memory bandwidth and ignored the harder problem of handling latency. As we've shown in describing on-chip caches, it's fairly straightforward how to provide high bandwidth in a system. A designer just needs to run multiple, wide busses at higher clock rates. Any or all of these techniques will do the trick for increasing bandwidth. Latency is almost impossible to get rid of, since we can define latency in terms of the number of internal CPU clock cycles it takes to perform a data transfer. Every increase in processor clock rate adds to the latency, unless the memory system is also improved.

Each stage of the memory hierarchy involves more latency. Moving off-chip adds a huge amount of latency, since the processor must often compete with other devices to get access to the relatively-slow DRAM memory on the motherboard. New DRAM technologies like RDRAM provide very high bandwidth, but the extra complexity of the memory bus actually increases the amount of latency in the memory system.

To illustrate the magnitude of the system latency problem, an on-chip cache miss on a fast system will average about 80 *processor clock cycles* of latency for that instruction.

### **Learning to Live with Latency**

Processor architects have been working to adapt to an environment with long memory latency. Clearly, clever cache design is a big part of the solution, since, on average, every 3rd instruction usually involves a memory operation. Typically, however, every 5th instruction will be some sort of conditional branch, making it very difficult for the processor to know which instructions need to be cached. This is why the various processor vendors each brag about their branch prediction algorithms, since a bad prediction will either waste memory time loading the wrong thing or force the processor to wait for main memory.

The best way to deal with latency in the system memory is to completely avoid these huge penalties for missing in the on-chip caches. The approach taken by Centaur processors (now Via/Cyrix) is to dedicate a huge part of their transistor budget to extremely large on-chip caches and clever branch prediction. This is a straightforward approach to balancing the memory hierarchy and achieving a low-cost, efficient system design.

A dramatic change in processor architecture came with a breaking of the traditional in-order execution stream. Computer architects refer to this new approach as speculative, out-of-order execution (renamed "Dynamic Execution" by the Intel marketing department). First seen on a PC with the Pentium Pro, the architecture allows instructions to execute in the order that compute resources become available, as long as those instructions have cleared any dependencies. The Pentium 4 can have 126 instructions "in flight", allowing long-latency operations to be working while the processor searches for other instructions it can execute.

The AMD Athlon architecture uses a similar approach to instruction re-ordering, gaining the same benefit of latency tolerance. A key feature of the cache design of all new processors is support for non-blocking loads, so that the cache memory system can service other requests while waiting for long-latency data.

### **New Latency-Tolerant Choices for the Motherboard Bus**

With the introduction of these new processors, the Pentium-class Socket 7 bus was finally retired to make way for new high-bandwidth and latency-tolerant system bus designs. Intel's Pentium Pro, Pentium II, Pentium III and Celeron all use a 64-bit, pipelined, split-transaction bus (P6 bus).

By overlapping memory requests, the processor is able to keep the bus operating more efficiently for long-latency operations. While a long-latency memory request is being serviced, the bus can continue to dispatch and receive data for other memory and I/O operations.

Intel also placed the off-chip L2 cache (in a Pentium Pro, Pentium II, and early Pentium III's) onto a "back-side bus" connecting to nearby L2 cache, so that the "front-side bus (FSB)" would have less memory traffic. This L2 cache integration moved the system bus further down the memory hierarchy, helping balance the design. Since the FSB only runs at speeds ranging from 66MHz (Celeron) to 133MHz, the peak bandwidth didn't increase dramatically from the Socket 7 approach.

The Pentium II processor was first offered in a "Slot 1" cartridge with L2 cache implemented as SRAM chips on a circuit board in the cartridge. This was a great way to get high-speed cache memory off the motherboard, allowing PC vendor to build lower-cost boards. In addition to the Slot 1 cartridge, Intel offers the P6 bus in a classic socketed package. Socket 370 (referring to its 370 pins) is a much lower-cost approach and has finally led to near cost parity with Socket 7 motherboards. Low-cost processors from alternative vendors like Cyrix/VIA also work in standard Socket 370 boards. Later in this article, we'll take [a closer look](#) at a Socket 370 motherboard.

#### **AMD, Intel and ... Digital Equipment?**

##### **AMD Turns to DEC for a Bus**

Rather than investing their scarce engineering resources inventing a new bus to compete with the complex P6 bus, AMD licensed the well-designed EV6 bus architecture from Compaq Computer's Digital Equipment Corp. unit. This bus was originally designed to provide the tremendous memory bandwidth needed for Alpha RISC processors and immediately gave AMD's Athlon processor a performance edge for applications that stress the memory system.

Chipsets implemented in original Athlon systems typically did not communicate with the memory subsystem as fast as the processor could communicate with the chipset, leading to an unbalanced design. More recent Athlon chipsets have helped bring the system architecture back into balance.

The Intel P6 bus is a classic shared bus where multiple devices share the same signals. The EV6 is a switched bus (similar to how some networking devices avoid congestion), so that each device opens up a channel for communicating packets of information in a split-transaction manner. In fact, up to 24 memory transactions (versus 8 on the P6) can be in process simultaneously on the EV6 bus, providing a high degree of latency tolerance.

**"The main advantage of the EV6 bus is that it provides much higher bandwidth, since address and data transfers occur on both edges of the clock."**

The main advantage of the EV6 bus is that it provides much higher bandwidth, since address and data transfers occur on both edges of the clock (similar to the double data rate DRAM we'll talk about soon). While the bus is advertised as a 200MHz (now 266 MHz) bus, the actual clock frequency is half this number. For calculating peak bandwidth, it makes little difference. At "266 MHz", the bus can deliver over 2.1 GBs/sec versus the 1.06 GBs/sec of a P6 FSB running at 133MHz.

One of the design advantages of the EV6 bus is that the architecture uses source-synchronous signaling, sending the clock signal with the data. This "forward clock" follows the same path on the motherboard as the data, helping the designer insure that data is sampled at the precise instant that the clock signal is going high or low. The P6 bus follows the traditional convention of using a common clock for several devices, and potential timing differences make it harder to scale up in frequency.

AMD also first offered their EV6-based parts in a cartridge package (Slot A) and has migrated to a cheaper, socketed version (Socket-A, also called Socket-462) for Duron and Athlon. This article will also take a detailed look at an off-the-shelf Socket-A motherboard.

## Intel Answers with the Pentium 4

The new processor from Intel came with a brand new bus architecture, necessitating an entirely new generation of motherboards. This bus bears many similarities to the EV6. It is also a source-synchronous bus, but it can transfer 2 addresses and four 64-bit (8 byte) pieces of data during each clock cycle (called "quad-pumped"). Since the bus clock runs at 100 MHz, that's effectively a 400MHz data rate with quad-pumping, and the architecture thus allows up to 3.2 GBs/sec of peak bandwidth (400MHz x 8 bytes).

Some might be curious about how a chip can transfer data 4 times when there are only 2 edges on the bus clock. The most common approach is for each bus device to use a delay-locked loop (DLL) circuit to synchronize to the clock and vary the data sampling point (in this case, moving the edge in quarter-clock increments). The same approach is used in a forth-coming generation of Quad DRAM with twice the bandwidth of DDR memory. (Check out a later section in this article for [more info on DDR DRAM](#).)

## Chipset Architectures

Lets move beyond the CPU and analyze the other components of a modern motherboard.

It's not accidental that the motherboard components seem to only be the supporting cast for the CPU, since Intel (and to some extent, Microsoft) has taken an active role in defining the architecture for the rest of the motherboard. For each new processor generation since the 486, Intel has designed the first chipsets. Even AMD has begun to offer their own chipsets as a way to insure early support for new system and processor features, though they haven't made dramatic changes to the system partitioning used by Intel-based systems. Competing chipset companies usually differentiate by offering faster speeds, higher integration and early support for new peripherals.

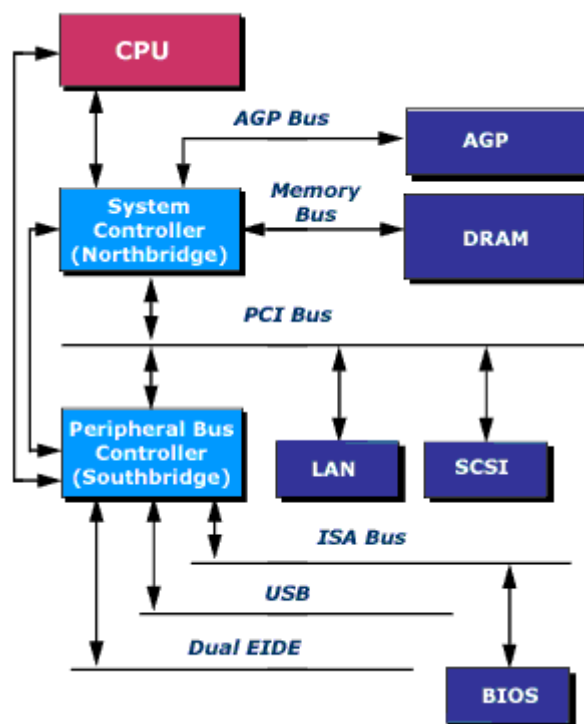


Figure 2: Top-level PC system architecture

## Chips in the North and South

Figure 2 shows the top-level system architecture for a modern desktop PC, and almost every motherboard follows this convention. The system architecture used to look much more complicated, but integration has reduced a chipset to just 2 main components--the North Bridge (NB) and the South Bridge (SB). The term "Bridge" comes from a reference to a device that connects multiple busses together. The

North/South nomenclature referred to whether a device lived above (North) or below (South) of the PCI bus on a block diagram. In the case of the North Bridge, the chip connects the front side bus [FSB] of the CPU to the DRAM bus, the AGP graphics bus, and the South Bridge. To a system designer, all the fast stuff lives in the North Bridge. The South Bridge is intended as the place to integrate all the (slower) peripherals like IDE, ISA, USB, etc.

### **Why Not Just One Chip?**

The fact that the 2 chips serve distinctly different roles is why PC designers have resisted the urge to integrate into a single chip. Since peripheral interface standards are rapidly changing, a motherboard vendor can keep the same North Bridge and upgrade just the South Bridge. It is also expensive to build a device with so many pins, especially since most chipsets are already "pad-limited". This term refers to the fact that silicon chips need to be big enough to physically attach all the bonding wires, even if the circuit design could be shrunk down further.

Some vendors plan to use this extra space inside the pad ring for integrating a Level 3 (L3) cache or a graphics processor, an integration strategy that hasn't yet proven to be cost-effective. In the last section of this article, we'll talk more about [these future trends](#).

### **Now Intel Calls them Hubs**

To add to the confusion, Intel has begun referring to their chipsets as "hubs". The North Bridge is called the Memory Controller Hub, and the South Bridge has become the I/O Controller Hub. These are admittedly more descriptive terms, but there isn't any basic difference in the function of these devices. However, one notable change is to migrate the North-to-South Bridge interface onto a dedicated, point-to-point interface. This is much better than forcing the South Bridge and its peripherals to share the PCI bus.

Even though the PCI bus has become just another South Bridge peripheral bus, we'll stick to the old North/South naming convention.

### **A Closer Look at North and South Bridges**

#### **North Bridge**

There is little functional difference between a North Bridge for the EV6 bus or the P6 bus. The function of the chip is to serve as a traffic cop for data moving between the four busses. The traffic cop must deal with a 4-way intersection where everyone wants easy access to the road that leads to DRAM. The key focus of a system designer is to efficiently handle all the requests for DRAM access. A well-designed North Bridge must balance those requests to make sure that no performance-killing bottlenecks occur.

In early chipset designs, the memory controller was very subservient to the CPU, since most data traffic was intended for this device. As we mentioned earlier, modern PC's move a lot more timing-critical media data throughout the system. The North Bridge must now allow "concurrency", meaning that each system device must appear to have dedicated access to memory.

#### **Using Buffers to Provide Concurrent Memory Access**

As an example, suppose the CPU misses in the on-chip cache and must refill the cache line from main memory. The processor cache refill can now happen concurrently with separate Direct Memory Access (DMA) transfer from a device on the South Bridge or the AGP bus. The memory isn't really accessed at the same time, since there is only a single interface from the chipset to the external memory subsystem. What the North Bridge must do is provide internal buffers to store a certain amount of data until the memory interface can transfer the data in a big, fast chunk.

Unlike the SRAM used for cache memory, DRAM memory has a huge penalty for the first access to a particular row in memory. After paying the latency tax, the DRAM memory can then stream data at full speed.

With enough buffering and some complex arbitration circuitry, a good North Bridge can provide enough concurrency to insure that the DRAM is used efficiently. As an example, in just one such buffer, the VIA KT133A North Bridge provides 16 levels (64 bits wide each) of data buffering for access from DRAM to



the PCI bus (where the South Bridge is usually connected). This particular buffer is very important for keeping data streaming to a device like an IDE hard disk.

Whether a buffer is big enough really depends on what sort of software is running on the system. Unfortunately, there isn't an easy way to fully evaluate the efficiency of a North Bridge design, except to run real-world media benchmarks, where the multiple North Bridge interfaces can be stressed concurrently.

We've already discussed the CPU interface in great detail. Let's take a look at the other 3 busses on the North Bridge:

### **The South Bridge Interface--Moving from PCI to a Point-to-Point Connection**

Using PCI to interface between the North Bridge and South Bridge is becoming a system bottleneck, since the chipset interconnect has to share a 33 MHz, 32-bit bus. Theoretically, a PCI bus can deliver a peak bandwidth of 133 MBs/sec, but average sustained throughput has been measured as low as 40 MBs/sec. The bus utilization gets better as the burst length increases. With IDE (disk drive) interfaces attempting to run at 100 MBs/sec for burst reads, the South Bridge peripherals have the ability to saturate the bus as they attempt to get to the main memory living off the North Bridge across a PCI-based South Bridge-to-North Bridge interconnect.

Recalling our earlier discussion of the need for [balance in the system design](#), it's clear that PCI can no longer carry all the South Bridge traffic in fast systems. Recognizing this trend, chipset vendors have created faster interfaces between the NB and SB. Unfortunately, there isn't yet compatibility between the various vendors, and board designers will no longer be able to select a South Bridge from a competing vendor.

Intel doesn't say much about their proprietary SB interface, referring to it as the "hub link". This is an 8-bit port, running at 66 MHz and transferring 4 bytes per clock. This gives Intel chipsets 266 MBs/sec of peak bandwidth. The bandwidth is also much better utilized than with a shared PCI connection, since Intel gathers up all the various peripheral memory requests into a linked-list of DMA transfers. The South Bridge DMA engine keeps the connection to the North Bridge memory busy with servicing all these memory requests.

AMD called their new South Bridge interface the "Lightning Data Transport (LDT)" for quite some time, and they've recently renamed it to "HyperTransport Technology". Instead of a single port, HyperTransport provides 2 channels for full-duplex operation. The interface can operate at very high clock rates, since it runs 2 wires for each signal (differential pairs).



*Advanced Micro Devices' AMD-760™ Chipset*

Said to run at over 400MHz with double data per clock, and capable of 800Mbps/sec for each pin pair, this interface can provide 800 MBs/sec for each 8-bit I/O connection (and 3.2GBs/sec each way for a 32 bit connection, for a theoretical aggregate of 6.4 GBs/sec). The reason all this sounds so vague is that AMD has yet to ship any devices using this scheme. However, AMD has licensed the technology to a number of companies who plan to incorporate it into future products. The AMD 760 DDR chipset (we'll examine later) still uses a PCI bus to get to the South Bridge.

VIA has defined their own South Bridge interface that they call "V-Link". Very similar to Intel's approach, this interface provides 266 MBs/sec of bandwidth and is available on the VT8233 South Bridge. This South Bridge currently is only paired with the Pro266 (P6) and the KT266 (AMD Athlon) North Bridges. These new chipsets were developed to support DDR memory.

### **The DRAM System Memory Interface**

There have been some lively developments in the DRAM world, and the controversy over standards has



a big impact on the North Bridge. Intel strongly promoted the Rambus memory architecture (RDRAM) for P6-class systems, since RDRAM's high-speed packet bus allows much higher bandwidth without resorting to the expense of wide memory interfaces. A single RDRAM 16-bit channel can provide up to 1600 MBs/sec (in the current desktop PC version--"PC800"), twice as much as SDRAM 64-bit memory running at 100MHz. Adding multiple RDRAM channels adds even more bandwidth. RDRAM's run at up to 400 MHz and require careful attention to signal integrity, including the use of a termination module if an RDRAM connector (RIMM) isn't populated with memory.

Because of stiff licensing fees and difficulty getting enough RDRAM volume to drive down costs, many analysts believe that the majority of desktop PC's will stay with SDRAM and migrate to DDR DRAM. Rambus may have trouble getting memory manufacturers to enthusiastically promote RDRAM, since the company has sued many of these chip suppliers for patent violations on SDRAM (and DDR). The Rambus patents apparently didn't come to light until after JEDEC (standards committee) finalized the SDRAM specification.

Right now, the Pentium 4 chipsets only support RDRAM, though Intel is working on a SDRAM version (code-named "Brookdale"). Because of their aggressive Pentium 4 ramp plan, Intel has no choice but to strongly endorse Rambus memory, and the Pentium 4 ramp alone may be enough volume to ensure price parity of RDRAM's. Acer and VIA are both working on DDR chipsets for the Pentium 4, and this will ease some of the market pressure on Intel. Rambus is developing faster memory designs, but they'll need a lot of luck (and legal peace) before they can become the long-term memory standard for desktop PC's.

For now, most chipsets support PC133 SDRAM's and provide 1.064 GB/sec of memory bandwidth from the 64-bit, 133MHz memory interface. Support for DDR DRAM doubles this to 2.1 GB/sec. The memory module naming convention for DDR can cause a great deal of confusion, since a Rambus channel uses PC600 or PC800 RIMM modules (600 or 800MHz). The Rambus naming convention refers to the "data clock" rate, so a PC800 Rambus device runs a 16-bit interface at 800MHz (400MHz double-data) to achieve 1600 MB/s of peak bandwidth. DDR DIMM's come in PC1600 and PC2100 versions, referring to the peak data rate of the entire module. This means that a single channel of PC800 RDRAM provides the same peak bandwidth as a PC1600 DDR memory system.

There is currently some controversy about whether the same motherboard should provide both SDRAM and DDR DRAM connectors. Memory vendors like Micron say it's a bad idea, since the timing is too tight to be reliable. However, the ALI and VIA DDR chipsets support this feature, but the AMD 760 is DDR only. At the time of this writing, some reviewers have noted problems with early SDRAM/DDR mixed boards.

Later, we'll take a closer look at the Asus A7M266 (Athlon 760-based) board.

### **The Accelerated Graphics Port Interface**

This point-to-point interface to the graphics subsystem rounds out the overview of the North Bridge, and most PC game enthusiasts would agree that it's an important part of the system architecture. The graphics accelerator has resided on the PCI bus, but the shared bus was becoming a system bottleneck for getting higher performance. There was also some concern by Intel and Microsoft that the graphics chips were becoming the central feature of the PC architecture, shifting the focus from the CPU and the operating system.

Some graphics cards were including nearly as much memory as the rest of the system, and there was a push toward "Media Processors" for the graphics adapter. A Media Processor is a specialized CPU that handles the demanding media tasks, reducing the need for a fast host processor. This was an ominous trend, and Intel developed the AGP interface as a way to help control the system partitioning for graphics.

As it was first envisioned, AGP would allow a graphics controller to use system memory for storing graphics texture information. The architecture would then evolve into systems with all the graphics data residing in system memory. Things haven't progressed in quite this manner, since the performance demands of modern graphics chips have skyrocketed. For new graphics chips to draw over 1 billion pixels/sec, they need fast, specialized memory dedicated to the graphics chip. For example, the nVidia

Gforce 2 Ultra uses a 128-bit, 230 MHz DDR memory, providing 7.36 GBs/sec of bandwidth.

There has been no cost-effective way for system memory to meet this performance, and the AGP interface became just a convenient way to offload graphics traffic from the PCI bus (and increase the bandwidth from the CPU to the graphics subsystem).

The situation is changing, since the AGP side of the North Bridge is now running at 4X mode. Originally designed as a 66 MHz interconnect, architecturally similar to a dedicated PCI bus, AGP performance soon scaled to allow 2 samples/clock (AGP 2X) and then 4 samples/clock (AGP 4X). With a 32-bit (4 byte) data path running at 66MHz and capable of 4 transfers per clock, the 4X interface yields 1.056 GBs/sec).

This much bandwidth to the graphics chip obviously is not balanced with a standard PC100 SDRAM memory (that transmits a max of 800MB/sec and shares the bandwidth with other devices), though PC 133 with its 1.064GB/sec rate comes closer to matching the bandwidth capability of the newest AGP 4X cards. The real benefit becomes available when matching AGP 4X with DDR or RDRAM memory systems.

Some low-cost motherboard implementations remove the graphics memory entirely and run with a "Unified Memory Architecture (UMA)". This UMA approach has been attempted using low-end graphics cores, but the 3D graphics performance was abysmal. A new generation of chipsets renames this approach "Shared Memory Architecture (SMA)" and uses better cores and DDR memory. By integrating the graphics controller into the North Bridge, the AGP bus can be entirely eliminated.

Leaving off the AGP bus may be fine for the mobile market, but most desktop customers still want the slot for upgrades. Later, we'll examine a motherboard based on Intel's 815 chipset. This chipset has both integrated graphics and an AGP port, though it only supports standard SDRAM.

#### **South Bridge: All but the Kitchen Sink**

##### **Everything but the Kitchen Sink--A Closer Look at the South Bridge**

While the North Bridge handles high-speed memory arbitration, the South Bridge connects with all the disparate peripherals and provides functions that make a PC different from any other computer system. A lot of old PC software still expects legacy devices to exist in a system, and this stuff is available through the South Bridge. Most legacy support is part of the ISA bus, an 8 MHz, 16-bit interface that has been difficult to kill. This bus dates back to the original IBM PC/AT and provides a whopping 16 MBs/sec peak bandwidth with far less sustained throughput.

##### **Death to the ISA Bus**

Most of you are quite familiar with the difficulty of migrating to Plug-and-Play with cards or onboard chips that use the ISA bus. Many new motherboards have dropped this bus entirely, but a lot of South Bridge chips still provide the bus as an option for the motherboard designer. Instead of using ISA, the South Bridge provides alternative low-cost interfaces for low-performance peripherals. These new interfaces are covered as part of the following comprehensive list of South Bridge features:

##### **PCI Bus**

Now that some South Bridge chips have a dedicated interconnection to the North Bridge (like Intel's hub link connection we described earlier), the PCI bus becomes just another peripheral bus. Getting rid of NB traffic will make PCI peripherals much more useful. It should be noted that a motherboard still has devices on the PCI bus, even if there aren't any cards in the slots. These PCI devices are integrated into the South Bridge of many chipsets, including the IDE controller, USB controller, SMBus controller, etc. Most chipsets create an internal PCI-to-PCI bridge, so that these devices don't take up resources from the main PCI bus.

##### **Low Pin Count Interface (LPC)**

One reason that the ISA bus has lasted so long is that many peripherals don't need the complexity and cost of a full PCI controller. To fill this need, Intel invented yet another bus for the South Bridge. This is a

simple 4-bit interface and is mainly used for connecting to the Super I/O chip. The Super I/O is where the really old legacy devices live, including the serial ports, parallel port, game port, PS/2 mouse/keyboard, infrared interface, and floppy disk controller. This same chip will often include pins that sample the RPM of the fans or monitor other system events. The Super I/O chip also has several general-purpose I/O pins.

### **Basic I/O System (BIOS)**

The BIOS is low-level software that controls devices on the motherboard. The processor executes the BIOS code when the PC is first booted, allowing memory testing and configuration of peripherals. By changing settings in the BIOS menu, the user can customize the operation of the motherboard, though the default BIOS settings are usually fine. Many of these settings involve complex timing adjustments to the chipset, and it's not a good idea to change them.

Most new motherboards have removed the configuration jumpers, allowing everything to be changed through BIOS software. Some motherboards have even added extra BIOS control for those overclockers who want to tweak a little more performance out of their system. Mainstream PC vendors, however, tend to shelter users from low-level device control, and prefer to hide such settings from their users. So if you are into total control of your BIOS and system tweaking, you should avoid systems from vendors like IBM (especially), Compaq, Dell, Gateway, etc. The real fun comes from buying a motherboard and putting together your own system. The ASUS board we'll review here has special circuitry and BIOS settings that allow users to increase the frequency in 1 MHz steps, making the board very popular with the overclocking crowd.

Intel calls their BIOS chip the Firmware Hub (FWH), but it is basically the BIOS running in FLASH (reprogrammable) memory. On an Intel chipset, the FWH shares pins with the LPC interface. Other sorts of simple interfaces may be used for the BIOS chip.



*click on image for full view*

### **SMBus**

This bus is a serial interface that is (mostly) compatible with the venerable i2C bus developed by Phillips. It's intended as a way to interface a simple external processor to monitor the health (voltage, temperature, etc.) of the system.

### **Universal Serial Bus (USB)**

This serial bus is designed for external devices such as mice, keyboards, scanners, cameras, etc. The data rate is relatively low (up to 12 Mbs/sec for USB 1.1), so it's not suitable for video or other high-end applications. Intel is promoting new versions of USB to compete with IEEE 1394 (Firewire) for these high-speed peripherals (we'll talk about these future technologies in the last section). The South Bridge chip will usually have one or two USB controllers, each able to manage 2 motherboard connectors. USB is designed to daisy-chain through external hubs to minimize the number of wires that must be connected to the PC.

It should be noted that non-powered USB hubs (like keyboards) are only rated for 100 mA per port, while devices like USB cameras need 500 mA to operate reliably. This limitation is just one of the reasons that motherboard vendors have been adding extra USB controllers.

### **IDE Interface**

The PC disk controller has been a rapidly-changing part of the PC system architecture, and it's unfortunately beyond the scope of this article to fully discuss this fascinating technology. The term Integrated Drive Electronics (IDE) means that most of the control for the disk drive has been integrated onto the drive's circuitry, instead of being part of the motherboard or add-in card. Meant as a low-cost alternative to SCSI (Small Computer System Interface), IDE technology has evolved to support high data rates and large-capacity drives.

To confuse the public even more, the ANSI (US standards board) designation is "Advanced Technology Attachment" (ATA). In the early to mid-90's IDE drive and interface technology was improved with the

higher capacity and faster rates of "Enhanced" IDE (EIDE) technology promoted by Western Digital and FastATA technology promoted by Seagate, which was essentially the same thing. Both provided various levels of DMA and programmed I/O data transfers.

The naming conventions have gotten a little more descriptive. If both the chipset and the drive support ATA-33, then the maximum transfer rate will be 33 MBs/sec. The actual drive mechanism of the older ATA-33 drives couldn't actually deliver that data rate, but cache memory that resides on the drive circuit board was able to take advantage of the full speed of the ATA-33 interface.

To run this interface even faster, a special 80-conductor cable is required (but note that it keeps the same 40-pin connector to plug into the drive and IDE interface on the motherboard or adapter card). This cable provides 2 wires for each signal, allowing the IDE interface to run at 66 MBs/sec (ATA-66) and 100 MBs/sec (ATA-100). The advantage of this cabling system is that the connector on the motherboard is the same for all 3 interfaces. Most chipsets support 2 IDE controllers, each supporting both a master and a slave. Systems can be expanded with PCI-based ATA expansion cards to provide even more IDE devices.

### **Audio Codec (AC) Link**

This chipset feature is designed to allow a digital connection to simple off-chip mixed signal (analog/digital) electronics for audio and telephony (modem/networking). By minimizing the amount of external circuitry, the rest of the audio/telephony function can be handled in the chipset with a combination of hardware and software. Intel created the AC Link specification to facilitate software implementations of these functions, though some power-users would prefer not to drain off CPU performance for this purpose.

The current version is AC'97 2.2, and it provides a 5-signal interface to an external codec (compression/decompression). In the case of audio, the AC Link would connect to a chip that includes a codec and digital-to-analog (D/A) converters for driving audio speakers and analog-to-digital (A/D) converters for sampling a microphone or other audio analog inputs.

For telephony, the external device also contains the physical interface (PHY) for connecting to a phone line, and AC'97 chips are becoming available for networking technologies.

As a system designer, using AC Link makes a lot of sense for cost reasons. However, there is some danger in replacing specialized hardware with software running on the host CPU. The performance may drop dramatically for high-end applications. In the case of sound chips, most computer games have multiple sound streams that must be mixed together. Often, these sound streams are sampled at different data rates, depending on the sound quality needed for each stream. The audio system must "up-sample" and "down-sample" these streams and then mix them together. This is just one example of the types of compute-intensive operations performed by a sound chip.

Another example is the processing of complex "head-related transfer functions" (HRTF) to create 3D positional audio. These functions usually require a PCI board with a DSP (Digital Signal Processor) and some local memory. Moving this processing onto the host will help sell faster CPU's, but it may not be the most efficient system design for high-end audio. (From an audio listening quality perspective, most users cannot tell the difference between a good PCI audio card and a much lower cost motherboard audio solution, assuming the same speakers are used).

Of course this more advanced audio hardware could be integrated into the South Bridge, but the trend is towards more host-based processing in system memory. If the external AC Link device is a modem, most of the processing occurs on the host. This is a direct migration of the "Soft Modem" that has become a popular way to reduce the cost of modem hardware. Eventually the host processor gets so fast that the performance loss is minimal. However, with new technologies, the move from dedicated hardware to software should be carefully considered.

### **Integrated Local Area Networking (LAN) Controller**

Networking is one such example where system designers are looking for ways to move processing off of

add-in cards and into the chipset where the CPU can have a more direct involvement. The AC Link (or AC Link + extra LAN pins) will be used for driving DSL connections, HPNA (Home Phone Networking Alliance), or even plain old Ethernet. The idea is that PC vendors will drop in special riser cards that include whichever interfaces are needed by the user.

The cost of the riser card will be less than a PCI card, since the PCI interface adds to the cost of chips. Here, again, one needs to be careful that the vendor isn't trying to cut out important hardware and move too much to the host processor.



By "hiding" a function in the chipset, it's becomes harder for the average user to evaluate the quality. It's no longer possible to just look at the part number to evaluate the quality. As an example, the integrated Ethernet core used by AMD is actually the same one AMD used for a discrete hardware implementation. It's possible to save design time by not messing with this proven core, even if they could have made the core smaller. Knowing this, you can be reasonably confident that the Ethernet won't have any performance loss or extra load on the CPU.

Partitioning networking tasks is much more complicated than we've described here. There are multiple layers to the networking "stack", and the PC host processor has always run the upper layers. This host-based processing is just moving further down the stack and getting closer to the physical interface. While this is the case in desktop systems, there is a reverse trend afoot to offload the CPU in servers, and move TCP/IP protocol processing, IPSEC, and SSL processing into network adapters - we've seen variations of this with recent network adapters from Alacritech, 3COM, and Intel. These and other technologies are also now being called "web accelerators".

The true test for any integrated function is to run benchmarks. If your graphics frame-rate drops when you switch from PCI audio to AC'97, then that's a good indication of extra work being moved to the CPU. The same would be true for running benchmarks of modem and network performance.

### **Other Functions of the South Bridge**

By describing all the interfaces on the South Bridge, we've covered most of the functions performed by this important chip. There are a lot of other PC devices in the chip, but most of them are only interesting to the software guys. These functions include DMA controllers, interrupt controllers, timers, real-time clocks, power management control, and various connections to the rest of the PC system.

### **Other Motherboard Features**

#### **Beyond the Chipset--Other Motherboard Features**

It's probably becoming fairly obvious that most of a PC's core processing logic has now been shrunk down to just a couple of chips. If a function could be integrated into the chipset, then years of PC system evolution has caused that to happen. The only motherboard components left are analog circuits, a few specialized chips, memory and connectors.

#### **VRM (Voltage Regulator Module)**

It used to be that every digital chip on a motherboard ran at the same voltage. That began to change as chip designers dropped voltage to save power or move into a more advanced semiconductor manufacturing process. The smaller transistor in an advanced process needs lower voltages; otherwise it might literally "arc" between the transistors. (This is a bad thing, adding to a long list of bad things that can happen to a chip from overclocking.) The processor has moved most quickly down this voltage curve, and now it needs a special voltage that is different from the 3.3V or 5V used by the rest of the board. New chipsets and memory are also starting to use lower voltages.

To make things even more interesting, the CPU will run faster at higher voltages and slower at higher temperatures. The power consumption goes up by the square of the voltage. This leads to more heat that must be removed by the CPU heatsink and fan. If the CPU gets too hot or runs at a voltage beyond what it was designed to handle, it can suffer permanent damage that will shorten its life.



*click on image for full view*

To walk this fine path between speed, voltage and power, Intel defined a special kind of voltage regulator for their new processors. A voltage regulator is a device that takes an input voltage of some value and outputs a stable voltage of a different value. The VRM is a programmable voltage regulator, taking a set of 5 VID (voltage identification) signals that are coded to generate a precise voltage. These VID pins are usually driven directly from the processor. This allows a processor to request a higher voltage in order to run at the advertised frequency. This is one of the ways that overclocking has happened, since processors marked with a slower speed grade will run faster if given a higher voltage. The CPU vendors have worked to combat this trick, but we'll leave the overclocking discussion for another article.

### **Clocks**

The PC motherboard has components running at several different frequencies. In system design, multiple clocks can be either asynchronous or synchronous. Two clock signals are said to be synchronous if one can be derived from the other. For instance, the FSB runs at a multiple of the internal CPU clock. As an example, a 600 MHz Pentium III would have a multiple of 6, running synchronously with the 100 MHz system bus. The PCI bus is derived from this same clock, so the PCI bus would run at 1/3 of the system clock (33 MHz).

### **Connectors**

We'll cover most of the connectors during our tour of a couple of real motherboards. Things have gotten a lot easier for connecting to a motherboard, since there are now fewer connectors and most of the critical ones are now "keyed" (and color coded) to prevent improper cable insertion. Not all of the features on a motherboard are needed for each system implementation, so you may find that several of the connectors are unused.

### **Jumpers**

Most new motherboards now offer a "jumper-less" mode where all functions are controlled through the BIOS. Often a new motherboard doesn't need to have a single jumper changed. Some motherboards allow users to disable the BIOS control and handle all settings through onboard jumpers.

### **Riser Cards**

In our discussion of AC'97, we mentioned the ability to avoid the cost of a full PCI card for audio or networking. Instead, there are a couple of competing standards for simple, low-cost cards that provide external connectors to audio devices, modems or networking. These riser cards plug into a special socket, instead of a PCI connector. From the back of the PC, it looks no different. Like many PC standards, there is a version promoted by Intel, and then there is a standard used by almost everyone else.

The Intel approach is called "Communication and Networking Riser" (CNR). We'll cover this in more detail during our case study of an Intel-built motherboard, the D815EEA. A competing riser card format is called "Advanced Communications Riser" (ACR), and there are at least 50 companies promoting this standard. The main difference is that ACR is a compatible upgrade from a previous standard (AMR), while Intel's approach is unique. This article won't try to make a value judgment about which standard is better, since it would require a long discussion (and really refers to an add-in card--not the motherboard). The main issues will be cost, performance and number of features supported on the riser card.

### **Motherboard Case Study: Intel D815EEA**

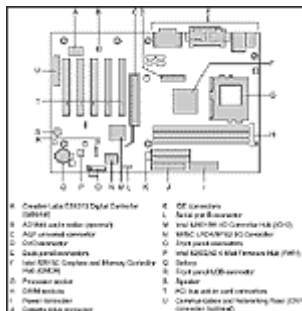
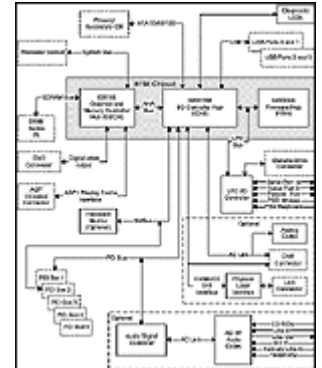
### **Case Studies of Sample Motherboards**



We've finally come to the end of our journey of motherboard technology. It's now time to apply this knowledge and take a brief look at a couple of real motherboards. Hopefully, the proceeding pages have given you an appreciation for the years of effort that have gone into bringing us to the point where such a powerful computer is contained on a single board.

### Intel D815EEA Motherboard Case Study

This motherboard was chosen for analysis because it's designed and manufactured by Intel. While it's not always true, usually Intel's technology initiatives end up on their own motherboards first. Intel is promoting various system partitioning and integration strategies, so we'll take a look at one of their newest low-end boards to see what they have in mind. We'll just hit some of the interesting highlights here. To get a full set of documentation, check out [Intel's website](#). Figure 3 shows the system block diagram for the D815EEA. It should be noted that this board isn't intended to be high-performance, so it isn't fair to make a direct comparison to the AMD board we'll examine next. Instead, the Intel board represents a low-cost, high-integration approach.



*click on image for full view*

The D815EEA is based on the 80815E chipset.

*click on image for full view*

Basically, the 'E' designation means it has a new South Bridge, the I/O Controller Hub 2 (ICH2). The ICH2 adds support for ATA-100 and a second USB controller. Since the Intel North Bridge includes a graphics controller, they refer to the chip as the "Graphics and Memory Controller Hub" (GMCH). The motherboard also has quite a few manufacturing options, mainly dealing with audio and networking. Figure 4 shows the D815EEA board layout, and Figure 5 is a picture of an actual board. We'll take a tour around the motherboard, looking at each major feature in turn:

### Processor Socket

This board supports Celeron or Pentium III processors in a variety of package technologies with different thermal characteristics. However, they all fit into the Pin Grid Array (PGA) Socket 370 connector. The socket has a small lever on the side to allow "Zero Insertion Force" (ZIF) installation of the processor. One important thing to look for on a motherboard is to make sure there is plenty of physical clearance around the processor, in case you want to put on a bigger heatsink. The bus speed depends on which processor is used. A Celeron only runs the bus at 66 MHz, while the motherboard supports Pentium III at either 100 or 133 MHz FSB (depends on the processor speed grade).



*click on image for full view*

### 82815E Graphics and Memory Controller Hub (GMCH)

This North Bridge contains most of the features we've described in this article, including the Intel Hub Link interface to the South Bridge. The chipset only supports SDRAM memory (up to PC133), so DDR-based systems will have higher performance. In describing the AGP interface, we'll talk more about the integrated graphics controller.

### 82801BA I/O Controller Hub (ICH2)

This is a very capable South Bridge chip and supports most of the modern peripherals we've discussed. The addition of a second USB controller (4 total ports) is a welcome feature. The ICH2 is obviously intended to promote host-based processing, since it supports optional AC'97 audio and CNR LAN functionality.

### 82802AB Firmware Hub (FWH)

The BIOS and some security features live in this chip.

### **SMSC LPC47M102 I/O Controller**

This is the Super I/O chip connected to the LPC bus. It includes all the standard legacy peripherals, along with fan control and monitoring pins.

### **PCI and CNR Slots**

You'll notice that there aren't any ISA slots on this motherboard, but there are 5 PCI connectors. The Intel CNR riser card would replace the 5th PCI slot. The CNR card would contain up to 2 AC'97 codecs and one LAN interface. The LAN interface on the CNR could be either an Intel 82562ET/MT Ethernet chip or an 82562EH HPNA chip (phone line networking). This motherboard could optionally have the 82562ET/MT chip on the motherboard, instead of using CNR.

For audio on CNR, Intel would probably use an Analog Devices AD1885 AC'97 codec. To Intel's credit, they admit to the CNR audio being "Basic Audio". The CNR connector is also hooked to the SMBus.

### **Memory Sockets**

There are 3 SDRAM DIMM connectors on the motherboard, supporting a total memory size from 32 MB to 512 MB. To use 133 MHz SDRAM, the FSB must support this bus speed.

### **AGP Connector**

This motherboard allows you to use either the integrated graphics controller on the 815 or to disable it by inserting a "real" AGP graphics card. AGP supports up to 4X mode, but we've learned that a 1 Gbyte/sec AGP port isn't well balanced with the 1 Gbyte/sec maximum bandwidth shared SDRAM system. It's unlikely that someone would buy this motherboard if they really wanted optimal AGP bandwidth. They would instead opt for a DDR or RDRAM system.

If all you're looking for is basic graphics/video performance, then you can just use the onboard graphics that is routed to a VGA connector on the back panel. To get better performance, the motherboard allows for a low-cost card to be inserted into the AGP connector. In a marketing move that is a dyslexic scramble of an accepted acronym, Intel decided to call this stripped-down AGP card a Graphics Performance Accelerator (GPA). (Why does Intel keep renaming things?) While the UMA/SMA architecture uses system memory for storing 3D textures, the 815 chipset can directly control a separate bank of memory that is located on the AGP/GPA card. This memory is organized as a 4 MB cache that acts as a high-speed buffer for graphics data stored in the system memory. For applications that don't need great 3D performance, this approach may be adequate.

### **Optional Audio Chips**

The motherboard may have a couple of empty chip spots on the board, unless you order the version that includes the higher-performance onboard audio. The motherboard supports a Creative Labs ES1373 sound chip. This is a capable chip and directly interfaces to its own AC'97 codec, the Crystal Semiconductor CS4297. The Creative Labs chip is connected to the PCI bus, and the outputs of the codec are wired to connectors on the back panel.

### **Digital Video Out (DVO) Connector**

This connector is from the 815's integrated graphics and would be connected to a video add-in card for output to a TV or digital display.

### **IDE and Floppy Connectors**

This motherboard has 2 IDE controllers, allowing up to 4 devices. As we mentioned earlier, to support ATA-66 and ATA-100, a special 80 conductor cable is needed. The floppy disk connector continues to be a standard part of all motherboards.

### **Onboard Speaker and Battery**

Instead of needing to cable to a speaker in the case, the motherboard has a small speaker mounted onboard. It also has a small battery for safekeeping the motherboard configuration and clock memory.

### Front Panel Connectors

Normally, the front panel is just a way to drive some indicator lights from the motherboard. However, the best place to put the 2 extra USB ports is on the front panel. There is a connector on the motherboard for attaching to the second USB controller. The motherboard also allows the Serial Port B to be used for a front panel infrared (IR) device. The IR port runs at 115 Kbits/sec for a distance of 1 meter.

### Rear Panel Connectors

The nice thing about ATX motherboards is there are fewer cables needed for connecting to the rear panel. Most connectors are attached to the motherboard, including the PS/2 mouse and keyboard, the 2 USB ports, the parallel port, and at least one serial port. This motherboard has a few extras. Unless you have a separate graphics card in the AGP slot, the integrated graphics is driven through a VGA connector on the back panel. The back panel can also have an RJ-45 LAN connector that is driven by the optional onboard LAN chip (if CNR LAN is not used). Similarly, if the onboard sound chips are installed, the audio input and output connectors are available on the back panel, as well as a MIDI/game port. The back panel also has 4 LED's that turn amber and green to indicate diagnostic information.

### Other Connectors

There are several miscellaneous connectors for attaching to fans, CDROM audio, chassis intrusion detection, front-panel LED's and front-panel switches.

### Jumpers

Unlike many motherboards, this Intel board just has a couple of jumpers. The main jumper is J7C1 and is mainly used in case the BIOS becomes corrupt and needs to be restored.

### Power Supply

The Voltage Regulator Module was discussed in an earlier section, and this motherboard has the VRM and several analog components (capacitors, resistors, etc.) for insuring that the chips receive clean power.

### Overall Conclusions About the D815EEA

This motherboard will likely find its way into systems built by cost-conscious PC manufacturers. With the integrated graphics and optional low-end audio, modem, and LAN, this would make a good basic system. The configuration is probably more tailored for a business customer or home user who doesn't need extra performance for running entertainment software.

### Motherboard Case Study: Asus A7M266

#### Asus A7M266 Motherboard Case Study

The other motherboard we'll examine is designed to support AMD Athlon and Duron processors. We chose this board for analysis because it is intended for higher-end applications and power-users. This is partly because of the support for DDR memory, but also because of the extra Asus features to support overclocking. Since the A7M266 is based on a combination AMD/VIA chipset, it makes a nice contrast to the Intel 815-based motherboard. We won't go through an exhaustive list of features like we did for the Intel board, but there are some interesting differences that highlight concepts we've covered in this article. The board supports all of the newest features, such as AGP 4X, ATA-100, and 4 USB ports. Figure 6 shows the layout of this board.



#### Support for AMD Socket A Processor, 266 MHz FSB and a Big Heatsink

In the photograph in Figure 7, notice the extra clearance around the processor socket. The cylindrical components are capacitors and help remove noise from the power supply signals. On the Asus board, the tall capacitors are located far enough away from the processor socket to allow an oversized heatsink and fan. The overclockers love this, since a cooler CPU tends to run faster than the rated speed (which assumes worst-case temperature). To help with thermal management, the Asus board has a temperature sensor located under the processor socket. This sensor is used to report the CPU temperature to the BIOS.

[click on image for full view](#)

### **Special Asus Chip for Hardware Monitoring**

One unique feature of most Asus boards is the Application Specific Integrated Circuit (ASIC) that Asus designed to monitor motherboard temperatures, voltages and fan speeds. Asus includes software that helps a user monitor these parameters. The BIOS could also be configured to bring up a warning message if any parameters get outside a user-defined tolerance.

### **AMD 760 North Bridge with a VIA VT82C686B South Bridge**

Since the AMD 760 uses a PCI South Bridge connection, Asus was able to use a well-known VIA chip for the South Bridge. Each motherboard must have a special version of the BIOS customized for the features of the board. As this article has shown, most of the features live in the South Bridge. Using the VIA South Bridge instead of the new AMD South Bridge probably helped Asus simplify the task of porting the BIOS. As we've learned, there is a potential system bottleneck between the NB and SB, since the AMD chipset relies on PCI and doesn't support a faster interconnect mechanism.

### **BIOS Allows 1 MHz Frequency Increments**

If the Athlon/Duron processor has been modified to allow overclocking, then the Asus motherboard allows the FSB frequency to be adjusted in 1 MHz steps. Recall that the processor internal frequency is a multiple of the bus frequency. As an example, a 1.1 GHz Athlon would have an 11X multiplier and a 100 MHz bus. The fine granularity of the Asus frequency control may allow a stable configuration that gets a few more MHz of performance, though we urge caution. The Asus board also has a full set of jumpers, in case a user would prefer not to use the BIOS. However, jumper control of the bus frequency is much more limited than is possible using the BIOS.

### **Audio Modem Riser (AMR) Allows Low-Cost Audio or Modem**

The 5th PCI slot is shared with a connector for AMR, similar to the way the Intel board used CNR for optional low-cost audio and telephony peripherals. As we described earlier, the new ACR (Advanced Communications Riser) card standard is a compatible upgrade of the older AMR connection used on this Asus board. For most users of this motherboard, it doesn't really matter. Since this is a higher-end motherboard, most users will opt for the better performance of PCI audio cards. It's also likely that home or business users won't need an analog modem for day-to-day communication needs, since they usually connect to a LAN or a broadband Internet device (DSL or cable modem). But it's still a good idea to equip desktop systems with analog modems for emergency communication purposes.. The Asus card supports an optional 3Com Ethernet chip on the motherboard.

### **Overall Conclusions About the A7M266**

The only obvious architectural drawback of this board is the lack of a high-speed port between the North and South Bridge chips. This would only be a bottleneck if several high-speed peripherals were connected to the South Bridge. By using DDR memory and a fast AGP 4X graphics card, this motherboard appears to be well-suited to high-performance entertainment software. Check out the full reviews of the Asus board (and the Intel board) in the Motherboard Roundup.

### **The Future of Motherboards**

#### **The Future for Motherboards**

It's a great time to be a computer technology enthusiast, since everything has gotten faster, cheaper, and easier to use. But where is all this going? What will happen to the general-purpose, personal computer in a world of "Information Appliances" where everything is becoming more specialized?

#### **Death of the Motherboard**

Earlier, we stated that the motherboard chipset has been shrunk down to just 2 main chips, and it is difficult to integrate much further. This won't last. New products will integrate the CPU, graphics, and the entire chipset. Often called "System on a Chip (SOC)", these new devices represent the next-to-last phase of digital integration. They still can't integrate enough memory yet, so there will continue to be external DRAM chips (and BIOS). Many of the analog functions for audio, video, and networking may also become integrated into the chipset in a process called "mixed signal" design, though there will always be some external power supply electronics. So far, these SOC devices are meant for low-end applications like Web Pads, Personal Digital Assistants (PDA's), or other smart "Information Appliances". However, this approach represents the eventual endpoint for PC integration.

It will soon be possible to build a low-end PC that uses a single integrated chip. In the semiconductor world, the big question is "Who will sell the chip?" Will it be the CPU companies, the chipset companies, the graphics companies, or even the memory companies? Those labels may no longer be appropriate in an SOC world.

**"For the low-end PC we've described, the motherboard no longer exists in a form that is meaningful to a hobbyist."**

What will the general-purpose PC look like? The box will probably be sealed and allow expansion by plugging components into something like "Device Bay" on the chassis. Device Bay is one of the standards for a connector that contains USB and Firewire, allowing peripherals like hard drives, network adapters, TV tuners, and etc. to be inserted or removed while the machine is running (hot-swapped). This is very similar to the PC-Cards used by laptops, and in some ways a sealed-box PC is like hooking a laptop to a monitor, keyboard and mouse.

For the low-end PC we've described, the motherboard no longer exists in a form that is meaningful to a hobbyist. Hopefully, there will be several vendors providing the integrated chips, and we can apply our system knowledge to evaluating the choices.

### **Innovation Won't Stop, and Motherboards will Never Die**

Fortunately, the features that have made PC's so popular will never go away. Some people can live with a specialized appliance, and a lot of the PC market may shift to other products. However, many of us still want to have our own computer. With a general-purpose machine, we can make it act like any of those other products. The highest performance and newest software is likely to always be introduced first on the PC. The rapid proliferation of features shows no sign of slowing, and integrated chips will probably always be at least one generation behind multiple chips on a motherboard (assuming fast bus technology like HyperTransport). For power users, the motherboard is here to stay.

### **Some New Technologies Coming to Motherboards**

There are many new technologies coming for the PC, making everything faster and easier to use. The new CPU's will demand faster memory and busses. While there are other technologies with innovative approaches, the likely market winners will bring direct upgrades to existing technology. Close on the heels of DDR DRAM is a natural evolution to Quad-Rate DRAM, pumping data out 4 times on each clock. Intel is promoting USB 2.0, allowing 480 Mbit devices while still supporting the existing USB peripherals. The PCI bus is evolving into PCI-X, providing over 1 GB/sec of bandwidth.

Most of these new technologies will first be applied to server architectures, so they'll be well-proven before they make it into mainstream motherboards. One technology that has been around a long time is multiprocessing. We didn't spend any time discussing this, since it hasn't been very useful to the desktop PC. This is only because most software hasn't taken effective advantage of multiple CPU's, but this will change as Microsoft releases Windows XP. This new MS operating system is built on the Windows 2000/NT kernel and will support multiple processors in the Professional version.

### **We've Barely Scratched the Surface of PC Technology**

We started this discussion by reminding our readers just how much fun it is to put together a new PC. Even if you buy a complete system, it's still nice to open it up and tinker around with the insides every once in awhile. Hopefully, this article has provided some background information and the confidence to personalize your computer for your own needs. Since there are so many parts of a PC motherboard, we weren't able to go into much detail in any specific area. However, there are many resources available on this Website for learning more about this fascinating technology. Let those other people sand furniture, glue plastic airplane parts or rebuild a carburetor. For us PC technology enthusiasts, our hobby is constantly changing, and that's what makes it so great!