Chapter 9

8086/8088 Hardware Specifications

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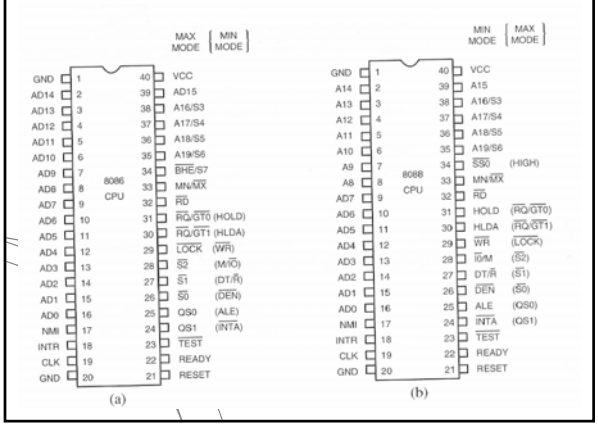
The 8086/8088

- Although these microprocessors are fairly old, they still are a good way to introduce the Intel family of microprocessors.
- Both machines are 16-bit microprocessors. The 8088 has an 8-bit data bus and the 8086 has a 16-bit data bus.
- Still used in embedded systems (cost is less than $1.



Pin Characteristics

- Input pins are TTL compatible and require only ±10µA of current.
- Output pins are also TTL compatible, but have a reduced logic zero drive current of 2.0 µA and a reduced logic 1 voltage level yielding a noise immunity of 350 mV.

Buses

- Data bus signals are D0-D7 for the 8088 and D0-D15 for the 8086.
- Address bus signals are A0-A19 for 1M byte of addressable memory space.
- The address and data pins are multiplexed as AD0-AD7 (8088) or AD0-AD15 (8086).
- The ALE signal is used to demultiplex the address/data bus and also the address/status bus.

RD

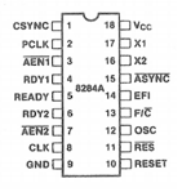
Main Control Signals

- The read signal ($\overline{RD}$) causes a read operation and the write ($\overline{WR}$) signal causes a write.
- The address bus contains wither a memory address or an I/O address. The IO/#M signal indicates the type of address on the address bus. If IO/#M = 0 the address is a memory address.
- The RESET input resets the microprocessor and causes the program to start executing at address FFFF0H. (16 bytes from the top of memory).

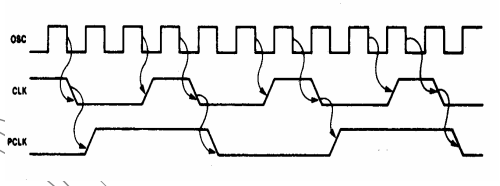
System Clock

- Time base for synchronization of internal and external operations is provided by *clock* (CLK) input signal.
- 8088 operates at 5MHz and 8MHz.
- 8086 at 5MHz, 8MHz, and 10MHz.
- 8284 clock generator and driver IC generates CLK.

Reset Circuit

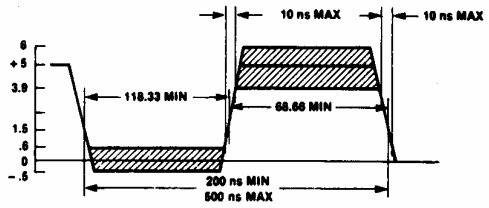


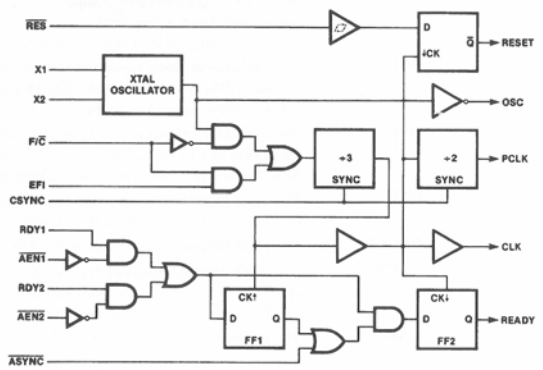
Relationship Between CLK and PCLK

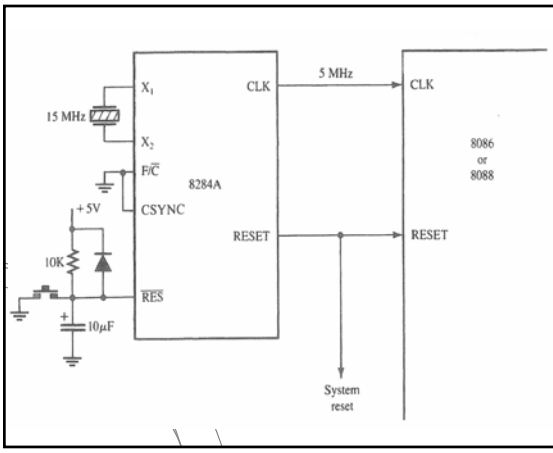


Example: If a 10MHZ 8086 MPU is to be driven by a 9MHz signal, want frequency crystal must be attached to the 8284?

CLK Waveform

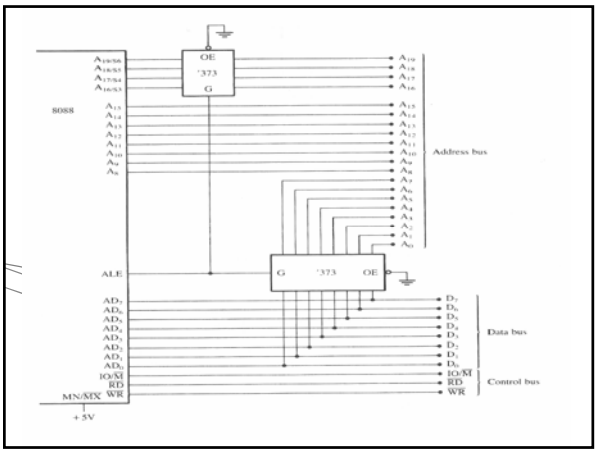


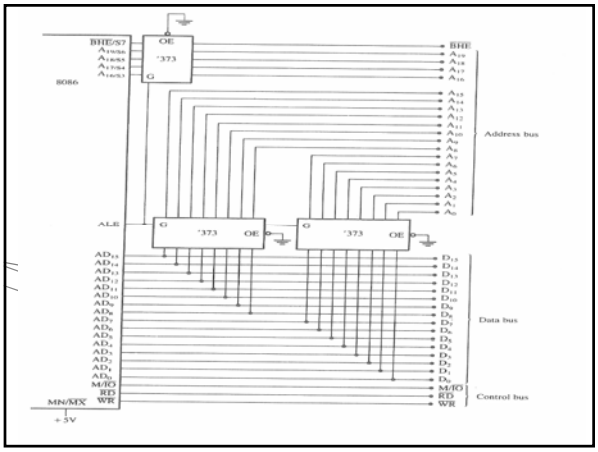




Demultiplex

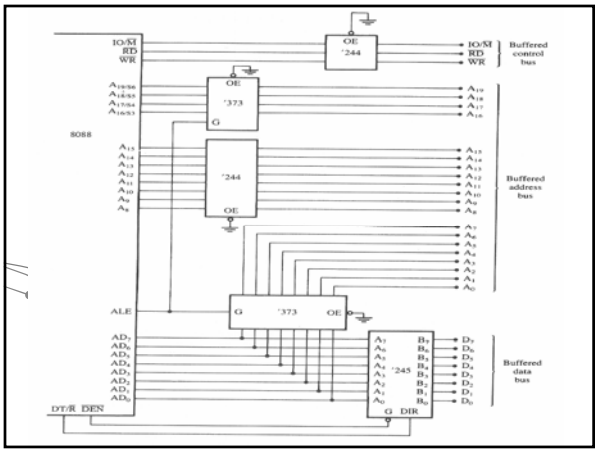
- The address/data and address/status buses are multiplexed to reduce the pin count. These buses must be demultiplexed to obtain all the signals for the system.
- The ALE signal from the microprocessor is used as a clock to a latch that demultiplexes the buses.

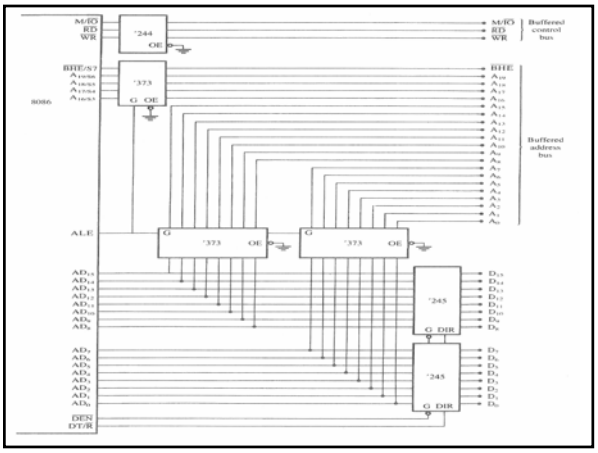




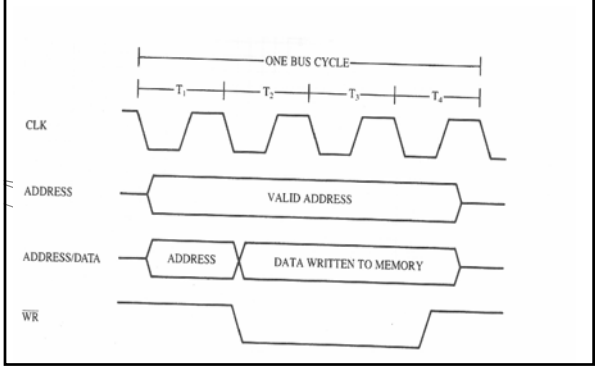
Buffering

- Since the microprocessor provides minimum drive current buffering is often needed.
- Address and control signal buffering is often accomplished with the 74ALS244.
- Data bus buffering of often accomplished with the 74ALS245 bidirectional bus buffer.

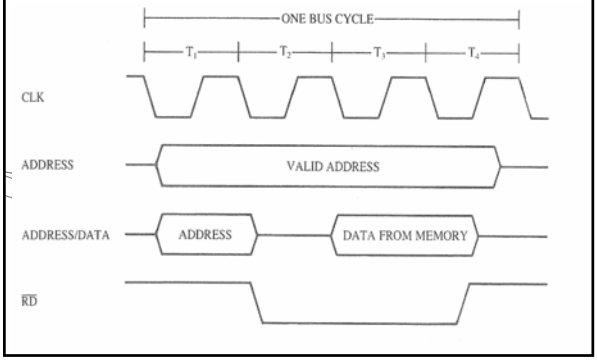


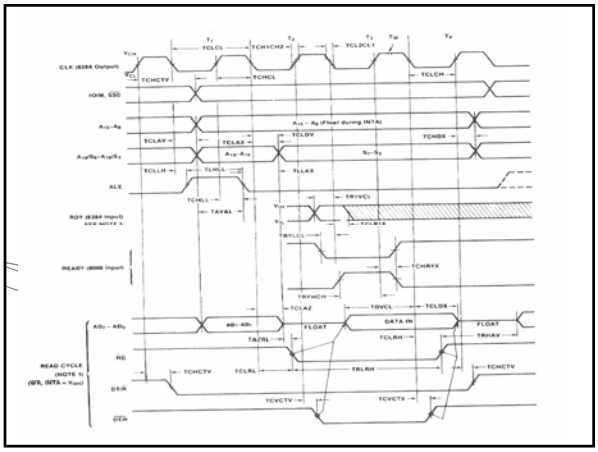


Write Timing



Read Timing

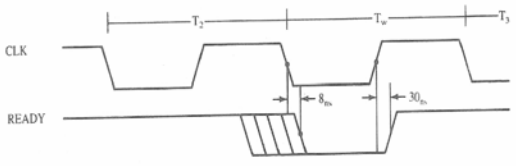




READY and Wait State

- If the memory or I/O device is too slow to connect directly to the microprocessor wait states are inserted into the timing with the READY signal.
- Wait states are additional clock pulses that length the access time allowed the memory or I/O.
- The READY signal is sampled by the microprocessor at the end of T2 and again in the middle of each wait state.

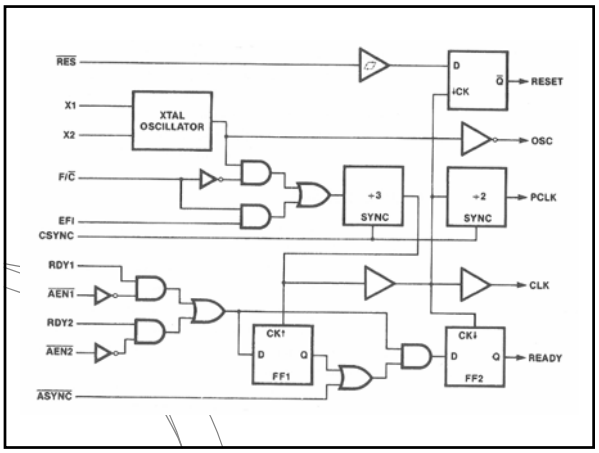
Ready Timing

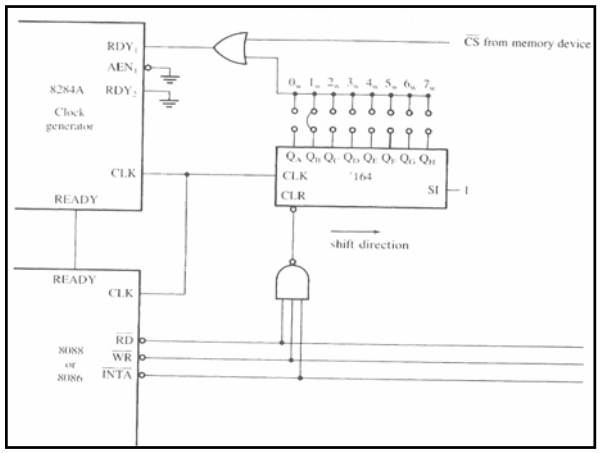


Example: What is the duration of the bus cycle in the 8088-based microcomputer if the clock is 8MHz and two wait states are inserted?

Access Time

- The amount of access time allowed the memory is 3 clocking periods minus the address setup time minus the data setup time.
- Tacc = 3 Clks – Tclav – Tdvcl





Minimum-Mode and Maximum-Mode Systems

- 8088/8086 can be configured in either of two modes: *minimum mode* and *maximum mode*.
- Minimum mode is selected by setting MN/$\overline{MX}$ input lead to logic 1.
- Minimum mode systems are typically smaller and contain a single microprocessor.
- Maximum mode systems are larger systems and with multiple processors.

Minimum-Mode and Maximum-Mode Systems

Common signals

Name	Function	Type
AD7–AD0	Address/data bus	Bidirectional, 3-state
A15–A8	Address bus	Output, 3-state
A19/S6–A16/S3	Address/status	Output, 3-state
MN/$\overline{MX}$	Minimum/maximum Mode control	Input
$\overline{RD}$	Read control	Output, 3-state
$\overline{TEST}$	Wait on test control	Input
READY	Wait state control	Input
RESET	System reset	Input
NMI	Nonmaskable interrupt request	Input
INTR	Interrupt request	Input
CLK	System clock	Input
V_{CC}	+5 V	Input
GND	Ground	

(a)

Minimum mode signals (MN/$\overline{MX}$ = V_{CC})

Name	Function	Type
HOLD	Hold request	Input
HLDA	Hold acknowledge	Output
$\overline{WR}$	Write control	Output, 3-state
IO/$\overline{M}$	IO/memory control	Output, 3-state
DT/$\overline{R}$	Data transmit/receive	Output, 3-state
$\overline{DEN}$	Data enable	Output, 3-state
$\overline{SSO}$	Status line	Output, 3-state
ALE	Address latch enable	Output
$\overline{INTA}$	Interrupt acknowledge	Output

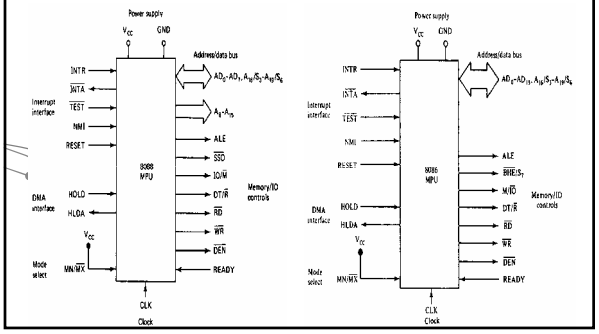
(b)

Maximum mode signals (MN/$\overline{MX}$ = GND)

Name	Function	Type
$\overline{RQ}/\overline{GT1}$, 0	Request/grant bus access control	Bidirectional
$\overline{LOCK}$	Bus priority lock control	Output, 3-state
$\overline{S2}$–$\overline{S0}$	Bus cycle status	Output, 3-state
QS1, QS0	Instruction queue status	Output

(c)

Minimum-Mode Interface Signals



Minimum-Mode Interface Signals

- Minimum-mode signals can be divided into the following basic groups: *address/data bus*, *status*, *control*, *interrupt*, and *DMA*.

Address/Data Bus

- Address bus: A0 – A19 for memory and A0 – A15 for I/O ports. A0 for LSB.
- Data bus: D0 – D7 for data. D0 for LSB.
- 8086: D0 – D15 for data.
- When acting as data bus, they carry read/write data for memory, input/output data for I/O devices, and interrupt-type codes from an interrupt controller.

Status Signals

- Status signals S6 – S3 are multiplexed with A19 – A16.
- S4 and S3 identify which of the internal segment registers was used to generate the physical address.
- S5 – logic of the internal interrupt enable flag.
- S6 – always at 0

S_4	S_3	Address Status
0	0	Alternate (relative to the ES segment)
0	1	Stack (relative to the SS segment)
1	0	Code/None (relative to the CS segment or a default of zero)
1	1	Data (relative to the DS segment)

Control Signals

- *Control signals* are to support memory and I/O interfaces.
- They control which type of bus cycle is in progress and in which direction data are to be transferred over the bus.

Interrupt Signals

- Interrupt request
- Interrupt acknowledge
- Test input – synchronize the operation of MPU to an event in external hardware.
- Nonmaskable interrupt (NMI) and reset (RESET).

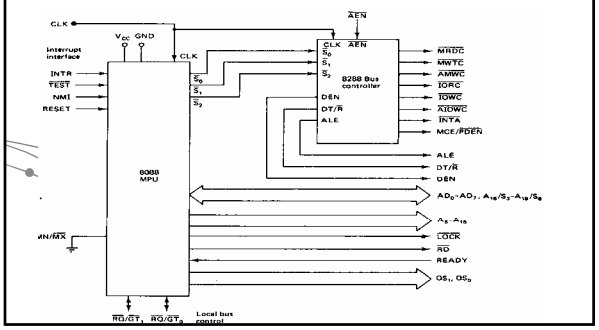
DMA Interface Signals

- Direct memory access (DMA) interface of 8088/8086 minimum-mode microcomputer system consists of the HOLD and HLDA signals.

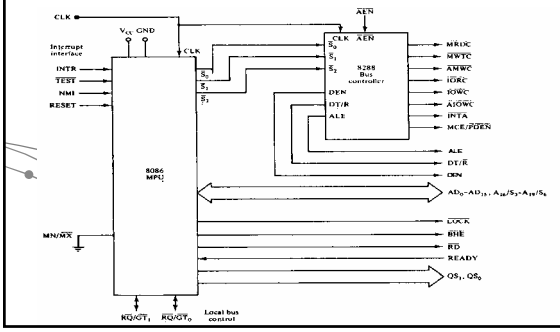
Maximum-Mode Interface Signals

- When in maximum mode, 8088/8086 produce signals for implementing a *multiprocessor*/*coprocessor system environment*.
- Common resources for all processors are called *global resources*.
- *Local* or *private resources* are assigned to specific processors.

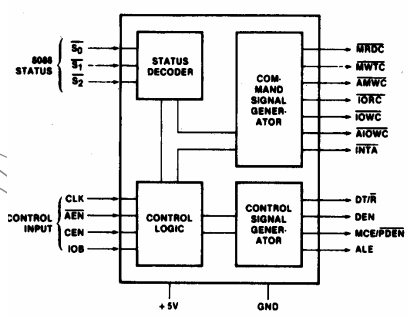
8288 Bus Controller: Bus Commands and Control Signals



8288 Bus Controller: Bus Commands and Control Signals



8288 Bus Controller: Block Diagram



8288 Bus Controller: Bus Status Codes

Status Inputs			CPU Cycle	8288 Command
$\overline{S2}$	$\overline{S1}$	$\overline{S0}$		
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Instruction Fetch	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

- Output signals: *interrupt acknowledge*, *I/O read command*, *I/O write command*, *advanced I/O write command*, *memory read command*, *memory write command*, *advanced memory write command*.

Maximum-Mode Interface Signals

- Lock signal – lock other processors.
- Queue status signals: QS0 and QS1.

QS1	QS0	Queue Status
0 (low)	0	No Operation. During the last clock cycle, nothing was taken from the queue.
0	1	First Byte. The byte taken from the queue was the first byte of the instruction.
1 (high)	0	Queue Empty. The queue has been reinitialized as a result of the execution of a transfer instruction.
1	1	Subsequent Byte. The byte taken from the queue was a subsequent byte of the instruction.

- Local bus control signals: *request/grant lines*.