CS201P
Assignment 7
Cache Simulator

1. Number of cache misses recorded-

   For cache block size 16 bits:

Size	Direct	FIFO 4-way	LRU 4-way
1024	1012176	1012176	1012176
2048	1012176	1012175	1012175
4096	1012175	1012174	1012174
8192	1012175	1012174	1012174

   For cache block size 32 bits:

Size	Direct	FIFO 4-way	LRU 4-way
1024	1012176	1012176	1012176
2048	1012176	1012176	1012176
4096	1012175	1012174	1012174
8192	1012173	1012174	1012174

   Miss ratios are-

   For cache block size 16 bits:

Size	Direct	FIFO 4-way	LRU 4-way
1024	1.000000	1.000000	1.000000
2048	1.000000	0.999999	0.999999
4096	0.999999	0.999998	0.999998
8192	0.999999	0.999998	0.999998

For cache block size 32 bits:

Size	Direct	FIFO 4-way	LRU 4-way
1024	1.000000	1.000000	1.000000
2048	1.000000	1.000000	1.000000
4096	0.999999	0.999998	0.999998
8192	0.999997	0.999998	0.999998

2. The cache details of my laptops are as follows. Used the command ‘sudo dmidecode -t cache’ for these.

Details/Cache	Size (in kB)	Type
L1-d	128	8-way Set-associative
L1-i	128	8-way Set-associative
L2	1024	4-way Set-associative
L3	6144	12-way Set-associative