Lecture 9: FPGAs vs. ASICs

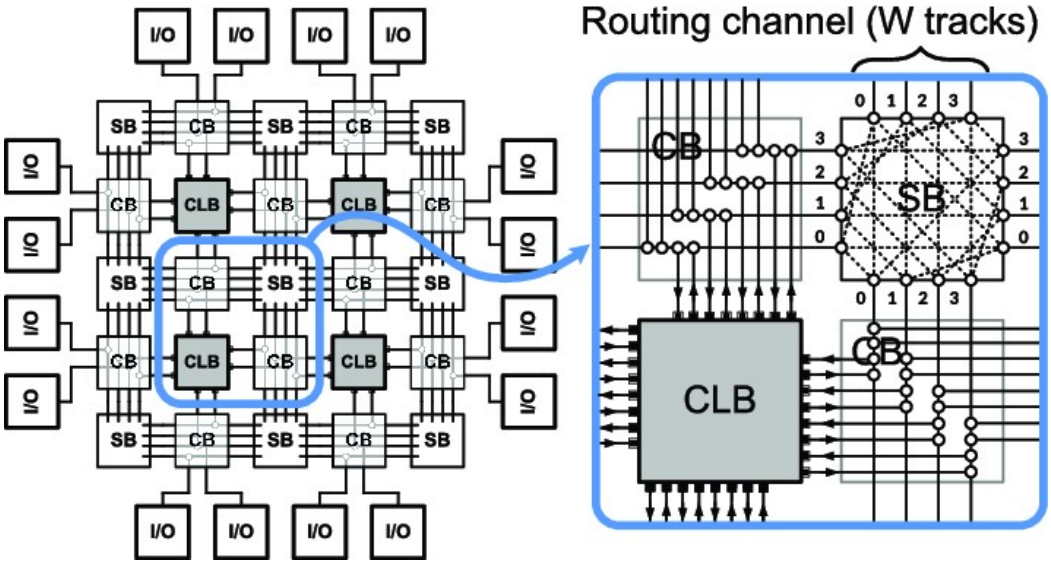
UC San Diego
JACOBS SCHOOL OF ENGINEERING
Electrical and Computer Engineering

Spectrum of Design Choices

Fast, Inflexible	**Choices**
Full Custom	Polygons
ASIC	Standard Cells (LTE Modem)
FPGA	Logic Network (Intel/Altera, Xilinx)
Specialized Processor	Program (e.g., GPUs)
GP Processor	Program (e.g., Intel x86, ARM)
Slow, Flexible	

General FPGA Layout

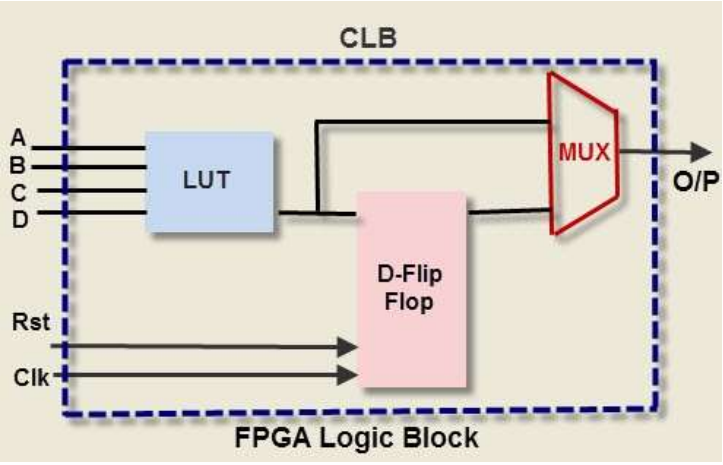
- "Wires" (Routing) implemented by programming connectivity boxes (CBs) and switch boxes (SB)



- "Logic gates" implemented by programming configurable logic blocks (CLBs)
- Modern FPGAs have more than 1 million equivalent logic gates

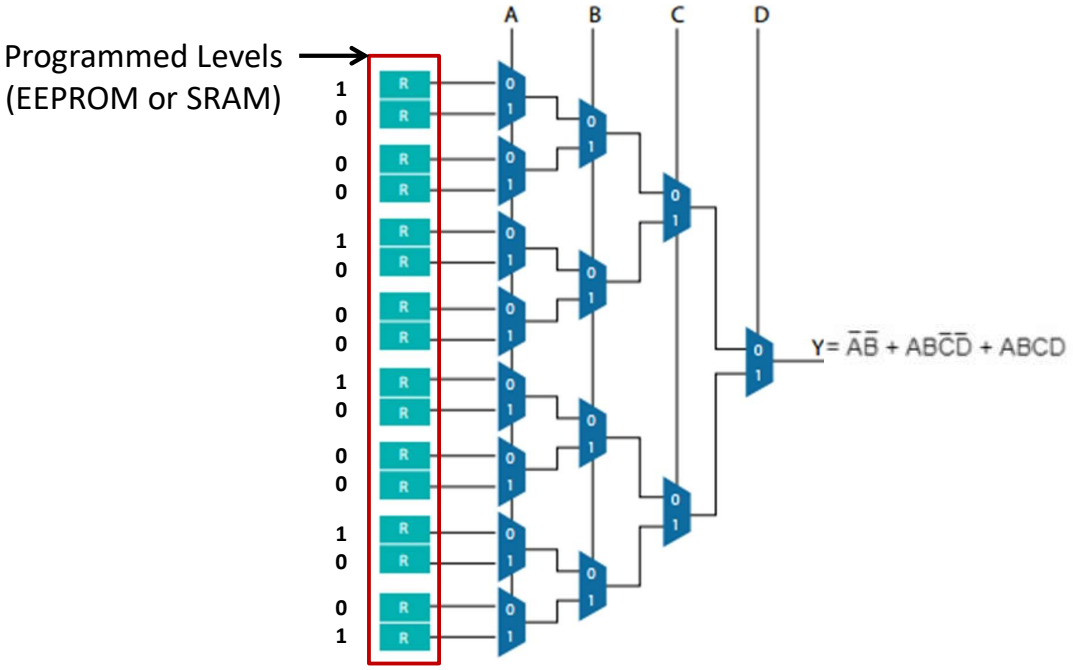
Configurable Logic Blocks

- Basic CLB comprises "Lookup Table" (LUT) and D-Flip Flop
- The MUX allows selection of either the LUT output or the D-FF output



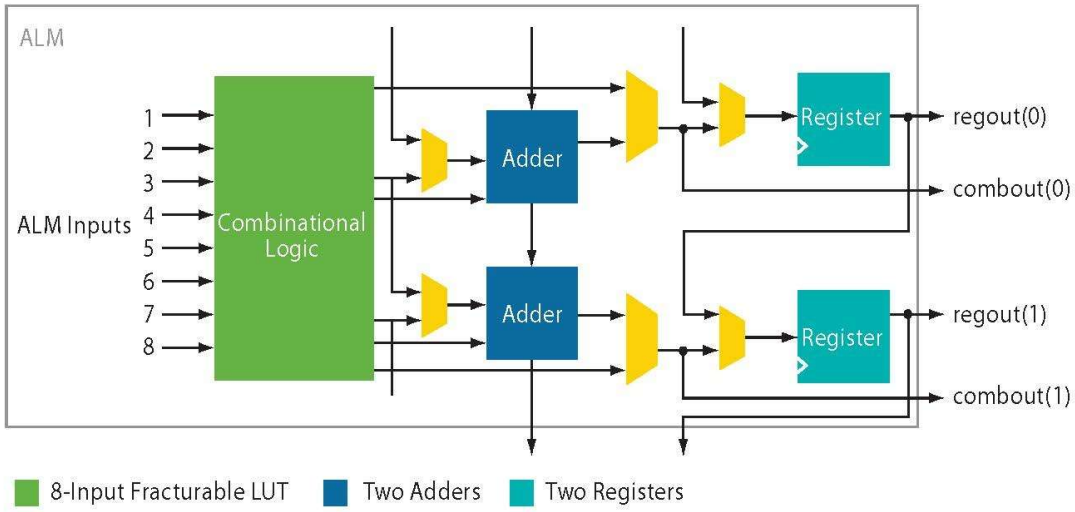
Lookup Tables (LUTs)

- Combinational functions created with programmed "tables" connected to cascaded multiplexers
- LUT inputs are MUX select lines



Intel Stratix II FPGA Architecture

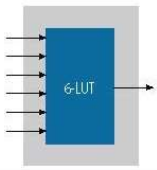
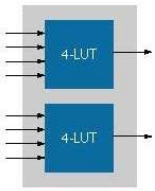
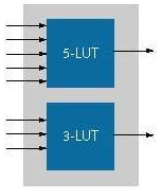
- The basic "Adaptive Logic Module (ALM) Block Diagram"



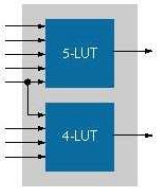
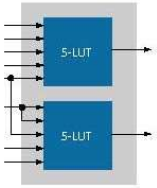
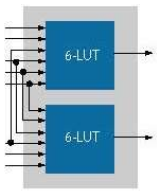
- Note the fast adder carry chain (does not require going out to programmable switch boxes)

ALM Flexibility

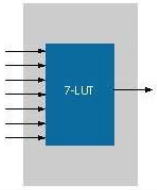
- Each ALM can be configured to one or two logic functions

	One Stratix II ALM can input any 6-input function.
	One Stratix II ALM can be configured to implement 2 independent 4-input or smaller LUTs. This configuration can be viewed as the "backward-compatibility" mode. Designs that are optimized for the traditional 4-LUT FPGAs can easily be migrated to the Stratix II family.
	One Stratix II ALM can be configured to implement a 5-LUT and 3-LUT. The inputs to the two LUTs are independent of each other. The 3-LUT can be used to implement any logic function that has 3 or fewer inputs. Therefore, a 5-LUT/2-LUT combination is also available.

ALM Flexibility

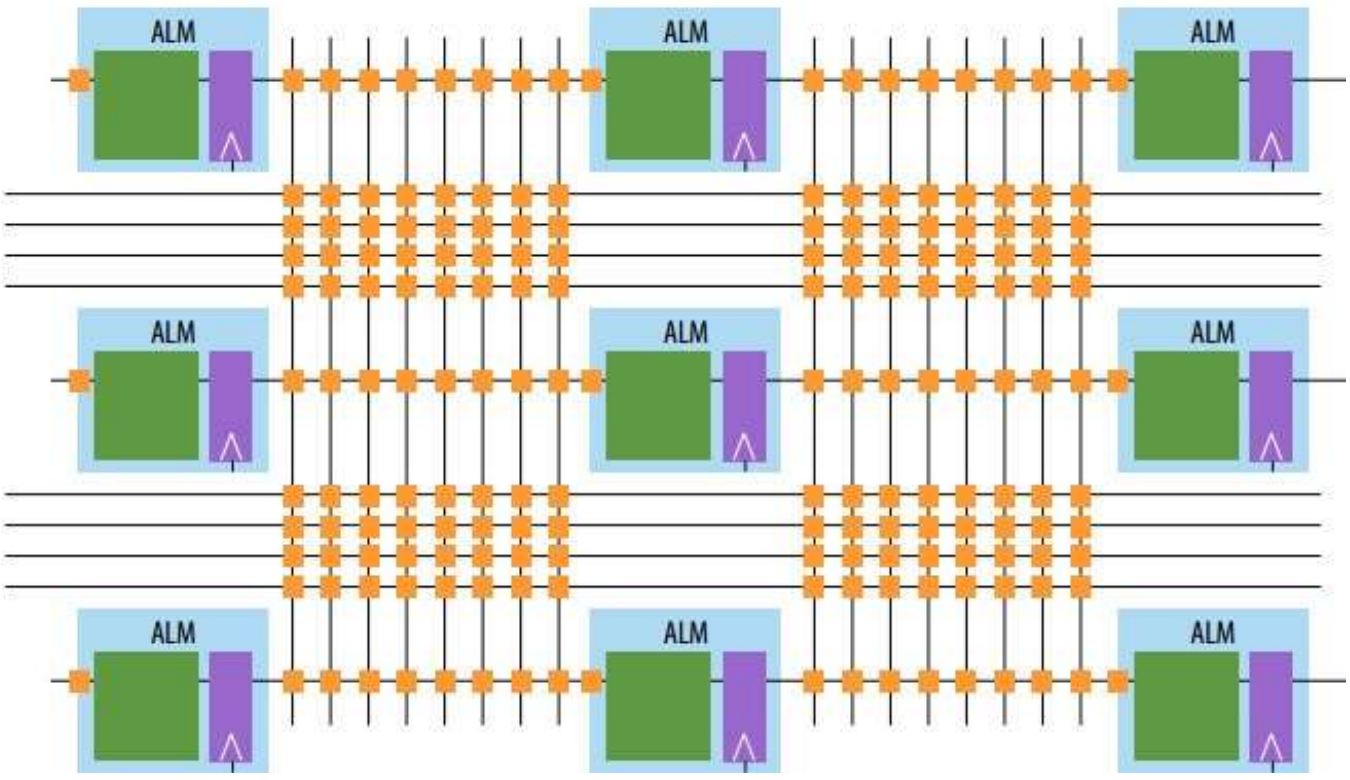
	One Stratix II ALM can be configured to implement a 5-LUT and a 4-LUT. One of the inputs is shared between the 2 LUTs. The 5-LUT has up to 4 independent inputs. The 4-LUT has up to 3 independent inputs. The sharing of inputs between LUTs is very common in FPGA designs, and the Quartus® II software automatically seeks logic functions that are structured in this manner.
	One Stratix II ALM can be configured to implement two 5-LUTs. Two of the inputs between the LUTs are common, and up to 3 independent inputs are allowed for each 5-LUT.
	If two 6-input functions have the same logic operation and 4 shared inputs, the two 6-input functions can be implemented in one Stratix II ALM. For example, a 4x2 crossbar switch with 4 data input lines and 2 sets of unique select signals requires four LEs in the Stratix family. In the Stratix II family, this function only requires one ALM. Another example is a 6-input AND gate. An ALM can implement two 6-input AND gates that have 4 common inputs. The same function would require 3 LEs if implemented in a Stratix device.

ALM Flexibility



One Stratix II ALM in the extended mode can implement a subset of a 7-variable function. The Quartus II sofware automatically recognizes the applicable 7-input function and fits it into an ALM. Refer to the *Stratix II Device Handbook* for detailed information about the types of 7-input functions that can be implemented in an ALM.

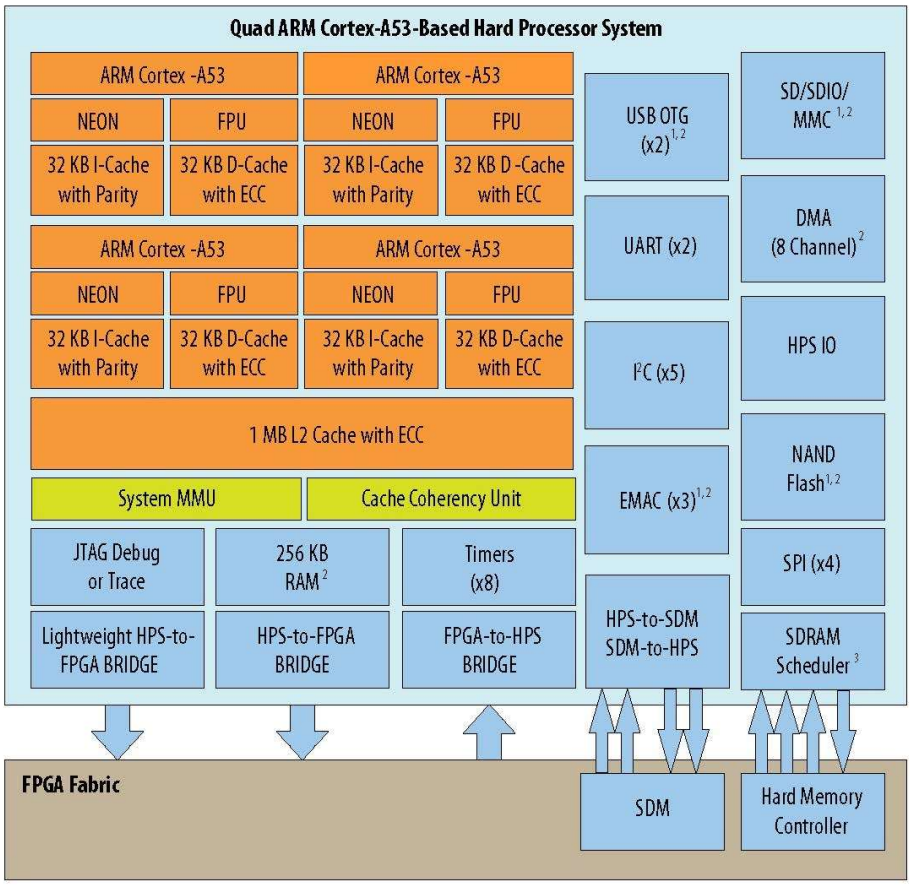
Connectivity Between ALMs



Latest Stratix 10

- Intel Stratix 10 GX 5500/SX 5500 FPGAs implemented in **14 nm** process
- Contains 1,867,680 ALMs, which can implement roughly **5,510,000** logic elements (logic gates).
- Contains **7,470,720** ALM registers
- Also contains **Quad ARM Cortex-A53** CPU cores

Integrated Quad ARM Cores

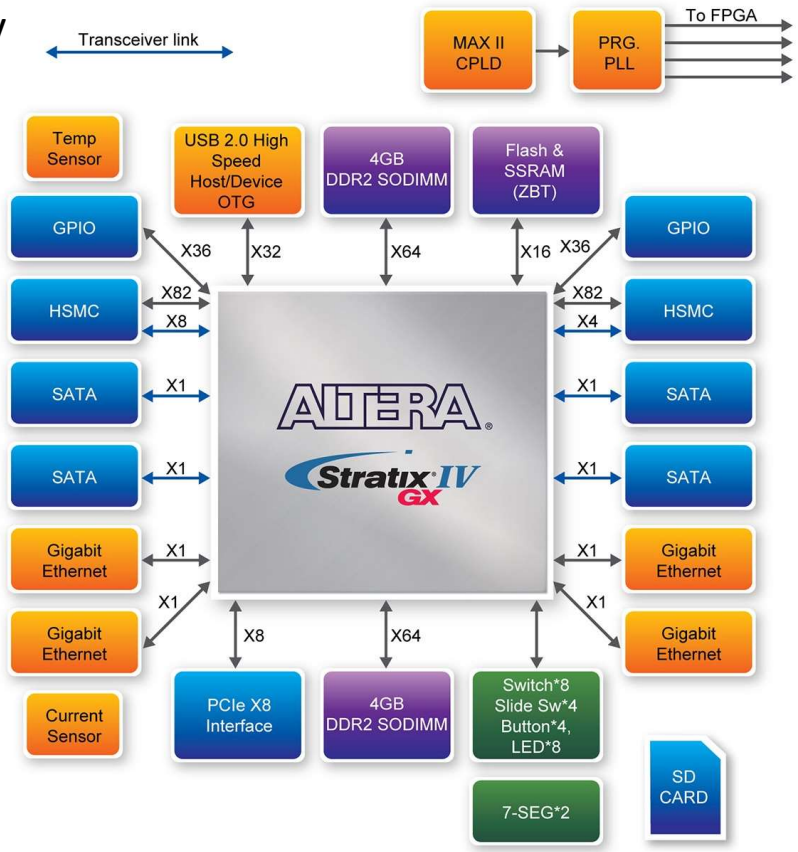


Many Built-In Interfaces

Modern FPGAs have many built-in interfaces.

- DRAM
- PCI Express
- USB
- SATA (disk drives)
- etc

Makes them easy to integrate into compute environments



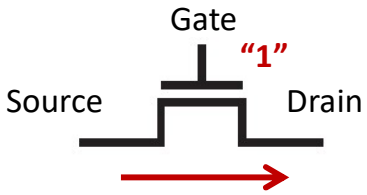
FPGA vs. ASIC

ASICs

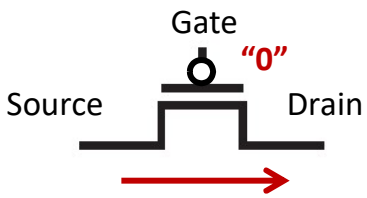
- ASIC (Application-Specific Integrated Circuit) designs are usually implemented using “standard cells”
- Standard cells are pre-designed layouts of transistors for implementation of common logic gates and registers (D-Flip Flops)
- Standard cells are be pre-characterized in terms of cell area, cell delay, and cell power consumption
- Simplifies design flow, design verification, and timing analysis

CMOS

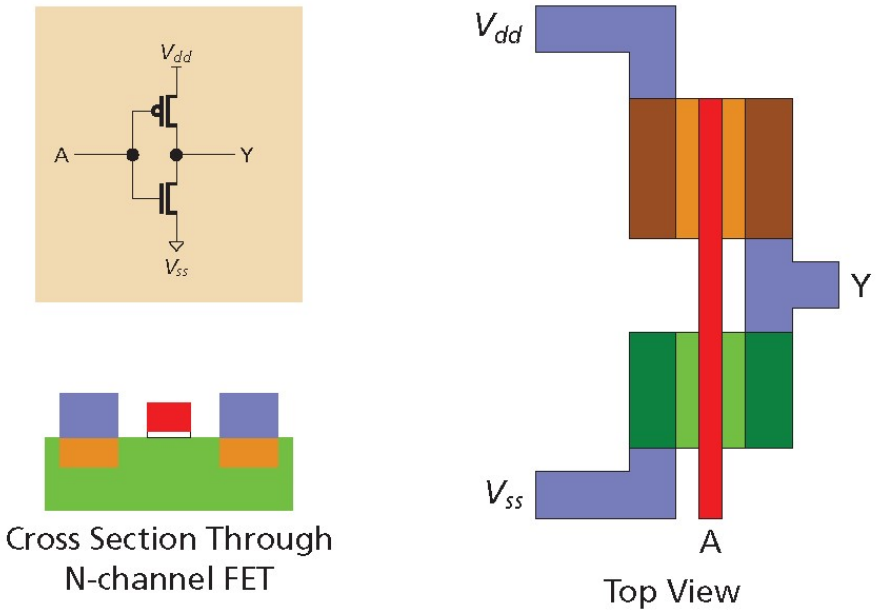
- N-Channel MOS (NMOS) transistors turn “ON” when the Gate voltage = “1”



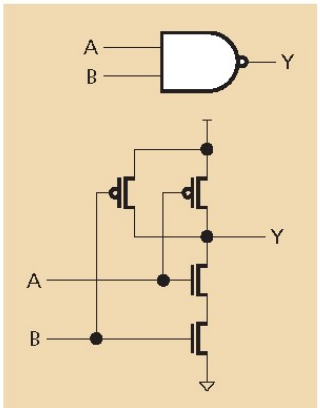
- P-Channel MOS (PMOS) transistors turn “ON” when the Gate voltage = “0”



CMOS Inverter Layout

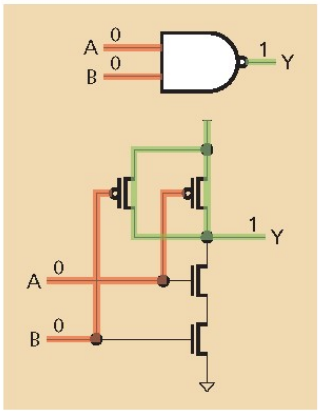


CMOS NAND Gate



Two-input NAND gate:
two n-FETs in series;
two p-FETs in parallel

CMOS NAND Gate



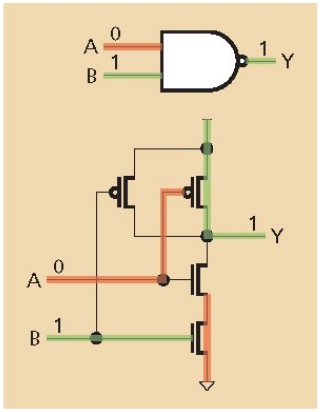
Both inputs 0:

Both p-FETs turned on

Output pulled high

Figure derived from slides by S. Edwards from his CSEE4840 class

CMOS NAND Gate



One input 1, the other 0:

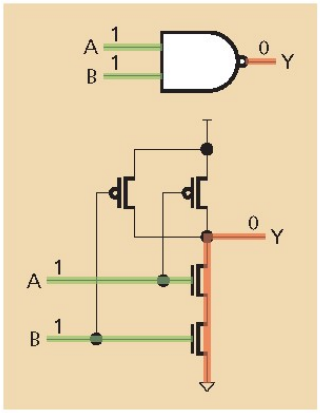
One p-FET turned on

Output pulled high

One n-FET turned on, but does not control output

Figure derived from slides by S. Edwards from his CSEE4840 class

CMOS NAND Gate



Both inputs 1:

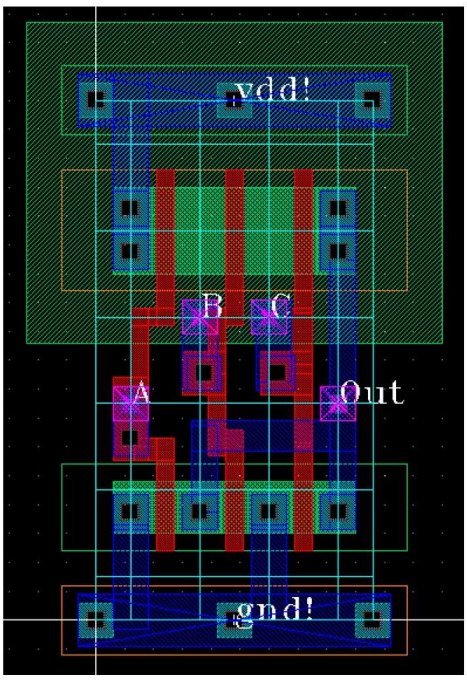
Both n-FETs turned on

Output pulled low

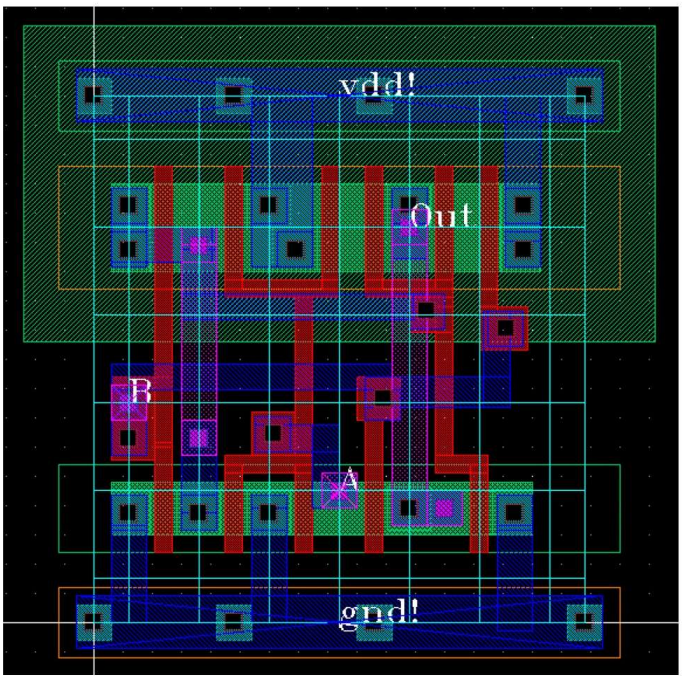
Both p-FETs turned off

Figure derived from slides by S. Edwards from his CSEE4840 class

Standard Cells of Logic Gates

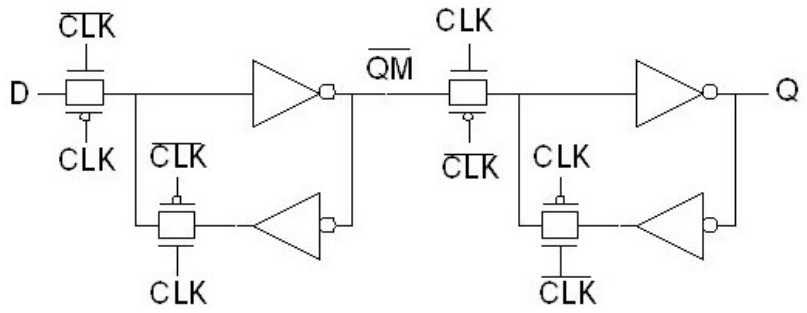


NOR-3



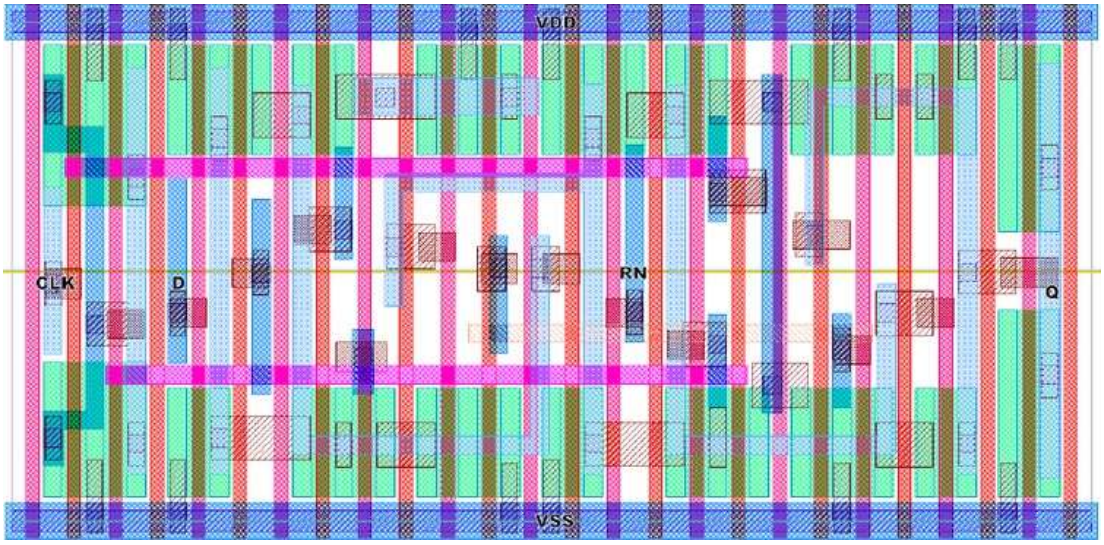
XOR-2

CMOS D-Flip Flop



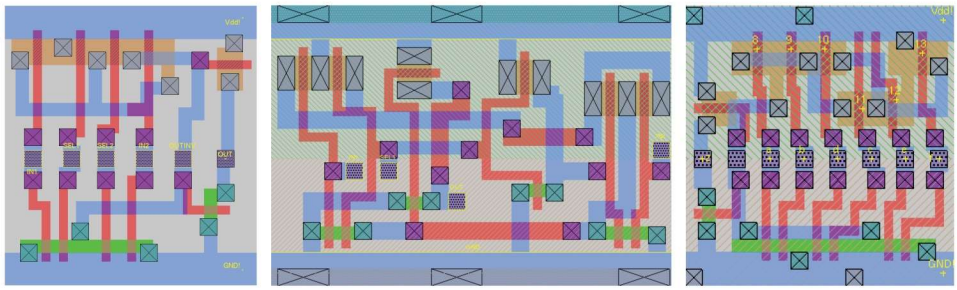
A "negative level-sensitive" latch A "positive level-sensitive" latch

Standard Cell of D-Flip Flop

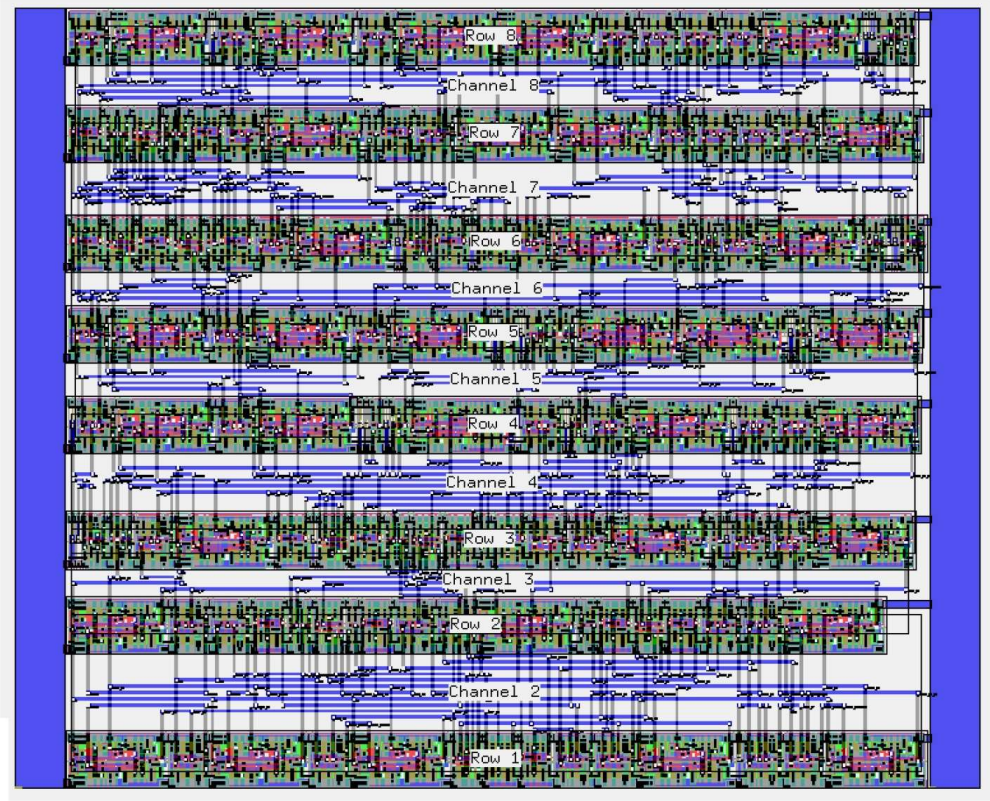


Edge-Triggered D-Flip Flop with Asynchronous Reset

Standard Cell Layout

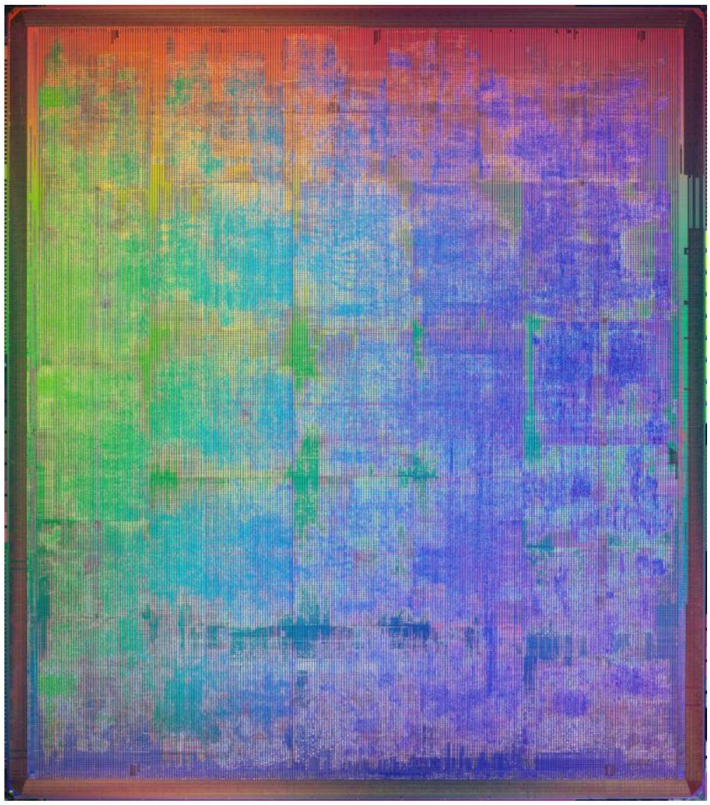


Standard Cell Layout



Standard Cell Layout

NVIDIA GeForce 8800
(600+ million transistors, about 60+ million gates)



Latest NVIDIA GPU

- NVIDIA Tesla GV100 GPU in **12 nm** process
- Contains **23 billion transistors**

Design Flows

- FPGA and ASIC have similar design flows