Varsha L. Thirumalai

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EDUCATION

San Jose State University **August 2022-Present**
Masters of Science in Electrical Engineering Expected Graduation: May 2024
Subjects Taken: Computer Architecture, Embedded SOC, Intelligent Autonomous Sys, Neural Networks GPA: 3.54/4

PES University **August 2015-May 2019**
Bachelor of Engineering in Electronics and Communications GPA: 3.02/4

SKILLS

- Programming Languages: C, Python, C++, Verilog
- SOC Design Fundamentals, Xilinx FPGA, Vivado, Raspberry Pi. Sensor Integration
- Protocols: CAN, I2C, SPI, AXI, ANB
- Tools: Git, Jira, Confluence, Slash Framework, Agile, Lean, NumPy. Pandas, Matplotlib, Scikit-Learn

WORK EXPERIENCE

Wipro Technologies- Client: Ford Motors **Jan 2020–May 2022**
Software Engineer Bangalore, India

- Developed firmware in C and validation tests in Python for components like windows, mirrors, wipers, seat control and latches. Created test Automation Scripts for the Body Control Systems, focusing on motor control, sensing, and actuation in embedded environments.
- Experienced on Script development, Test cases Analysis, Making test plans, writing tests, bug fixing.
- API development using Python and C.
- Improved the test result efficiency to 65% by creating a system plan before Regression Testing in the lab.
- Created a Python script for regression testing that detects bugs, immediately alerts during system failures or setup issues, slashing false failure rates and false positives each by 50%. This efficiency saved two days and cut costs by up to 10k dollars.
- Met quarterly performance metrics with 89% accuracy in test results and improved lean and agile skills, underscoring the importance of precise communication for adapting to evolving client and user expectations. Mentored and guided 3 new joiners in the team in initial work and process, and helped them ramp up in 1 months' time.

PROJECTS

2D detection using Yolov3 on PYNQ Z2 FPGA[in progress]

- Developed scripts for evaluating and deploying LPYOLO, a low-precision YOLO variant designed for efficient face detection on FPGA platforms, as detailed in the associated paper.
- Utilizes Brevitas, a PyTorch-based library, for quantization-aware training (QAT) of models, enhancing their performance and compatibility with low-precision hardware environments.
- Models are prepared for FPGA deployment by converting them into the ONNX format, ensuring interoperability and ease of use across different platforms and tools.
- Employs FINN, a cutting-edge framework from Xilinx Research Labs, for optimizing and executing deep neural network models on FPGAs, specifically demonstrated on a PYNQ-Z2 board for real-world applications

Tic-tac-toe on VGA Peripheral Interface Integration with Cortex M0 [link]

- Engineered a system that incorporated a Cortex-M0 processor, AHB-Lite bus, AHB VGA peripherals, and internal memory, all deployed on an Artix A7 FPGA board.
- Utilized Keil Software to craft test programs in C, showcasing the tic-tac-toe mechanics. This effectively highlighted the seamless hardware-software interplay within the embedded system, with simulations and verifications carried out. Building upon this foundational program, I devised the logic for a two-player snake game and successfully executed it on the board.

Designed an IoT-driven vending machine for a lab equipment [link]

- Vending machine using Arm Cortex M3, integrated cash transaction mechanism and RFID. Used DC motors instead of Stepper thereby reducing equipment costs by 30% and prevented wastage of components by 18% through precise dispensing mechanisms.

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