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### **OBJECTIVE**

Graduate Design Verification Intern at Hillsboro, Austin, or Santa Clara

#### EDUCATION

## Portland State University

Portland, OR

M.Sc Electrical and Computer Engineering, 4.0 / 4.0

Fall 2021 - Spring 2023

- Relevant Courses:
  - \* ECE 581: ASIC Modelling and Synthesis (Dr. Xaiyou Song) Fall 2021
  - \* ECE 585: Microprocessor System Design (Mark Faust) Fall 2021
  - \* (tentative) ECE 586 : Computer Architecture (Mark Faust) Winter 2022
  - \* (tentative) ECE 587: Advanced CompArch I (Yuchen Huang) Spring 2022
  - \* (tentative) ECE 588: Advanced CompArch II (Yuchen Huang) Fall 2022

### College of Engineering, Pune

Pune, Maharashtra, India

B. Tech Electronics and Telecommunication Engineering, 3.2 / 4.0 (7.99/10)

May 2015 – June 2019

### EXPERIENCE

# • Tejas Networks

Mumbai, Maharashtra, India August 2019 - August 2021

Research and Development Engineer

- **Networking Technologies**: Working with DHCP, VLAN tagged Traffic management, VPNs, Downstream Ingress Bandwidth, HQOS queuing, Traffic Shaping Profiles, etc.
- $\circ$  C/C++: The software used for configuring switching capabilities of a network card is largely based in C for device drivers and C++ for higher level UI.
- **Linux**: Network switching cards employ a modified linux kernel. Extremely familiarized with linux and its utilities. All development done in vim text editor and bash terminal environment.
- **Feature Development**: Implemented Zero Touch In-Band Management feature request by Tejas Network's client with inputs from the Sales team and feedback from QA team.
- o Python: Extensive scripting to trivialize monotonous commands with flexibility to adapt to situations.
- o Training: Trained new recruits to the team and enabled them to contribute meaningfully.

## DOT Sys Technologies

Mumbai, Maharashtra, India

Design Intern

May 2018 - August 2018

- **Transistor Theory**: Implemented Pulse Width Modulation to control voltage and current levels to make a programmable power supply within the constrains of Transistor hardware.
- **Power Electronics**: Used loose capacitors, inductions and Transformers to convert main lines supply to transistor switching compatible levels.
- **Arduino**: Made a Programmable Battery Charger with UI implemented on Arduino + Transistor Theory and Power Electronics to manage the charging functionality.

### Eduvance

Mumabai, Maharashtra, India May 2017 - January 2018

Intern (B. Tech. Final Year Project - Smart Paper Tracking System)

- o **IoT**: Used RPi to collect data from devices via Bluetooth and IBM cloud services to implement data storage, sync, and decision making on cloud
- **Bluetooth**: Used Cypress Semiconductors PSOC4-BLE boards as portable markers to be attached to files to track them and provide information to RPi for syncing.

# PROJECTS

- dram-controller: A bank parallel DDR4 memory controller with access scheduling written in System Verilog.
- fifo: Parameterized multi-port fifo for simultaneous reads and writes.
- i2c: 12C master and slave implemented in Verilog, currently re-writing code in to System Verilog.
- ffind: Small wrapper for find command in linux to make it accept grep-like arguments. Written in golang and rust.
- Music-Player-GO: Feature Contributions to open source Music Player app. Written in kotlin.

#### Personal publications

• Modified MD5 Algorithm for Low-End IoT Edge Devices.: Viraj Khatri, Dr. Vanita Agarwal. ICCCNT2019