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Abstract

Digital (*i.e.* droplet-based) microfluidics, by the electrowetting-on-dielectric (EWOD) mechanism, has shown great potential for a wide range of applications, such as lab-on-a-chip. While most reported EWOD chips use a series of electrode pads essentially in one-dimensional line pattern designed for specific tasks, the desired universal chips allowing user-reconfigurable paths would require the electrode pads in two-dimensional pattern. However, to electrically access the electrode pads independently, conductive lines need to be fabricated underneath the pads in multiple layers, raising a cost issue especially for disposable chip applications. In this article, we report the building of digital microfluidic plates based on a printed-circuit-board (PCB), in which multilayer electrical access lines were created inexpensively using mature PCB technology. However, due to its surface topography and roughness and resulting high resistance against droplet movement, as-fabricated PCB surfaces require unacceptably high (~500 V) voltages unless coated with or immersed in oil. Our goal is EWOD operations of aqueous droplets not only on oil-covered but also on dry surfaces. To meet varying levels of performances, three types of gradually complex post-PCB microfabrication processes are developed and evaluated. By introducing land-grid-array (LGA) sockets in the packaging, a scalable digital microfluidics system with reconfigurable and low-cost chip is also demonstrated.

Index Terms

Electrowetting; electrowetting on dielectric (EWOD); lab-on-a-chip; microfluidics; micro total analysis system (μ TAS); surface tension

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I. BACKGROUND

A. Digital Microfluidics

DIGITAL (*i.e.* droplet-based) microfluidics use discrete fluid packets as carriers to achieve various fluidic functions, bio-chemical reactions, and detections in the microscale. Although droplet manipulations can also be performed inside microchannels [1], [2], non-channel configurations allow for much simpler systems and do not require external pressure sources (*i.e.* eliminating the need for pumps and valves). Also, electrically-driven channel-free devices are flexible for operators, allowing electronically reconfigurable two-dimensional movement on surfaces. Manipulation of droplets or bubbles has been achieved with various driving mechanisms such as electrostatic [3], dielectrophoretic (DEP) [4], continuous electrowetting (CEW) [5], electrowetting [6], electrowetting-on-dielectric (EWOD) [7], temperature gradient

[8] or acoustic wave [9]. Voltage-driven mechanisms usually consume minimal power and do not suffer from Joule heating, although they often require high voltages (*e.g.* over 100 V). By controlling the surface wettability of a dielectric solid layer using electric potential through EWOD, aqueous droplets can be manipulated on the surface dry in air [7] or immersed in oil [6]. Because initial resistance against droplet movement (analogous to static friction of a solid object) is all but eliminated if immersed in oil, an EWOD chip proven for dry-surface operation works when immersed in oil as well but not vice versa. The following essential microfluidic functions for droplets have been achieved in air: droplet creation from bulk liquid (*i.e.* digitization), movement along a programmable path, merging with other droplets, and division into smaller droplets [10]. Since a wide range of aqueous and nonaqueous liquids can be manipulated [11], biomedical applications such as protein MALDI-MS analysis [12] and clinical diagnostics for human physiological fluids [13] have been successfully demonstrated. The advances in the field of electrowetting are well described in the recent reviews [14], [15].

B. Two-dimensional digital microfluidics plates

The advantages of digital microfluidics lie mostly in its simplicity and reconfigurability for parallel liquid operation in large scale, which requires two-dimensional addressable control sites for droplet manipulation [7], [10]. For an electrical control method such as EWOD, this means a two-dimensional plate with the ability to electrically access (*i.e.* reference) each point independently in the MxN grid. While simple fabrication of EWOD chips with a single layer of conduction lines can produce a variety of electrode patterns dedicated to specific microfluidics protocols, such chips do not allow for full reconfigurability. Furthermore, as the number of electrodes in a two-dimensional pattern increases, the number of conduction lines from the inner electrodes to the external control circuit increases likewise. These access lines must run through the electrode gaps, which should be minimized in order to maintain the driving efficiency of EWOD, as illustrated in Fig. 1(a). As a result, the size of an electrode array is quite limited in practice unless additional layers of electrical conducting lines are introduced. To fully utilize the capabilities of the digital microfluidic mechanism, innovative chip design and device fabrication are desired.

The most general design for a two-dimensional electrode array would require a multilayer arrangement of electrical connections, where each of its MxN electrodes are accessed directly and independently through underlying layers of wires, as shown in Fig. 1. (b). Multiple conducting layer structures can be made using typical integrated circuit (IC) fabrication methods (with special care if high voltage is required) on glass or Si substrates, as demonstrated by Gascoyne *et al.* [16] with a 32x32 DEP programmable fluidic process chip on a silicon-on-insulator (SOI) IC chip. However, cost is an issue for such microfluidic devices, which have much larger areas than typical IC chips, because producing them requires multiple thin-film deposition, lithography, patterning and planarization steps. Since many biomedical applications prefer disposability to avoid cross-contamination, it is likely that using multi-layered chips produced via IC fabrication methods is prohibitively expensive. In addition, IC-like high-density chips would demand extra cost for fluid or electrical interconnections, where no standards exist. The approach for disposable microfluidic chips, therefore, would call for low-cost chip fabrication methods as well as a system using a convenient and reusable packaging scheme.

To allow for two-dimensional EWOD operations without fabricating multiple metal layers, Fan *et al*. [17] have reported a cross-referencing design by orthogonally arranging two parallel chips, each having a single electrode layer, as shown in Fig. 1(c). By energizing the row and column electrodes with opposite signals, the electrode spots at their intersection become most hydrophilic and thus the droplet moves toward them. However, the simultaneous driving of multiple droplets in this cross-referencing device is limited due to its need for time-multiplexed driving scheme [18]. Furthermore, since the electrodes on both the top and bottom chips need to be connected to the control circuit, the electrical connections and device packaging are more complex.

II. Multi-layer PCB for digital microfluidics

A. The idea

The problems stated above may be addressed by using a printed circuit board (PCB) as the substrate for two-dimensional electrode arrays, as first demonstrated by Gong and Kim [19]. Commercial PCBs can accommodate up to 30 separate wiring layers, which are electrically accessed through drilled vias that have Cu-electroplated inner walls. For its maturity and low cost, PCB has already been utilized for microfluidic systems. For example, through post-processing steps such as etching, the Cu layer can be machined into diffusers/nozzles, pump chambers [20], and thermal flow sensing electrodes [21]. Also, hot embossing and multilayer lamination steps have been used to build entire microfluidic channels, pumps and valves in the PCB polymer substrate [22]. Table I lists fabrication methods, electrical capabilities, feature sizes, device sizes and typical fabrication costs for IC processes, PCB technology, widely used PDMS molding and in-house cleanroom processes. The in-house cleanroom process is listed here to show the extra cost that may be added to PCB substrate devices if any post processes would be made. The comparison shows that PCB is a good candidate for microfluidics applications, providing respectable feature sizes at very low fabrication costs. It is important to note that, with the advancement of the PCB technology, existing and fast advancing high-density electrical packaging methods for PCBs will be readily applicable for digital microfluidics. The compatibility of PCB for digital microfluidics is demonstrated in this paper through EWOD-based devices and systems.

B. Basic fabrication: PCB-EWOD plate Type 1

A multilayer PCB can be used directly as an EWOD substrate by adapting the surface-mount solder pads to be the electrodes for EWOD actuation. We have developed and evaluated a 4-layer PCB substrate (from a commercial prototype PCB manufacturer) for EWOD application. Fig. 2 shows one such device with an 8x8 electrode array composed of 1.5 mm square electrode pads. The gap between electrodes is 75 μm, the connecting via at each electrode is 200 μm in diameter, and the top Cu layer is 25 μm thick (Fig. 2(a,b)). The pattern and arrangement of the EWOD electrodes are shown in Fig. 2(d). For electrical connection to the external control circuit, wires are routed from the topside EWOD electrodes, through the underlying three metal layers, to the pads that surround the plate.

Since the glass transition temperature of FR4 (the polymer used as PCB substrate material) is 185 °C, PCBs cannot be subjected to high-temperature processes such as plasma-enhanced chemical vapor deposition (PECVD) silicon dioxide deposition (~300 °C), which is often used for building the EWOD dielectric layer on glass or Si substrates. However, films created via lower-temperature PECVD processes tend to exhibit poor dielectric properties. Therefore, parylene, deposited at room temperature, has been chosen as the dielectric material. Furthermore, the conformal coating of parylene plugs the connection vias, help flattening the device surface. Parylene has a dielectric constant of 3.2, lower than that of silicon dioxide (4.5), but still is sufficiently effective for typical EWOD actuation. Although parylene itself is hydrophobic (contact angle around 107°), 2000 Å AF1600 Teflon is spin-coated on top of it to make the surface more hydrophobic (contact angle around 120°). As shown in Fig. 1b, a glass plate coated with transparent 2000 Å indium tin oxide (ITO) and 2000 Å Teflon is then placed on top of this Type-1 PCB-EWOD plate to ground the droplets. Appropriate spacers (75–1000 μm thick) are inserted between the two plates to define the gap height.

C. Experimental results and performance analysis

For EWOD actuation, the pressure difference (ΔP) between the two ends of the droplet, caused by the EWOD-induced contact angle difference ($\theta_1 - \theta_2$), is the driving force for droplet movement, expressed in Eq. 1, where g is droplet surface tension, ε_r is the dielectric constant of the dielectric layer, t is its thickness, A is the area of droplet, and ε_o is the electric permittivity of free space [7]. By rearranging Eq. 1, we obtain Eq. 2, which shows that the minimum voltage required to induce enough contact-angle change to create motion against resistances is proportional to the square root of the dielectric layer thickness t. The major failure mechanism of EWOD actuation is electrolysis due to dielectric breakdown (or current leakage) of the dielectric layer. The maximum voltage one can apply before the occurrence of current leakage is expected to be proportional to the dielectric thickness, t (Eq. 3). If we plot the voltages vs. the dielectric thickness according to Eqs. 2 and 3, the intersection point indicates the minimum thickness of the dielectric layer required for the device to have droplet actuation before current leakage (*i.e.* electrolysis) occurs [23]. The minimum thickness can be calculated as Eq. 4.

$$\Delta P=\gamma(\theta_1-\theta_2)=\frac{1}{2}CV^2=\frac{1}{2}\frac{\varepsilon_r\varepsilon_0 A}{t}V^2 \tag{1}$$

$$V_{\min}=\sqrt{\frac{2\gamma(\theta_1-\theta_2)_{\min}t}{\varepsilon_r\varepsilon_0 A}} \tag{2}$$

$$V_{breakdown}=tE_{breakdown}=V_{\min} \tag{3}$$

$$t_{\min}=\frac{2\gamma(\theta_1-\theta_2)}{\varepsilon_r\varepsilon_0 A E_{breakdown}^2} \tag{4}$$

If the surface has a higher resistance against the droplet movement, *i.e.*, larger contact-angle changes ($\theta_1 - \theta_2$) are required, the minimum dielectric thickness should be larger. PCB substrates have more topography and rougher surfaces than glass or Si substrates, and thus impose more resistance against the droplet movement. As a result, thicker dielectric layers and higher operation voltages are called for EWOD actuation. On the other hand, a wet surface, *i.e.*, coated with or immersed in oil, also significantly reduces the drag against the droplet motion, so that thinner dielectric layers and lower driving voltages can be used. Note, however, that our goal is to develop PCB EWOD devices capable of operating droplets in air, *i.e.*, with high performance. One can see that EWOD chips designed for a droplet-in-air operation a the higher drag force also work for droplet-in-oil operation with less drag force, but the opposite is not necessarily true.

A series of tests have been conducted on PCB-EWOD plates to obtain the droplet driving performance in air and oil as shown in Table II. At least 7 μm thick parylene and 500 V of driving voltage were needed for successful droplet actuation in air. This operation voltage is 10 times larger than that on a glass or Si substrate, on which 2000 Å PECVD oxide is sufficient [23]. Such a high operation voltage may cause electrical shorts on the PCB. Also, it requires a high voltage source, a special control circuit, and extra safety protection for microfluidic systems. Decreasing the operation voltage is an important challenge for the PCB-EWOD plate.

Our tests showed driving voltage can be reduced to around 200 V if the PCB-EWOD plate is immersed in oil (140 V threshold driving voltage was reported in [24] with different device configuration), but it is against our ground goal of having the device for both air and oil environment.

To determine the cause of very high moving resistance on the PCB substrate, we analyzed the following experimental observations. When we initially placed a droplet between two adjacent electrodes on a PCB-EWOD plate with 1 μm thick parylene, the droplet could move easily back and forth with 70–80 V, but failed to move further onto the next electrode pad. After careful examination, we learned that the trench between the electrodes prevented the droplet from crossing over. In comparison, electrode pads on a glass or Si substrate, having electrode thicknesses of 1000–2000 Å and gaps of 4–10 μm, allowed a droplet to spread to an adjacent electrode, even without EWOD voltage. This spreading actually enabled EWOD actuation from one electrode to the next. Now, consider the trenches formed in the path of droplet movement by features on the PCB substrate (*i.e.* 10 μm thick Cu electrode pads and 75 μm wide gaps between them). To move between two electrodes, a droplet must first fill in or jump over the trench in order to contact the adjacent electrode, which must then pull the droplet by EWOD. At the same time, the droplet also needs to be pulled off the previous trench, which poses a significant pull-back resistance. As a result, a much larger operation voltage was required to achieve continuous movement. Immersing or smearing the device surface with silicone oil [24], [25] can fill trenches and improve operation, but again it is not a desirable solution for us. Interdigitated electrode patterns [6] would help droplet transfer between adjacent electrode pads. Unfortunately, such patterns are not available in the current PCB standards, and, even if they were available, any resultant improvement would be quite limited by the large feature size of the PCB fabrication.

III. Post-PCB microfabrication processes

Our approach for decreasing the operation voltage is to improve the surface flatness and reduce the gaps between the driving electrodes by adding post-PCB microfabrication processes in house. Since each added steps of the microfabrication process significantly increases the cost, we develop three types of processes with increasingly complex fabrication steps, so that users can choose the simplest (*i.e.* cheapest) type that their particular application demands.

A. PCB-EWOD plate Type 2

By wet etching, we completely removed the electrodes on top of the PCB, while protecting center holes, in order to achieve a flat surface. Then, by depositing and patterning a thin metal layer (2000 Å) as shown in Fig. 3(a), we created a smoother surface, on which droplet functions (moving and cutting) can be performed with as little as 70 V_{AC} at 1 kHz on the PCB-EWOD plate coated with 1 μm parylene and 2000 Å Teflon [19]. However, EWOD performance on this Type-2 PCB plate was still not as good as that on a glass or Si substrate, and cutting and creation of droplets required higher driving voltages and were more vulnerable to electrolysis. To improve the performance further, we addressed two more challenges associated with EWOD on PCB substrates.

First, the connection vias increase the drag force for the droplet movement on the surface. During movement, we observed that droplets tend to pin around the vias and experience substantially increased resistance. Furthermore, the via holes, limited by PCB technology to be 200 μm or larger in diameter, would create a problem for droplet movement when the distance (*i.e.* spacer height) between the top and bottom plates is small. The channel height needs to be smaller than a critical value to allow the droplet creation and cutting [10]. However the internal pressure of droplets squeezed between the two plates increases as the gap height decreases [26]. If the gap is too small (comparable to the vias diameter), it may drive the liquid into the vias. In addition to impeding movement, the liquid in the vias caused significant electrolysis, because less parylene is deposited inside the vias. Second, the surface of the PCB substrate (general FR4) is rough. After a 2000 Å Teflon coating, the measured surface roughness was around 1–2 μm, which is 1000s of times larger than that on polished glass or Si substrates. Since the static resistance against droplet sliding increases when the difference between the advancing and receding angle, θ_{adv} and θ_{rec}, respectively, increases (essentially proportional to $\gamma(\cos\theta_{adv} - \cos\theta_{rec})$), surface roughness is an important factor. The advancing and receding contact angles on the Teflon-coated PCB surface were 133° and 96°, respectively, compared with 118° and 107° on Teflon-coated polished glass or Si. In other words, the resistance due to contact-angle hysteresis on the PCB surface was found to be 3–4 times larger than that on the polished glass or Si substrates.

B. PCB-EWOD plate Type 3 and Type 4

To further address the above problems, we developed two additional post-PCB processing methods that involve chemical mechanical polishing (CMP), a widely used technique in IC fabrication to make very flat and smooth silicon surfaces. As shown in Fig. 3(b), the connection vias on the PCB substrate were filled with silver powder conductive epoxy by the prototype PCB manufacturer. For the first step of post-processing, the Cu layer was lapped down by CMP enough to expose the filling epoxy and PCB surface (FR4). Further CMP served to polish the PCB surface, now consisting of bare FR4 with silver epoxy dots. After the surface was polished, we deposited and patterned a thin metal layer, and coated a dielectric layer as well as a hydrophobic layer to obtain a high-performance Type-3 PCB-EWOD plate.

However, because FR4 polymer is soft, the above polishing process did not necessarily work ideally. To obtain a highly polished surface, the PCB should be coated with a harder polymer which then serves as the polished material. We experimented with two types: liquid photo imageable (LPI) solder mask, coated by the manufacturer, and SU-8, coated in-house. As shown in Fig. 3(c), processing started with CMP lapping of the hard polymer in order to uncover the Cu contact holes, followed by polishing of the resultant Cu and polymer surface. The roughness of a well-polished surface (optimized with different polish slurries and process parameters) was measured as smooth as 100 Å on this Type-4 PCB-EWOD plate. Although this roughness is still ten times larger than that on the polished glass or Si substrates (10 Å), the contact-angle hysteresis of a water droplet on it is much smaller than that on the unpolished device. Consequently, the driving voltage has been further reduced.

We made a series of tests on Type-4 PCB-EWOD devices with different dielectric thicknesses and driving voltages to characterize their performances. The droplet movement speeds at different driving voltages are measured on these substrates by taking the video of droplet movement between the EWOD electrodes. As summarized in Fig. 4, we have tested five cases: (1) glass substrate with 0.5 μm parylene in air, (2–4) Type-4 PCB-EWOD plates with 0.5 μm, 0.8 μm and 1.2 μm parylene in air, and (5) Type-4 PCB-EWOD plate with 0.5 μm parylene immersed in 1 cSt silicone oil (Clearco Products Co.). All of these substrates are coated with 2000 Å Teflon as the top hydrophobic coating. We documented the threshold voltages for the droplet movement on each substrate. We also confirmed that the speed of droplet movement increased fast with voltage since the EWOD driving force increases parabolically with the voltage. The oil-filled device had much smaller driving voltage, even smaller than glass substrate in air, since silicone oil lubricates the surface and smoothes the rough surface. These results show the Type-4 PCB-EWOD device has the comparable performance as glass substrate with the same dielectric thickness. A device with thicker dielectric layer would require higher driving voltage but also reduce the possibility of electrolysis. For the driving voltage range of 50–200 V, the existing high-voltage control circuits for portable microfluidic system [18] can be used without modification, giving us the freedom to optimize the PCB-EWOD device with best performance and minimal electrolysis.

C. Comparison of PCB-EWOD plate Types 1–4

To summarize fabrication of PCB-EWOD plates, four different types with increasing sophistication have been described. (1) Type 1 is a plate with a dielectric and a hydrophobic layer deposited directly onto an as-received regular PCB substrate (Fig. 1(c)). (2) For Type 2, the thick Cu layer on a PCB was removed by wet etching, and then thin electrodes were deposited and patterned, followed by dielectric and hydrophobic layer coatings (Fig. 3(a)). (3) For Type 3, the top Cu layer was removed from a PCB that has its vias filled as received. After polishing the surface by CMP, thin electrodes were deposited and patterned, followed by dielectric and hydrophobic layer coatings (Fig. 3(b)). (4) For Type 4, the top Cu layer was removed from a PCB that has filled-vias and a hard polymer coated as received. After polishing the surface by CMP, thin electrodes were deposited and patterned, followed by dielectric and hydrophobic layer coatings (Fig. 3(c)). These four methods produced increasingly superior PCB-EWOD plates (*i.e.* through flatter surface, reduced roughness, and lower contact-angle hysteresis, all leading to higher EWOD performance) but with increasing fabrication costs.

Table III lists and compares the surface conditions the four different methods produced as well as those of polished glass or Si substrates. While fabrication of the best-performance PCB-EWOD plates costs the most, we estimate that, if mass-produced, it is still economical enough even for some disposable applications. Different methods are reported so that one may choose a cheaper method for less demanding microfluidic operations (such as droplet translations only) or droplets in an oil-lubricated environment.

IV. Packaging

Electrical connection and control requirements for direct-referencing EWOD devices increase rapidly with array size (grid number) and quickly overwhelm the system design. There exist many high-density (as small as 0.7 mm pitch), high connection number (thousands of pins) packages for IC chips, such as ball grid array (BGA), pin grid array (PGA), and land grid array (LGA). To utilize these package sockets for EWOD devices made on glass or Si substrates, wire bonding is needed to connect electrical pads on the device to a dedicated chip carrier, which is not reusable and would comprise a large portion of the total cost. We note that a LGA package scheme, a recent development in IC electronics, would circumvent the above problem for packaging PCB-EWOD plates. Instead of using pins or balls, the LGA socket has spring-loaded pins, or other vertical connection components [27] that can connect the contact pads on the bottom surface of a PCB-EWOD plate, fabricated the same way as surface mount pads, to the top surface on the control circuit board, as shown in Fig. 5. Therefore, by designing the contact pad array on the backside of the PCB-EWOD plate and introducing the LGA socket, the PCB-EWOD plate can serve not only as a microfluidic chip but also as packaging carrier for EWOD chips. This scheme eliminates the need for electrical connections in packaging, *i.e.* wire bonding for glass or Si EWOD devices. If droplets can be created from the on-chip reservoir by the EWOD actuation without any external help (*e.g.* pressurized droplet injection), the package for sample loading is also simplified for the system. Large on-chip reservoirs were formed by designing large electrode pads (*e.g.* 9–16 times the droplet electrode size), so that smaller droplets can be created from these reservoirs. The sample liquid was introduced into the on-chip reservoir by placing a large droplet from a pipette at the side edge of the PCB-EWOD plate.

As shown in Fig. 5, a packaging method has been developed based on the LGA packaging scheme. The LGA socket, oriented to correspond to the contact pad array on the backside of the PCB-EWOD plate, is inserted for electrical connection between the EWOD chip and the control circuit board. Since the number of electrodes (*i.e.* EWOD array sites) does not pose the limitation any more, design of the PCB-EWOD plate packaged with the LGA scheme is now scalable, a significant advantage for system development. The top pressure lid (see Fig. 5), with sample reservoirs and loading holes, covers and fixes the EWOD chip with screws providing the required contact force between the backside electrode pads and the LGA sockets. All of the LGA socket, pressure lid, and control board are reusable, and the PCB-EWOD plate can be replaced without bonding or soldering. The presented packaging scheme greatly simplifies the system development, enables scalable design of the system, and empowers disposable digital microfluidics applications.

Performance of an 8x8 array PCB-EWOD plate with the LGA packaging and on-chip reservoir was evaluated by testing the essential microfluidic operations. Type-4 PCB-EWOD plate as shown in Fig. 3(c) has the smoothest surface and the best EWOD performance. The spacers between the transparent top plate and PCB-EWOD plate at the bottom defined the gap height of 100 μm to allow droplet creation and cutting [10]. As shown in Fig. 6(a–i), with 80 V_{AC} at 1 kHz, comparable to that on glass or Si substrates, multiple droplets were simultaneously created from the on-chip reservoirs, moved on an arbitrary routine defined by the users, mixed together and cut into smaller droplets again, confirming digital microfluidic operations comparable to the regular glass- or Si-based EWOD plates. Type 3 and Type 2 plates were operational albeit with inferior performance. Type 1 plate, on the other hand, needed to be immersed in oil for successful operations.

V. Conclusions

A direct-referencing EWOD plate for digital microfluidics has been developed using a multi-layer PCB substrate. Four different post-PCB processing methods have been developed, resulting in PCB-EWOD plates with varying performance and fabrication cost. On the high-performance PCB-EWOD plates, the microfluidic operations of droplets were comparable to those on polished glass or Si substrates. The low cost of commercial PCB substrate fabrication, and comparable costs for the post processing, make the PCB-EWOD plate viable even for disposable applications, while being two-dimensional (*i.e.* reconfigurable). Also developed was a packaging scheme using LGA socket, which greatly simplifies the system development and enables scalable microfluidics.

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Biographies

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Chang-Jin "CJ" Kim received his Ph.D. in Mechanical Engineering from the University of California at Berkeley in 1991. He received his B.S. from Seoul National University and M.S. from Iowa State University along with the Graduate Research Excellence Award.

Since joining the faculty at UCLA in 1993, he has developed several MEMS courses and established a MEMS Ph.D. major field in the Mechanical and Aerospace Engineering Department. Directing the Micro and Nano Manufacturing Laboratory, he is also an IRG Leader for the NASA-supported Institute for Cell Mimetic Space Exploration (CMISE) and a founding member of the California NanoSystems Institute (CNSI) at UCLA. His research is in MEMS and nanotechnology, including design and fabrication of micro/nano structures, actuators and systems, with a focus on the use of surface tension.

Professor Kim is the recipient of the 1995 TRW Outstanding Young Teacher Award, the 1997 NSF CAREER Award, and 2002 ALA Achievement Award. Professor Kim has served on numerous Technical Program Committees, including Transducers and the IEEE MEMS Conference, and on the US Army Science Board as Consultant. He is currently chairing the Devices and Systems Committee of the ASME Nanotechnology Institute, and serving as a Subject Editor for the IEEE/ASME Journal of MEMS, on Editorial Advisory Board for IEEJ Transactions on Electrical and Electronic Engineering, and on National Academies Panel on Benchmarking the Research Competitiveness of the US in Mechanical Engineering.

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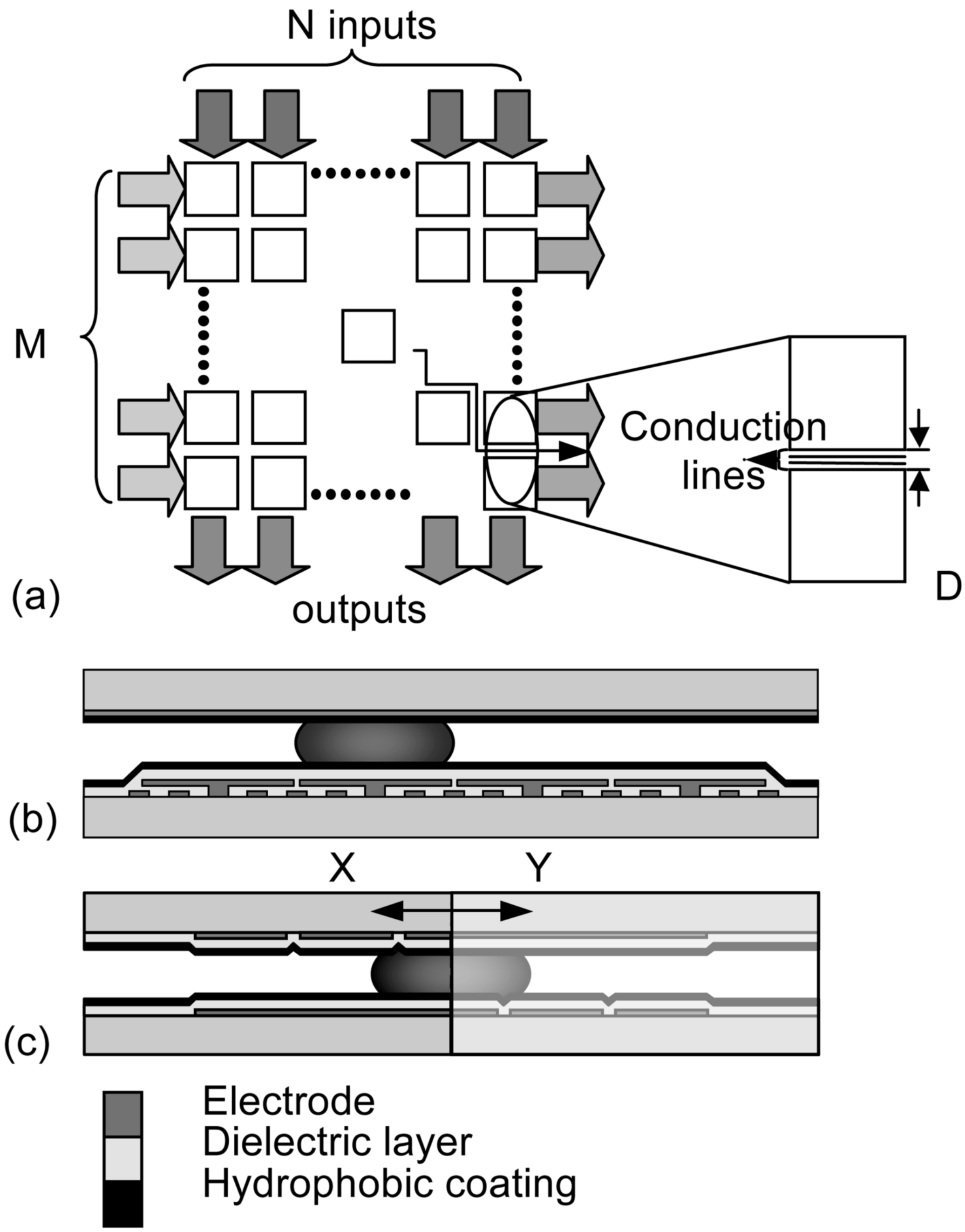

Fig. 1.
Accessing individual electrodes in an MxN 2-D array for reconfigurable digital microfluidics. (a) Access for MxN grid made with single electrode layer fabrication. (b) Direct-referencing with two electrode layers. (c) Cross-referencing technique with single electrode layer

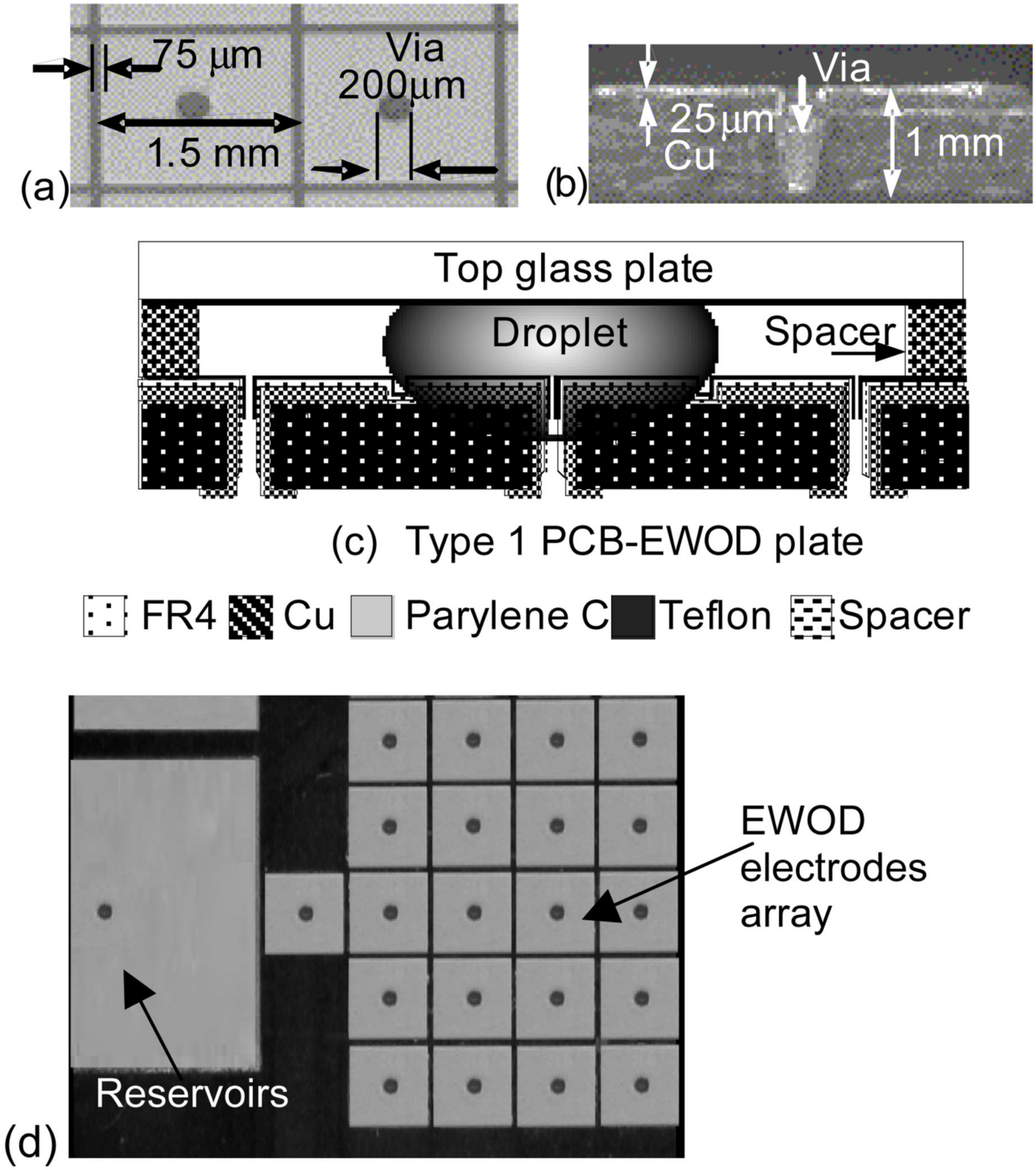

Fig. 2.
Direct-referencing EWOD device fabricated on four-layer printed circuit board (PCB), Type 1. (a) Optical top view of the PCB substrate, (b) optical cross-sectional view of the PCB substrate, (c) cross-sectional schematic of PCB-EWOD plate with top cover-plate on and a droplet in position surrounded with air, (d) part of the 8x8 array PCB-EWOD device, showing a big electrodes as liquid reservoir and 5x4 driving electrodes.

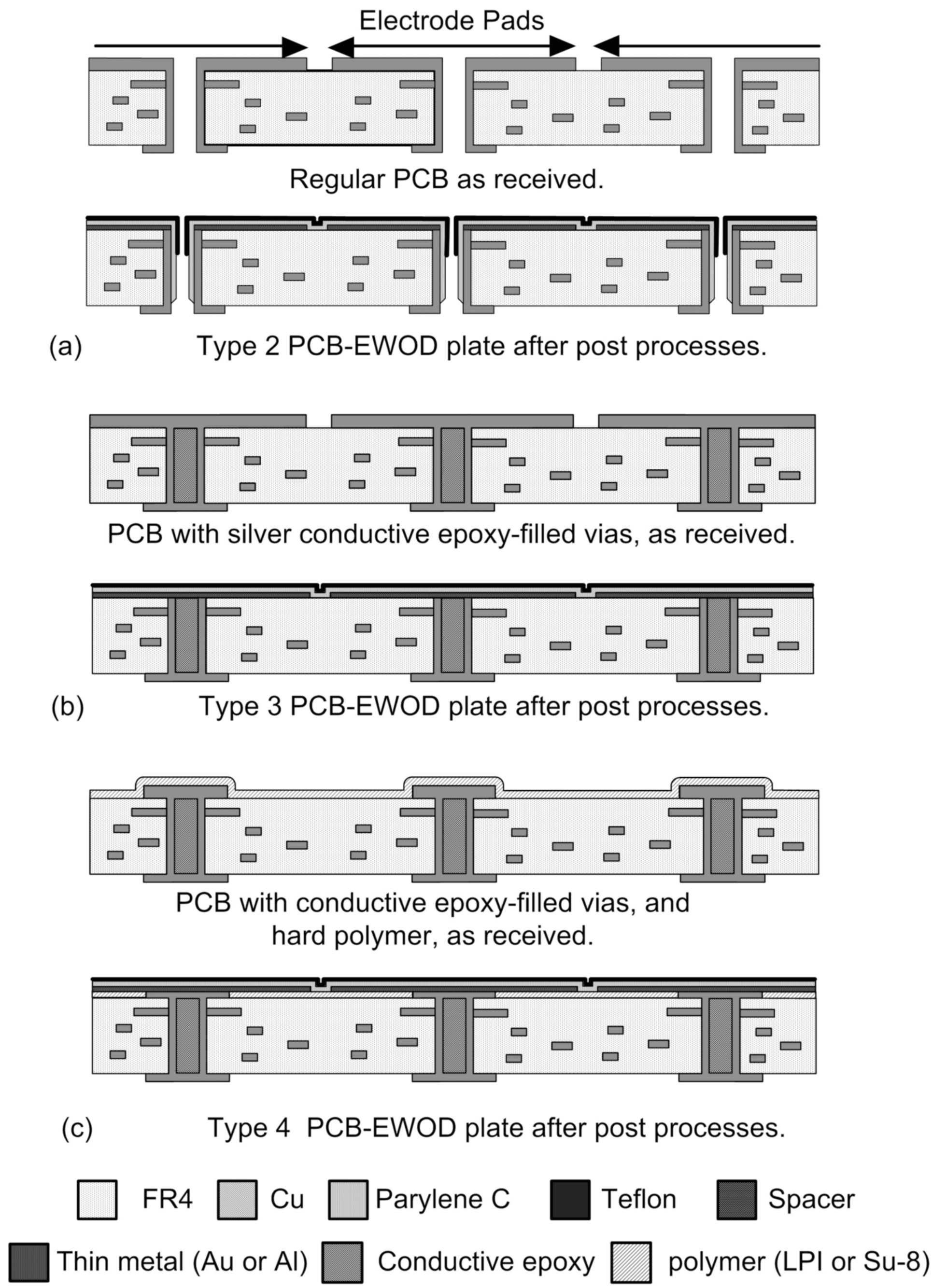

Fig. 3.

Three different post-processing methods on PCB substrate to improve EWOD performance: (a) Type 2. Wet etch top Cu layer and redeposit thin metal layer, (b) Type 3. CMP lapping and polishing Cu layer and PCB surface, (c) Type 4. CMP lapping and polishing coated hard polymer (LPI or Su-8) and Cu layer.

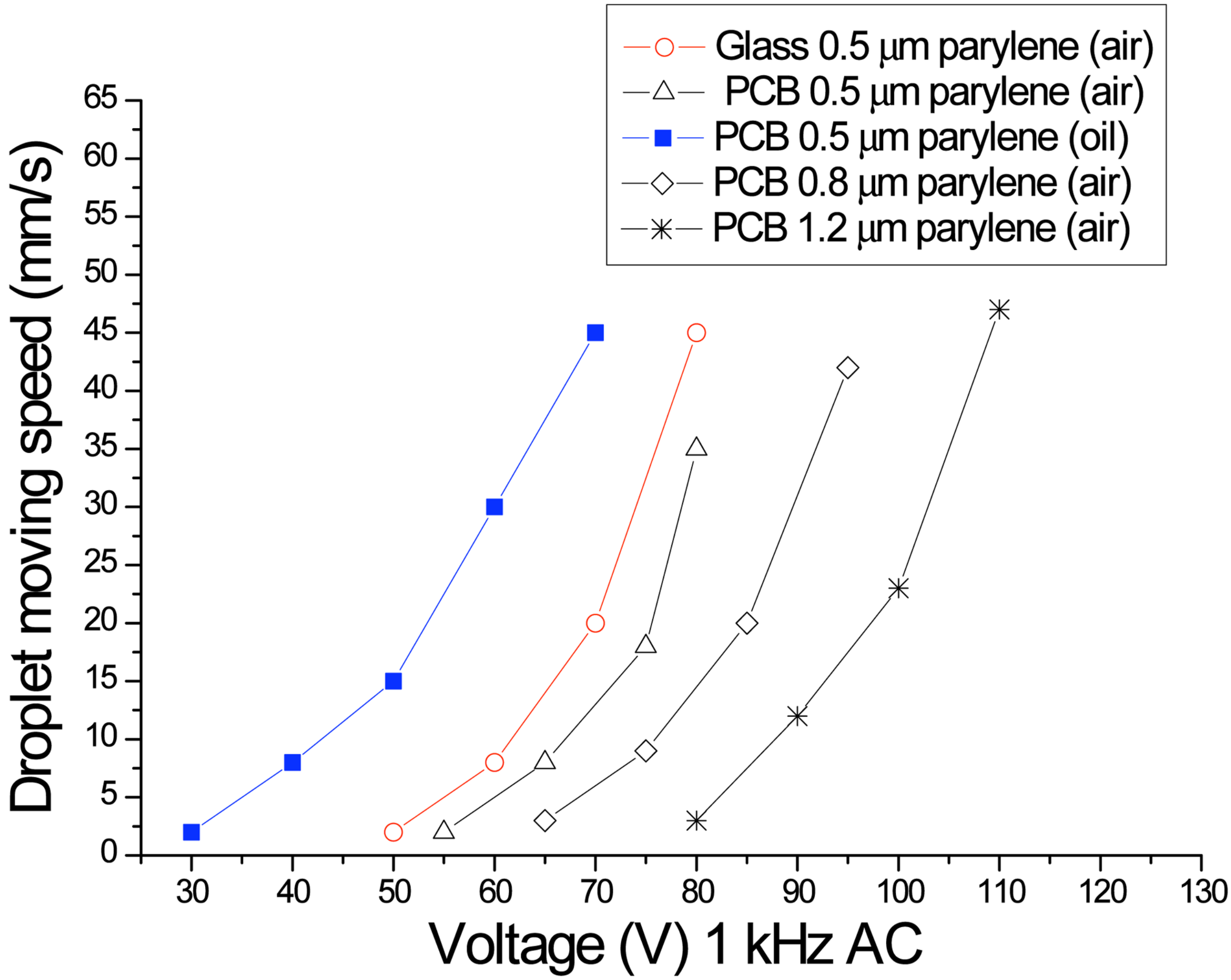

Fig. 4.

Moving speed of droplet vs. driving voltages measured on Type-4 PCB-EWOD plates with different dielectric thicknesses. Tests in oil environment and a glass device are added for comparison.

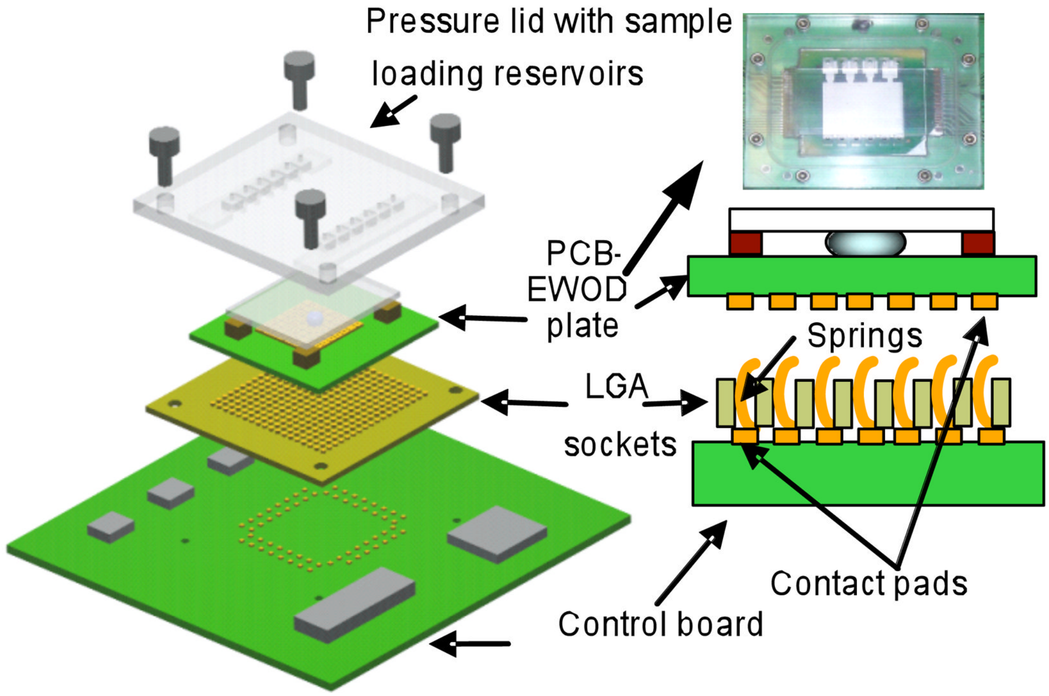

Fig. 5.
PCB EWOD device disposable package with LGA socket and pressure lid.

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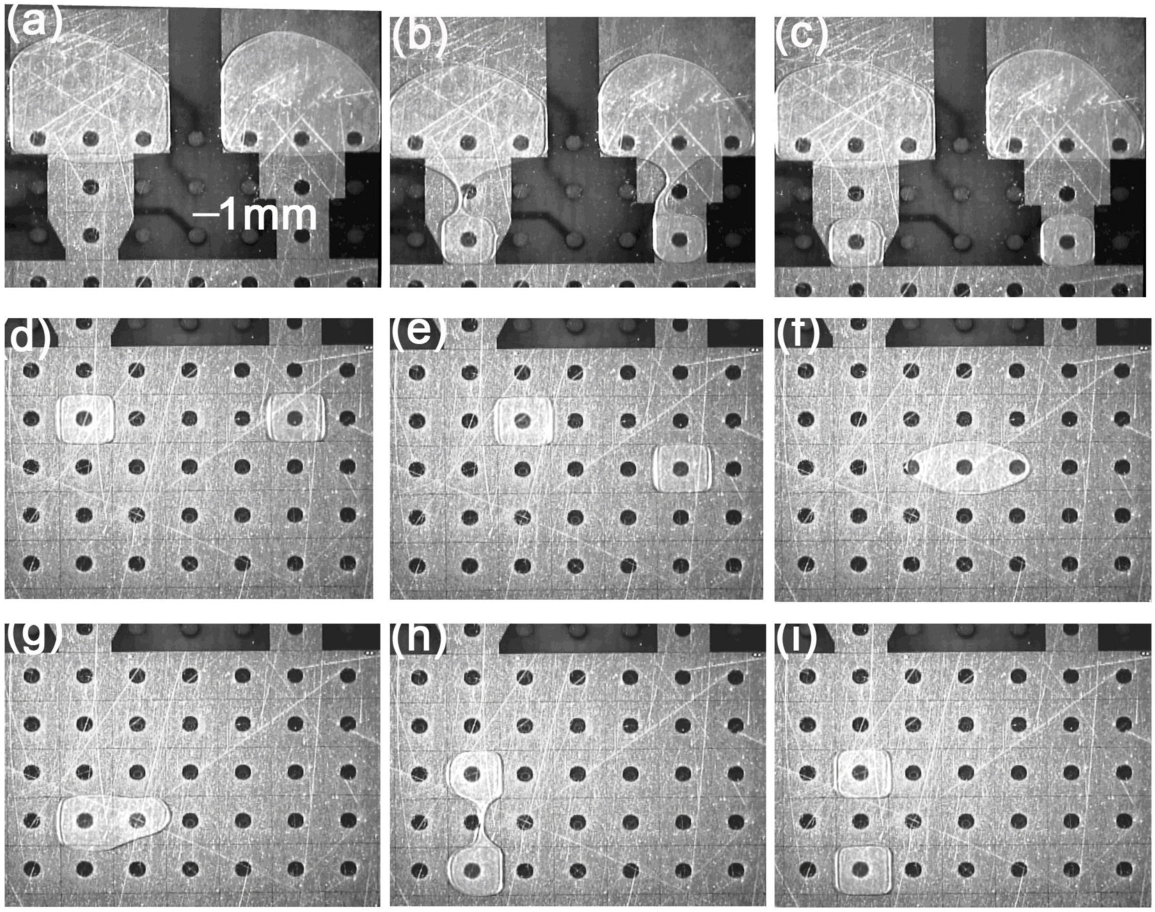

Fig. 6.

Demonstration of sequential microfluidics operations on 8x8 grids PCB-EWOD plate (type 4) using 80VAC at 1 kHz. (a–d) show that two droplets are created from two droplet reservoir and then transported on the two-dimensional surface. Subsequently they are merged, mixed and moved as one large droplet together (e–g). Finally they are cut into two small droplets (h, i).

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TABLE I

Comparison of IC, PCB, plastic molding And in-house cleanroom technologies

Manufacturing technology	Fabrication method	Electrical compatibility	Typical feature size	Typical device size	Typical fabrication Cost
IC industry	Thin film planar & photolithography	2–10 layers	0.13–1 μm	1–10 mm	$31/cm^2$[a]
PCB	Electroplating & multi-layer lamination	2–30 layers	75–250 μm	1–100 cm	$0.021/cm^2$[b]
PDMS molding	Molding &soft lithography	1 layer	10 μm–10 mm	1–10 cm	Not commercial
In-house cleanroom	Thin film planar & photolithography	1–3 layers	2–100 μm	10–100 mm	$2 /cm^2$[c]

[a] Listed for MOSIS AMIS ABN (1.50 μm) two-metal-layer process from http://www.mosis.org/orders/prices/amis/price_domestic_amis_abn.html. With multilayer stacking, the price will increase as number of layers. Cost for mass production should be lower.

[b] Data for 60000 in^2 production fabrication for four-layer PCB. Source from http://www.ultimatepcb.com/price_sample.php.

[c] The price is quoted as 30 min chemical mechanical polishing (CMP) for thin film planar, l metal layer thin film deposition, photolithography and patterning with the UCLA Nanoelectronics Research Facility (Nanolab) and labor costs. With multilayer stacking, the price will increase with the number of layers. Cost for mass production should be lower.

TABLE II

EWOD operation voltage vs. Parylene thickness on Type-1 PCB-EWOD plate. A layer of Teflon (2000 Å) is covered on the Parylene for all the cases.

Parylene thickness (μm)	Operation voltage (V)	EWOD actuation	Electrolysis	Environment
1	70–80	Moves between two electrodes, but does not continue	Yes	Air
2	~200	Moves between two electrodes, but does not continue	Yes	Air
4	~400	Moves continuously	Some around the vias	Air
7	~500	Moves continuously	No	Air
7	~200	Moves continuously	No	Oil

TABLE III

Different EWOD substrates vs. surface property, EWOD performance and fabrication cost

Fabrication method	Surface topography	Surface roughness	Contact angle hysteresis	Driving voltage [a]	Moving speed [b]	Major fabrication cost
As-fabricated PCB (Fig. 1a)	75 µm trench and 200 µm via	15000 Å	34°	500 V [c]	N/A	PCB substrate
Wet etching (Fig. 3a)	Flat surface but 200 µm via	15000 Å	34°	70 V	6 mm/s	PCB + one-layer electrode process
CMP + filled vias (Fig. 3b)	Flat surface	5000 Å	28°	60 V	7.8 mm/s	PCB + CMP + one-layer electrode processes
CMP + filled vias + polymer (Fig. 3c)	Flat surface	100 Å	20°	55 V	13 mm/s	PCB + CMP + one-layer electrode processes
Glass or Si substrate	Flat surface	10 Å	13°	50 V	20 mm/s	Glass/Si + multilayer electrode processes +CMP

[a] Driving voltages are the minimum voltage to move droplets on 0.5 µm parylene device.

[b] Moving speeds are measured on 0.5 µm parylene devices driven by 70 V_{ac} at 1 kHz.

[c] 500 V is the minimum voltage for working devices with 7 µm parylene.