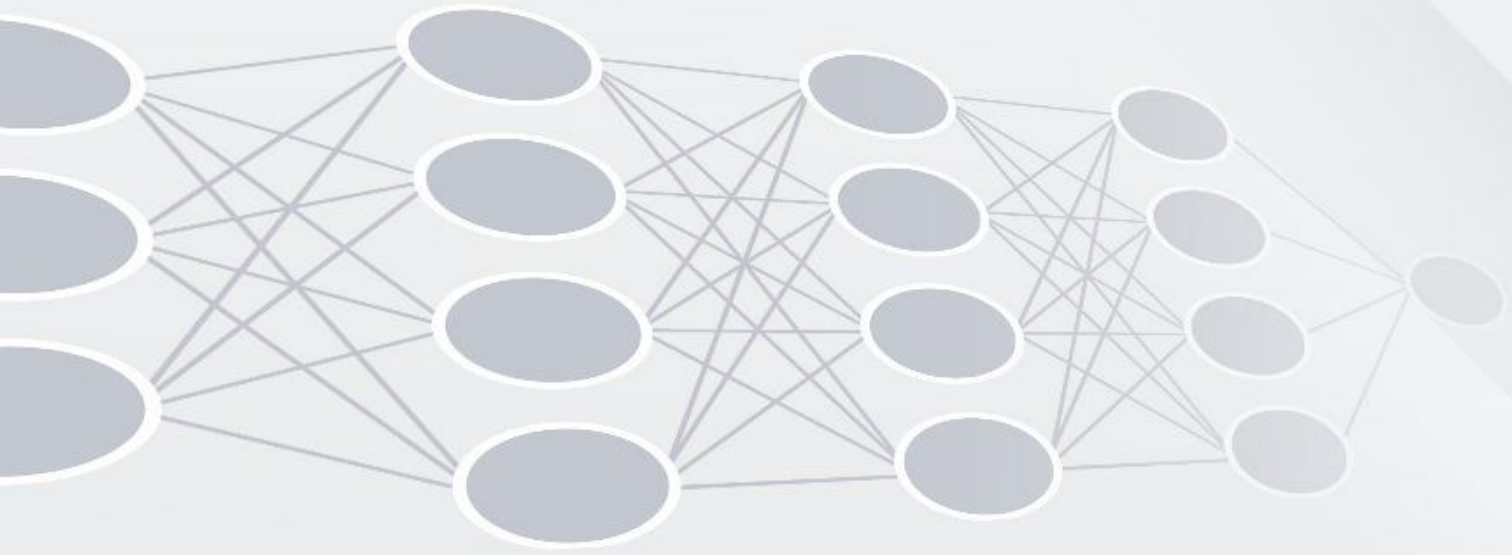
PIMIC

Listen™

VL130 Datasheet

Preliminary



About Documentation

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1 Introduction

1.1 General Description

VL130 is an advanced AI Keyword Spotting (KWS) SoC designed with next-generation processing-in-memory (PIM) technology. This breakthrough AI architecture offers significant enhancements in compute and power efficiency.

VL130 achieves remarkable power savings. The chip consumes 20uA as it listens for human voice and consumes less than 50uA running AI inferencing directly on an analog microphone output. This impressive power efficiency allows VL130 to perform AI KWS for years using just a coin-cell battery.

Overall, VL130's breakthrough PIM technology provides a significant advancement in power efficiency, enabling always-on, continuous, and reliable voice and time-series AI inferencing for diverse industrial and consumer edge device applications.

1.2 Features

- One wake word & 30 keywords detections
- Always-ON running for speech detection & recognition
- Power consumption of 20uA for always-listen and <50uA when inferencing for keywords.

1.3 Applications

- Smart glasses
- Wearables
- Headsets and true wireless earbuds
- Remote controls
- Smart appliances

2 System Architecture

VL130 contains 2 operational domains: the always-on or AON domain, and the on-off switchable or OOD domain. The AON domain consists of modules that will remain powered on during all operations of the chip. These include the I2C interface to the host, the audio pre-processing, and the VAD (Voice Activity Detect) modules.

During operation, the AON domain remains powered on to continuously monitor and pre-process the incoming audio stream from the analog microphone. When the audio pre-processor detects human voice, it turns on the OOD domain. AI inferencing of the voice stream will then be performed. If the inference found a pre-defined wake word or a key word, VL130 will assert the "Wake" signal and save the inferenced key word to the data registers in the AON domain for consumption by the host via the I2C interface.

2.1 Block Diagram

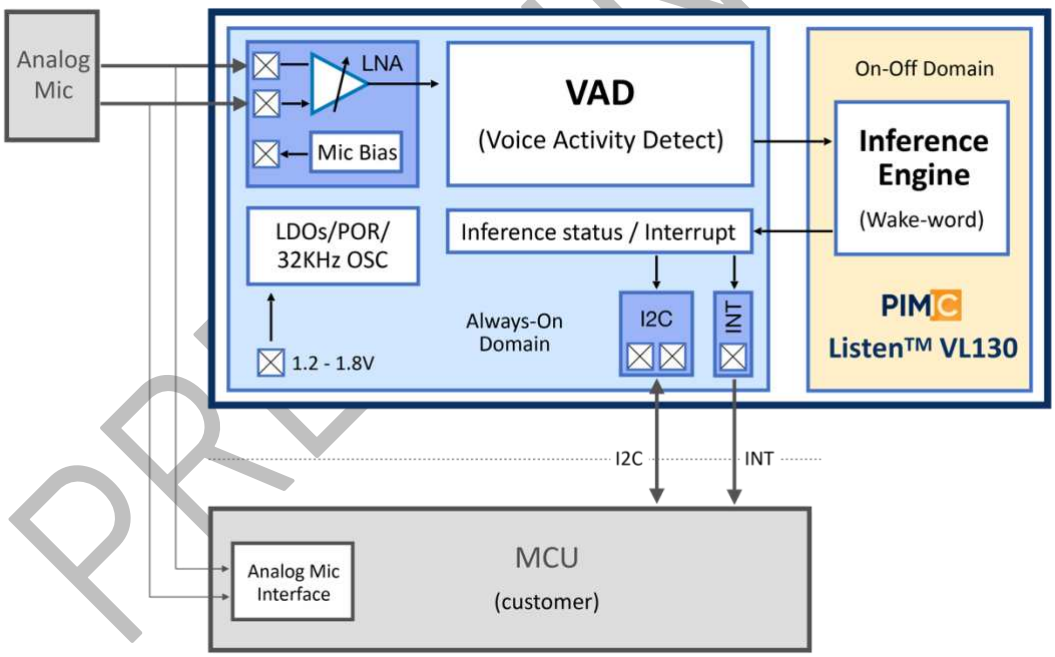

Figure 1: VL130 Block Diagram

3 Smart Microphone Application System

VL130 transforms a standard analog microphone module into a voice KWS smart microphone module. VL130 takes the output of the analog microphone, without interfering with the regular audio path, and performs AI inferencing on the microphone signal to detect occurrences of pre-defined wake word and key words. Upon spotting a pre-defined key word, the chip asserts the "wake" signal to the main processor (MCU in Figure **2**) and provides the inference results via the I2C interface to the MCU for further processing. In this configuration, VL130 enables the smart microphone module to continuously listen for key word occurrences in the incoming voice stream at extremely low power consumption, only waking up the more power-hungry MCU when necessary.

VL130 achieves this transformation without any design changes required at the system level involving the microphone module and subsequent processor.

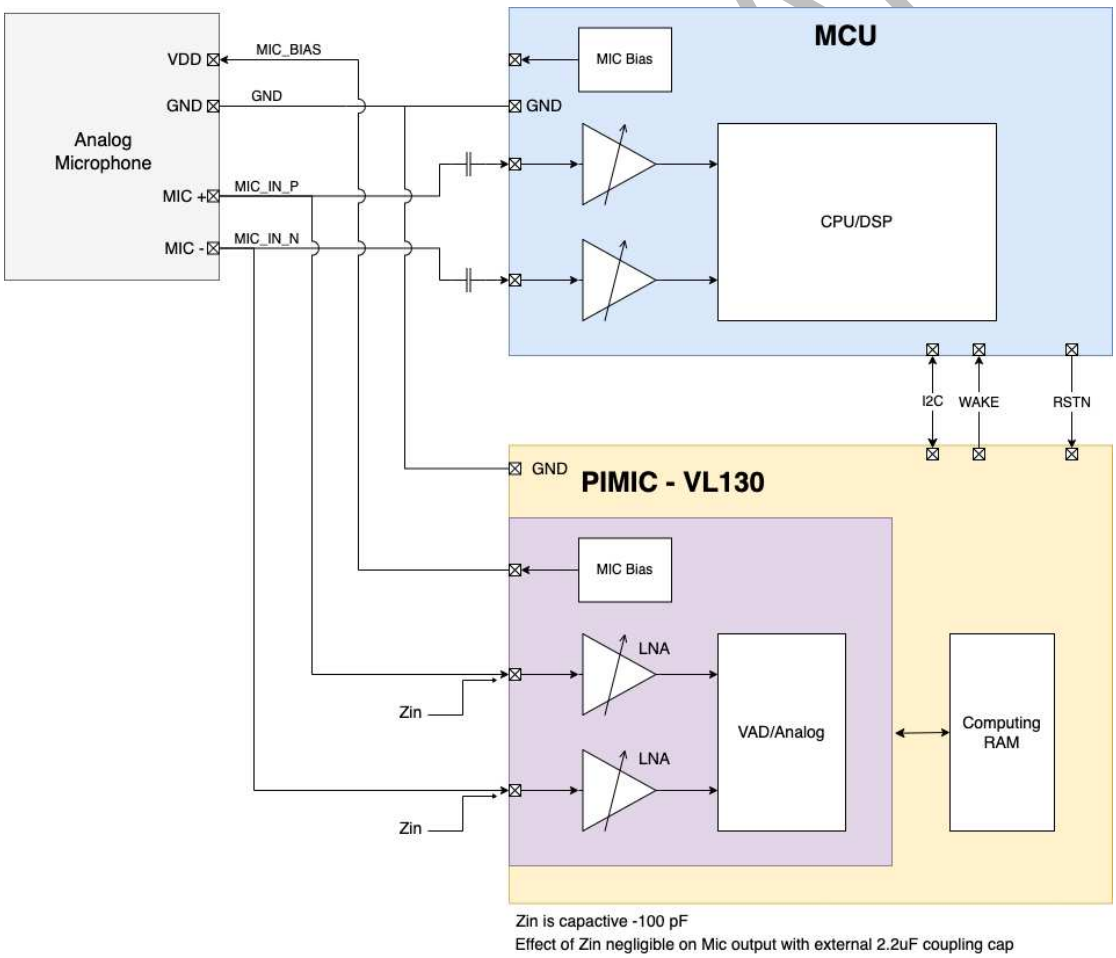

Figure 2: Microphone Input Block Diagram

4 DC Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Parameter	Value
Storage temperature	-55 °C to 150°C
Operating temperature	-20 °C to +85°C
Digital supply voltage range	1.62 V to 1.98 V
Analog supply voltage range	1.62 V to 1.98 V

4.2 Recommended Operating Conditions

Table 2: Power Supply Domains

Supply group	Description	Min	Typ	Max	Unit
VDD	Digital supply	1.62	1.8	1.98	V
AVD	Analog supply	1.62	1.8	1.98	V
BIAS	MIC BIAS	1.62	1.8	1.98	V

Table 3: Operating Temperature Ranges

Parameter	Min	Typ	Max	Unit
Ambient temperature	-20	25	85	° C
Junction temperature	-40	25	125	° C

4.3 Digital I/O Specifications

Table 4: Digital I/O Specifications @ typical conditions 1.8V, 25 deg C.

Parameter	Description	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	-0.3		0.3*VDD	V
V_{IH}	Input High voltage	0.9*VDD		VDD+0.3	V
V_{OL}	Output low voltage			0.7	V
V_{OH}	Output high voltage	0.9*VDD			V
I_{OH}	Output high drive current	4	8	13	mA
I_{OS}	Output standard drive current	5	9	14	mA
t_{LH}/t_{HL} (standard drive)	Rising time/Falling time @standard drive with 12pf load 10%~90%			4	ns
t_{LH}/t_{HL} (high drive)	Rising time/Falling time @high drive with 12pf load 10%~90%			3	ns
R_{PU}	GPIO Pull-up resistance		105K		Ω
R_{PD}	GPIO Pull-down resistance		107K		Ω

5 AC Electrical Characteristics

5.1 Clock Timing

VL130 integrates an on-die 32.768kHz RC oscillator and PLL and does not require an external clock to operate.

5.2 Voice Activity Detection (VAD) and Keyword AI Inferencing

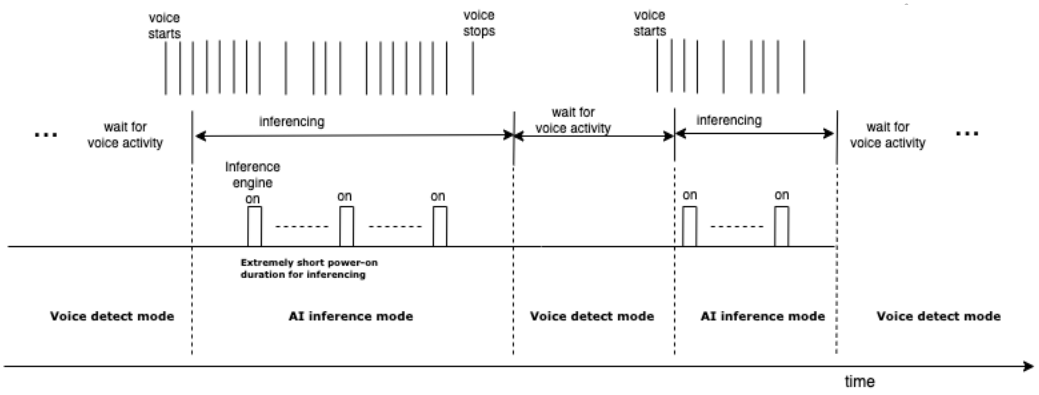

Figure 3: VAD and Keyword AI Inferencing Timing

VL130 saves power by dividing its operation into VAD (Voice Activity Detection) mode and AI inference mode. The chip continuously listens for human voice at extremely low power consumption levels. When human voice is detected, AI inferencing engine kicks in periodically for very short amount of time, owing to its highly efficient performance, to check if the voice stream contains any wake word or key word, until the voice activity stops. At that point, VL130 shuts down the inference engine to save power and goes back into the VAD always-listen mode for the next voice cycle and the mode operation repeats.

6 Pin and Signal Description

6.1 Pin Diagram

This pin assignment is preliminary and is subject to change.

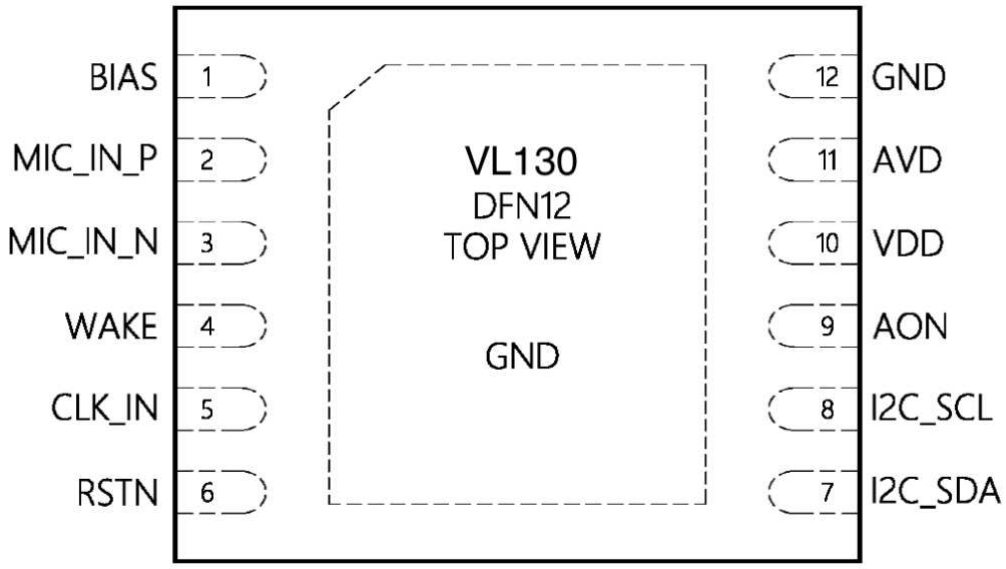

Figure 4: DFN12 Pin Diagram

6.2 Pin List

Table 5: VL130 Pin Definitions

Pin #	Pin name	Pin type	Description
1	BIAS	Analog	MIC BIAS
2	MIC_IN_P	Analog	MIC P port
3	MIC_IN_N	Analog	MIC N port
4	WAKE	Output	Wake up to host chip
5	CLK_IN	Input	Clock input (Only for debugging)
6	RSTN	Input	Reset (active low)
7	I2C_SDA	I/O	I2C data
8	I2C_SCL	Input	I2C clock
9	AON	Power	Always-on supply 0.8V generated by on-chip LDO (connect an external 1uF cap to VSS)
10	VDD	Power	Digital power supply 1.8V
11	AVD	Power	Analog power supply 1.8V
12	GND	Power	Ground
13	GND	Power	Ground (exposed pad)

6.2.1 BIAS

The VL130 provides one MIC bias pin, which can be used to power various microphones. It is recommended that the microphones do not draw more than 4mA from the MICBIAS pin. There are options for connecting internal 2 Kohm resistor to the microphone and for low noise or low power mode. If MICBIAS is used in low power mode, typically 100nF or 200nF capacitor can be used along with MIC Bias level at VDDA. In the low noise mode, external 1uF or 4.7uF capacitor can be omitted by register settings when MIC Bias is used to power analog microphones.

6.2.2 MIC_IN_P/ MIC_IN_N

The VL130 takes audio inputs from two pins MIC_IN_P and MIC_IN_N for differential analog microphone. For single output analog microphone, only MIC_IN_P is used. The VL130 only adds a small 100pF capacitive load to microphone so the audio effects is negligible.

6.2.3 WAKE

This signal is used to interrupt or wakeup the application processor when the Wakeword/Keyword is detected.

6.2.4 CLK_IN

The VL130 provides an option only for debugging purposes to use an externally supplied 32kHz clock for the chip. This signal is not used for normal operation.

6.2.5 RSTN

The VL130 provides an external hardware reset pin. Drive this pin to low and then high to reset VL130 via hardware signaling.

6.2.6 I2C_SDA/I2C_SCL

VL130 provides one slave I2C peripheral and supports the following features:

- Peripheral mode with ID: 0x5E.
- 7-bit addressing.

The I2C slave peripheral handles communication between NC100 and the host MCU.

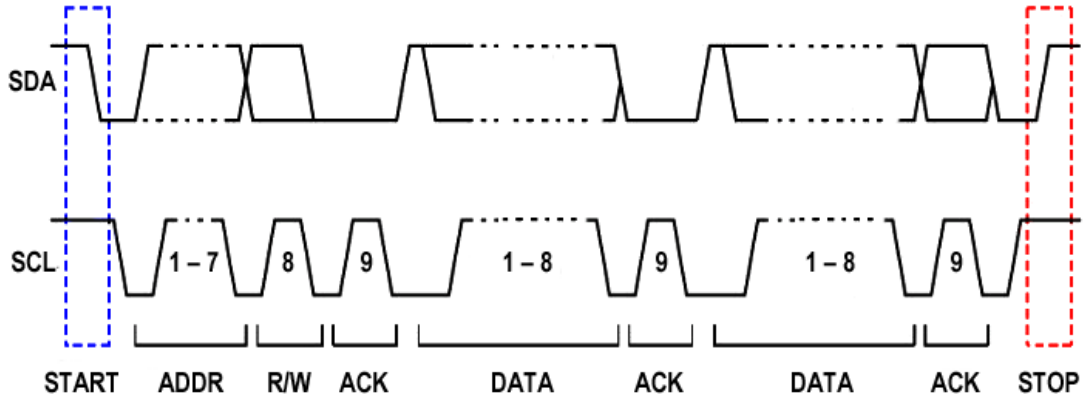

Figure 5: I2C Interface Signaling

The I2C interface consists of the SDA (data) and SCL (clock) signals.

An I2C operation begins with a START condition, which is a HIGH-to-LOW transition of I2C_SDA while I2C_SCL is HIGH (see Figure 5).

Following a START condition, the host device (host MCU) outputs an 8-bit sequence. The 8-bit sequence can represent a 7-bit device address to the peripheral device (for example, NC100) and a control bit, or it can simply represent an 8-bit data byte.

When it represents 7-bit address and control bit, the control bit indicates either a READ or a WRITE operation to the peripheral device. When the control bit is HIGH, it indicates the host is initiating a READ operation from the peripheral device. When the control bit is LOW, it means the host is initiating a WRITE operation to the peripheral device. If the 7-bit address matches the address of the peripheral device, the peripheral device will output an ACK (defined in the next section) during the 9th I2C_SCL clock period.

To allow for the ACK response, the host device releases the I2C_SDA bus after transmitting 8 bits. This action will result in the I2C_SDA bus to float HIGH (due to the pull-up resistors on the bus), allowing the peripheral device to drive the bus in the 9th I2C_SCL clock period, depending on the data transfer status as the following:

If the data transfer was successful, the peripheral device pulls the I2C_SDA line LOW to indicate to the host device that the data transfer was successful.

If the data transfer was not successful, the peripheral device does not drive the I2C_SDA and the I2C_SDA line therefore remains high to indicate a data transfer failure to the host device.

An I2C interface operation is terminated by a STOP condition, which is a LOW-to-HIGH transition of I2C_SDA while 12C_SCL is HIGH. A STOP condition at the end of a read or

write operation places the host device in a standby mode and leaves the I2C_SDA bus undriven (floats HIGH) to allow another host on the bus to drive the next data transfer.

7 Analog Microphone Inputs

As shown in Figure 6, the analog microphone inputs are connected to VL130 and the host MCU in the system with its BIAS provided by VL130.

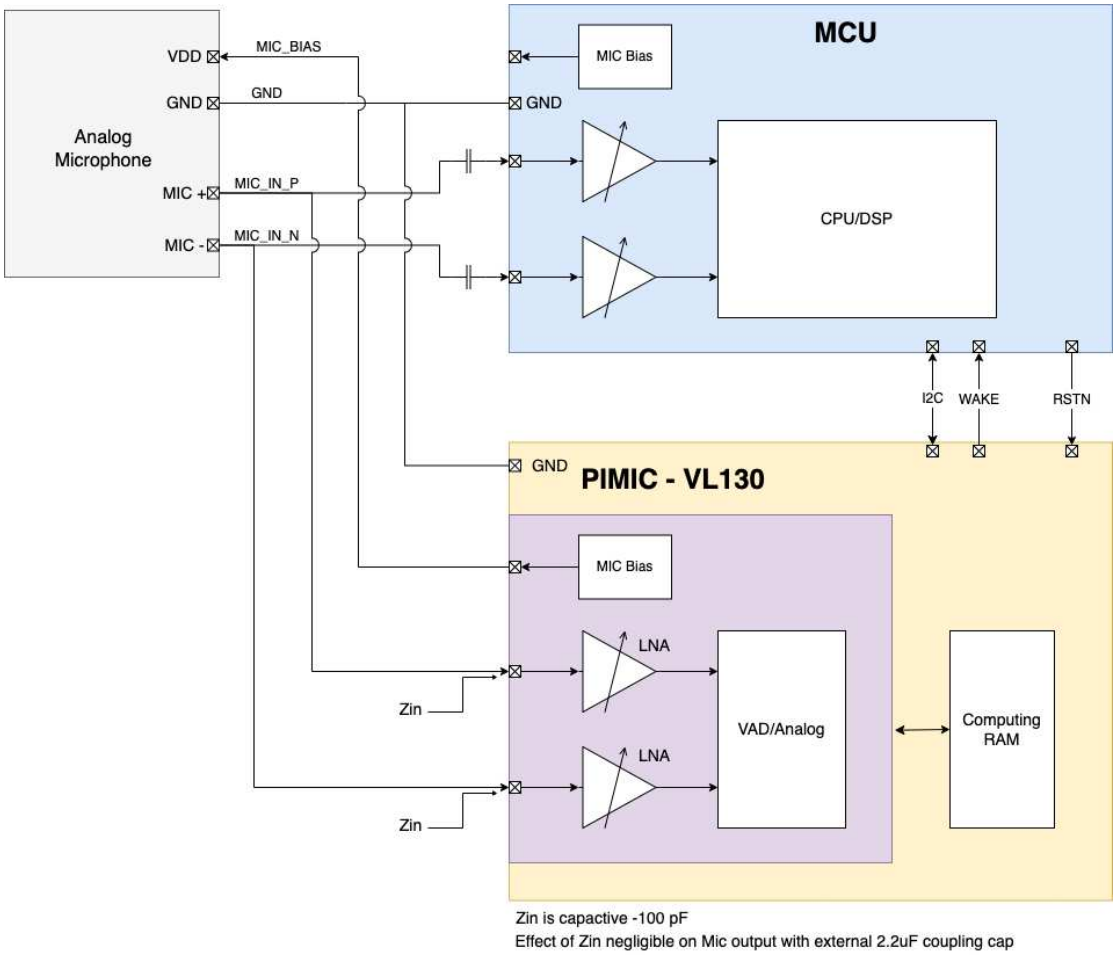

Figure 6: Microphone Input Block Diagram

8 Mechanical Information

8.1 DFN12 Package Dimensions

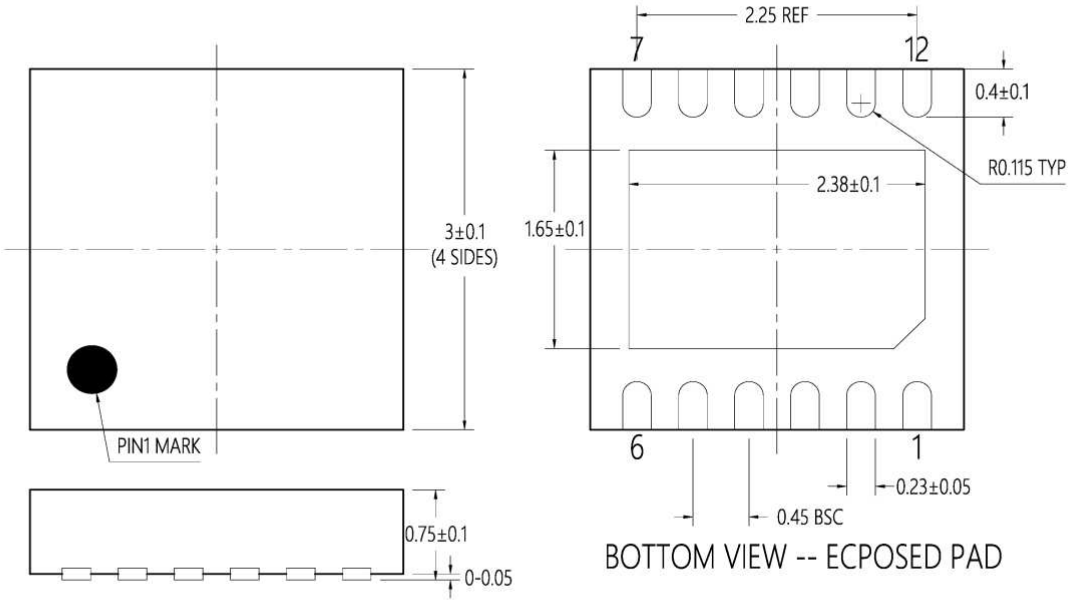

Figure 7: DFN12 Package Outline

8.2 DFN12 Solder Pad Pitch and Dimensions

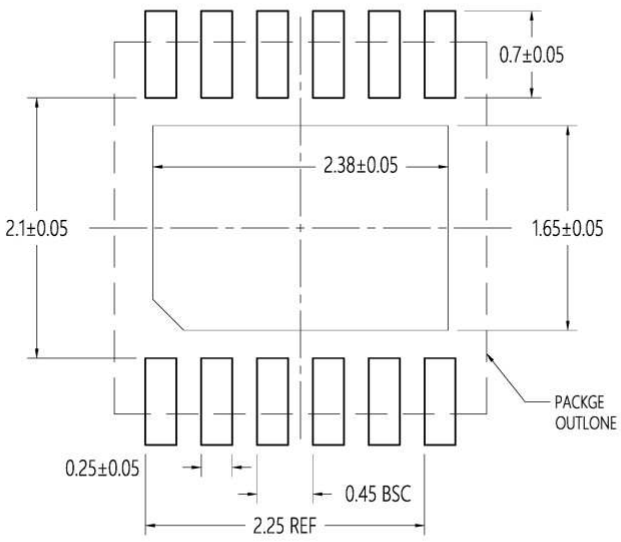

Figure 8: DFN12 Solder Pad Pitch and Dimensions

9 Reference Design

9.1 Signal-ended Output Analog Microphone

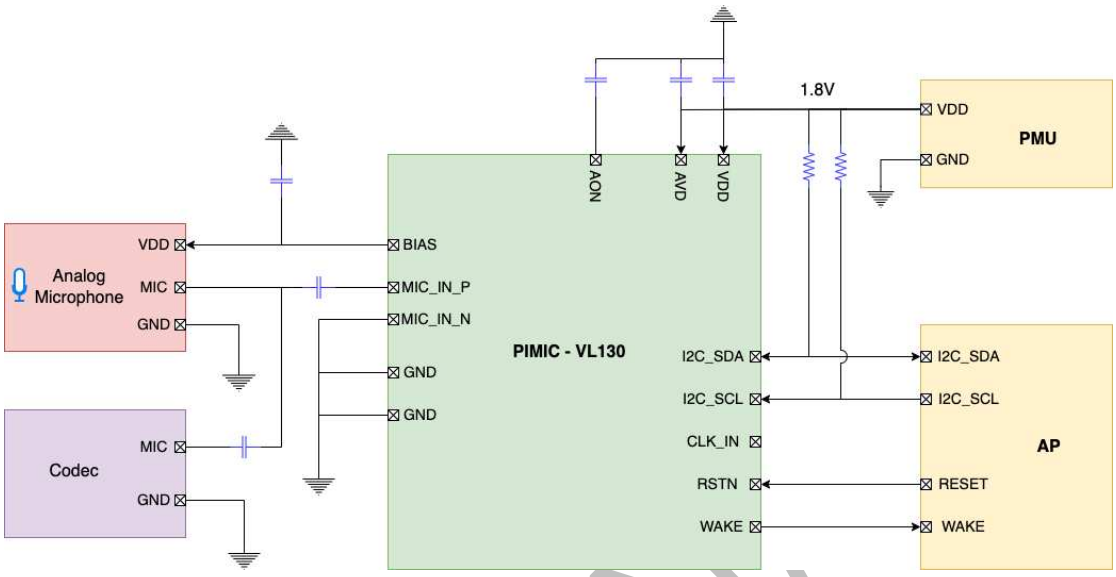

Figure 9: Single-ended Output Analog Microphone

9.2 Differential Output Analog Microphone

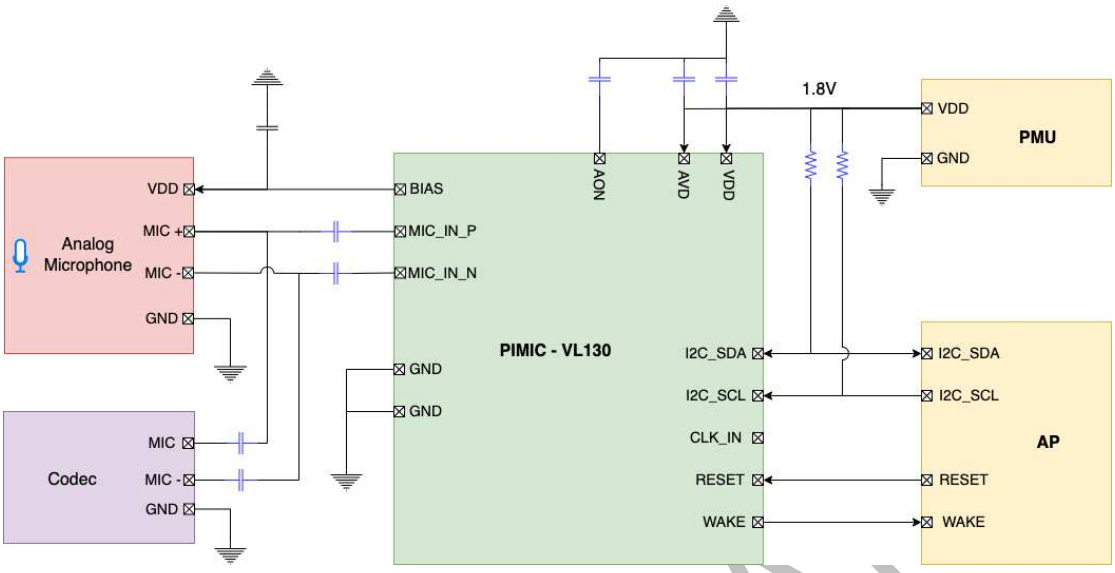

Figure 10: Differential Output Analog Microphone

Revision History

Revision	Description	Date
v1.0.0	Initial external release.	2024-05-15
V2.0.0	Part number and package update.	2024-05-19
v3.1.0	Updated package pins and features.	2024-05-24
V3.2.0	Updated diagrams and I2C operation descriptions, minor corrections.	2025-01-14

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