Clarity™ NC100 I2C Protocol and Registers

The Clarity chip uses a command-based I2C implementation. Every read/write transaction must be initiated with a write of the command to use, followed by the actual read/write, then terminated with a write of the clear command.

In the following instructions, steps with “to mimic our testbench” means that this step should not be necessary, but is included to mirror our regressions and known working setups.

I2C Defines

- Slave ID (Left Channel): **0x2A**
- Slave ID (Right Channel): 0x7F – 0x2A = **0x55**
- Read Set: **0x12**
- Read Clear: **0xED**
- Write Set: **0x10**
- Write Clear: **0xEF**

Single Read Example

Transaction 1

1) Start Bit
2) 7-bit Slave ID
3) Wr bit
4) ACK (from slave)
5) Read Set CMD
6) Register ADDR (1 Byte)
7) Stop Bit

Transaction 2

1) Start Bit
2) 7-bit Slave ID
3) Rd bit
4) ACK (from slave)
5) 4 Bytes Data (from slave)
6) Stop Bit

Transaction 3

1) Start Bit

2) 7-bit Slave ID
3) Wr bit
4) ACK (from slave)
5) Read Clear CMD
6) Read Clear CMD (x2 to mimic our testbench)
7) Stop Bit

Single Write Example

Transaction 1

1) Start Bit
2) 7-bit Slave ID
3) Wr bit
4) ACK (from slave)
5) Write Set CMD
6) Register ADDR (1 Byte)
7) Stop Bit

Transaction 2

1) Start Bit
2) 7-bit Slave ID
3) Wr bit
4) ACK (from slave)
5) Register ADDR
6) 4 Bytes Data (from master, MSB first)
7) One dummy byte (0x00) from master (to mimic testbench)
8) Stop Bit

Transaction 3

1) Start Bit
2) 7-bit Slave ID
3) Wr bit
4) ACK (from slave)
5) Write Clear CMD
6) Write Clear CMD (x2 to mimic our testbench)
7) Stop Bit

Registers and Working Values

The following registers should be written with the corresponding values as indicated in the table below for Clarity to perform environmental noise cancellation (ENC). While Clarity supports a range of PDM clock frequencies (please see the "Clarity™ NC100 Datasheet" for a list of PDM frequencies supported), for now, please set PDM clock frequency to 3.072MHz.

Register address	Purpose	Required value	Remark
0x3	PDM frequency	0x0 - 0x3 (Default 0x3)	0) 768kHz 1) 1.536MHz 2) 2.304MHz 3) 3.072MHz
0x5	Operation mode (Enable ENC)	0x0 or 0x2	0x0) Set to ENC mode 0x2) Set to Bypass mode (no ENC)
0xF	PDM mode	0x0	

The following register(s) is optional. Use only when necessary.

Register address	Purpose	Default value	Remark
0x6 (bits 12:3)	PDM2PCM_CTL GAIN	0x24 (bits 12:3) or decimal 36	Input gain control. Use read-modify-write to only write specific bits

This gain value may need to be tuned depending on the microphone used and the amplitudes of the incoming audio stream and noise content. This gain implementation is a naive version for testing and is not meant to replace an amplifier in production.

Revision History

Revision	Description	Date
V1.0	First release	2025/1/4
V1.1	Added GAIN register	2025/2/10
V1.2	Clarify ADDR width and gain values, add supported frequencies	2025/6/16