Victor Isaac Torres Muro

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Summary

Pursuing a M.S. in Computer Engineering with experience in manufacturing at the automotive industry. Currently performing computer vision, machine learning and FPGA research as a Research Assistant at Arizona State University. Seeking a full-time position starting Summer 2022.

Technical Skills

Programming: Python (Pytorch, Torchvision, Tensorflow, OpenCV), C++ (basic), MATLAB-Simulink

Other applications: Linux, Command Line, Git, Vitis AI, Vivado, AutoCAD, Solidworks, Microsoft Office

Education

M.S. Computer Engineering – Arizona State University, Tempe, AZ August 2020 – May 2022
GPA: 3.8 / 4.0 | **Courses:** VLSI, HW Acceleration and FPGAs, Machine Learning, Machine Vision, Computational Imaging

B.S. Mechatronic Engineering – ITESM, Cd. Juárez, México August 2013 – May 2018
GPA: 94 / 100 | **Study Abroad semester:** Hochshule Esslingen, Germany

Research and Academic Projects

- **Research: Adaptive subsampling** – Implemented adaptive subsampling pipeline involving deep learning (YoloV3, tinyYoloV3, ECO) and classical computer vision algorithms on a Xilinx FPGA board.
- **Research: Event camera object tracker** – Trained off-the-shelf neural networks to detect objects recorded using neuromorphic camera dataset. Leveraged use of representation techniques found in literature (voxel-grid, reconstruction from events). Using Pytorch and torchvision libraries.
- **Class Project (Machine Learning): Object tracker –** Trained custom CNN to perform detection and classification of MNIST digits captured with an event camera. Using Tensorflow deep learning library.
- **Class Project (Computational Imaging): Denoising NN –** Trained UNet to correct noisy images. Custom dataset generated by simulating photon-shot noise, read noise and ADC noise. Using Pytorch and torchvision libraries.
- **Class Project (VLSI): Convolution + Max-pooling engine design** – Developed a 4x4 convolution engine for deep learning applications and implemented on 7nm CMOS technology. Wrote behavioral System Verilog module. Synthesized using Design Compiler. Performed place-and-route using Innovus. Accomplished DRC and LVS clean in Virtuoso. Assured functional verification at every step.

Professional Experience

Research Assistant – Imaging Lyceum at ASU August 2020 – Current
- Deploying computer vision and machine learning algorithms on FPGAs.
- Improving imaging for outdoor robotic vision applications with neuromorphic (event) cameras.

Product Coordinator – Robert Bosch GmBH August 2017 – October 2019
- Responsible for all activities related to Manufacturing Engineering of Electronic Control Units (ECUs).
- Engineering change management implementation for existing products.
- Coordination of trial runs to meet project deliverables (i.e. Initial samples, EWAK-series, PV-runs).

Awards

- **Fulbright-García Robles scholarship** – Binational sponsored grant to study master's degree in the US.