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Letter of Support for Junliang Hu

Overseas Research Attachment Programme

Dear Members of the Engineering Panel,

I am pleased to confirm my support for Junliang Hu, Ph.D. candidate at The Chinese University of Hong Kong (CUHK), who intends to participate in the Overseas Research Attachment Programme (ORAP) and conduct research under my mentorship at Virginia Tech.

Junliang Hu will be attached to my research group from June, 2025 to December, 2025. During this time, they will work on tiered memory systems support for modern cloud environment, which aligns well with our ongoing research in enhancing systems support for modern and emerging hardware. I am confident that this collaboration will be mutually beneficial, contributing to Junliang Hu's academic growth while also advancing our research efforts.

To facilitate Junliang Hu's research activities, our institution will provide access to laboratory facilities, computing resources, and hardware equipment accesses. We will also provide academic support of regular one-on-one meetings and community integration through introduction to relevant researchers in our department and broader research network who work on related topics.

I am confident that Junliang Hu possesses the necessary technical background and research potential to make significant contributions during this attachment. Our research environment will provide an excellent platform for broadening their research horizons while establishing valuable international collaborations that will benefit both institutions.

Sincerely,

Huaicheng Li

Bio: Huaicheng Li is an Assistant Professor in the Department of Computer Science at Virginia Tech. Before joining VT, he earned his Ph.D. in Computer Science from the University of Chicago in 2020 and completed a two-year postdoctoral fellowship at CMU's Parallel Data Lab (PDL).

His research group focuses on building systems-level support for emerging storage and memory hardware technologies, optimizing workloads for enhanced performance predictability, efficiency, and programmability. His work has been recognized with several prestigious awards, including an NSF CAREER Award (2024), an IEEE Micro Top Picks 2024 Honorable Mention, a Distinguished Paper Award at ASPLOS (2023), a Best Paper Award at SYSTOR (2022), and two Best Paper nominations at FAST (2017 and 2018).