Model Question Paper- I with effect from 2022

CBCS SCHEME

First/ Second Semester B.E Degree Examination, _____

Basic Electronics (BBEE103/203)

TIME: 03 Hours Max.Marks:100

Notes:

- 1. Answer any FIVE full questions, choosing at least ONE question from each MODULE
- 2. VTU Formula Hand Book is Permitted
- 3. M: Marks, L: Bloom's level, C: Course outcomes.

		Module - 1	M	L	C
Q.1	a	Explain forward and reverse biasing VI characteristics of PN junction.	6	L2	CO1
	b	A Zener diode has a breakdown voltage of 10V. it is supplied from a voltage source varying between 20 to 40 V in series with a resistance of 820Ω . Using ideal Zener diode model obtain minimum and maximum zener currents.	7	L2	CO1
	c	With neat circuit diagram and waveforms explain the working of bridge rectifier.	7	L2	CO1
		OR			
Q.2	a	Explain how zener diode can be used as a voltage regulator.	6	L2	CO1
	b	Explain with neat diagram and waveform working of the half wave rectifier and also derive an expression for the efficiency and ripple factor	7	L2	CO1
	c	In a full-wave rectifier, the input is from 30-0-30 V transformer. The load and diodeforward resistance are 100 Ω and 10 Ω respectively. Calculate the average load current, average load voltage and rectifier efficiency.	7	L2	CO1
		Module – 2			
Q.3	a	Explain input and output characteristics of the common emitter configuration	6	L2	CO2
	b	Make use of N-channel enhancement type MOSFET and describe the	7	L2	CO2
	c	Explain various currents and voltages flowing through the BJT transistor.	7	L3	CO2
		OR			
Q.4	a	Explain the transistor biasing circuit with relevant expressions.	7	L2	CO2
	b	characteristics.	7	L2	CO2
	c	Define α and β . Determine the relationship between α and β	6	L2	CO2

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		Module – 3			
Q5	a	Briefly discuss the ideal characteristics of the Opamp.	7	L2	CO2
Ų	b	Design the circuit diagram for the output voltage $Vo = -5(0.1V_1 + .2V_2 + 10V_3)$. Also draw the neat circuit diagram.	7	L3	CO2
	c	Derive an expression for integrator or differentiator.	6	L2	CO2
		OR			
Q.6	a	Design the circuit for the output voltage $v_o = 2 \int v_1 dt + 0.4 \frac{dv_2}{dt} + 10 v_3$	7	L2	CO2
	b	Derive an expression for integrator or differentiator.	6	L3	CO2
	c	Derive an expression for the 3 input summing circuit.	6	L2	CO2
		Module – 4			
Q.7	a	Solve a) $(725.25)_{10} = (?)_2 = (?)_{16}$ b) $(1111001111110001)_2 = (?)_8 = (?)_{16}$ Build the equation $Y = AB + CD + E$ to realize using	6	L2	CO3
	b	 a) NAND Gates b) NOR Gates 	7	L2	CO3
	c	Construct and describe Full Adder with neat logic diagram and truth table.	7	L3	CO3
		OR			
Q.8	a	State and prove <i>DeMorgan0s</i> theorem for three input variable.	6	L2	CO3
	b	Subtract (101) ₂ from (1101) ₂ using 1's and 2's complement method.	7	L3	CO3
	c	Construct and describe Half Adder with neat logic diagram and truth table.	7	L2	CO3
		Module – 5		_	_
Q.9	a	Explain potentiometric type transducer	6	L2	CO5
	b	A strain gauze with gauze factor of 2 is subject to a 0.28mmstarin. the wire dimensions are 50 cm length and 30 μ m diameter, and unstrained wire resistance is 55 Ω . Calculate the change in wire resistance and diameter if the entire length of the wire is strained positively.	7	L3	CO5
	c	Define Modulation Explain the need of modulation	7	L3	CO4
	•	OR			•
Q.10	a	Explain LVDT with relevant diagrams.	8	L3	CO5
A.10	b	A parallel plate capacitive transducer has a plate area $(l x w) = (40mm \times 40mm)$ and plate spacing d=0.5mm. Calculate the device capacitance and displacement that causes the capacitance to change by 5 pF. Also determine the transducer sensitivity,	5	L2	CO5
	c	Describe the blocks of the basic communication system.	7	L3	CO4