MINI-PROJECT’S REPORT

ROUND 2

LOGIC DESIGN (LAB) – CC01

__________ GROUP 9 __________

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CHAPTER 1: INTRODUCTION

1. TOPIC:

Running LEDs is usually used for decorating stores, buildings, companies. A Running LEDs circuit should support multiple running types.

Design and implementation a Decorative LED lights system on Altera DE2i-150 board.

Functionalities:

- Support at least 2 rules:

  - **Rule 1**: Leds start with a length of 3 at the right edge. Leds run from right to left, when the 3-led line to the left edge, leds navigation from left to right.
  - **Rule 2**: LEDs run from the two edges to middle until all LEDs are ON (bright), then turn OFF from left to right.

- Support at least 3 level of running speed on DE2I-150 (frequency): 1Hz, 2Hz, and 4Hz
(You can use higher frequencies for simulation)
- Display rule number, mode, speed on 7-segment LEDs.
- Support 2 mode: **automatic** (LEDs run from rule 1 -> rule 2 -> back to rule 1) and **hand control** (repeat one specified rule).

2. GOALS:

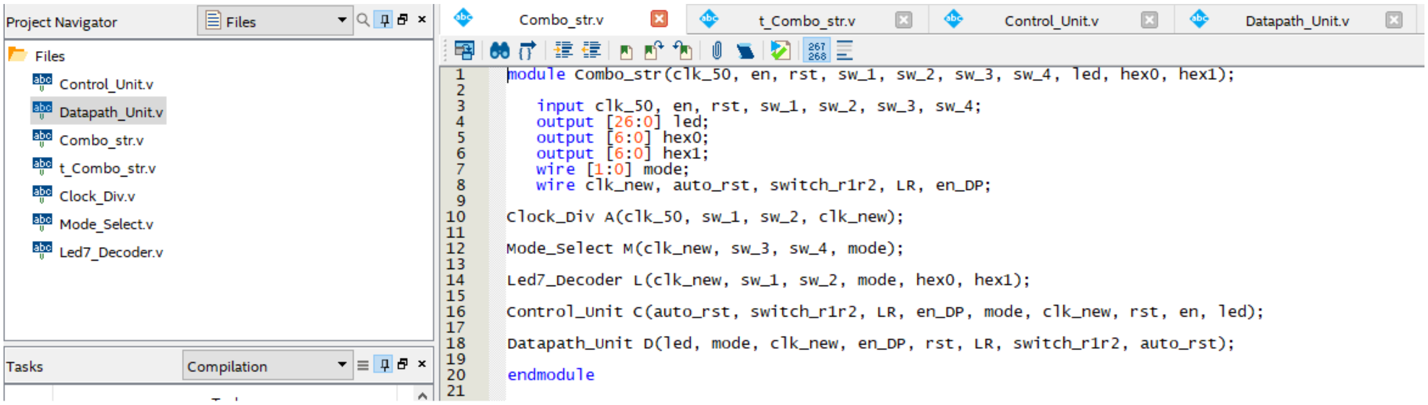
Practice and understanding:

- Edge trigger and Level trigger
- Blocking and non-Blocking assignment.
- Experiments on real FPGA technology – DE2I150 board

3. SOFTWARE AND HARDWARE USED:

Quartus Prime 19.1 Lite Edition, ModelSim and DE2i-150 FPGA board

4. INSTRUCTIONS:



```
module Combo_str(clk_50, en, rst, sw_1, sw_2, sw_3, sw_4, led, hex0, hex1);

   input clk_50, en, rst, sw_1, sw_2, sw_3, sw_4;
   output [26:0] led;
   output [6:0] hex0;
   output [6:0] hex1;
   wire [1:0] mode;
   wire clk_new, auto_rst, switch_r1r2, LR, en_DP;

Clock_Div A(clk_50, sw_1, sw_2, clk_new);

Mode_Select M(clk_new, sw_3, sw_4, mode);

Led7_Decoder L(clk_new, sw_1, sw_2, mode, hex0, hex1);

Control_Unit C(auto_rst, switch_r1r2, LR, en_DP, mode, clk_new, rst, en, led);

Datapath_Unit D(led, mode, clk_new, en_DP, rst, LR, switch_r1r2, auto_rst);

endmodule
```

(top-level entity module)

- **LEDs, switches, buttons and 7-segment LEDs used:**

    - All LEDs (18 LEDR + 9 LEDG) → [26:0] led
    - Switches:

SW[0], SW[1] (to select SPEED) → {sw_1, sw_2}

2’b01 (1 Hz), 2’b10 (2 Hz),

2’b11 (4 Hz), 2’b00 (50 MHz - board frequency)

SW[2], SW[3] (to select MODE) → {sw_3, sw_4}

2’b01 (repeat rule 1), 2‘b10 (repeat rule 2),

2’b11: (automatic), 2’b00: all LEDs are off.

- Buttons:

KEY[0] (reset) → rst, to set things ready or to switch modes

KEY[1] (enable) → en, to start running LEDs

- 7-seg LEDs:

HEX0 (display MODE) → [6:0] hex0

HEX1 (display SPEED) → [6:0] hex1

- **How it works: (pictures in Chapter 2 to demonstrate)**

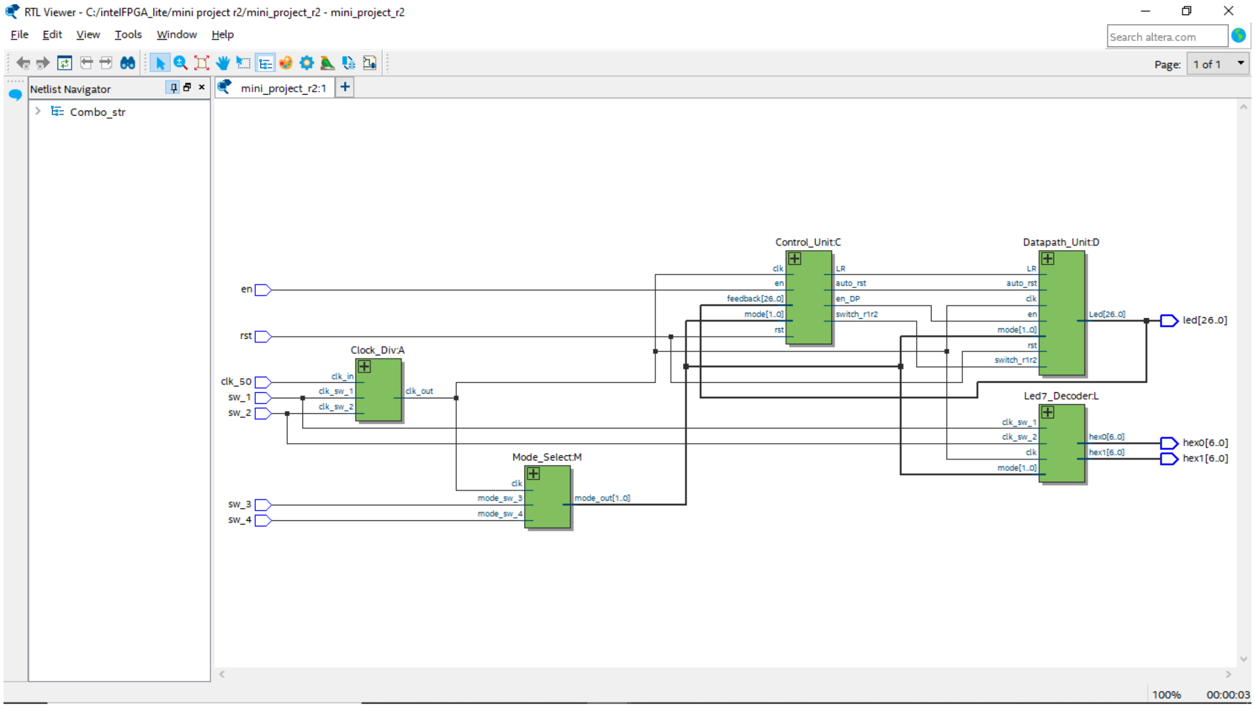
- MANUAL/AUTOMATIC: select SPEED, MODE, turn on rst for a second, then turn it off and press en.

For example: to run mode 1 (repeat rule 1) with frequency 50 MHZ, first turn off SW[0], SW[1], then turn off SW[2] and turn on SW[3], turn on KEY[0] for a second and turn it off, then hit KEY[1] to begin.

- SWITCHING MODEs: to switch among three modes manually, first run MODE 1 (or 2, 3), after a while, hit KEY[0] to set things ready, then select SWs to another MODE and turn off KEY[0] to begin.

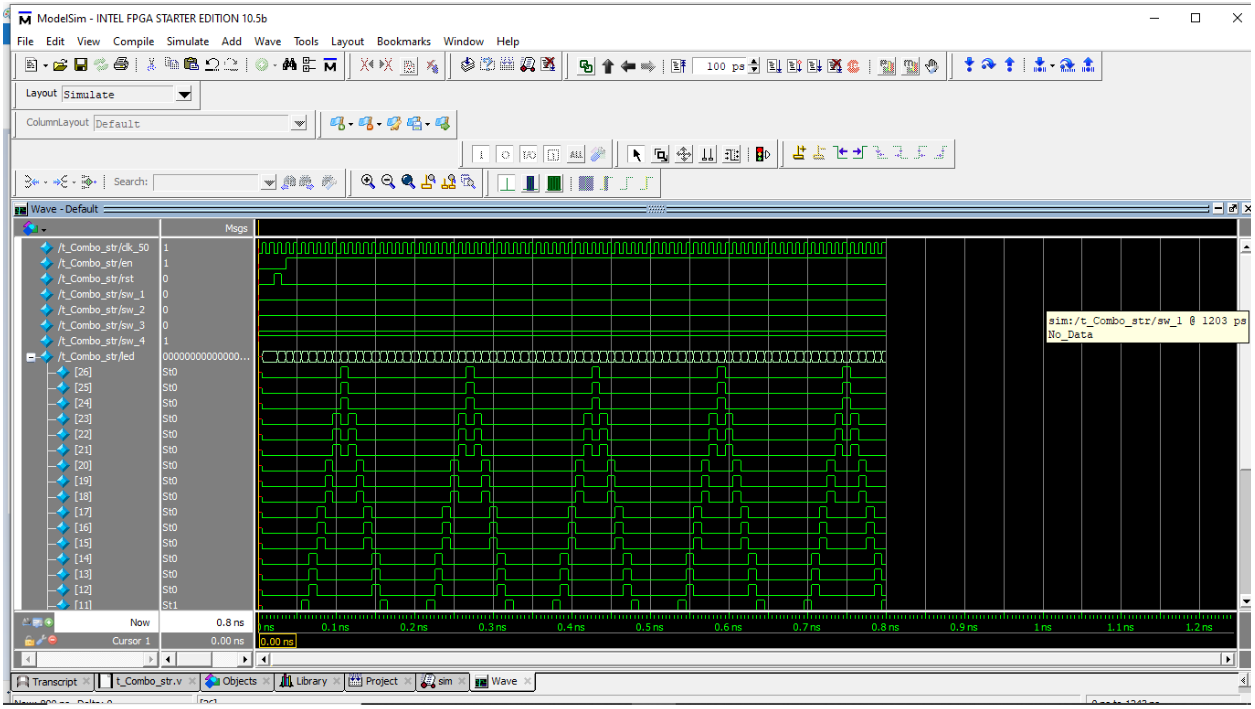
CHAPTER 2: DESIGN AND IMPLEMENT

RTL Viewer:



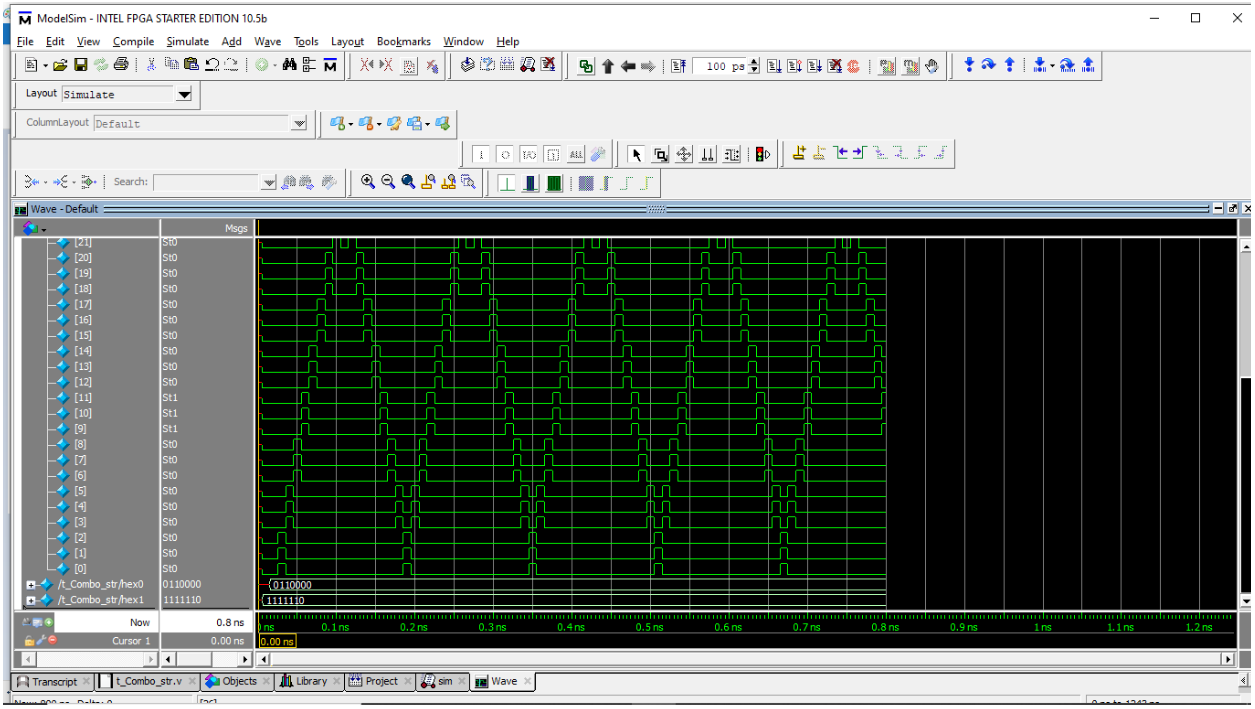
CHAPTER 3: EXPERIMENTS

MODE 1 (REPEAT RULE 1) - 50 MHZ

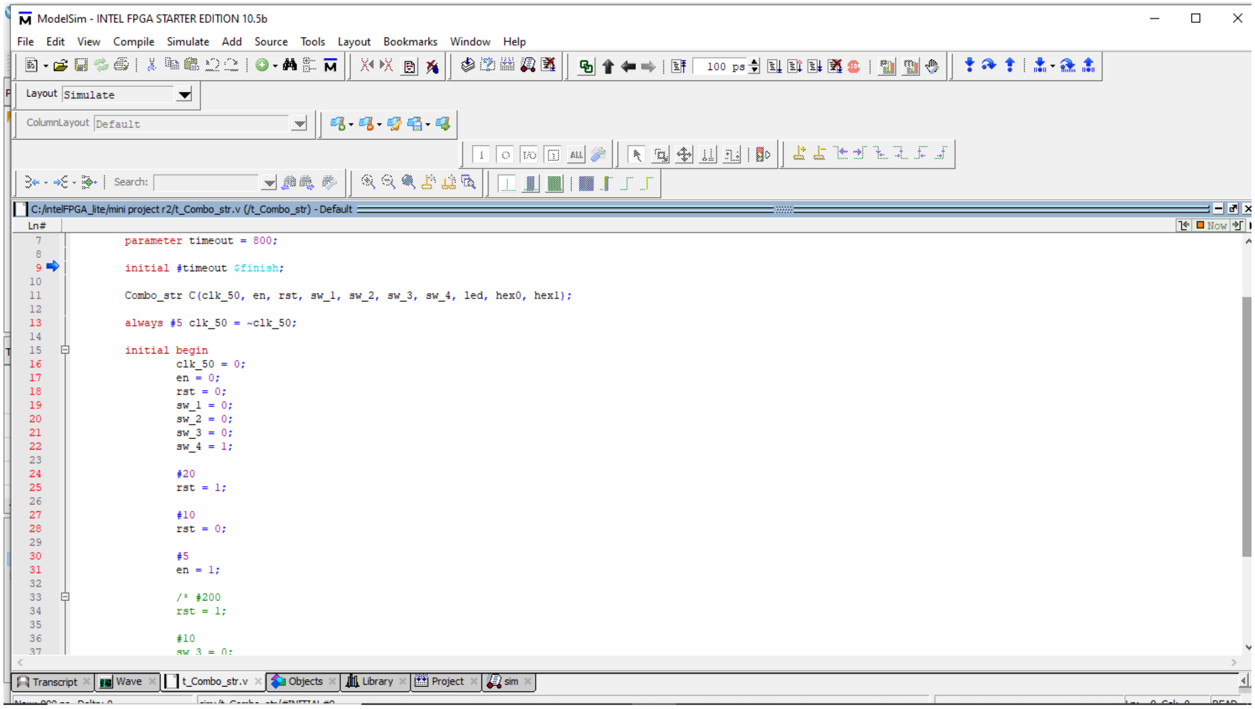

ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Layout Simulate
ColumnLayout Default
Search:
Wave - Default
Msgs
0 ns 0.1 ns 0.2 ns 0.3 ns 0.4 ns 0.5 ns 0.6 ns 0.7 ns 0.8 ns 0.9 ns 1 ns 1.1 ns 1.2 ns
Transcript t_Combo_str.v Objects Library Project sim Wave

	Msgs
/t_Combo_str/clk_50	1
/t_Combo_str/en	1
/t_Combo_str/rst	0
/t_Combo_str/sw_1	0
/t_Combo_str/sw_2	0
/t_Combo_str/sw_3	0
/t_Combo_str/sw_4	1
/t_Combo_str/led	00000000000000...
[26]	St0
[25]	St0
[24]	St0
[23]	St0
[22]	St0
[21]	St0
[20]	St0
[19]	St0
[18]	St0
[17]	St0
[16]	St0
[15]	St0
[14]	St0
[13]	St0
[12]	St0
[11]	St1
Now	0.8 ns
Cursor 1	0.00 ns

sim:/t_Combo_str/sw_1 @ 1203 ps
No_Data


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Layout Simulate
ColumnLayout Default
Search:
Wave - Default
Msgs
0 ns 0.1 ns 0.2 ns 0.3 ns 0.4 ns 0.5 ns 0.6 ns 0.7 ns 0.8 ns 0.9 ns 1 ns 1.1 ns 1.2 ns
Transcript t_Combo_str.v Objects Library Project sim Wave

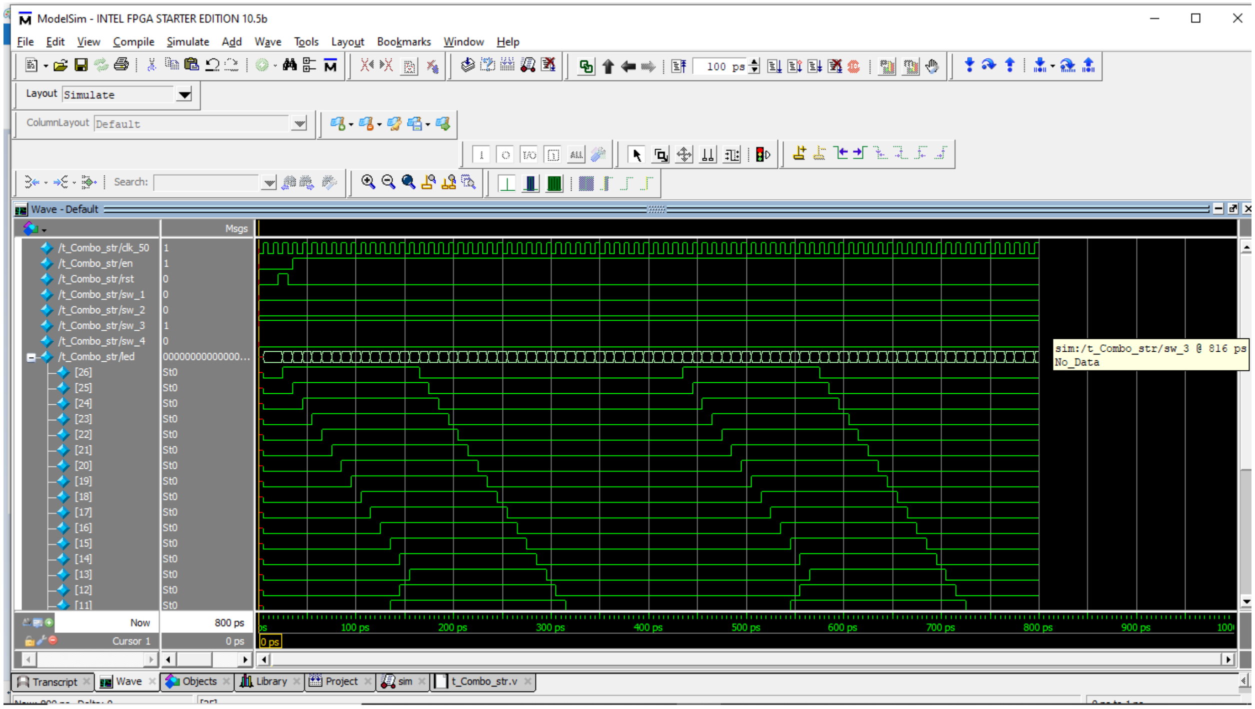
	Msgs
[21]	St0
[20]	St0
[19]	St0
[18]	St0
[17]	St0
[16]	St0
[15]	St0
[14]	St0
[13]	St0
[12]	St0
[11]	St1
[10]	St1
[9]	St1
[8]	St0
[7]	St0
[6]	St0
[5]	St0
[4]	St0
[3]	St0
[2]	St0
[1]	St0
[0]	St0
/t_Combo_str/hex0	0110000
/t_Combo_str/hex1	1111110
Now	0.8 ns
Cursor 1	0.00 ns


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Layout Simulate
ColumnLayout Default
Search:
C:/intelFPGA_lite/mini project r2/t_Combo_str.v (/t_Combo_str) - Default
Ln#
Transcript
Wave
t_Combo_str.v
Objects
Library
Project
sim

```
        parameter timeout = 800;

        initial #timeout $finish;

        Combo_str C(clk_50, en, rst, sw_1, sw_2, sw_3, sw_4, led, hex0, hex1);

        always #5 clk_50 = ~clk_50;

        initial begin
                clk_50 = 0;
                en = 0;
                rst = 0;
                sw_1 = 0;
                sw_2 = 0;
                sw_3 = 0;
                sw_4 = 1;

                #20
                rst = 1;

                #10
                rst = 0;

                #5
                en = 1;

                /* #200
                rst = 1;

                #10
                sw_3 = 0;
```

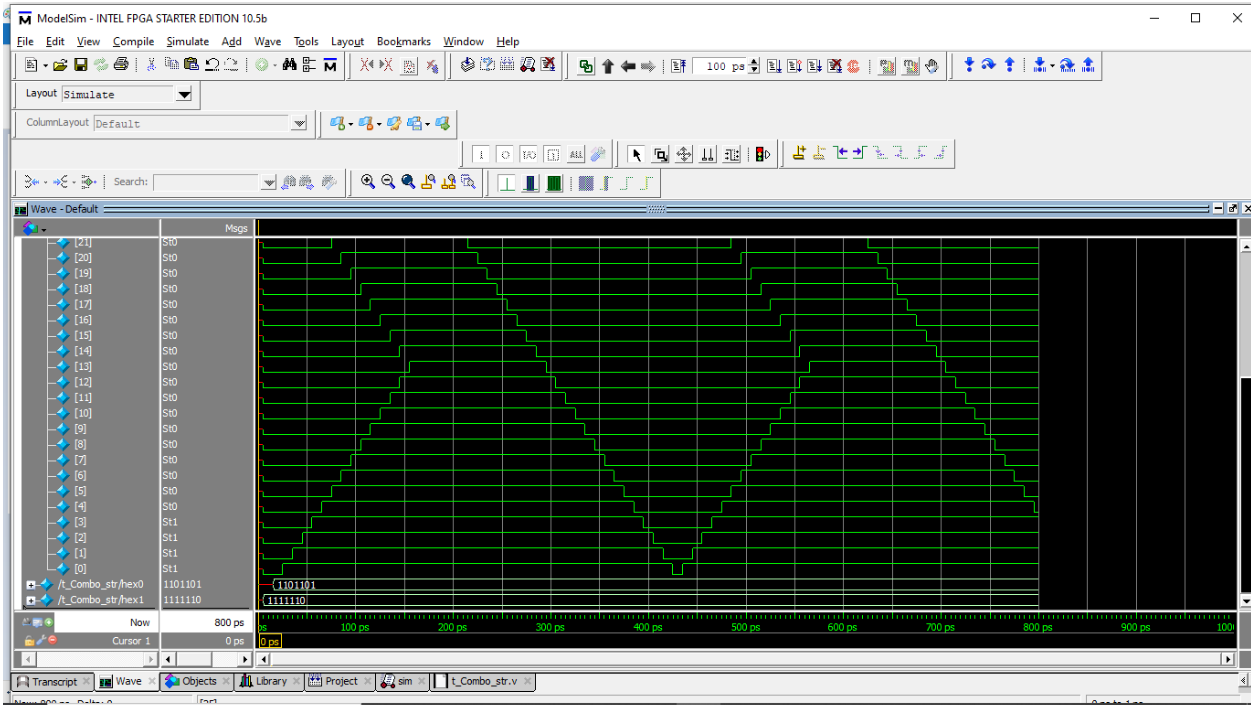
(testbench for mode 1)

MODE 2 (REPEAT RULE 2) – 50 MHZ

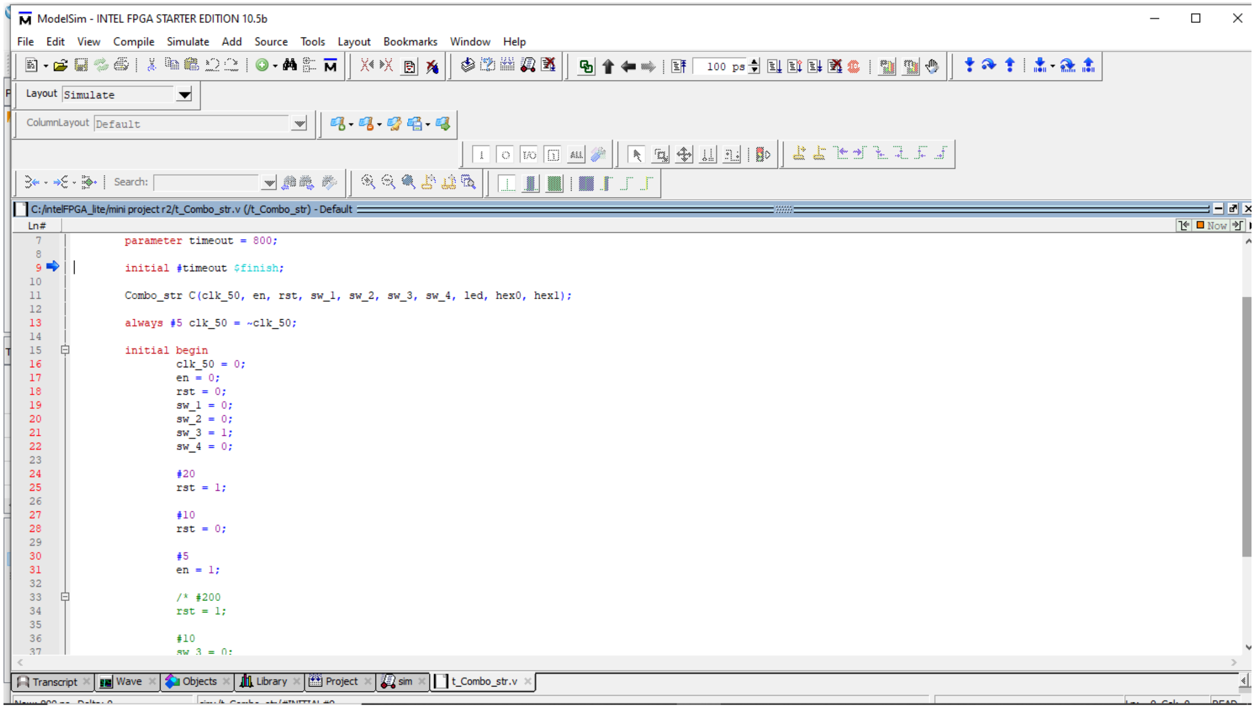


```
/t_Combo_str/clk_50   1
/t_Combo_str/en       1
/t_Combo_str/rst      0
/t_Combo_str/sw_1     0
/t_Combo_str/sw_2     0
/t_Combo_str/sw_3     1
/t_Combo_str/sw_4     0
/t_Combo_str/led      00000000000000...
  [26]                St0
  [25]                St0
  [24]                St0
  [23]                St0
  [22]                St0
  [21]                St0
  [20]                St0
  [19]                St0
  [18]                St0
  [17]                St0
  [16]                St0
  [15]                St0
  [14]                St0
  [13]                St0
  [12]                St0
  [11]                St0
Now                   800 ps
Cursor 1              0 ps
```

```
sim:/t_Combo_str/sw_3 @ 816 ps
No_Data
```



	Msgs
[21]	St0
[20]	St0
[19]	St0
[18]	St0
[17]	St0
[16]	St0
[15]	St0
[14]	St0
[13]	St0
[12]	St0
[11]	St0
[10]	St0
[9]	St0
[8]	St0
[7]	St0
[6]	St0
[5]	St0
[4]	St0
[3]	St1
[2]	St1
[1]	St1
[0]	St1
/t_Combo_str/hex0	1101101
/t_Combo_str/hex1	1111110
Now	800 ps
Cursor 1	0 ps

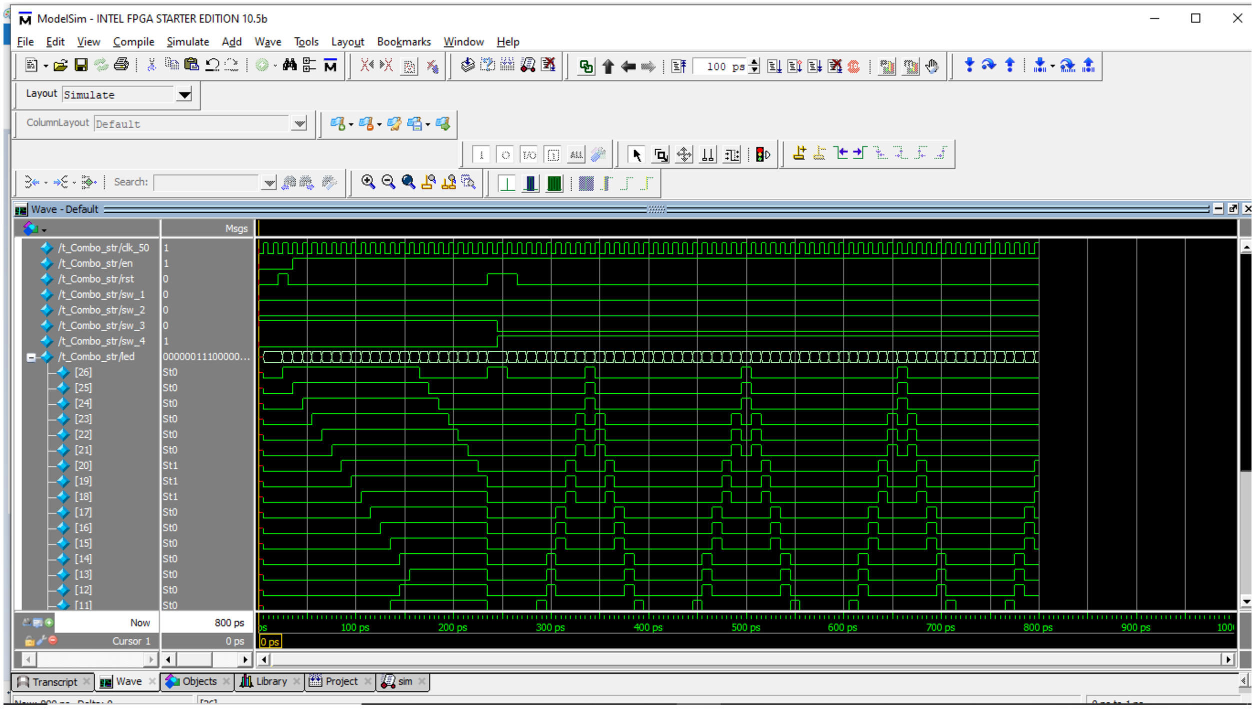

ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Layout Simulate
ColumnLayout Default
Search:
Ln#
Transcript
Wave
Objects
Library
Project
sim
t_Combo_str.v

C:/intelFPGA_lite/mini project r2/t_Combo_str.v (/t_Combo_str) - Default

```
        parameter timeout = 800;

        initial #timeout $finish;

        Combo_str C(clk_50, en, rst, sw_1, sw_2, sw_3, sw_4, led, hex0, hex1);

        always #5 clk_50 = ~clk_50;

        initial begin
                clk_50 = 0;
                en = 0;
                rst = 0;
                sw_1 = 0;
                sw_2 = 0;
                sw_3 = 1;
                sw_4 = 0;

                #20
                rst = 1;

                #10
                rst = 0;

                #5
                en = 1;

                /* #200
                rst = 1;

                #10
                sw_3 = 0;
```

(testbench for mode 2)

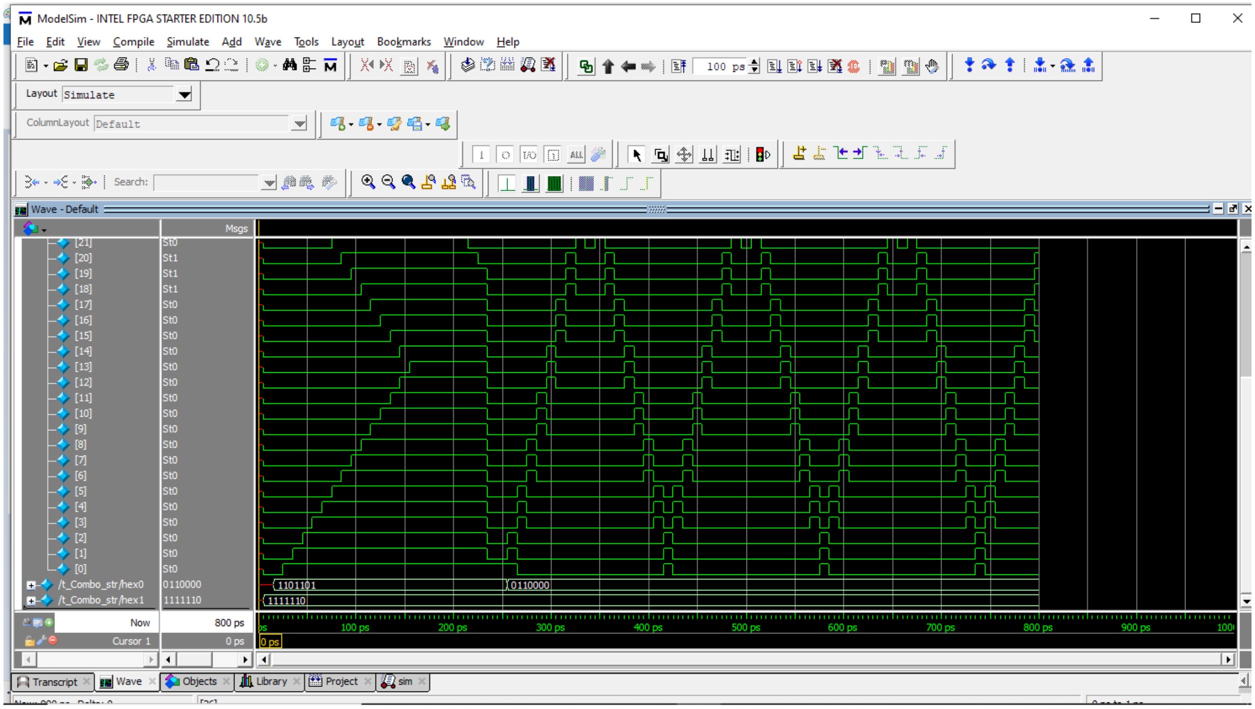
SWITCH FROM MODE 2 TO MODE 1 (MANUALLY)



ModelSim - INTEL FPGA STARTER EDITION 10.5b

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Layout Simulate
ColumnLayout Default
Search:
Wave - Default
Msgs
100 ps 200 ps 300 ps 400 ps 500 ps 600 ps 700 ps 800 ps 900 ps 100
Transcript Wave Objects Library Project sim

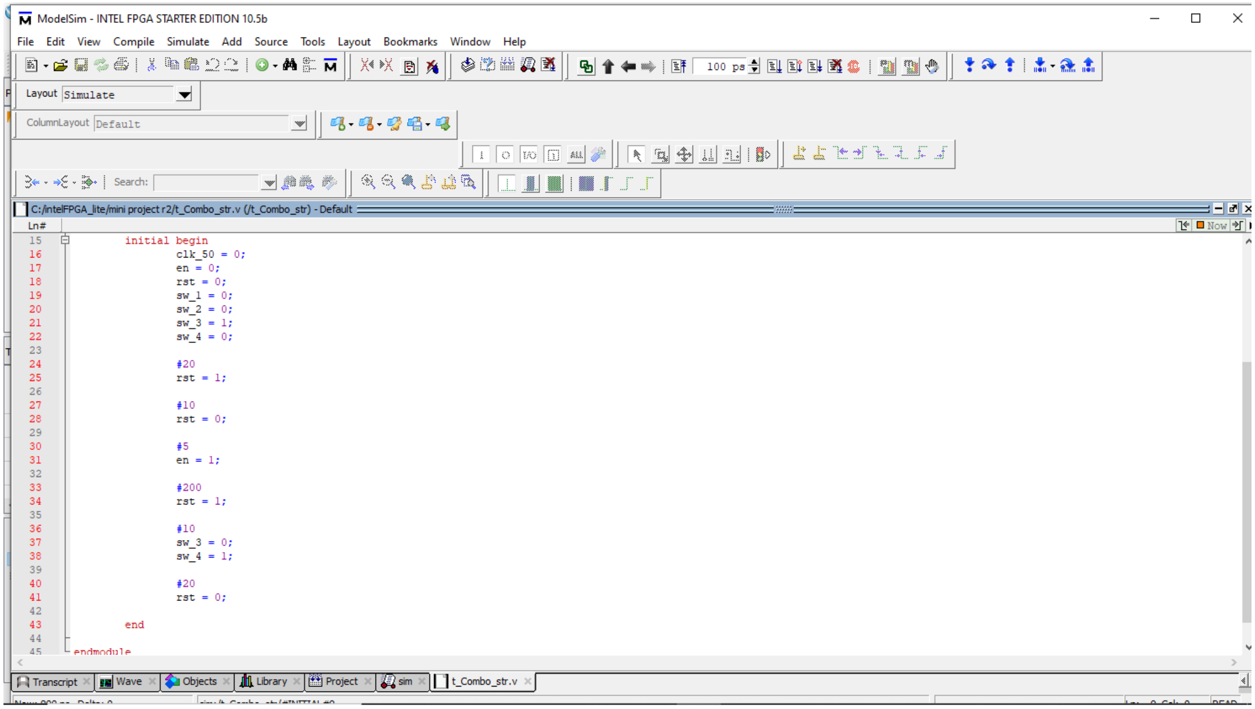
```
/t_Combo_str/clk_50   1
/t_Combo_str/en       1
/t_Combo_str/rst      0
/t_Combo_str/sw_1     0
/t_Combo_str/sw_2     0
/t_Combo_str/sw_3     0
/t_Combo_str/sw_4     1
/t_Combo_str/led      000000111000000...
  [26]                St0
  [25]                St0
  [24]                St0
  [23]                St0
  [22]                St0
  [21]                St0
  [20]                St1
  [19]                St1
  [18]                St1
  [17]                St0
  [16]                St0
  [15]                St0
  [14]                St0
  [13]                St0
  [12]                St0
  [11]                St0
Now                   800 ps
Cursor 1              0 ps
```



ModelSim - INTEL FPGA STARTER EDITION 10.5b

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Layout Simulate
ColumnLayout Default
Search:
Wave - Default
Msgs
1101101
0110000
1111110
100 ps 200 ps 300 ps 400 ps 500 ps 600 ps 700 ps 800 ps 900 ps 100
Transcript Wave Objects Library Project sim

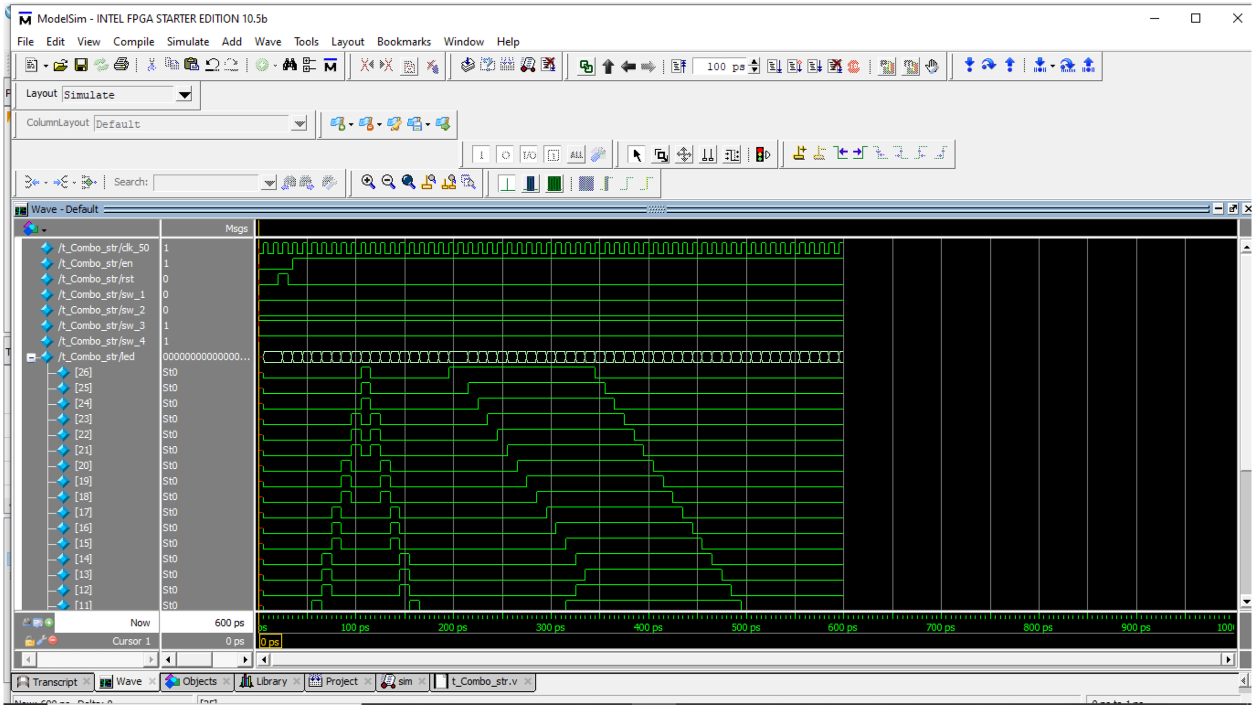
```
  [21]                St0
  [20]                St1
  [19]                St1
  [18]                St1
  [17]                St0
  [16]                St0
  [15]                St0
  [14]                St0
  [13]                St0
  [12]                St0
  [11]                St0
  [10]                St0
  [9]                 St0
  [8]                 St0
  [7]                 St0
  [6]                 St0
  [5]                 St0
  [4]                 St0
  [3]                 St0
  [2]                 St0
  [1]                 St0
  [0]                 St0
/t_Combo_str/hex0     0110000
/t_Combo_str/hex1     1111110
Now                   800 ps
Cursor 1              0 ps
```


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Layout Simulate
ColumnLayout Default
Search:
C:/intelFPGA_lite/mini project r2/t_Combo_str.v (/t_Combo_str) - Default
Ln#
Transcript Wave Objects Library Project sim t_Combo_str.v

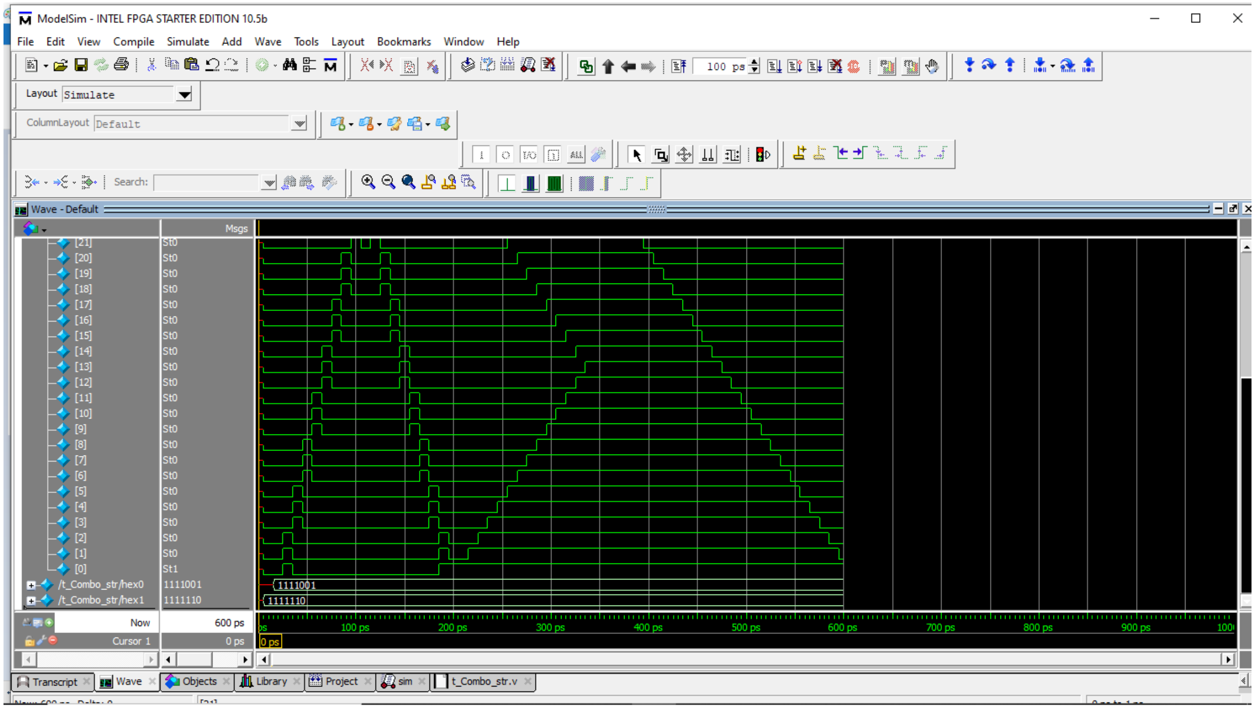
```
        initial begin
                clk_50 = 0;
                en = 0;
                rst = 0;
                sw_1 = 0;
                sw_2 = 0;
                sw_3 = 1;
                sw_4 = 0;

                #20
                rst = 1;

                #10
                rst = 0;

                #5
                en = 1;

                #200
                rst = 1;

                #10
                sw_3 = 0;
                sw_4 = 1;

                #20
                rst = 0;

        end

endmodule
```

(testbench for mode 2-mode 1)

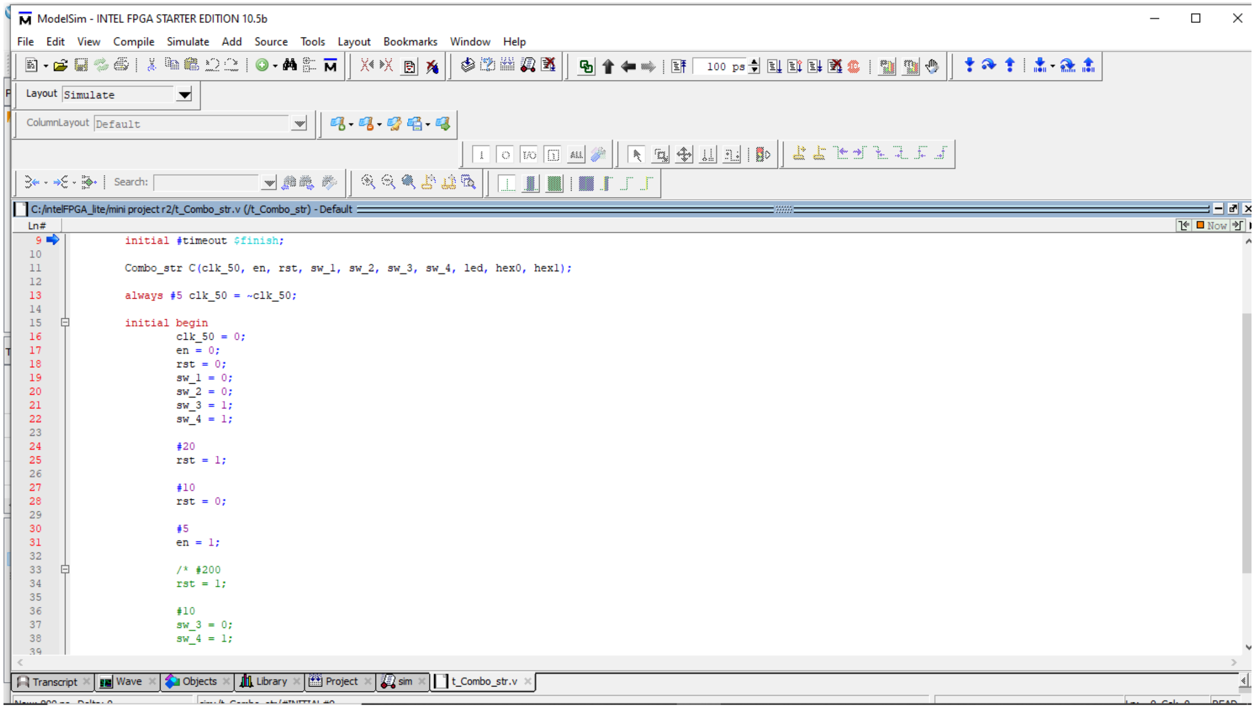
MODE 3 (AUTOMATIC) – 50 MHZ


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Layout Simulate
ColumnLayout Default
Search:
Wave - Default
Msgs
100 ps
200 ps
300 ps
400 ps
500 ps
600 ps
700 ps
800 ps
900 ps
Transcript Wave Objects Library Project sim t_Combo_str.v

```
/t_Combo_str/clk_50   1
/t_Combo_str/en       1
/t_Combo_str/rst      0
/t_Combo_str/sw_1     0
/t_Combo_str/sw_2     0
/t_Combo_str/sw_3     1
/t_Combo_str/sw_4     1
/t_Combo_str/led      00000000000000...
  [26]                St0
  [25]                St0
  [24]                St0
  [23]                St0
  [22]                St0
  [21]                St0
  [20]                St0
  [19]                St0
  [18]                St0
  [17]                St0
  [16]                St0
  [15]                St0
  [14]                St0
  [13]                St0
  [12]                St0
  [11]                St0
Now                   600 ps
Cursor 1              0 ps
```



```
Layout      Simulate
ColumnLayout Default

[21]                 St0
[20]                 St0
[19]                 St0
[18]                 St0
[17]                 St0
[16]                 St0
[15]                 St0
[14]                 St0
[13]                 St0
[12]                 St0
[11]                 St0
[10]                 St0
[9]                  St0
[8]                  St0
[7]                  St0
[6]                  St0
[5]                  St0
[4]                  St0
[3]                  St0
[2]                  St0
[1]                  St0
[0]                  St1
/t_Combo_str/hex0    1111001
/t_Combo_str/hex1    1111110
Now                  600 ps
Cursor 1             0 ps
```


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
100 ps
Search:
Ln#
Now
Transcript
Wave
Objects
Library
Project
sim
t_Combo_str.v

```
Layout      Simulate
ColumnLayout Default

C:/intelFPGA_lite/mini project r2/t_Combo_str.v (/t_Combo_str) - Default

	initial #timeout $finish;

	Combo_str C(clk_50, en, rst, sw_1, sw_2, sw_3, sw_4, led, hex0, hex1);

	always #5 clk_50 = ~clk_50;

	initial begin
		clk_50 = 0;
		en = 0;
		rst = 0;
		sw_1 = 0;
		sw_2 = 0;
		sw_3 = 1;
		sw_4 = 1;

		#20
		rst = 1;

		#10
		rst = 0;

		#5
		en = 1;

		/* #200
		rst = 1;

		#10
		sw_3 = 0;
		sw_4 = 1;
```

(testbench for mode 3)

CHAPTER 4: CONCLUSION AND FUTURE WORK

STRONG/WEAK ASPECTS:

- Strong aspects: easy to operate with simple steps, can run with different frequency and can switch among modes.
- Weak aspects: hard to maintain and modify, as the main modules contain a lot of codes, especially mode 3 case with many nested if-else statements.

CONCLUSION:

Running LEDs is usually used for decorating stores, buildings, companies. A Running LEDs circuit should support multiple running types. This is the first step to understand and practice on electrical circuits.

LINK (REPORT, VERILOG CODEs & PICTUREs):

https://drive.google.com/drive/folders/1wy285Zsd5sYwbxgYdZ6HzD2tn5iAathA?usp=sharing

(folder *codes* includes: Control_Unit.v, Datapath_Unit.v, Combo_str.v, t_Combo_str.v, Clock_Div.v, Mode_Select.v and Led7_Decoder.v)

DUTY ROSTER:

MAIN CODER, IDEA & REPORT	**IDEA, SUPPORT**	**SUPPORT**
Việt Tú	Minh Trung	Khôi Nguyên