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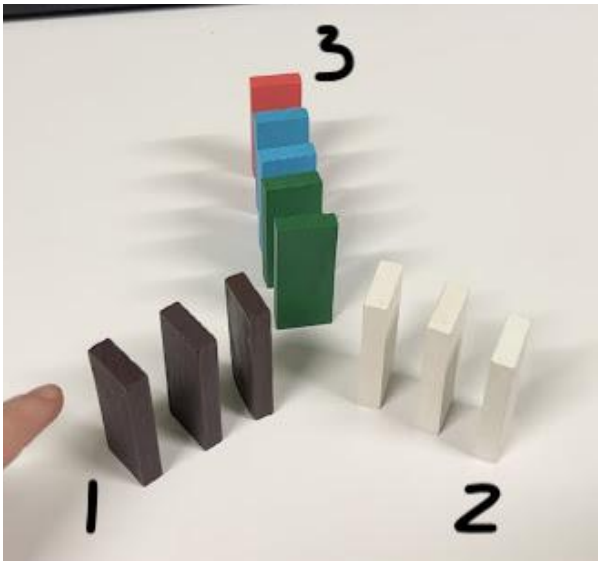
Lab 1 Report

I. Measurement:

	AND gate	OR gate	XOR gate	Half adder	Full adder
Reset time	30s	32.1s	60s	125s	Est. 180s
Propagation delay	1.03s	0.94s	1.82s	3s (both inputs) 1.74s (one input)	Est. 5s

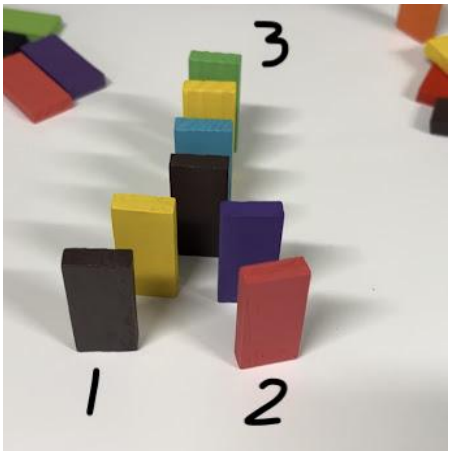
II. Diagrams:

AND gate:



Note: 1. A (input 1), 2. B (input 2), 3. Y (output)

OR gate:

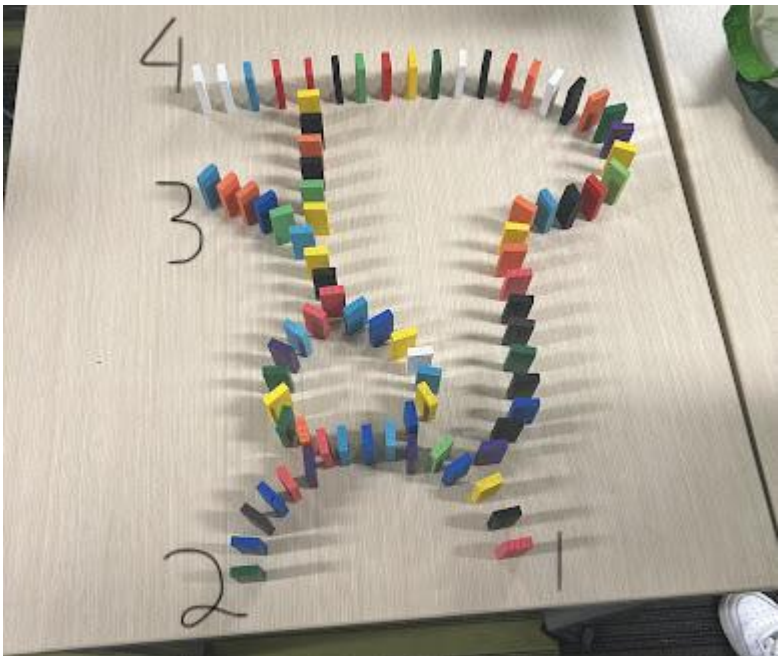


Note: 1. A (input 1), 2. B (input 2), 3. Y (output)

XOR gate:

Note: 1. A (input 1), 2. B (input 2), 3. Y (output)

Half adder:



Note: 1. A (input 1), 2. B (input 2), 3. Sum, 4. Carry

Full adder:

III. Truth tables:

Simple logic gates:

A	B	AND	OR	XOR
0	0	0	0	0
0	1	0	1	1
1	0	0	1	1
1	1	1	1	0

Half Adder:

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full Adder:

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

IV. Analysis:

Propagation delay is the length of time starting from when the input to a logic gate becomes stable and valid (when knocking down A and/or B dominoes), to the time that the output of that logic gate is stable and valid (when domino Y is knocked down).

We can see a discrepancy in the propagation delay time between simple logic gates: AND, OR, XOR gates and higher order logic gates: Half adder, Full adder. The order of propagation delay time from least to most is: AND, OR, XOR, Half adder, Full adder. AND gate and OR gate take approximately the same time because they have straightforward computation. We suspect Full adder takes the longest since it is the combination of two half adders and OR gate, thus performing more complex computation.

The more complex gates take more time to produce output than the simpler ones. A half adder computes the logic of an AND and XOR gate, whereas a full adder computes the logic of two half adders and OR gate. This added complexity results in a longer propagation delay, as more time is needed to perform the additional computations.

Another reason for the discrepancy in propagation delay is due to the fact that higher order logic circuits, such as the Half Adder and Full Adder, are designed to perform carry propagation which increases the complexity of the circuit and increases the delay time. This carry propagation process is not present in the simple gates. This might be because of more dominoes (more circuits so more distance to get to output) and more gates affect the speed of dominoes to get to output.

V. Portfolio Videos

here