Ryerson University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

Course Title:	ELECTRONNIC CIRCUITS I
Course Number:	ELE404
Semester/Year (e.g.F2016)	W2021

Instructor:	Fei Yuan

Assignment/Lab Number:	8
Assignment/Lab Title:	Design Project

Submission Date:	April 18th, 2021
Due Date:	April 18th, 2021

Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
Vinayak	Vinayak	500983169	6	unnatvinayak

*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: http://www.ryerson.ca/senate/current/pol60.pdf

TABLE ON CONTENTS:

Unnati Vinayak
ELE404 Design Project
Section 6

INTRODUCTION & BACKGROUND:

The purpose of this project is to design, simulate, analyze, and implement a circuit which meets a set of specifications. The requirements are listed below:

Specifications

- Power supply: $+10V$ relative to the ground;
- Quiescent current drawn from the power supply: ***no larger than*** $10\ mA$;
- No-load voltage gain (at $1\ kHz$): $|A_{vo}| = 50\ (\pm 10\%)$;
- Maximum no-load output voltage swing (at $1\ kHz$): ***no smaller than 8 V peak to peak;***
- Loaded voltage gain (at $1\ kHz$ and with $R_L = 1\ k\Omega$): ***no smaller than*** 90% ***of the no-load voltage gain;***
- Maximum loaded output voltage swing (at $1\ kHz$ and $R_L = 1\ k\Omega$): ***no smaller than 4 V peak to peak;***
- Input resistance (at $1\ kHz$): ***no smaller than*** $20\ k\Omega$;
- Amplifier type: ***inverting or non-inverting;***
- Frequency response: ***20 Hz to 50 kHz (−3dB response);***
- Type of transistors: ***BJT;***
- Number of transistors (stages): ***no more than 3***;
- Resistances permitted: ***values smaller than*** $220\ k\Omega$ ***from the E24 series***;
- Capacitors permitted: $0.1\ \mu F$, $1.0\ \mu F$, $2.2\ \mu F$, $4.7\ \mu F$, $10\ \mu F$, $47\ \mu F$, $100\ \mu F$, $220\ \mu F$;
- Other components (BJTs, diodes, Zener diodes, etc.): ***only from your ELE404 lab kit.***

Notes:

- The output voltage must be free from distortions (clipping, etc.) in all test conditions.
- The source resistance, R_s, must be 600 Ω for all tests.

The designed amplifier must be AC-coupled for the load and the signal source, but the coupling between its intermediate stages may be of AC or DC type as per the designer's choice. There are no restrictions in terms of using NPN or PNP transistors.

Note that there is no right or wrong design, as long as the aforementioned specifications are met.

Based on the above specifications, the following circuit was designed. The value for R_S was specified to be 600Ω for all tests. The values for other resistors, capacitors, and input voltage were obtained by calculations and/or trial and error.

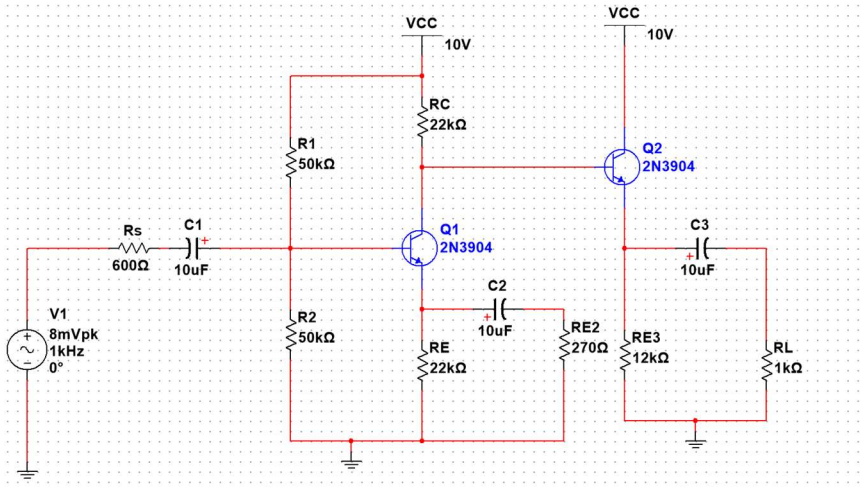


Figure 1: The circuit shown above is the circuit which was designed and implemented on Multism. The Pre-lab consists of the calculations done on the circuit.

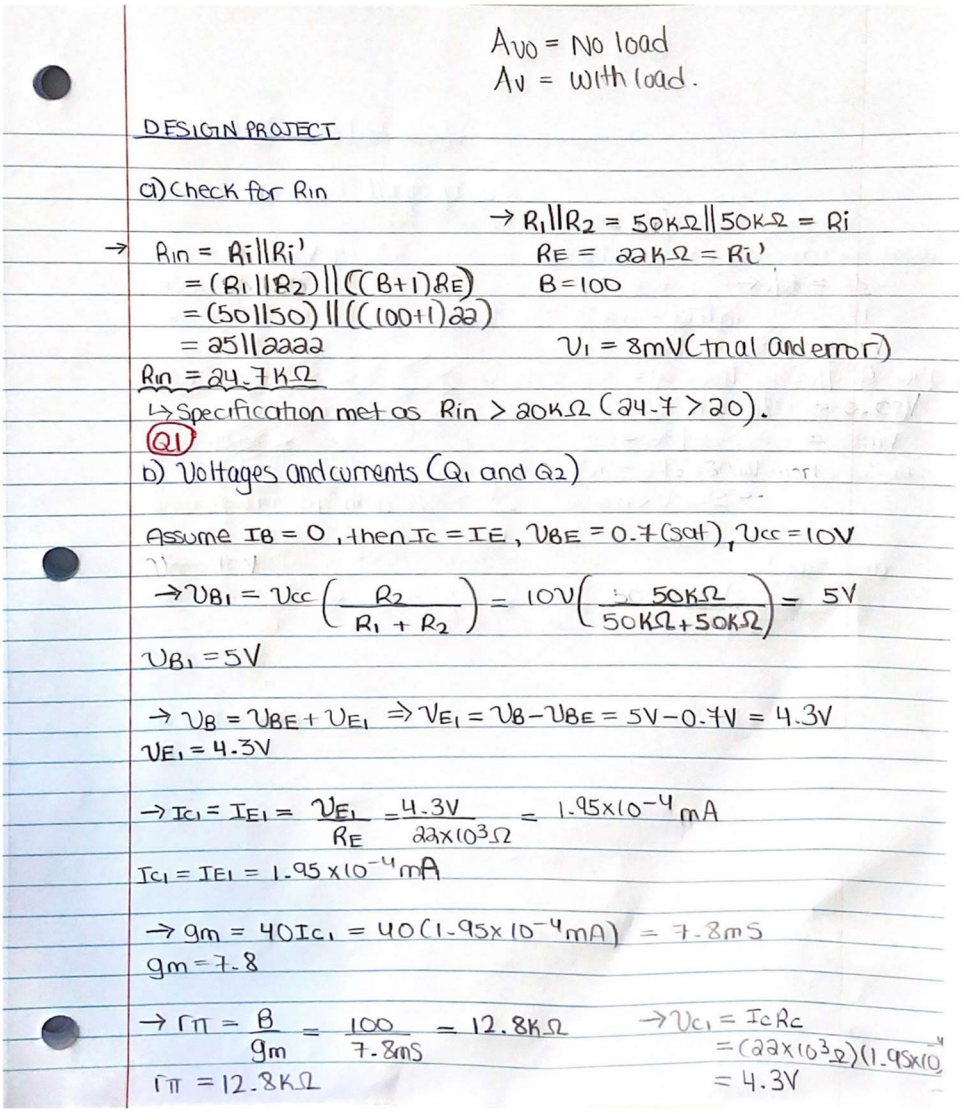
Unnati Vinayak
ELE404 Design Project
Section 6

PRE-LAB:

All the calculations are done in the *Pre-lab* section of the lab report. The calculations show how specific values for resistors, capacitors, and input voltages work to meet the requirements listed in the *Background & Introduction.*

The following assumptions were made for the calculations:

1. B = 100
2. $V_{BE(Sat)} = 0.7V$
3. $V_{CE\ (active)} = 0.3V$
4. $I_B = 0A$



Unnati Vinayak
ELE404 Design Project
Section 6

(22)

Assume $I_B = 0$, $V_{B2} = V_{C1}$, $I_{C2} = I_{E2}$

$\rightarrow V_{E2} = V_{B2} - V_{BE}$
$= 4.3V - 0.7V$
$= 3.6V$
$\rightarrow V_{E2} = 3.6V$

$\rightarrow I_{C2} = I_{E2} = \frac{V_{E2}}{R_{E3}} = \frac{3.6V}{12 \times 10^3 \Omega} = 3 \times 10^{-4} A = 0.3mA$

$I_{C2} = I_{E2} = 0.3mA$

$\rightarrow g_m = 40 I_{C2} = 40(0.3mA) = 12mS$
$g_m = 12mS$

$\rightarrow r_\pi = \frac{\beta}{g_m} = \frac{100}{12 \times 10^{-3}} = 8.3K\Omega$

$r_\pi = 8.3K\Omega$

Unnati Vinayak
ELE404 Design Project
Section 6

c)

→ Common-Emitter (gain) ∴ $\frac{v_\pi}{v_i} = \frac{g_m(R_C \| (r_{\pi 2} + \beta(R_{E3} \| R_L)))}{1 + g_m B}$

$$= \frac{12[22 \| (8.3 + 100(12 \| 1))]}{1 + 12(0.270)}$$

$$= \frac{12(18.041)}{4.24}$$

$$= 51.0556$$

→ (No load gain) ∴ $\frac{g_{m2}(R_{E3})}{1 + g_{m2}(R_{E3})} = \frac{(12)(12)}{1 + (12)(12)} = 0.99$

→ (load gain) ∴ $\frac{g_{m2}(R_{E3} \| R_L)}{1 + g_{m2}(R_{E3} \| R_L)}$

$$= \frac{12(12 \| 1)}{1 + 12(12 \| 1)}$$

$$= 0.917$$

∴ $A_{VO} = 51.056$ and $A_V = (0.917)(51.056) = 46.8$

$A_{VO} = 51.056$

$A_V = 46.8$

Unnati Vinayak
ELE404 Design Project
Section 6

d) Maximum loaded/not-loaded voltage gain:

Max V_o(load) = $V_{CC} - (V_{B2} + V_{CE})$
= $10V - (4.3V + 0.3V)$
= $5.4V$

$5.4 > 4 \Rightarrow$ maximum loaded output voltage is no smaller than 4V.

Max V_o(no load): $R_C = 5K\Omega$

$V_{C1} = R_C(I_{E1})$
$= (5 \times 10^3)(1.95 \times 10^{-4})$
$= 0.975V$

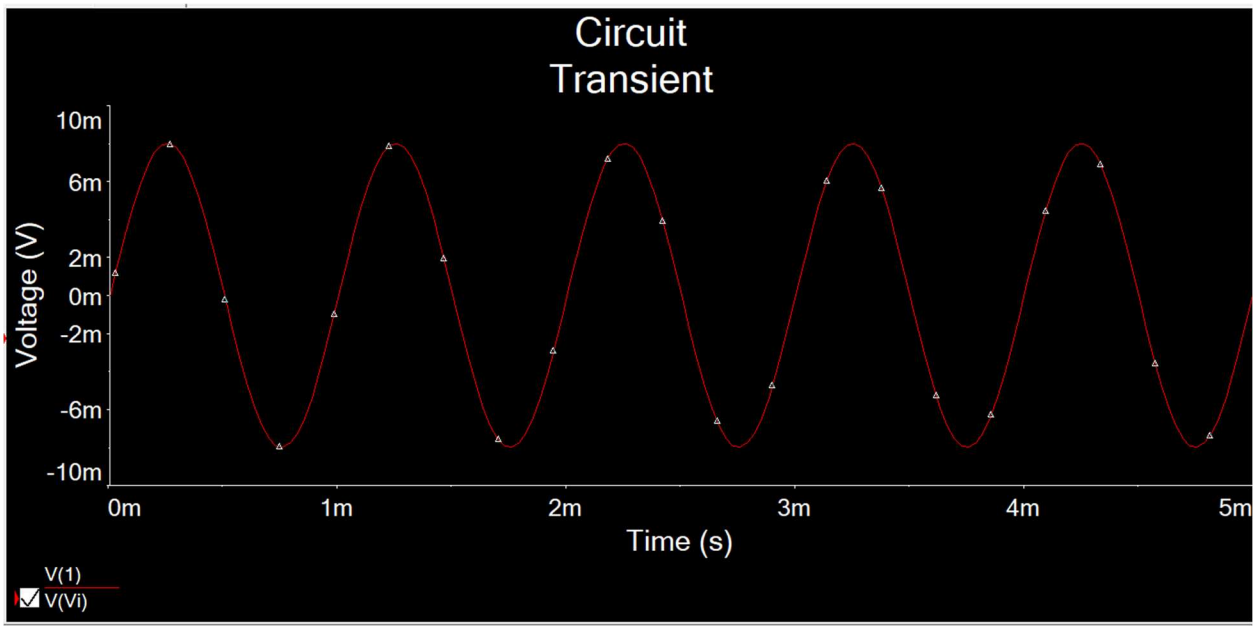
Then $V_{B2} = V_{C1} = 0.957V$

Max V_o(no load) = $V_{CC} - (V_{B1} + V_{CE})$
= $10V - (0.975V + 0.3V)$
= $8.725V$

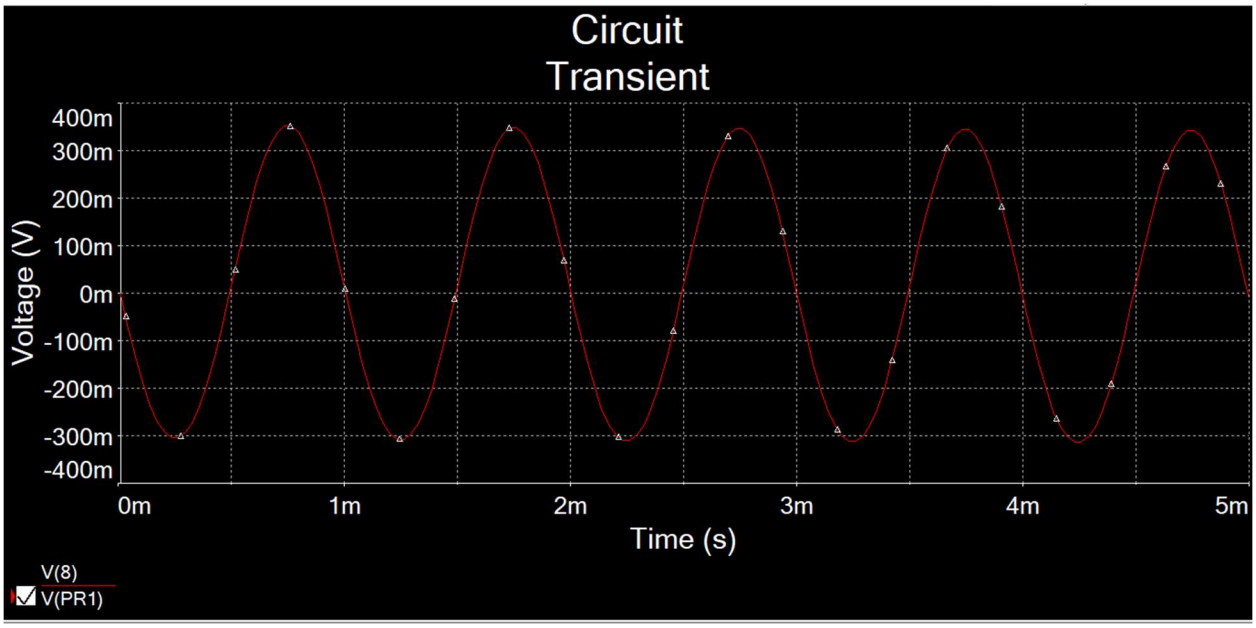
$8.725V > 8V \Rightarrow$ maximum no-load output voltage is no smaller than 8V.

LAB EXPERIMENT & RESULTS:

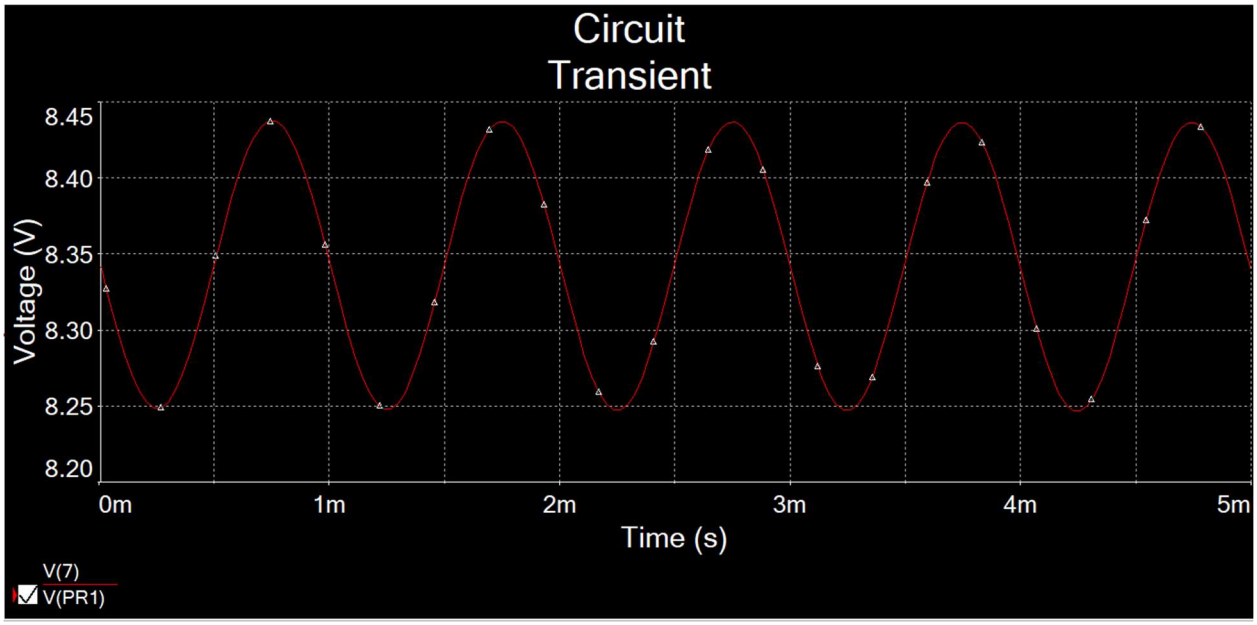
The *Lab Experiment & Results* section contains the graphs obtained from the circuit in *Figure 1.*



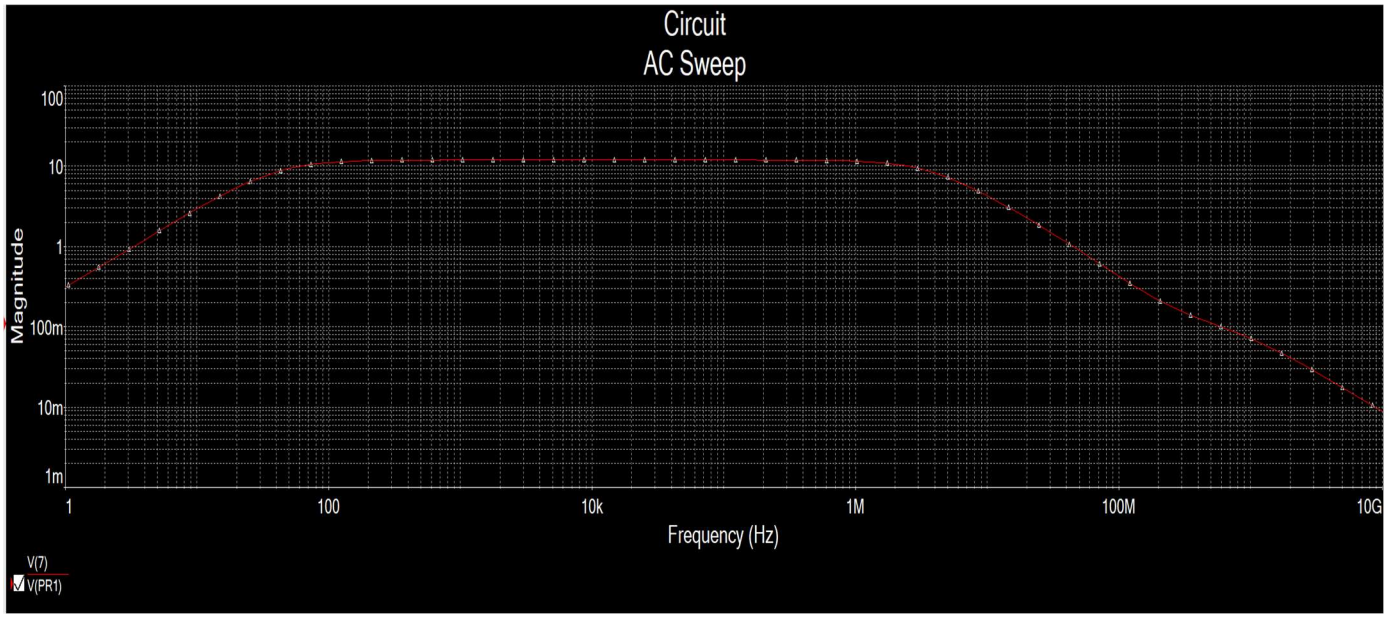
Graph 1: The following graph is for the input voltage.



Graph 2(a): This graph is for the output voltage with the load R_L = 1k **Ω**.



Graph 2(b): The following graph is for the input voltage without the load R_L.



Graph 3: This magnitude graph shows that the transistor is active from 20Hz – 50kHz.

CONCLUSION & REMARKS:

The Common Emitter (CE) Amplifier is used to amplify/increase voltage gain. Since there is an expected voltage drop, I used the CE amplifier. The calculations are shown in the Pre-lab.

The Common Collector (CC) Amplifier can take a large load while maintaining the wanted voltage gain. The CC amplifier does not depend on if there is a load or no load. It results in approximately the same voltage gain. The CC amplifier does not help increase voltage gain, but it does help maintain it.

A major source of error is in the calculations. The circuit was implemented on Multism, which means that conditions are ideal. However, the calculations consisted of rounding. Rounding a certain parameter impacted the other parameters as well; this turns into a major source of error in the project. For example, g_m, $R_{in,}$ and node voltages were rounded in the calculations. These values were then used to calculate the voltage gain.

I found the project more challenging compared to the 7 labs. I think this is because we were required to design, implement, and analyze our own circuit to meet the specifications, whereas the labs were heavy based on using given circuits to obtain graphs and measure related parameters. However, this project was helpful as in the future knowing how to design, implement, and analyze your own circuit would be a major requirement.