NI-STC3 Timing and Synchronization Technology

Publish Date: Apr 30, 2014

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1. Introduction

NI-STC3 timing and synchronization technology delivers a new level of performance to National Instruments X Series multifunction data acquisition (DAQ) devices. This technology is the driver behind the advanced digital, timing, triggering, synchronization, counter/timer, and bus-mastering features.

For more information about X Series, see "What Is X Series?"

2. Retriggerable Analog and Digital Output

A retriggerable task is a measurement task that executes a specified operation each time a specific trigger event occurs. Previous generations of synchronization and timing technology were only able to retrigger counter operations, which could provide retriggerable sample clocks for other tasks but created fairly complex code. NI-STC3 technology now equips all acquisition and generation tasks with inherent retriggerable capabilities with a single NI-DAQmx property node.

More specifically, analog and digital outputs generate a specified amount of samples from the output buffer for each trigger. With this feature, the user can load waveforms into the output buffer and generate a unique waveform corresponding to each incoming trigger. As seen in Figure 1, each unique waveform placed into the output buffer must contain the same amount of samples because the number of samples written per trigger must remain constant. Figure 1 also shows a preloaded analog output buffer and what the output waveform looks like as it is generated.

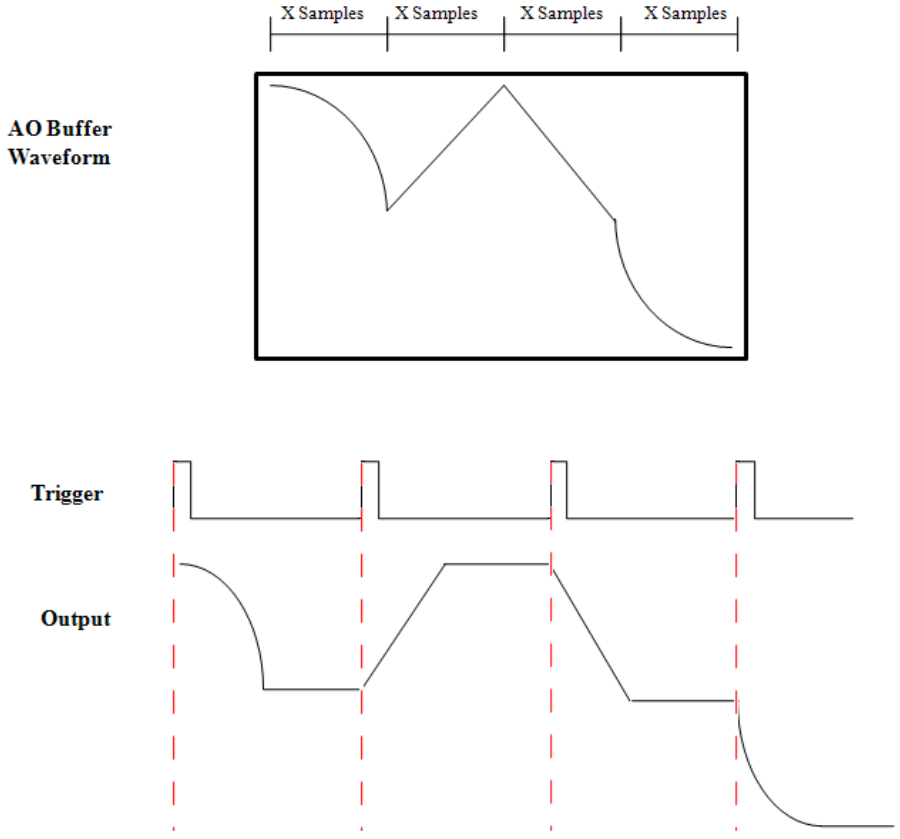


Figure 1. Retriggerabe Analog Output

At each trigger edge, X samples are generated and the last sample generated by the waveform is held at the output until another trigger occurs. Figure 2 below shows the NI LabVIEW and NI-DAQmx code to achieve this functionality. This code differs slightly from its nonretriggerable counterpart only in the retriggerable property node that is being set. Although this example writes all samples to the buffer before generation starts, the user still has the ability to write to the buffer during generation as well.

Figure 2. Retriggerable Analog Output Code

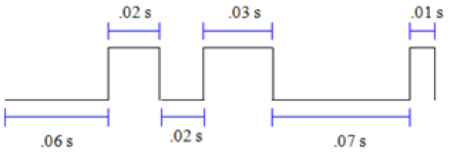
3. 100 MHz Timebase

NI-STC3 technology also provides a faster 100 MHz timebase, replacing the 80 MHz timebase used by previous devices for many counter applications. The 100 MHZ timebase is also used to generate analog and digital sampling or update rates, compared to a 20 MHz timebase used in prior devices. For generating arbitrary sampling rates, the generated clock rate can now be significantly closer to the user requested rate because of this 5x speed improvement. In addition, the faster timebase and improved device front end reduce the time between triggering and the first sample clock edge, which improves the responsiveness of the device to triggers.

4. Buffered Counter Output

NI-STC3 technology integrates four 32-bit, 100 MHz counters that each provides more functionality than those on any previous data acquisition device.

Buffered counter output gives the user the ability to preload multiple pulse specifications into an onboard buffer. With these specifications, different pulses can be generated with high and low times. The user can fill the array with active and idle times, active and idle ticks, or frequency and duty cycle. The active and idle ticks specify how many ticks of a selected Internal or External Timebase the pulse will stay high and low for. Figure 3 shows a pulse train with a varying period and how this signal can be represented in three different ways.



	Active Time (sec)	Idle Time (sec)	Frequency (Hz)	Duty Cycle (%)	Active Ticks	Idle Ticks
Pulse 1	.02	.06	12.5 Hz	25	2000000	6000000
Pulse 2	.03	.02	20Hz	60	3000000	2000000
Pulse 3	.01	.07	12.5	12.5	1000000	7000000

Figure 3. Buffered Counter Output Specified in Three Different Methods

The user also has the ability to output their pulse train based on implicit or sample clock timing types. By using implicit timing, all pulses specified in the buffer will output consecutively. The output signal can also be selected as running once through the buffer or outputting the consecutive pulses in the buffer continuously. Figure 4 demonstrates finite and continuous buffered counter output using implicit timing.

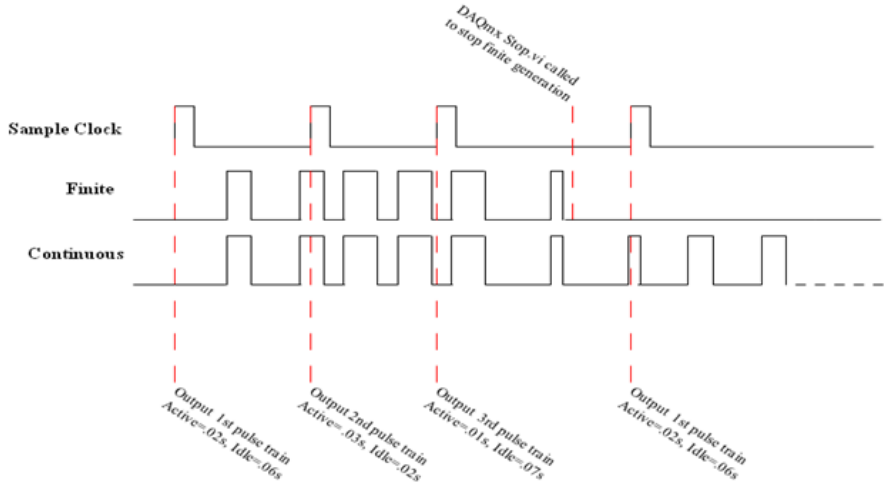
Output Buffer

Active Time (sec)	Idle Time (sec)
.02	.06
.03	.02
.01	.07

Figure 4. Finite versus Continuous Buffered Counter Output

By using sample clock timing, the user can specify a clock source and output the next pulse in the output buffer. While the counter is waiting for the next sample clock edge, it continuously outputs a pulse train with the current specifications of the frequency and

duty cycle. If a sample clock edge is high during a cycle of the current pulse train, the counter waits until the start of the next cycle to output the new pulse train. Once again, the output signal can be chosen to run through the output buffer once or continuously. Figure 5 shows an example of finite and continuous buffered counter output using sample clock timing.



Output Buffer

Active Time (sec)	Idle Time (sec)
.02	.06
.03	.02
.01	.07

Figure 5. Finite versus Continuous Buffered Counter Output Using a Sample Clock

5. Buffered Counter Input

Traditionally, buffered counter input operations used the implicit or sample clock timing type depending on the type of task. If a buffered edge count was performed, the user would supply their own sample clock to gate the count and place it into a buffer. If a buffered period or frequency measurement was performed, implicit timing would then be selected. By selecting implicit, the user informs the NI-DAQmx driver that the measured period or frequency value should be latched into a buffer at the end of each cycle of the incoming signal.

Buffered counter input functionality, using NI-STC3 technology, has improved on its predecessors' capabilities in the areas of buffered period and frequency measurements. Although the user can continue selecting implicit as the timing type, the user can now select sample clock as well. When using a sample clock as the timing type, buffered frequency and period measurements are made by counting both an internal timebase (counted by embedded counter) as well as the unknown signal of interest up until the rising edge of the sample clock. However, the sample clock is a signal that must be specified and created by the user. The ideal frequency of the internal timebase is then divided by its count to find the effective frequency up to the next sample clock edge. Figure 6 shows all three signals, how buffering occurs based on sample clock edges, and what calculations are made to find the unknown signal's frequency.

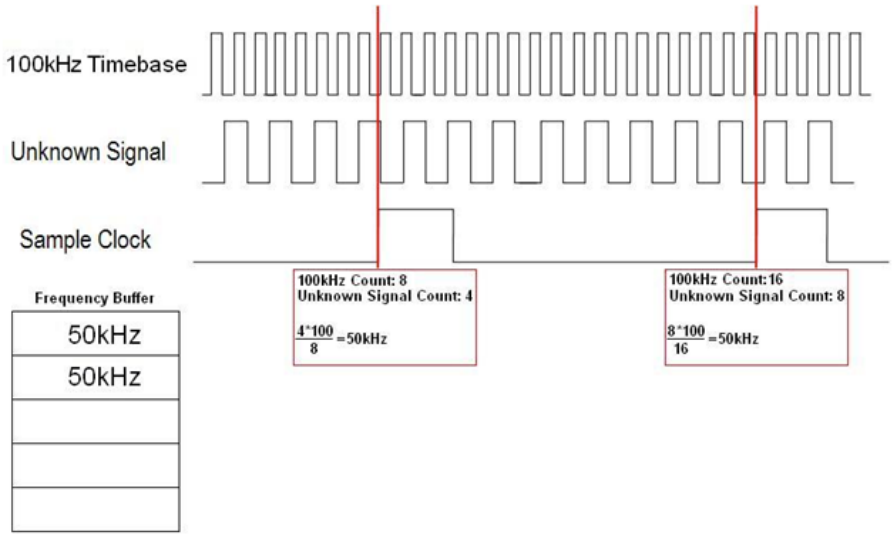


Figure 6. Buffered Counter Input Using the 100 kHz Timebase

6. Digital I/O Features

NI-STC3 technology also provides several features for the digital I/O and programmable function input (PFI) lines on X Series devices. This includes programmable power-up states, watchdog timers, event detection, and new PFI filtering.

There are now two additional timing engines on each X Series device, for the digital input and digital output. With previous devices, you would need to correlate the digital I/O to another clock, such as the analog input sample clock or a counter output. With the new included timing engines for digital input and digital output, you can now execute digital I/O completely independently from other subsystems, which frees up other resources on the device and lets you run digital I/O at different rates.

For more details on these features, see the X Series User Manual.

7. Example LabVIEW Code

Find the following examples in the LabVIEW Example Finder to provide a starting point for the applications discussed in this document.

- Acq&Graph Voltage Int Clk-Retriggerable.vi
- Gen Dig Pulse Train-Buff-Implicit-Cont.vi
- Gen Dig Pulse Train-Buff-Sample Clock-Cont.vi
- Meas Pulse-Buffered-SampleClocked-Cont.vi
- Generate PWM Signal.vi
- Cont Write Dig Port-Int Clk.vi

8. Summary

With NI-STC3 technology, users can now accomplish more advanced analog, digital, and counter operations than ever before. In addition, applications that previously required additional onboard resources or were difficult to program can now execute independently and with less NI-DAQmx code.

9. Next Steps

Read the “What Is X Series” white paper

See more details of NI-STC3 timing and synchronization technology in the **X Series User Manual**