

EMBEDDED SYSTEM COURSE

LECTURE 8: PERIPHERAL ADC

Learning Goals



- Understanding basis concepts about A/D converter.
- Understanding on how to configure the ADC module in KL46.
- Understanding on how to create a simple project for ADC module.

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- ❖ Introduction to A/D converter.
- ❖ Overview on KL46 ADC modules
- ❖ Periodic Interrupt Timer (PIT) Module

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- ❖ **Introduction to A/D converter.**
- ❖ Overview on KL46 ADC modules
- ❖ Periodic Interrupt Timer (PIT) Module

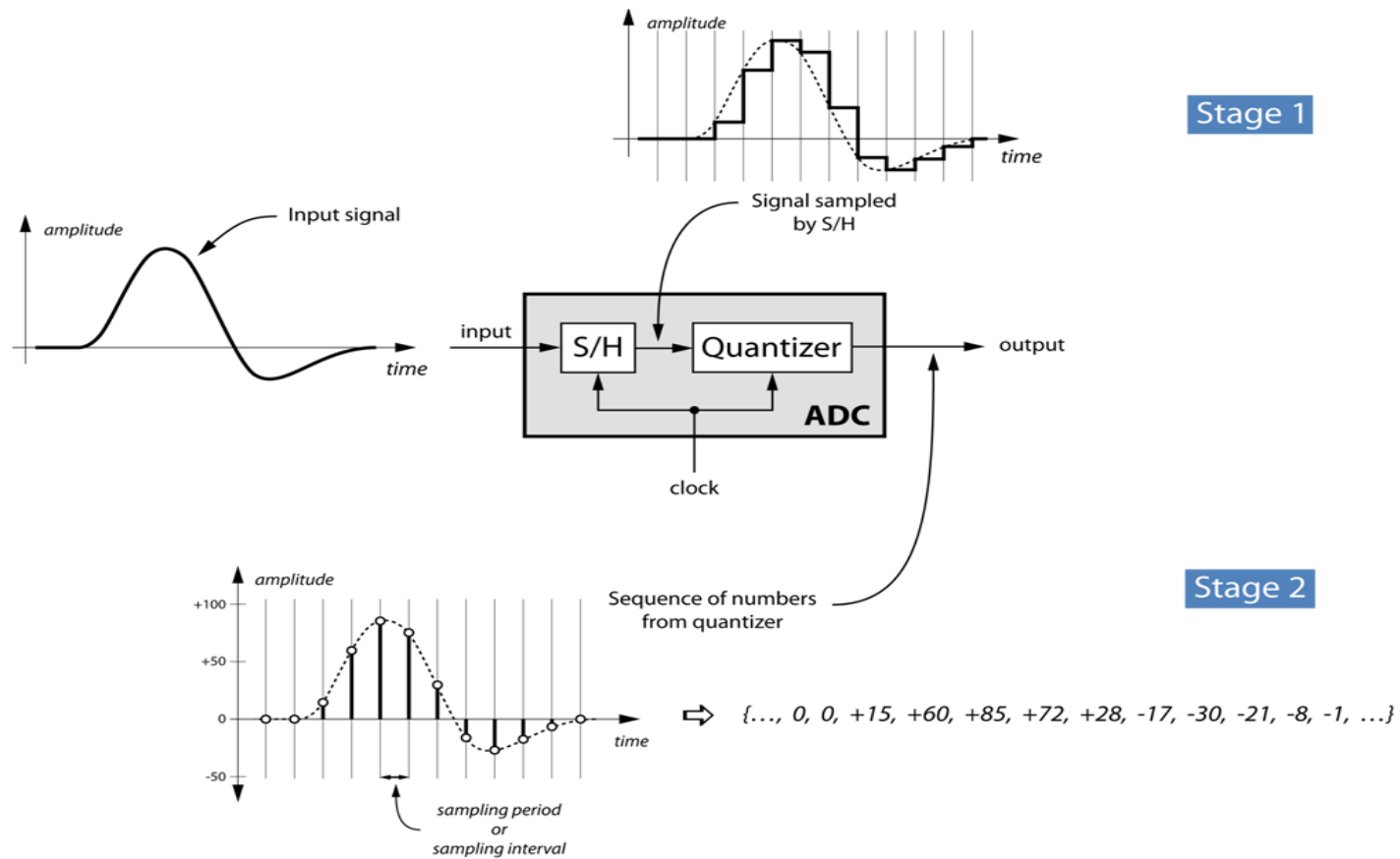
What is A/D converter?

The main purpose of the A/D converters within a data acquisition system is to convert conditioned analog signals into a stream of digital data so that the data acquisition system can process them for display, storage, and analysis.



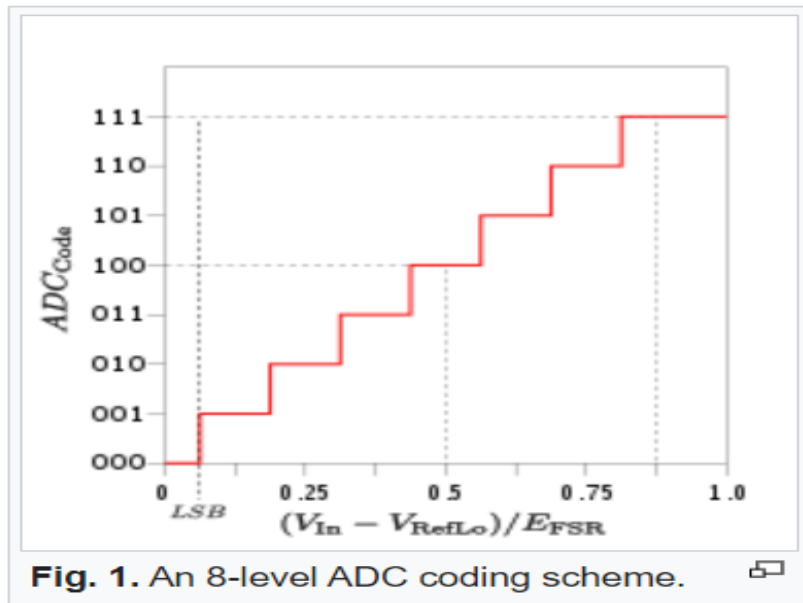
ADC converter takes an analog signal and converts it into the digital domain

What Do A/D Converters Do?



What is resolution?

The resolution of the converter indicates the number of different, ie discrete, values it can produce over the allowed range of analog input values.



(wiki)

What is the Sampling Rate?

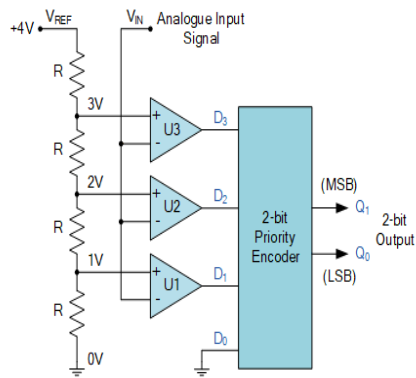
- An analog signal is continuous in time and it is necessary to convert this to a flow of digital values. It is therefore required to define the rate at which new digital values are sampled from the analog signal. The rate of new values is called the *sampling rate* or sampling frequency of the converter.
- The Nyquist–Shannon:

(wiki)

A/D converter architecture

- Flash ADC
- Successive-approximation ADC
- Ramp-compare ADC
- Delta-encoded ADC or counter-ramp
- ...

2-bit Analogue to Digital Converter Circuit



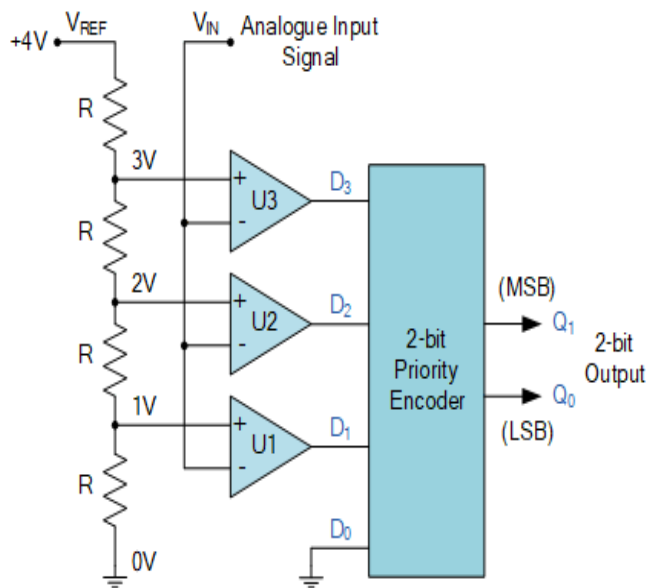
2-bit A/D converter Output

Analogue Input Voltage (V_{IN})	Comparator Outputs				Digital Outputs	
	D ₃	D ₂	D ₁	D ₀	Q ₁	Q ₀
0 to 1 V	0	0	0	0	0	0
1 to 2 V	0	0	1	X	0	1
2 to 3 V	0	1	X	X	1	0
3 to 4 V	1	X	X	X	1	1

A/D converter architecture

- Flash ADC

2-bit Analogue to Digital Converter Circuit

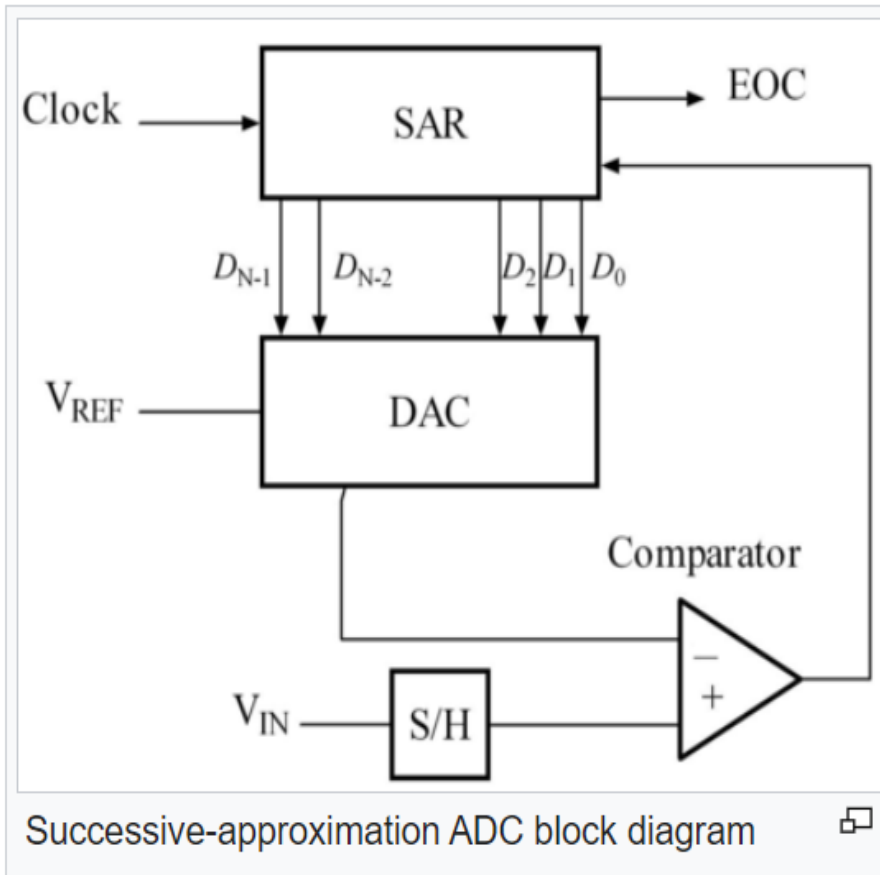


2-bit A/D converter Output

Analogue Input Voltage (V_{IN})	Comparator Outputs				Digital Outputs	
	D ₃	D ₂	D ₁	D ₀	Q ₁	Q ₀
0 to 1V	0	0	0	0	0	0
1 to 2V	0	0	1	X	0	1
2 to 3V	0	1	X	X	1	0
3 to 4V	1	X	X	X	1	1

A/D converter architecture

Sucessive-approximation ADC



Key

DAC = digital-to-analog converter

EOC = end of conversion

SAR = successive approximation register

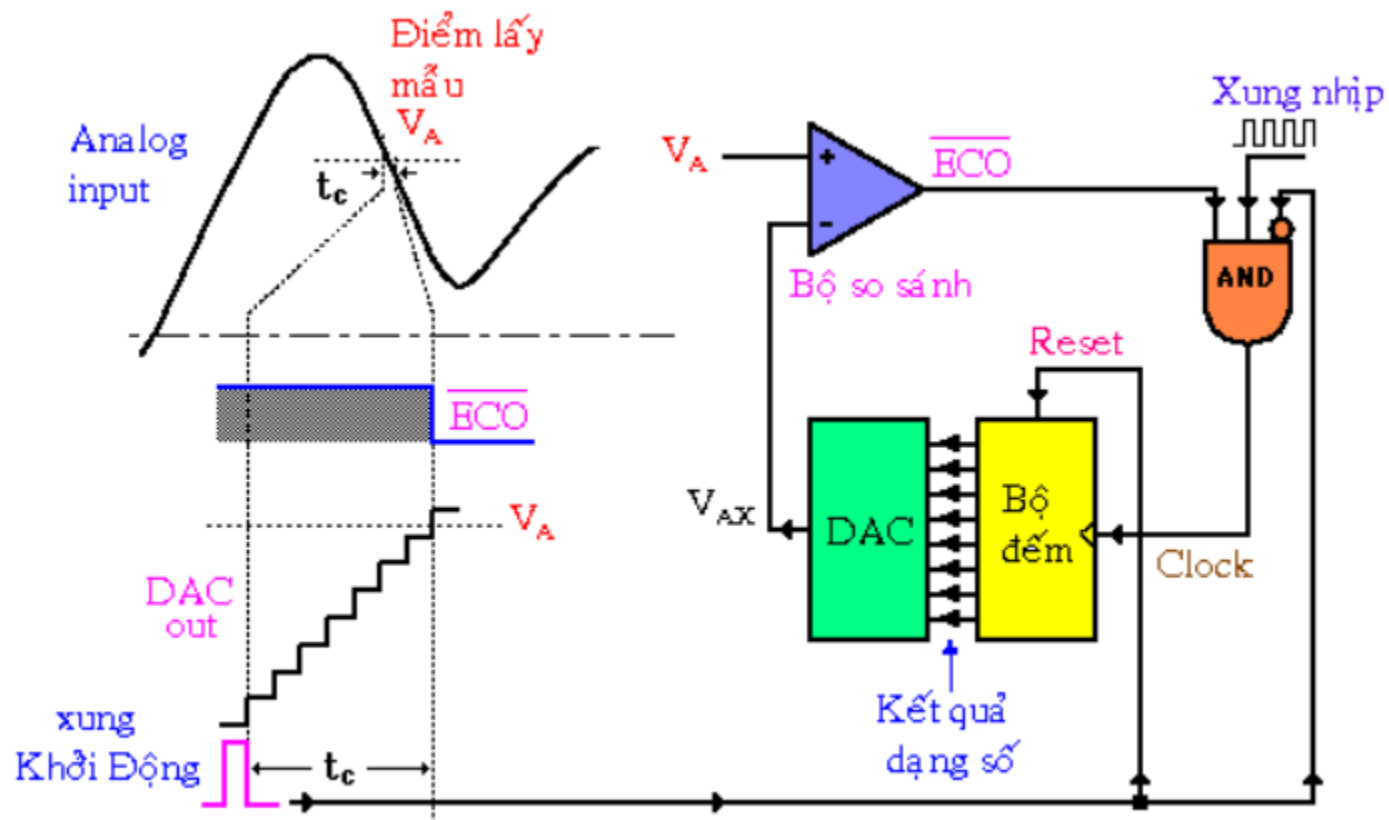
S/H = sample and hold circuit

V_{IN} = input voltage

V_{REF} = reference voltage

A/D converter architecture

Ramp-compare ADC



Hình 5.20 DAC dạng sóng bậc thang

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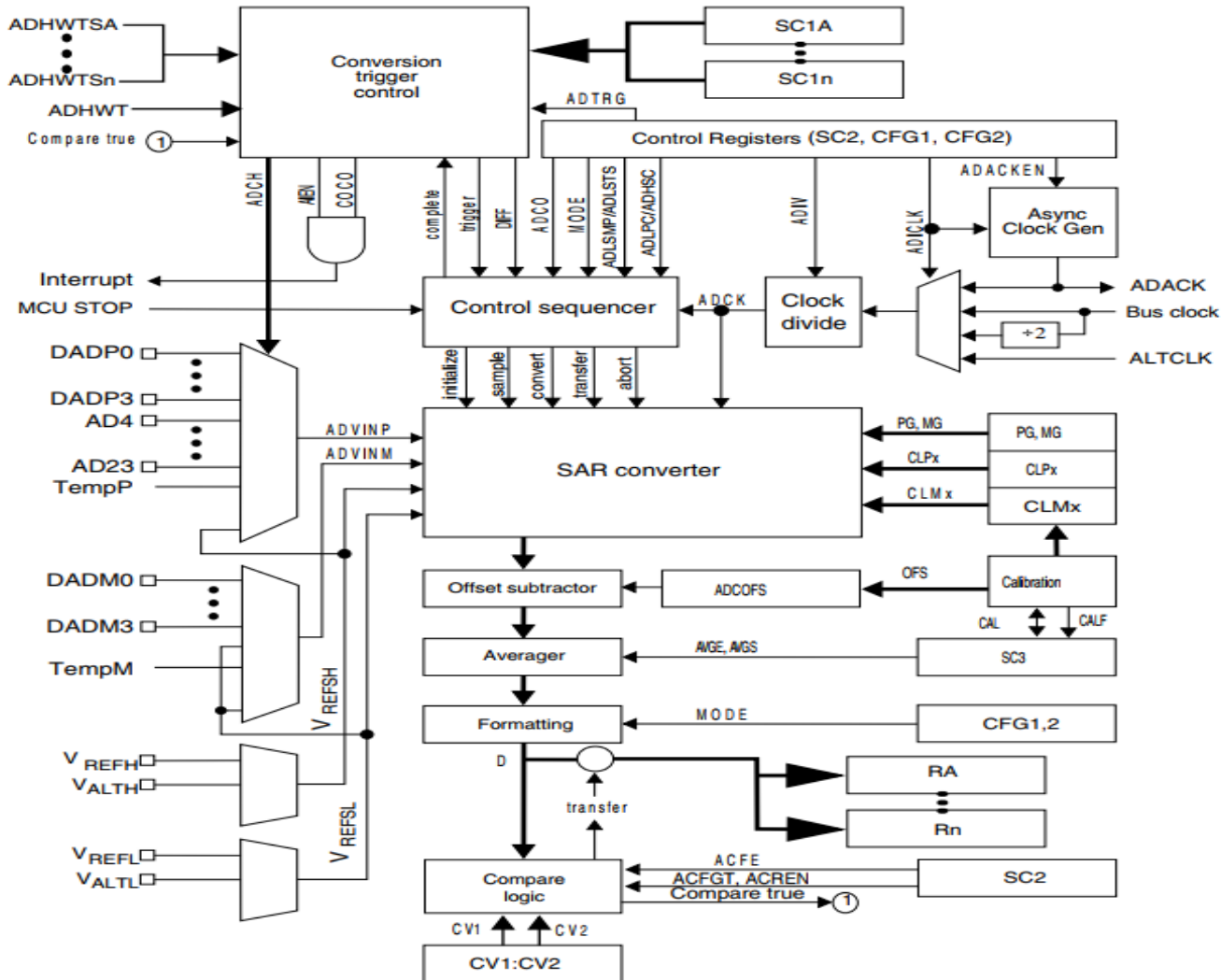
- ❖ Introduction to A/D converter.
- ❖ **Overview on KL46 ADC modules**
- ❖ Periodic Interrupt Timer (PIT) Module

MKL46Z ADC features



- Linear successive approximation algorithm with up to 16-bit resolution
- Up to four pairs of differential and 24 single-ended external analog inputs
- Output modes:
 - differential 16-bit, 13-bit, 11-bit, and 9-bit modes
 - single-ended 16-bit, 12-bit, 10-bit, and 8-bit modes
- Output format in 2's complement 16-bit sign extended for differential modes
- Single or continuous conversion, that is, automatic return to idle after single conversion
- Conversion complete/hardware average complete flag and interrupt
- Input clock selectable from up to four sources
- Selectable hardware conversion trigger with hardware channel select
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value

MKL46Z ADC Block Diagram



MKL46Z ADC Register

ADC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
4003_B000	ADC Status and Control Registers 1 (ADC0_SC1A)	32	R/W	0000_001Fh	28.3.1/476
4003_B004	ADC Status and Control Registers 1 (ADC0_SC1B)	32	R/W	0000_001Fh	28.3.1/476
4003_B008	ADC Configuration Register 1 (ADC0_CFG1)	32	R/W	0000_0000h	28.3.2/479
4003_B00C	ADC Configuration Register 2 (ADC0_CFG2)	32	R/W	0000_0000h	28.3.3/481
4003_B010	ADC Data Result Register (ADC0_RA)	32	R	0000_0000h	28.3.4/482
4003_B014	ADC Data Result Register (ADC0_RB)	32	R	0000_0000h	28.3.4/482
4003_B018	Compare Value Registers (ADC0_CV1)	32	R/W	0000_0000h	28.3.5/483
4003_B01C	Compare Value Registers (ADC0_CV2)	32	R/W	0000_0000h	28.3.5/483

Table continues on the next page...

How to program for adc?



Question & Answer



Thanks for your attention !

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