Embedded System Course

Lecture 9: Peripheral I2C

- *<Considering to the lesson duration, it is recommended to design the slides where each of them takes in average about 3 minutes to present. Time for exercise and case-study is estimated and allocated separately>*

- *<The author may use the Notes part to provide more detail information for instructor. Slides and Notes are to be printed and given to trainer as Instructor manual>*

Lesson Objectives

- *Understanding basis concepts about I2C and how to transmit/receive data via I2C bus*
- *Understanding on how to configure the KL46 I2C module.*

Table of contents

- *Introduction to I2C*
- *Freedom KL46 I2C*

Section 1: Introduction to I2C

Requirements and Problems

Requirements and Problems

Customer requirements:

- *Serial and synchronous*
- *2 wires*
- *Large number of devices*
- *Multi-masters, multi-slaves*
- *2 devices communicate at a time*
- *Switching device role runtime*
- *Handshake and Plug-play*

Requirements and Problems

UART	SPI
Asynchronous serial	Synchronous serial
2 wires	>4 wires
2 devices	Multiple-devices
-	One master, multi-slave
-	Not support switch role runtime
Addition wires for handshake	Addition wires for handshake

Problem #1

- *Synchronous serial*
- *Two-wires*

⇒ *1 wire for synchronous clock*

⇒ *1 wire for data*

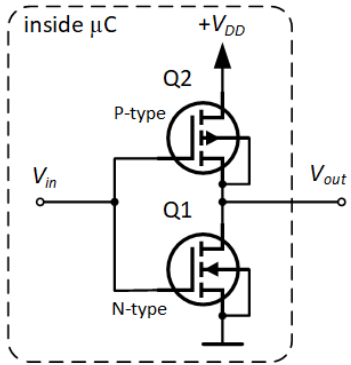
- *Large number of devices*
- *Multi-masters, multi-slaves*
- *Switching device role runtime*

⇒ *2 wires are both **Input** and **Output***

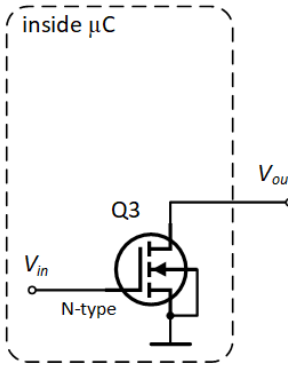
Problem #1

GPIO modes:

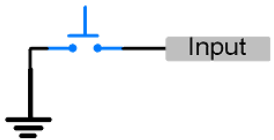
- *Output:*
  - ✓ *Push-pull*
  - ✓ *Open-drain*
- *Input:*
  - ✓ *Analog*
  - ✓ *Floating*
  - ✓ *Pull down*
  - ✓ *Pull up*



push-pull output

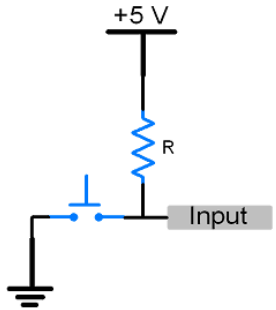


open-drain output



switch close = 0 V
switch open = undefine

High Impedance State

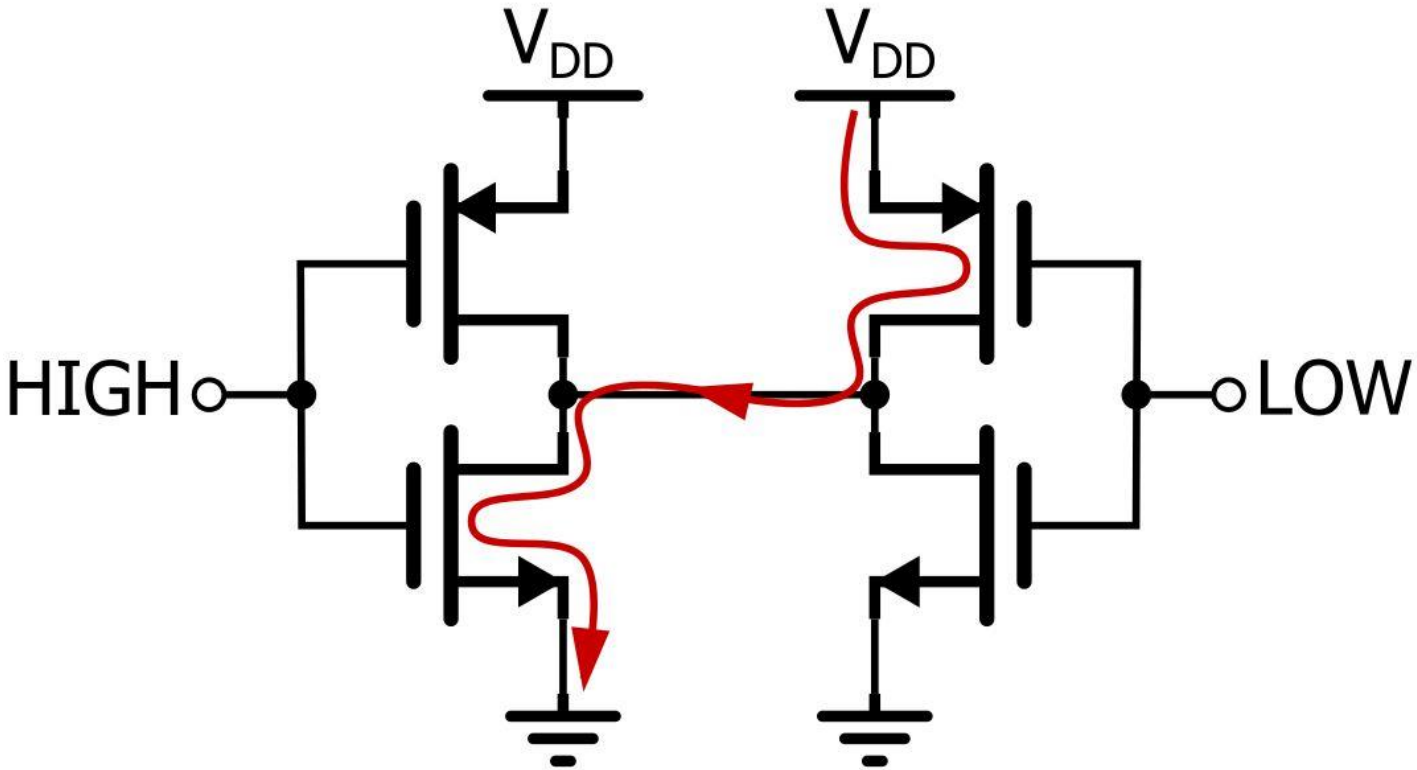


switch close = 0 V
switch open = +5 V

Pull-Up resistor

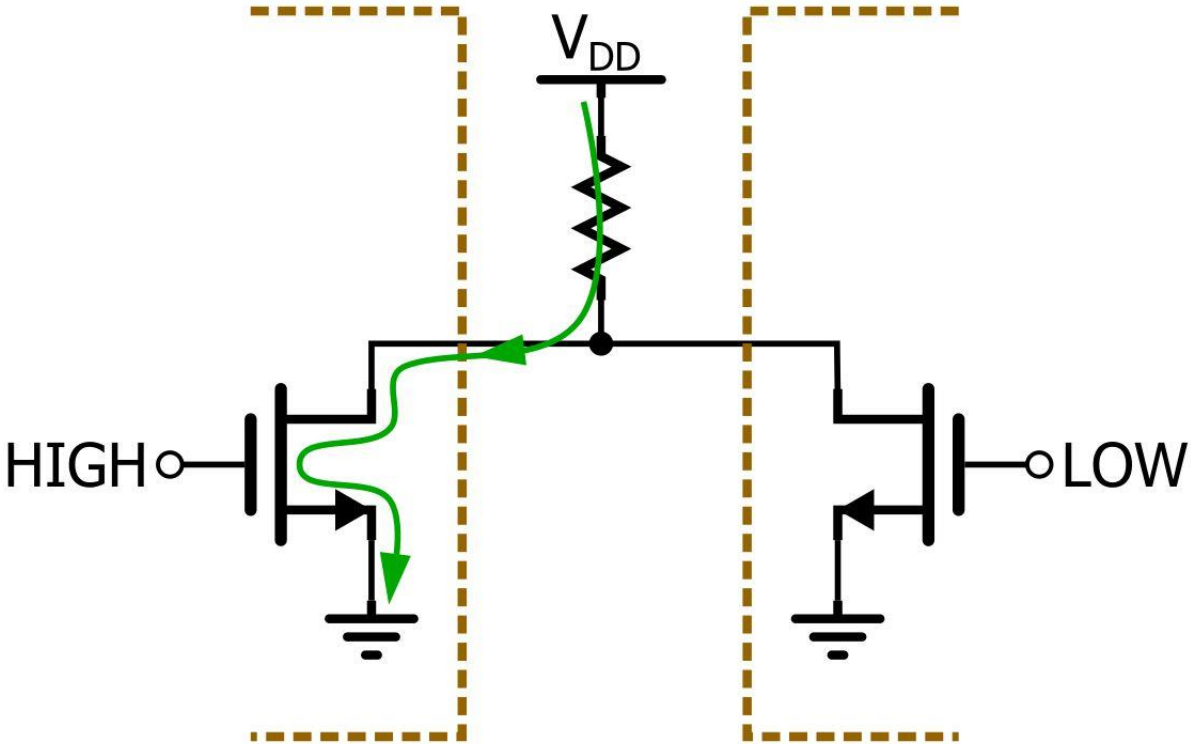
Solution #1

Push-pull



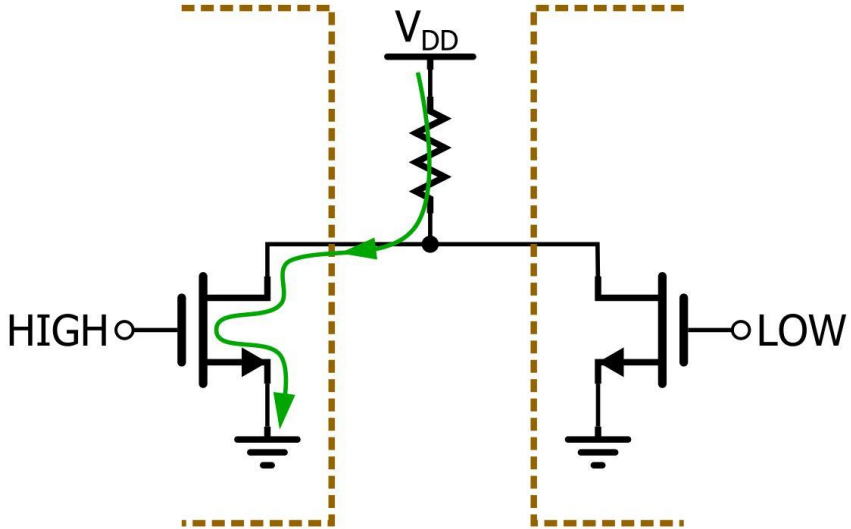
Solution #1

Open drain



Solution #1

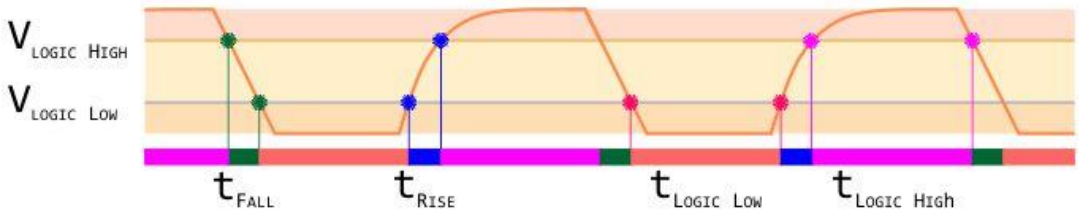
Which master is ignored on the bus?



Problem #2

- *Semiconductor devices always contain capacitance*

$$t \sim RC$$



⇒ *Pull-up resister with high resistance value will decrease frequency of this communication protocol.*

⇒ *But lower resistance value will be cause of higher current (I) in circuit.*

Solution #2

- *Provide devices, PCB with lower capacitance value*
- *Decrease number of devices in circuit to decrease capacitance of circuit*
- *Customers have to calculate value of the pull-up resisters.*

Problem #3

- *How do master select one slave to communicate at a time?*

- *How do master and slave handshake, plug-play?*

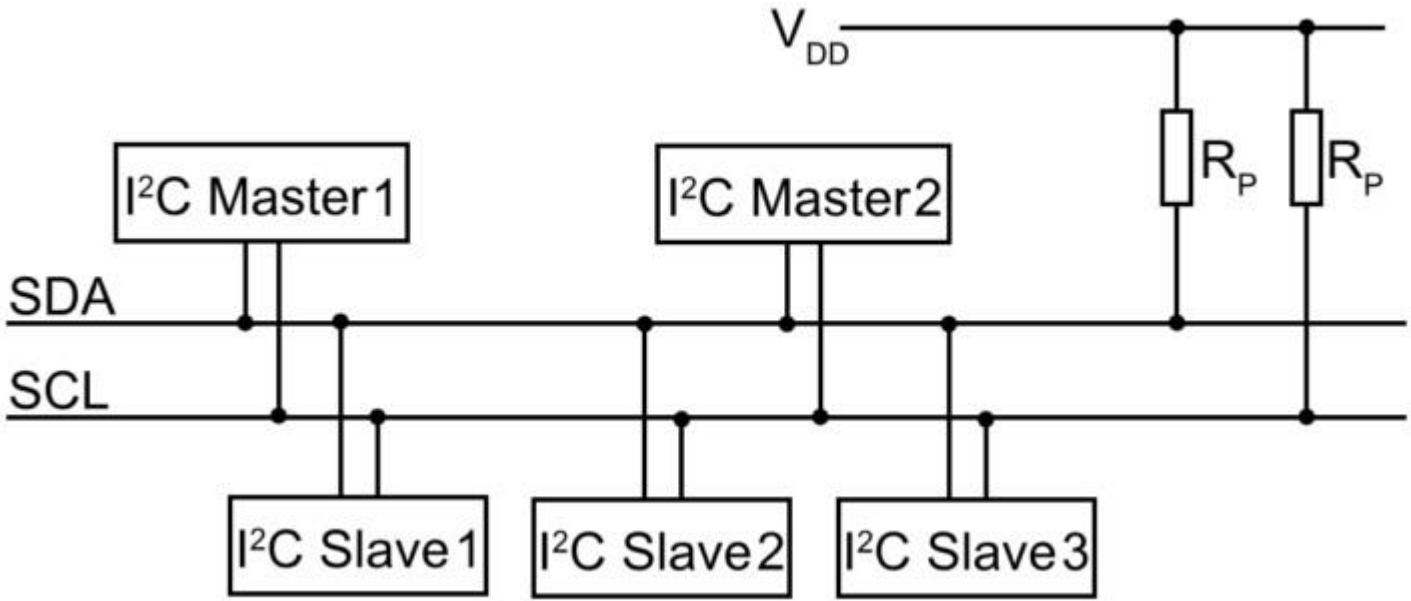
Solution #3

- *Provide each device in this bus a unique address*

- *Handshaking and Plug-play:*
  - ✓ *1 bit ACK/ NACK after each byte*
  - ✓ *Slave controls the clock*


TADA
LOOK WHAT I DID

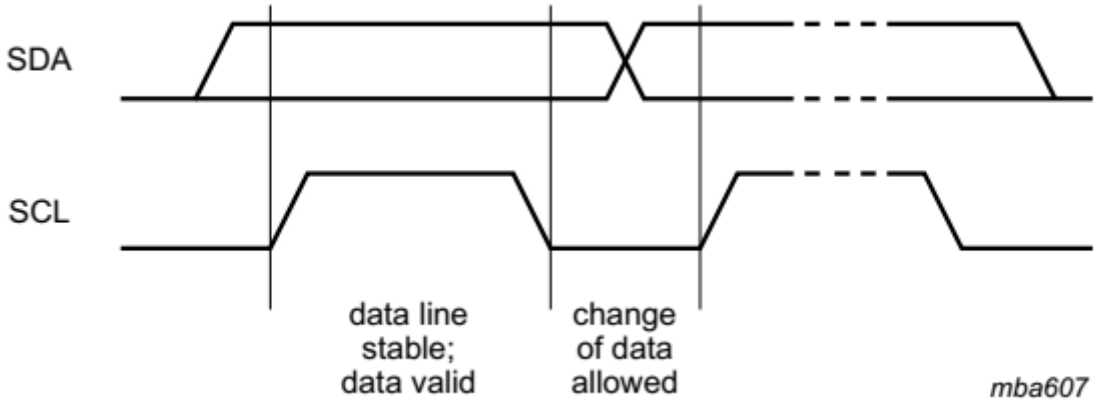
Inter integrated circuit introduction



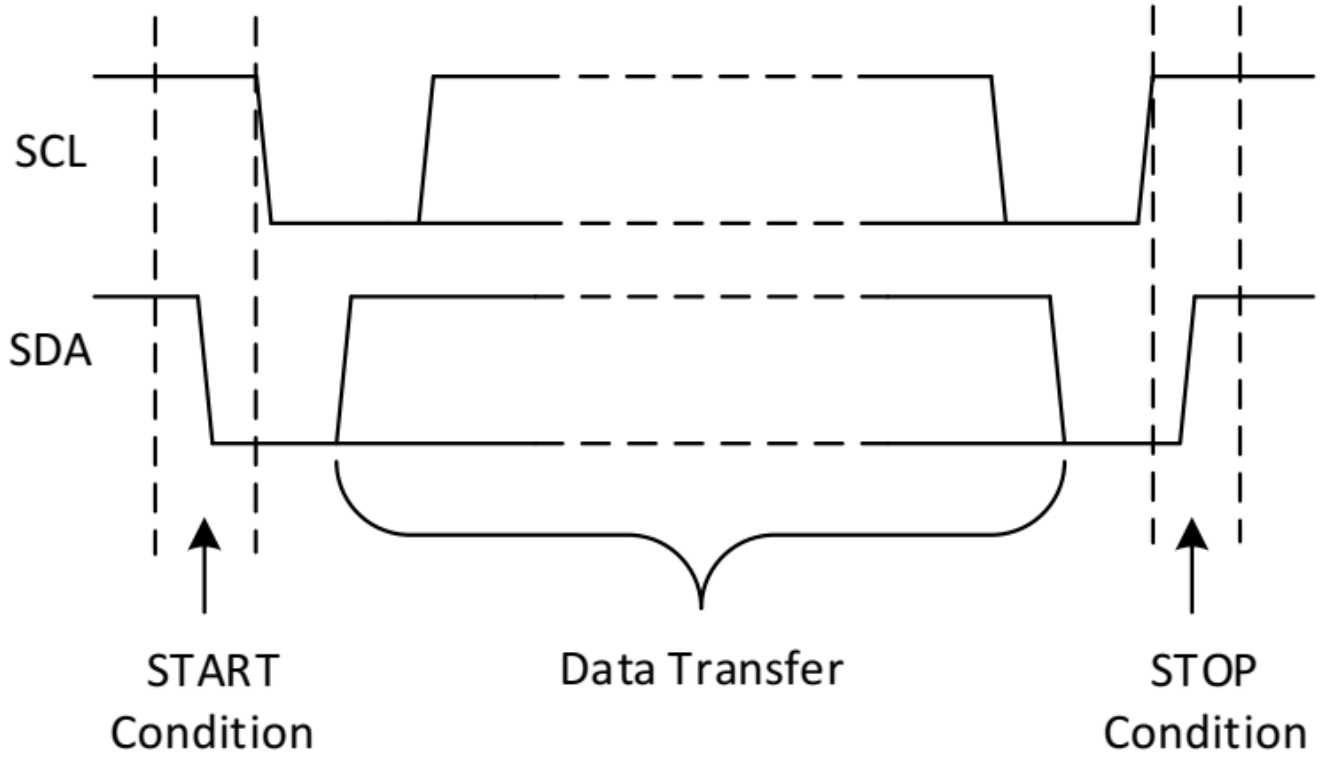
Inter integrated circuit introduction

- *Speed:*
  - ✓ *Standard mode: up to 100 kbit/s*
  - ✓ *Fast mode: up to 400 kbit/s*
  - ✓ *Fast mode plus: up to 1Mbit/s*
  - ✓ *High-speed mode: up to 3.4Mbit/s*
  - ✓ *Ultra-fast mode: up to 5Mbit/s (unidirectional bus)*
- *Max capacitance load: 400pF*
- *Address length: 7 or 10 bit*
- *Voltage level: various, typical voltages used are 1.8V, 3.3V, 5V*

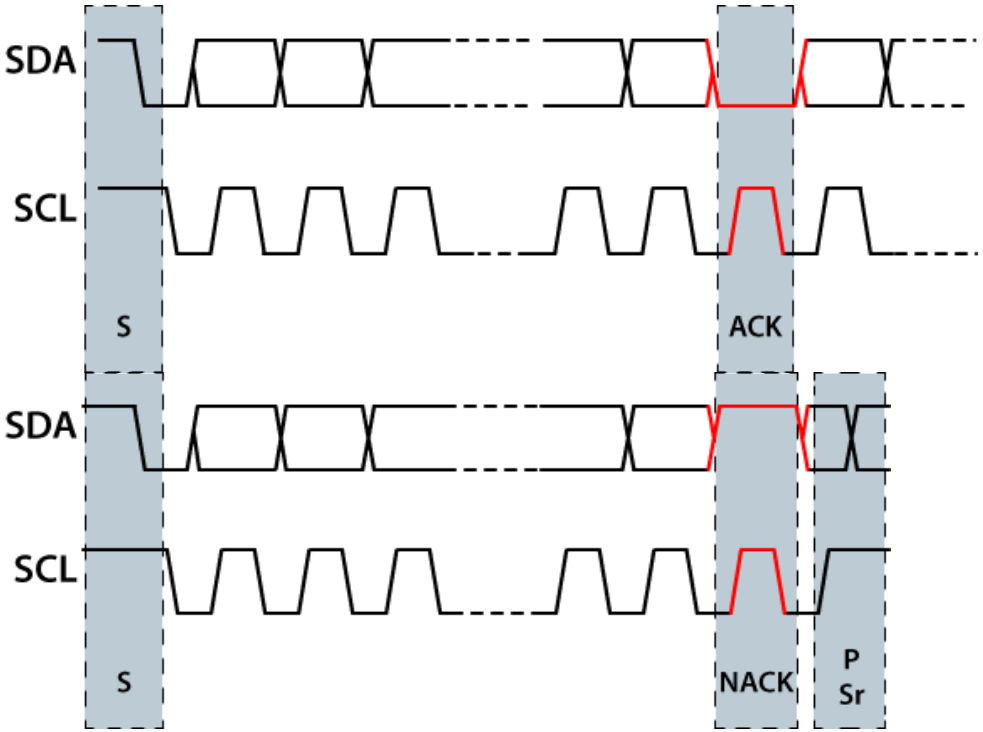
Data


SDA
SCL
data line stable; data valid
change of data allowed
mba607

Start and Stop



ACK and NACK

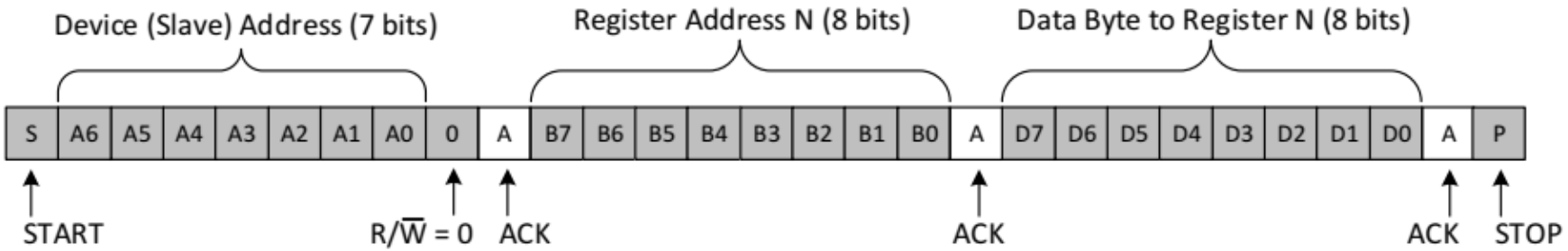


Data transmission

Master Controls SDA Line

Slave Controls SDA Line

Write to One Register in a Device

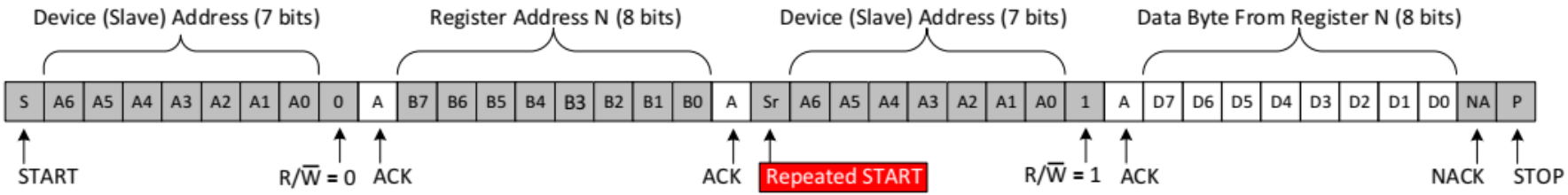


Data reception

Master Controls SDA Line

Slave Controls SDA Line

Read From One Register in a Device



I2C procedure

1. *Wait the bus is free*
2. *Send START*
3. *Provide CLOCK*
4. *Send ADDRESS, R/W bit*
5. *Receive ACK/NACK*
6. *Send or receive DATA*
7. *Receive ACK/NACK after each 8bit*
8. *Send STOP*

Pull-up resistor

$$R_P(min) = \frac{(V_{CC} - V_{OL}(max))}{I_{OL}} \qquad R_p(max) = \frac{t_r}{(0.8473 \times C_b)}$$

Parameter		Standard Mode (Max)	Fast Mode (Max)	Fast Mode Plus (Max)	Unit
t_r	Rise time of both SDA and SCL signals	1000	300	120	ns
C_b	Capacitive load for each bus line	400	400	550	pF
V_{OL}	Low-level output voltage (at 3 mA current sink, V_{CC} > 2 V)	0.4	0.4	0.4	V
	Low-level output voltage (at 2 mA current sink, V_{CC} ≤ 2 V)	–	0.2 × V_{CC}	0.2 × V_{CC}	V

Section 1: Summary

- *I2C characteristics*
- *Data transmission and reception*

Section #1: Q&A

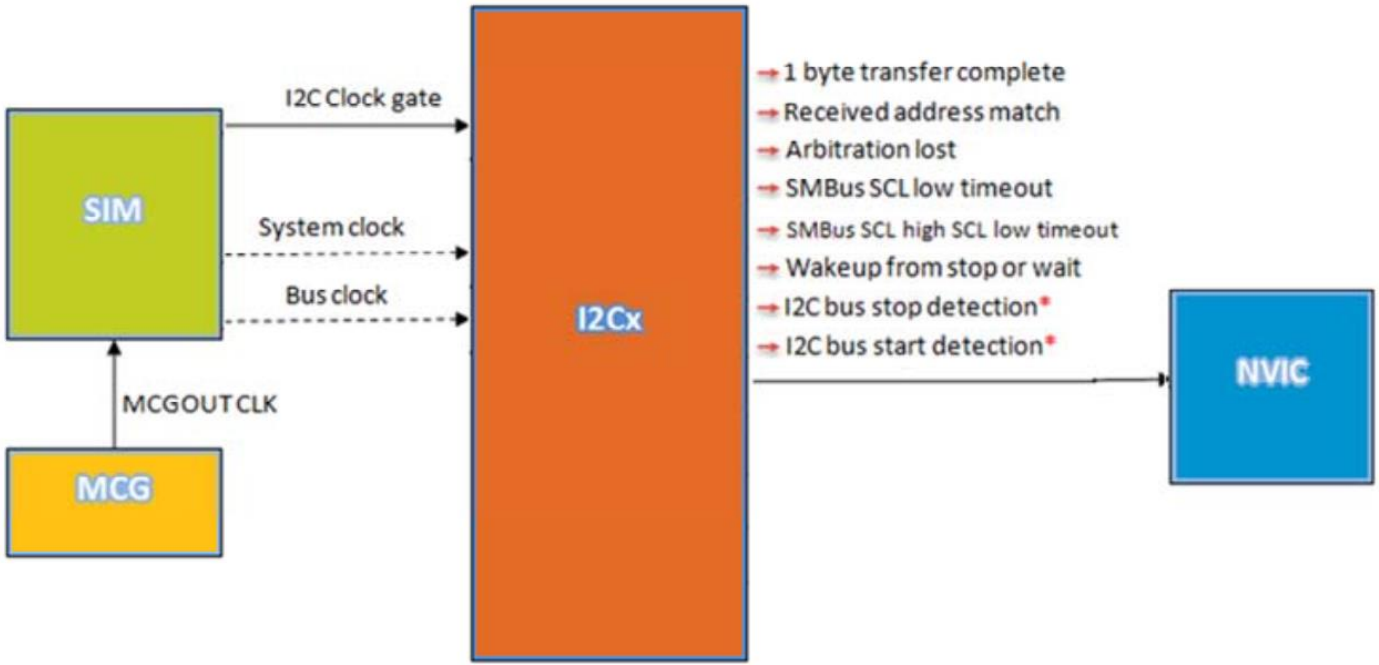
Section 2: Freedom KL46 I2C

Freedom KL46 I2C introduction

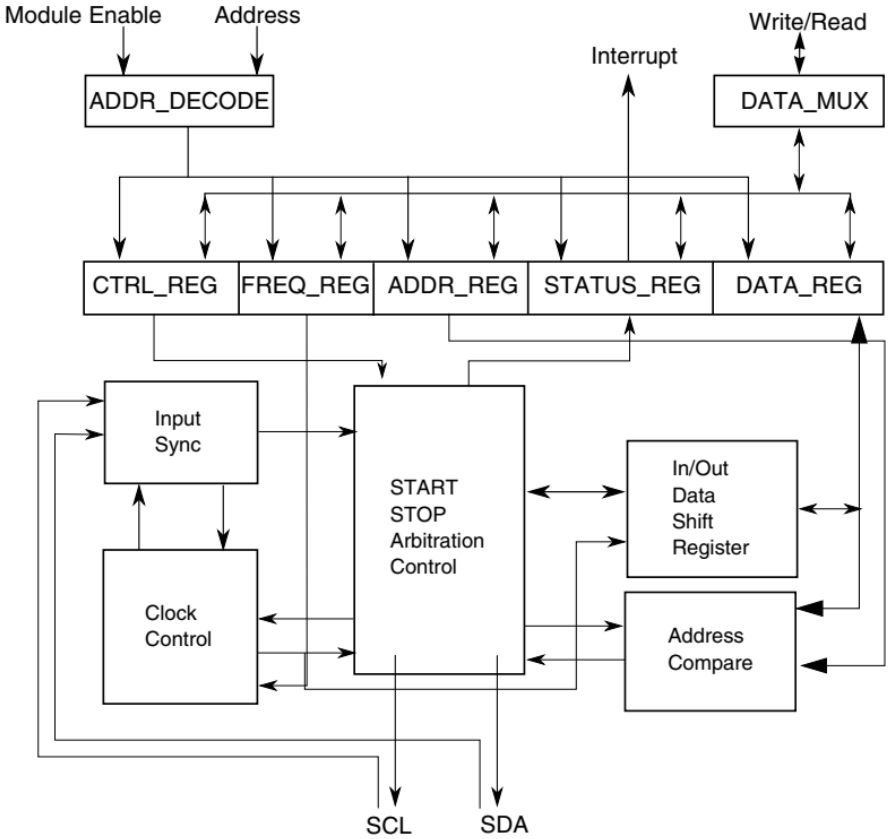
KL46 I2C main features

- *I2C bus specification support*
- *Software-selectable acknowledge bit*
- *Interrupt-driven byte-by-byte data transfer*
- *Arbitration-lost interrupt with automatic mode switching from master to slave*
- *Calling address identification interrupt*
- *Bus busy detection*
- *General call recognition*
- *DMA support*
- *Support for System Management Bus (SMBus) Specification, version 2*

I2C interconnections



I2C functional block diagram



Initialization

Slave:

1. *1. Write: Control Register 2*
   - ✓ *to enable or disable general call*
   - ✓ *to select 10-bit or 7-bit addressing mode*
2. *Write: Address Register 1 to set the slave address*
3. *Write: Control Register 1 to enable the I2C module and interrupts*
4. *Initialize RAM variables (IICEN = 1 and IICIE = 1) for transmit data*
5. *Interrupt routine*

Initialization

Master:

1. *Write: Frequency Divider register to set the I2C baud rate*
2. *Write: Control Register 1 to enable the I2C module and interrupts*
3. *Initialize RAM variables (IICEN = 1 and IICIE = 1) for transmit data*
4. *Initialize RAM variables used to achieve the routine shown in the following figure*
5. *Write: Control Register 1 to enable TX*
6. *Write: Control Register 1 to enable MST (master mode)*
7. *Write: Data register with the address of the target slave*

Further study

- *I2C Ultra-fast mode*
- *I3C*
- *SMBus*
- *PMBus*
- *IPMI*
- *ATCA*
- *DDC*

References

1. *NXP - UM10204 - I2C-bus specification and user manual - Rev. 6 - 4 April 2014*
2. *TI - SLVA704 - Understanding the I2C Bus - June 2015*
3. *Philips Semiconductors - AN10216-01 - I2C Manual – March 24, 2003*
4. *TI – SLVA689 - I2C Bus Pullup Resistor Calculation – Feb 2015*
5. *NXP - KL46 Sub-Family Reference Manual - Rev. 3, July 2013*
6. *NXP – I2C for Kinetis MCUs*

Lesson Summary

- *Introduction to I2C*
  - ✓ *Open-drain pin*
  - ✓ *Pull-up resistor*
  - ✓ *Arbitration*
  - ✓ *Handshake, Plug-play*
  - ✓ *…*
- *Freedom KL46 I2C*
  - ✓ *Block diagram*
  - ✓ *Initialization*
  - ✓ *…*

Q&A

Thank you