Implementation of Low Dynamic Power & Area Optimized 16-bit Reversible ALU

-Utkarsh Mishra

1. Design

- Today's Computer chips are facing a severe problem with power dissipation in addition to that heat generation. Reversible logic reduces power consumption as zero-energy computation has inspired it.

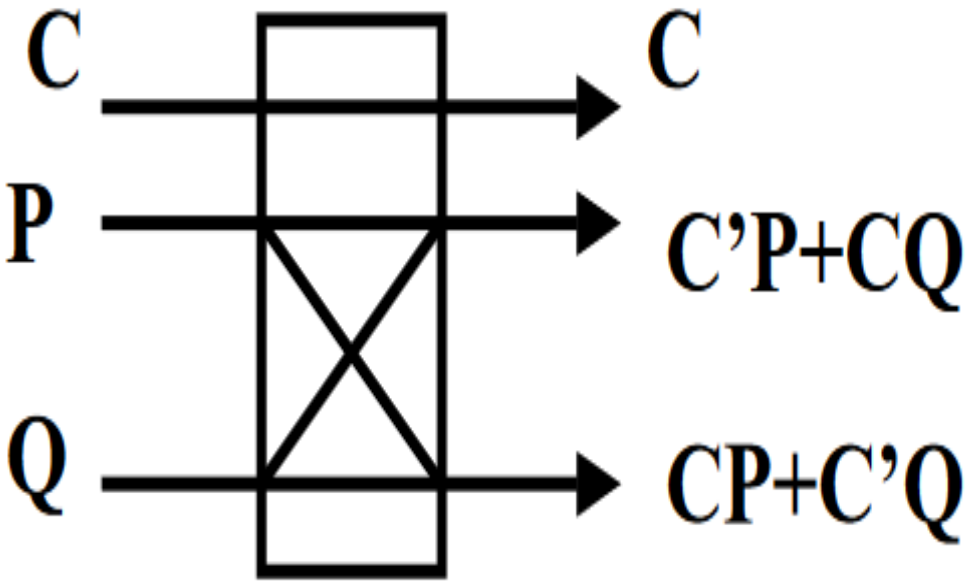
- My VLSI project describes Design and Implementation of 16-Bit ALU built using reversible decoder controlled combinational circuits on Spartan3E (XC3S500E-FG320-5) FPGA.

Reversible Gates.

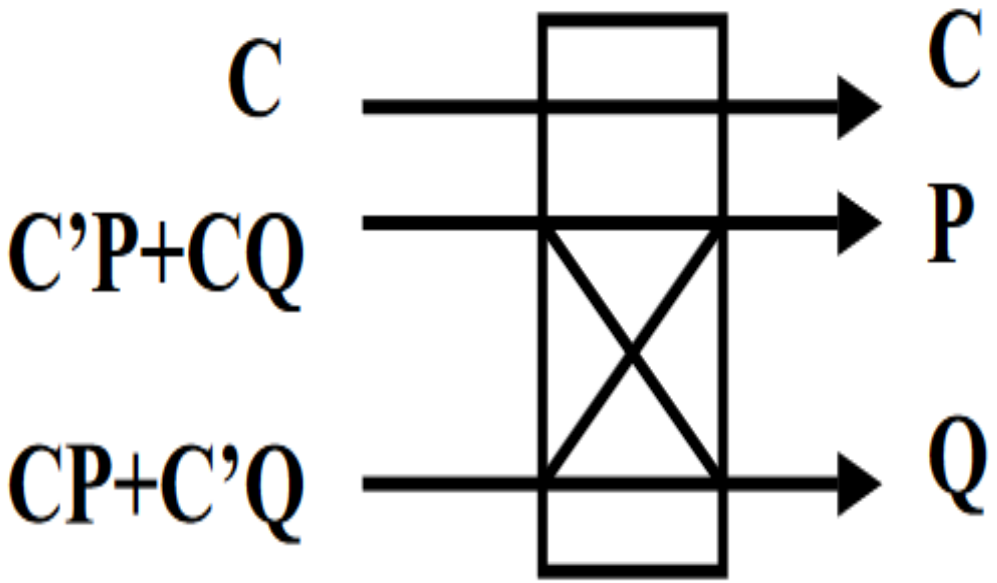
- A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs.

- Also, in the synthesis of reversible circuits direct fan-Out is not allowed as one–to-many concept is not reversible.

Fredkin Gate



Inverse Fredkin Gate

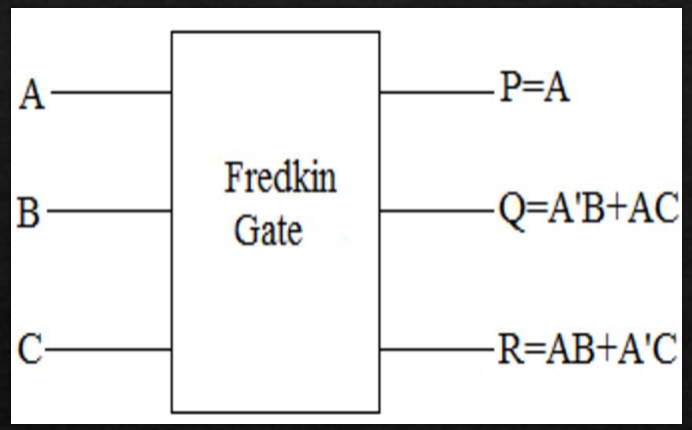


How this works?

- Rolf Landauer, 1961. Whenever we use a logically irreversible gate we dissipate energy into the environment.
- The loss of information is associated with laws of physics requiring that one bit of information lost dissipates kTln2 of energy.

- Landauer/Bennett: all operations required in computation could be performed in a reversible manner, thus dissipating no heat!
- And so according to a second law of thermodynamics: ds = dq/T(for reversible process)

Some reversible gates.



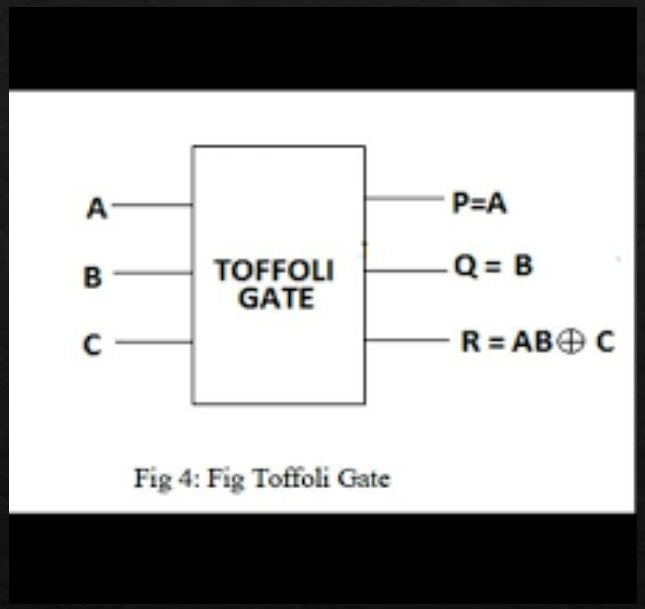
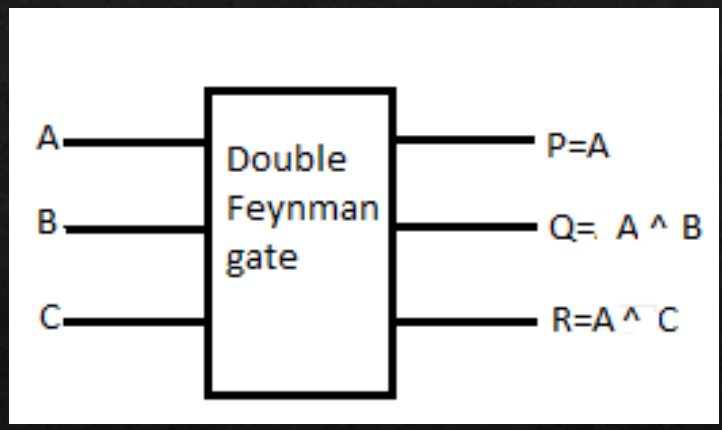
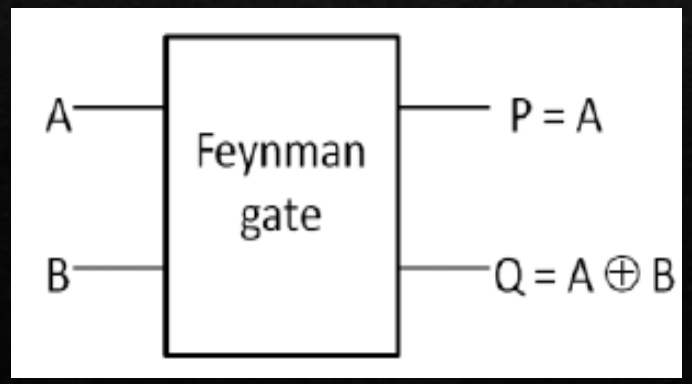
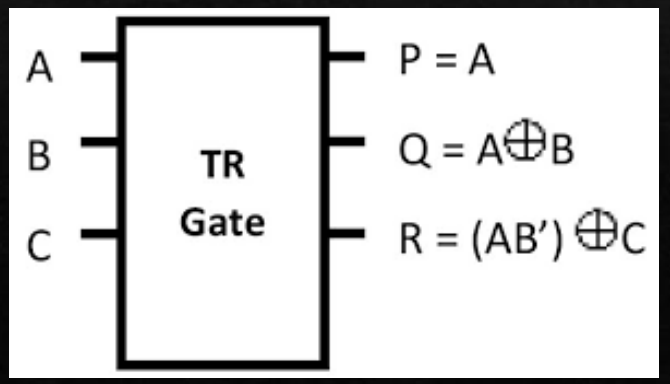
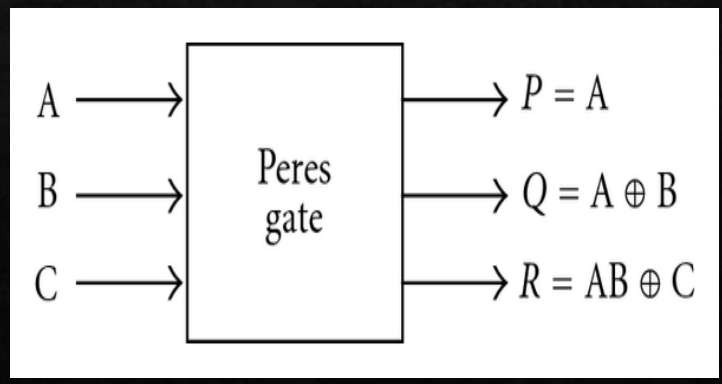


Fig 4: Fig Toffoli Gate



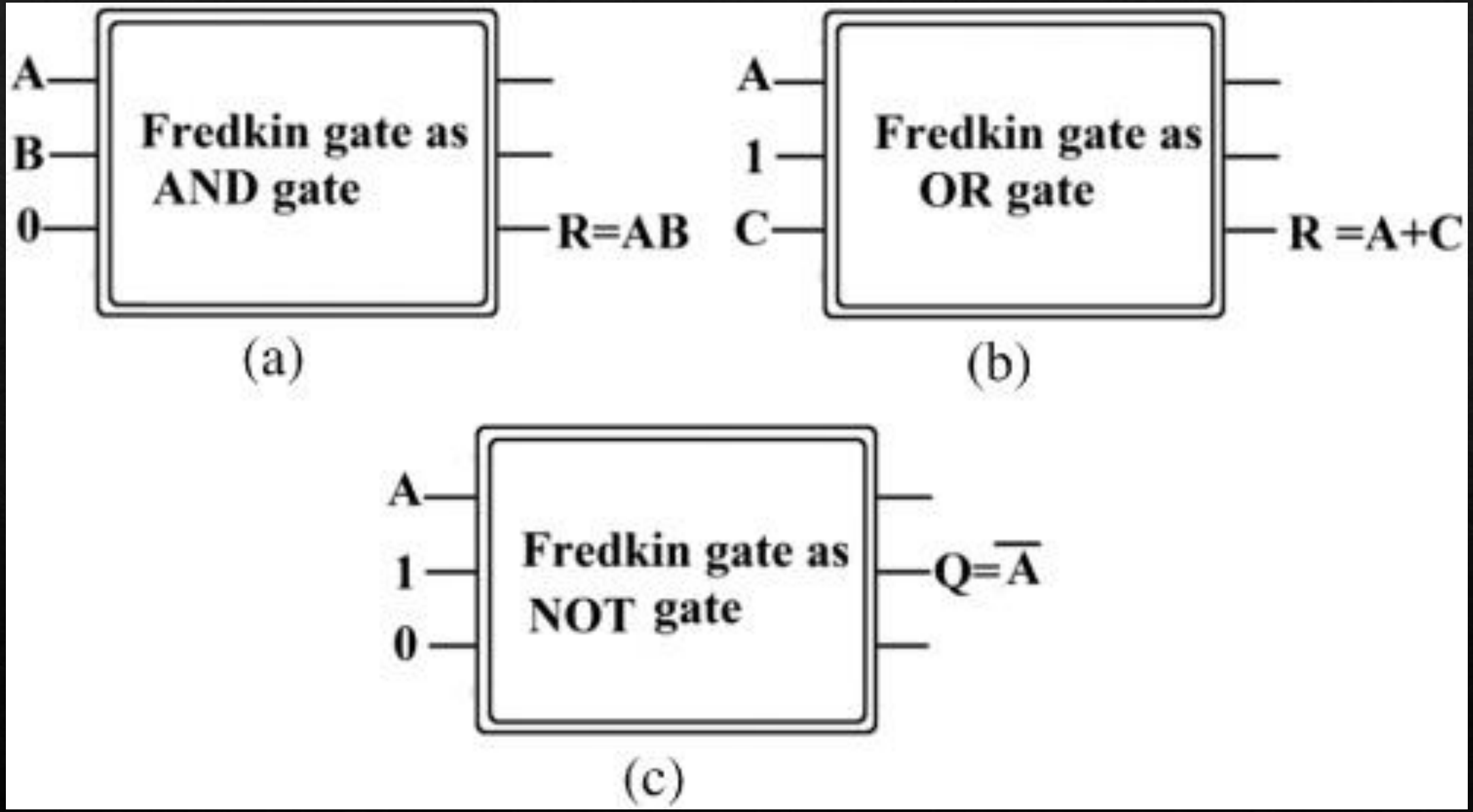




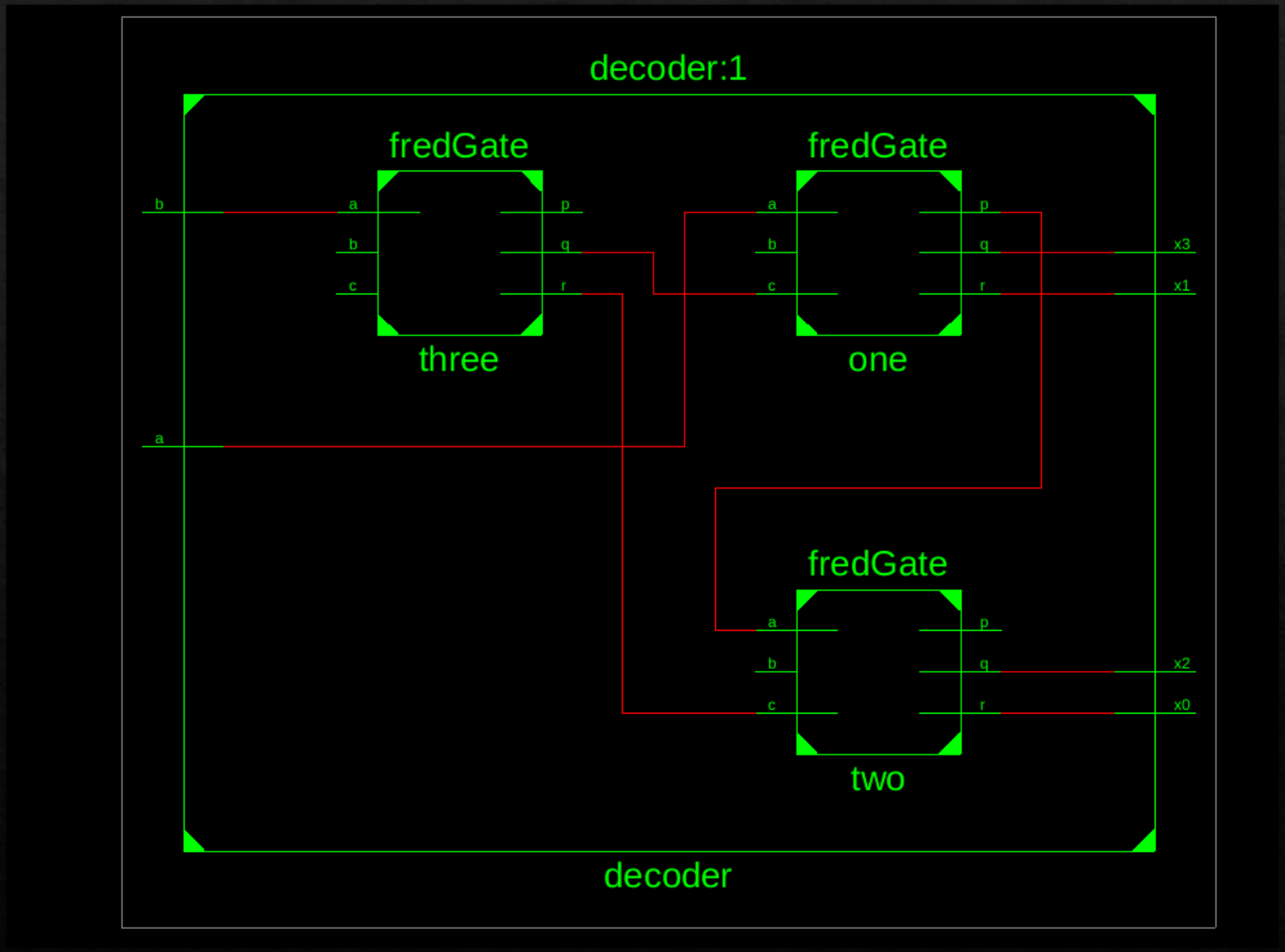


2. Workflow used-

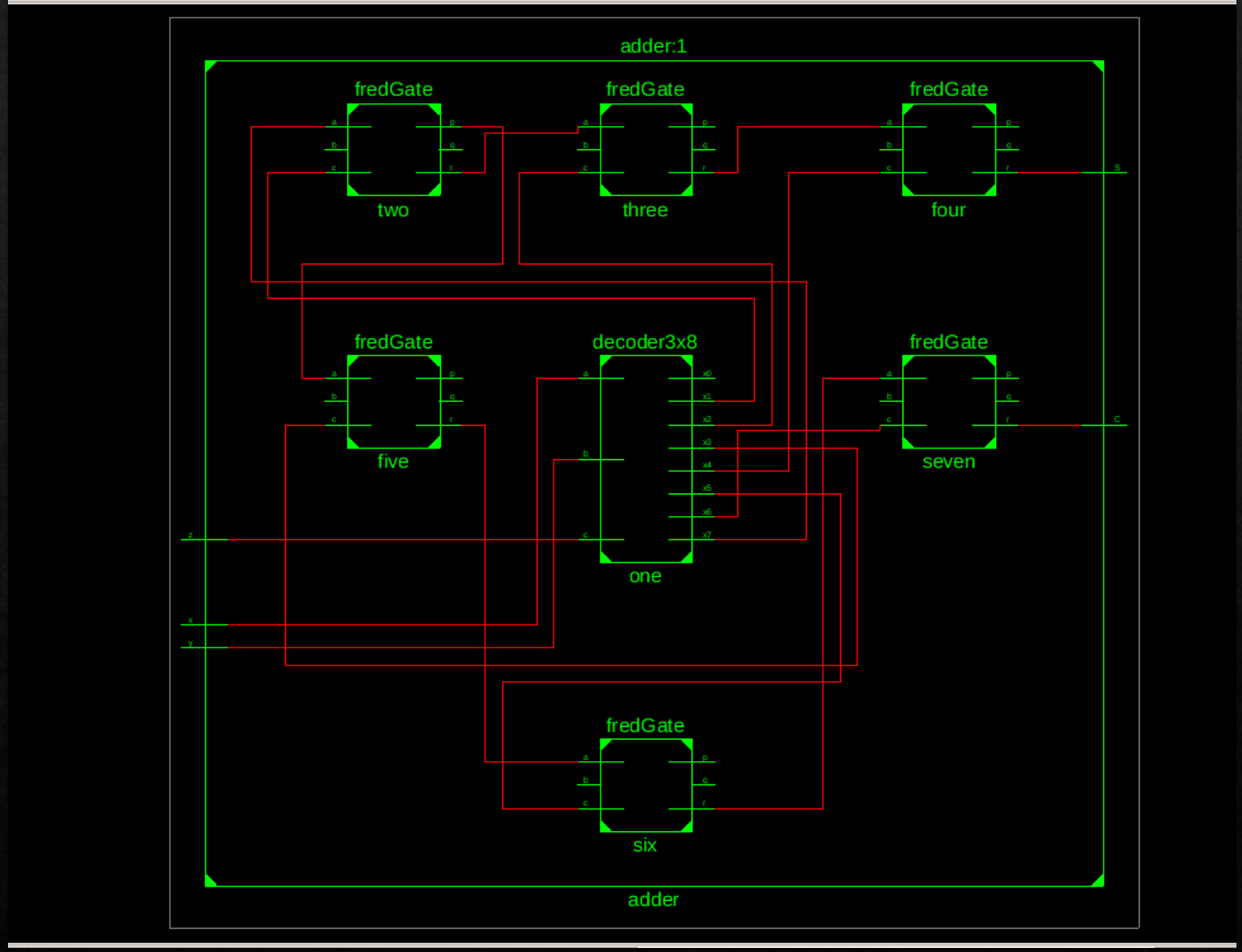
- Application Specific integrated circuit (Primary)
- Field Programmable gate array (Secondary)


A
B
0
Fredkin gate as
AND gate
R=AB
(a)
A
1
C
Fredkin gate as
OR gate
R =A+C
(b)
A
1
0
Fredkin gate as
NOT gate
Q=$\overline{A}$
(c)

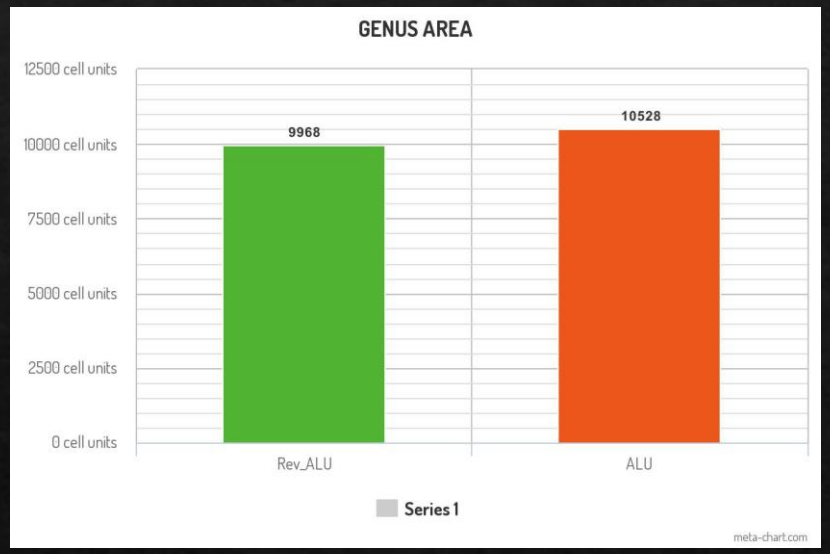
Decoder-

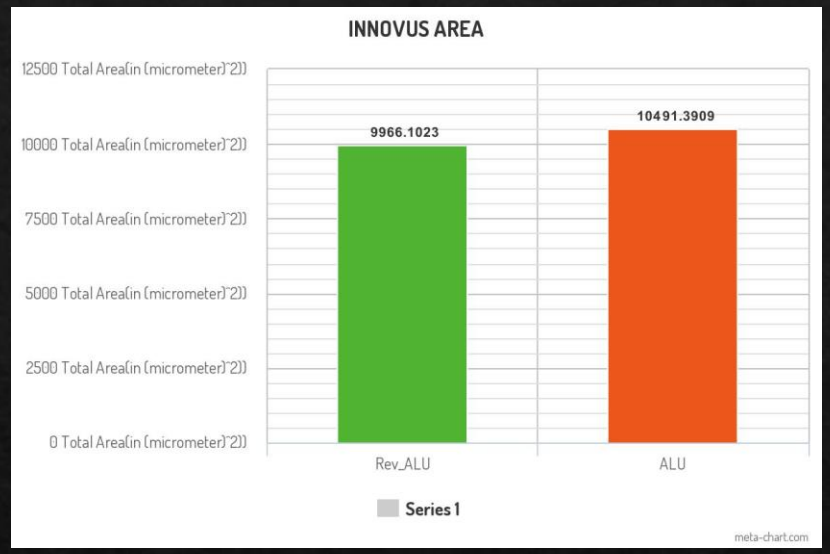

decoder:1
fredGate
fredGate
b
a
b
c
p
q
r
three
a
b
c
p
q
r
x3
x1
one
a
fredGate
a
b
c
p
q
r
x2
x0
two
decoder

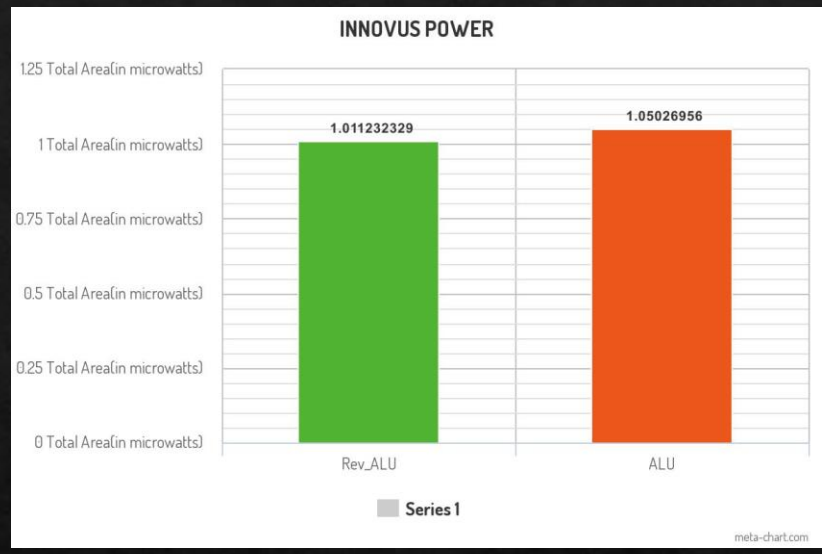
Adder-


adder:1
fredGate
two
fredGate
three
fredGate
four
fredGate
five
decoder3x8
one
fredGate
seven
fredGate
six
adder

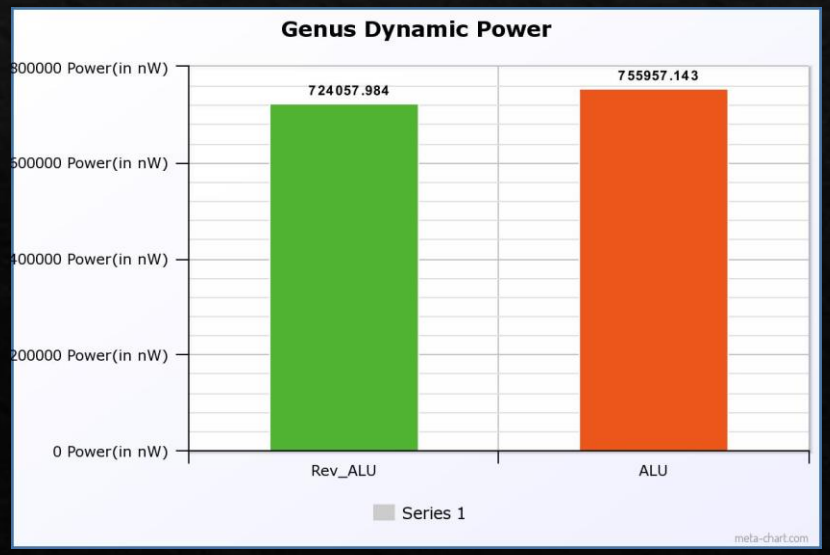
3.Results-

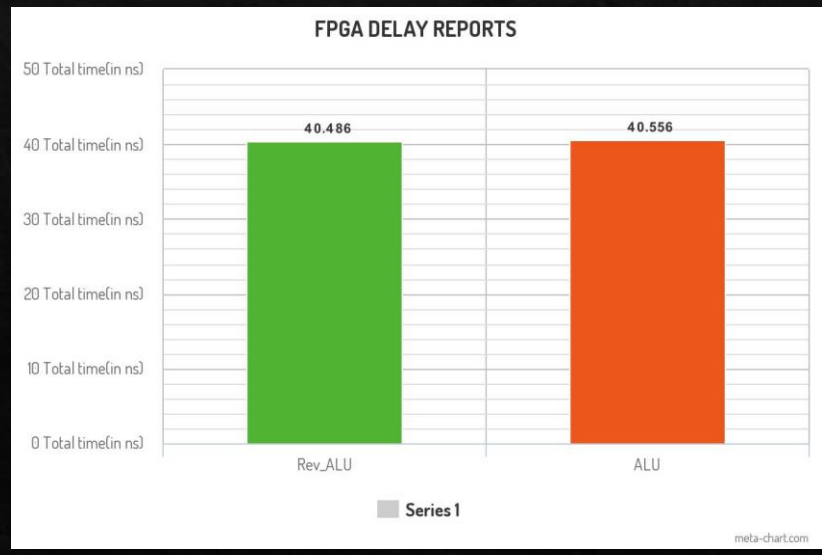

GENUS AREA
12500 cell units
10000 cell units
7500 cell units
5000 cell units
2500 cell units
0 cell units
9968
10528
Rev_ALU
ALU
Series 1
meta-chart.com


INNOVUS AREA
12500 Total Area(in (micrometer)^2))
10000 Total Area(in (micrometer)^2))
7500 Total Area(in (micrometer)^2))
5000 Total Area(in (micrometer)^2))
2500 Total Area(in (micrometer)^2))
0 Total Area(in (micrometer)^2))
9966.1023
10491.3909
Rev_ALU
ALU
Series 1
meta-chart.com

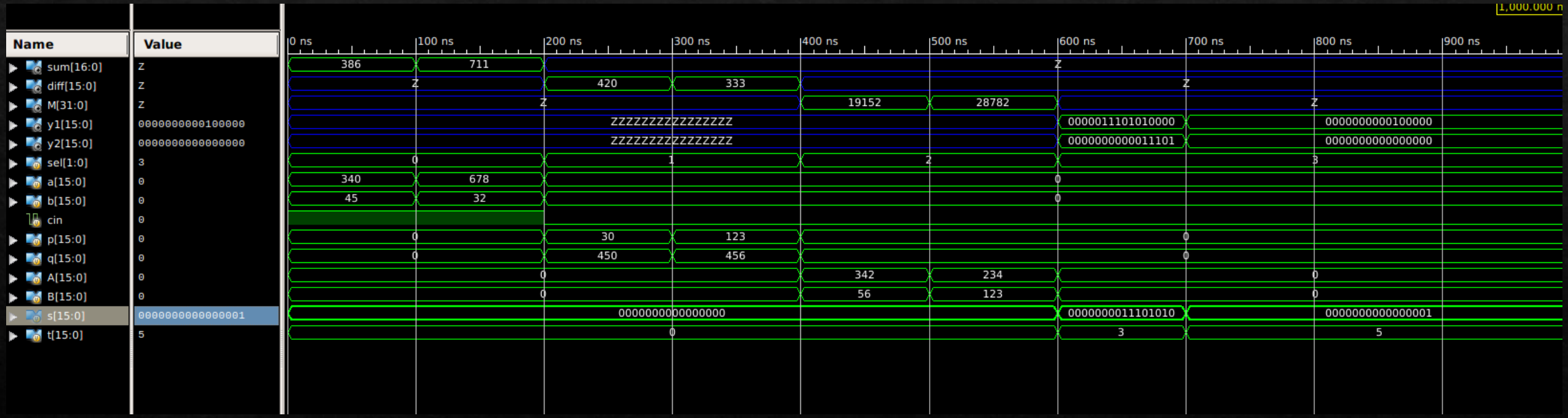

INNOVUS POWER
1.25 Total Area(in microwatts)
1 Total Area(in microwatts)
0.75 Total Area(in microwatts)
0.5 Total Area(in microwatts)
0.25 Total Area(in microwatts)
0 Total Area(in microwatts)
1.011232329
1.05026956
Rev_ALU
ALU
Series 1
meta-chart.com


GENUS POWER
1000 Total Power(in microwatts)
800 Total Power(in microwatts)
600 Total Power(in microwatts)
400 Total Power(in microwatts)
200 Total Power(in microwatts)
0 Total Power(in microwatts)
777.123379
814.690707
Rev_ALU
ALU
Series 1
meta-chart.com

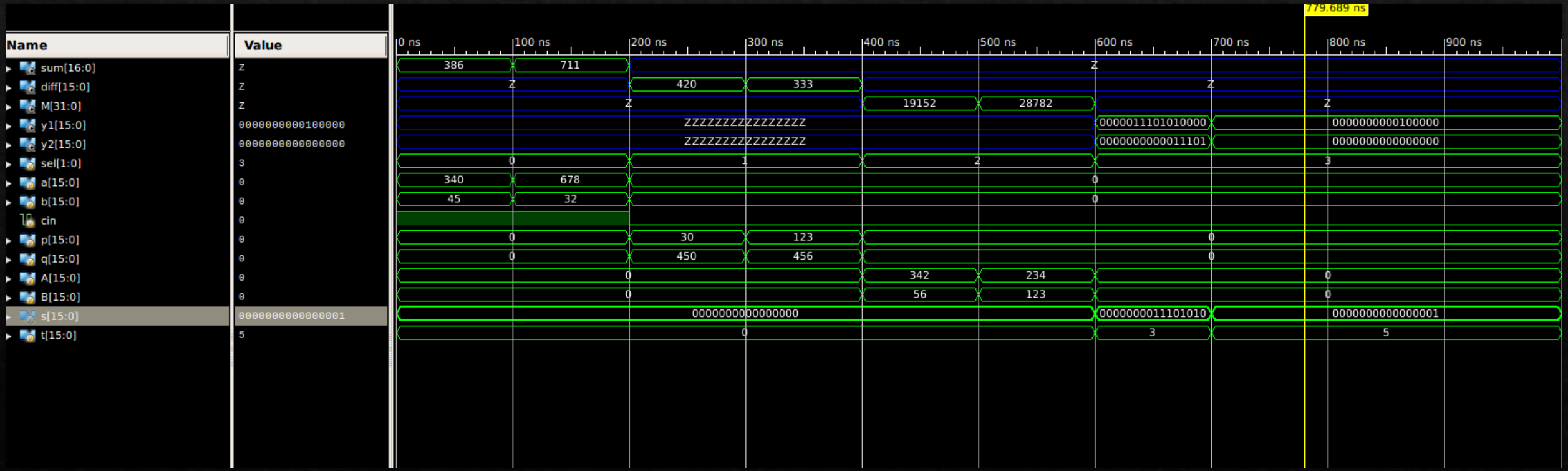

Genus Dynamic Power
800000 Power(in nW)
600000 Power(in nW)
400000 Power(in nW)
200000 Power(in nW)
0 Power(in nW)
724057.984
755957.143
Rev_ALU
ALU
Series 1
meta-chart.com


FPGA DELAY REPORTS
50 Total time(in ns)
40 Total time(in ns)
30 Total time(in ns)
20 Total time(in ns)
10 Total time(in ns)
0 Total time(in ns)
40.486
40.556
Rev_ALU
ALU
Series 1
meta-chart.com

Timing diagrams- ALU



Rev_ALU-


779.689 ns
Name
Value
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
sum[16:0]
diff[15:0]
M[31:0]
y1[15:0]
y2[15:0]
sel[1:0]
a[15:0]
b[15:0]
cin
p[15:0]
q[15:0]
A[15:0]
B[15:0]
s[15:0]
t[15:0]
0000000000100000
0000000000000000
0000000000000001

Results to be looked for.

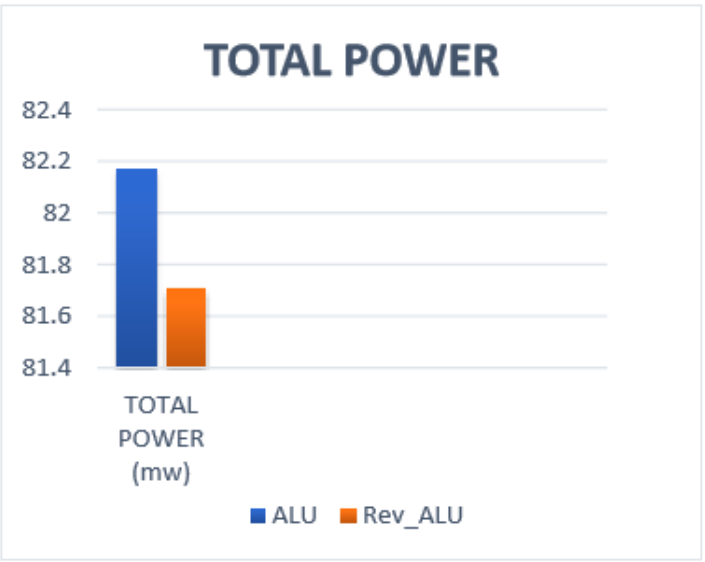


Figure 20: Total power consumption Rev_ALU vsALU.

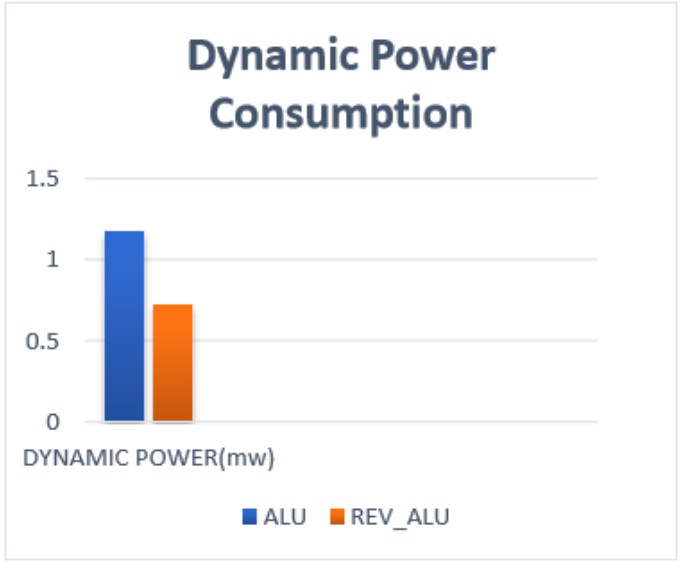


Figure 19: Representing dynamic power consumption Rev_ALU vs ALU.

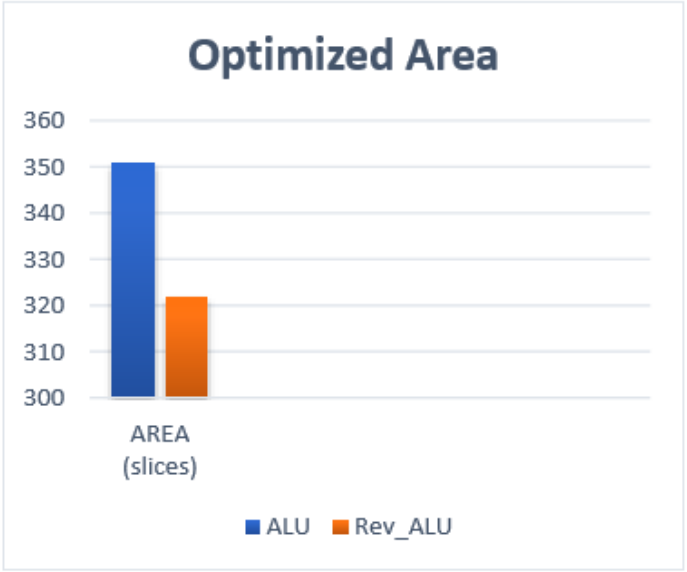


Figure 18: Representing Area Rev_ALU vs ALU

4.Comparison

	Genus Area (in cell-units)	Genus Power (in microwatts)	Innovus Power (milliwatts)	Innovus Area(micrometer-square)
ALU	10528	814.690707	1.05026956	10491.3909
Rev_ALU	9968	777.123397	1.011232329	9966.1023

	Total Power (microwatts)	Area (Slices)
Rev_ALU(Paper)	81.71	322
ALU (Paper)	82.17	351