



香港中文大學  
The Chinese University of Hong Kong

# CENG3420

## Lab 2-1: RISC-V RV32I Assembler

Chen BAI & Yuxuan ZHAO  
Department of Computer Science & Engineering  
Chinese University of Hong Kong  
[cbai@cse.cuhk.edu.hk](mailto:cbai@cse.cuhk.edu.hk) &  
[yxzhao21@cse.cuhk.edu.hk](mailto:yxzhao21@cse.cuhk.edu.hk)

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- ② Introduction to RV32I
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- ④ RISC-V-LC Assembler
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# Introduction

Use C programming language to finish lab assignments in following weeks.

- Lab 2.1 – implement an RISC-V-LC Assembler
- Lab 2.2 – implement an RISC-V-LC ISA Simulator
- Lab 3.x – implement an RISC-V-LC Simulator

### NOTICE

Lab2 & Lab3 are challenging!

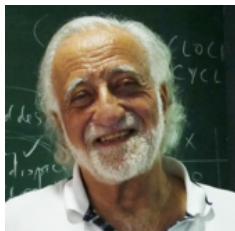
Once you have passed Lab2 & Lab3, you will be more familiar with RV32I & a basic implementation!

- Assembly language – symbolic (we have learned in Lab1)
- Machine language – binary
- **Assembler** is a program that
  - turns symbols into machine instructions, e.g., riscv64-unknown-elf-as
- **Simulator** is a program that
  - mimics the behavior of a processor
  - usually written in high-level language, e.g., spike

# Introduction

Our Lab2 & Lab3 are Inspired by LC-3b

- LC-3b: **Little Computer 3, b** version.
- Relatively simple instruction set
- Used in CS & CE teaching courses
- Developed by Yale Patt@UT & Sanjay J. Patel@UIUC



In Lab2-2, our RV32I ISA Simulator integrates

- RISC-V 32 general-purpose registers
- 32-bit data and address
- 25+ instructions (including pseudo instructions)

In Lab3, 4 more special-purpose registers will be added:

- Program Counter ([PC](#))
- Instruction Register ([IR](#))
- Memory Access Register ([MAR](#))
- Memory Data Register ([MDR](#))

# Introduction to RV32I

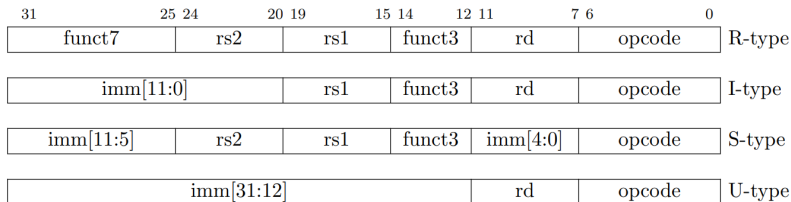


- The instruction encoding width is 32-bit.
- Each instruction is aligned with a **four-byte** boundary in memory.
- RV32I only manipulates integer numbers and no multiplication or division.
- Our labs are based on the official RISC-V ISA manual:  
<https://github.com/riscv/riscv-isa-manual/releases/download/Ratified-IMAFDQC/riscv-spec-20191213.pdf>.

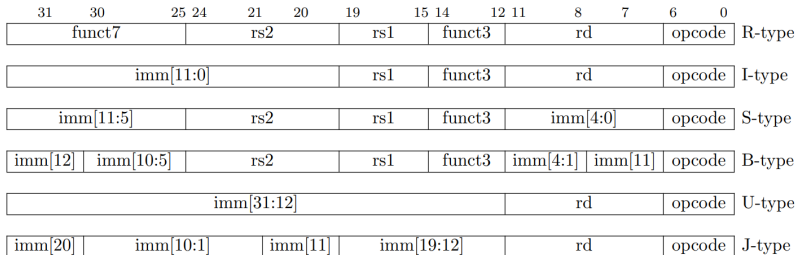
- **Integer Computational Instructions**
- **Control Transfer Instructions**
- **Load and Store Instructions**
- Memory Ordering Instructions
- Environment Call and Breakpoints
- HINT Instructions

# Introduction to RV32I

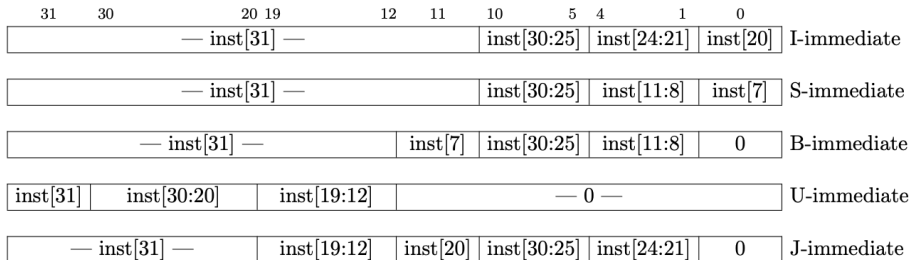
- Four core instruction formats



- Two variants of the instruction formats



# Introduction to RV32I



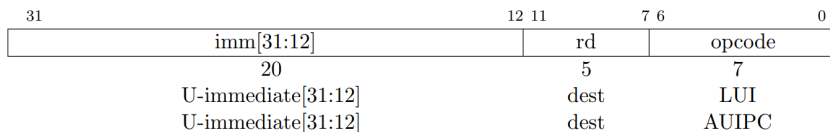
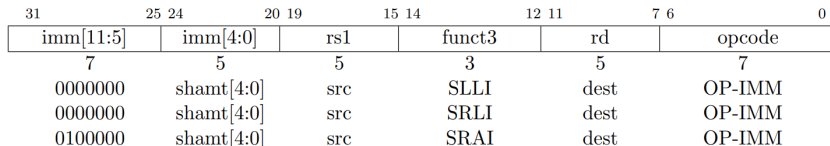
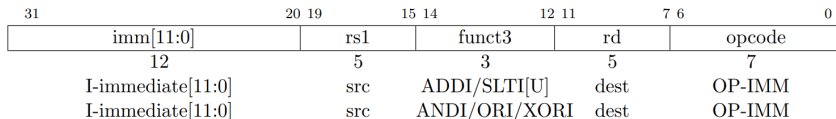
## Immediate values encodings

If a value, e.g., 0xabcd, is encoded with I, S, B, U, or J format, can you write how it is encoded?

- Integer Register-Immediate Instructions
  - addi, slti, andi, ori, xori, slli, srli, srai, lui
- Integer Register-Register Instructions
  - add, slt, and, or, xor, sll, srl, sub, sra

# Introduction to RV32I

## Integer Register-Immediate Instructions



# Introduction to RV32I

## Integer Register-Register Instructions

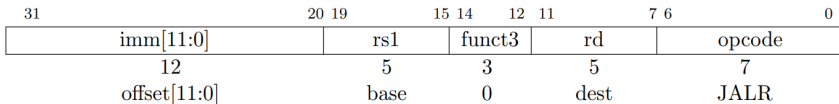
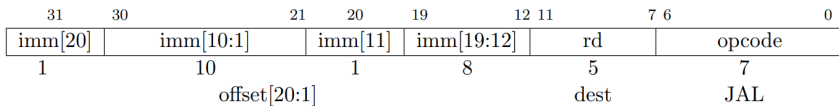
31	25 24	20 19	15 14	12 11	7 6	0
funct7	rs2	rs1	funct3	rd	opcode	
7	5	5	3	5	7	
0000000	src2	src1	ADD/SLT/SLTU	dest	OP	
0000000	src2	src1	AND/OR/XOR	dest	OP	
0000000	src2	src1	SLL/SRL	dest	OP	
0100000	src2	src1	SUB/SRA	dest	OP	

- Unconditional Jumps
  - jal, jalr
- Conditional Branches
  - beq, bne, blt, bge



# Introduction to RV32I

## Unconditional Jumps



# Introduction to RV32I

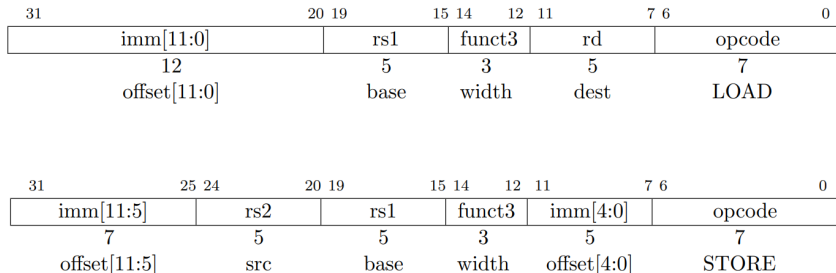
## Conditional Branches

31	30	25	24	20	19	15	14	12	11	8	7	6	0
imm[12]	imm[10:5]	rs2	rs1	funct3	imm[4:1]	imm[11]	opcode						
1	6	5	5	3	4	1	7						
offset[12 10:5]		src2	src1	BEQ/BNE	offset[11 4:1]		BRANCH						
offset[12 10:5]		src2	src1	BLT[U]	offset[11 4:1]		BRANCH						
offset[12 10:5]		src2	src1	BGE[U]	offset[11 4:1]		BRANCH						

- Load
  - lb, lh, lw
- Store
  - sb, sh, sw

# Introduction to RV32I

## Load and Store Instructions



The [EEI](#) will define whether the memory system is little-endian or big-endian. In RISC-V, endianness is byte-address invariant.

# RISCV-LC Code Specifications

## NOTICE

To make labs easy, I have added some self-defined directives.

- Label specification: no colon and one code line cannot contain only labels.
- No .data and .text directives
- Add one pseudo instruction: LA
- Add one self-customized directive: .FILL
- Add one halt instruction: HALT

Label specification: no colon and one code line cannot contain only labels.

```
1      la a0, AL
2      lw a0, 0(a0)
3      blt a0, zero, L1
4 ▼ L1  addi a7, a0, 13
5      bge zero, a7, L1
```

Specification examples

Add one pseudo instruction: LA. LA is translated to two RV32I instructions: `lui` and `addi`.

```
1      la a0, A # lui a0, 0x0; addr = 0x0
2      # addi a0, a0, 0x8; addr = 0x4
3      A .FILL -2 # addr = 0x8
```

Translate `la` to `lui` and `addi`



.FILL is similar to .byte, .word, etc.

```
30  
31    AL    .FILL -2  
32    BL    .FILL -9  
33
```

.FILL directive

# RISCV-LC Assembler

# Lab 2-1 Assignment

## Pre-requisites

- Learn Linux/MacOS terminal commands, and we prefer using Linux/MacOS
- Install `git` in your computer: `sudo apt-get install git`
- Learn `git` from the reference: <https://git-scm.com/docs/gittutorial>
- Learn `Makefile` from the reference: <https://makefiletutorial.com/>

### Get Latest Updates of the Lab

- Click <https://github.com/baichen318>.

- Click the **Follow** button.

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**Chen BAI**  
baichen318

I am currently a second-year Ph.D. student at the Department of Computer Science and Engineering of The Chinese University of Hong Kong.

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Python 5
- vim.config** (Public)  
My own custom configurations for the Vim editor  
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An Agile RISC-V SoC Design Framework with in-order cores, out-of-order cores, accelerators, and more  
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- Raspberry-Pi-SmartCar** (Public)  
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Python 1

**Click the button to follow me!**

# Lab 2-1 Assignment

## Pre-requisites – Get RISC-V LC Assembler

Please visit the website for more information:

<https://github.com/baichen318/ceng3420>

### Get the RV32I Assembler

In the terminal of your computer, type these commands:

- `git clone https://github.com/baichen318/ceng3420.git`
- `cd ceng3420`
- `git checkout lab2.1`

### Compile (Linux/MacOS environment is suggested)

- `make`

### Run the assembler

- `./asm benchmarks/isa.asm isa.bin` # you can check the output machine code: isa.bin  
if you have implemented the assembler

Now, let me take a live demo – by walking through the code repo to learn the assembler.

- Know the codes organizations.
- `addi` example in **asm.c**
- `add` example in **asm.c**
- `beq` example in **asm.c**
- `lb` example in **asm.c**

# Lab 2-1 Assignment

### **Finish the RV32I assembler including 25 instructions in asm.c as follows**

- Integer Register-Immediate Instructions: slli, xori, srli, srai, ori, andi, lui
- Integer Register-Register Operations: sub, sll, xor, srl, sra, or, and
- Unconditional Jumps: jalr, jal
- Conditional Branches: bne, blt, bge
- Load and Store Instructions: lb, lh, lw, sb, sh, sw

These unimplemented codes are commented with [Lab2-1 assignment](#)



## Verification of Implementations

Verify your codes with these benchmarks (inside the `benchmarks` directory)

- `isa.asm`
- `count10.asm`
- `swap.asm`

Compare your output with `.bin` file. If both of them are the same, you are correct!

A quick verification command in the terminal: `make validate # generate reports inside the tools directory.`

## Submission Method:

Submit a zip file including source codes and a report **after** the whole lectures of Lab2 into **Blackboard**.

### Tips

Inside `docs`, there are three valuable documents for your reference!

- `opcodes-rv32i`: RV32I opcodes
- `riscv-spec-20191213.pdf`: RV32I specifications
- `risc-v-asm-manual.pdf`: RV32I assembly programming manual