

Name	Type	Description
GPP_B15 / <b>TIME_SYNC0</b> / ISH_GP7	I	<b>Time Synchronization:</b> Used for synchronization both input (latch time when pin asserted) and output (toggle pin when programmed time is hit).
GPP_B14/ <b>TIME_SYNC1</b> / SPKR / ISH_GP6	I	<b>Time Synchronization:</b> Used for synchronization both input (latch time when pin asserted) and output (toggle pin when programmed time is hit).
GPP_B2 / <b>VRALERT#</b>	I	<b>VR Alert:</b> ICC Max. throttling indicator from the PCH voltage regulators. VRALERT# pin allows the VR to force PCH throttling to prevent an over current shutdown. PMC based on the VRALERT# and messages from the processor. The messages from the processor allows the processor to constrain the PCH to a particular power budget.
<b>WAKE#</b>	I/OD	<b>PCI Express* Wake Event in Sx:</b> Input Pin in Sx. Sideband wake signal on PCI Express* asserted by components requesting wake up. <i>Notes:</i> <ul style="list-style-type: none"> <li>This is an output pin during S0ix states hence this pin can not be used to wake up the system during S0ix states.</li> <li>An external pull-up resistor is required.</li> </ul>
<b>VCCST_OVERRIDE</b>	O	<b>VccST Override:</b> Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWGOOD_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.
GPP_F22 / <b>VNN_CTRL</b>		<b>VNN_Control:</b> External bypass rail control pin. Without requiring BIOS to be involved during the S0ix states. This pin use to control of the VCC_VNNEXT_1P05 voltage.
GPP_F23 / <b>V1p05_CTRL</b>		<b>V1p05_Control:</b> External bypass rail control pin. Without requiring BIOS to be involved during the S0ix states. This pin use to control of the VCC_V1P05EXT_1P05 voltage.

## 22.3 Integrated Pull-Ups and Pull-Downs

Signal	Resistor Type	Value	Notes
<b>ACPRESENT</b>	Pull-down	15 kohm - 40 kohm	1
<b>LAN_WAKE#</b>	Pull-down	15 kohm - 40 kohm	1
<b>PWRBTN#</b>	Pull-up	20 kohm +/- 30%	
<b>SUSACK#</b>	Pull-up	20 kohm +/- 30%	
<b>WAKE#</b>	Pull-down	15 kohm - 40 kohm	1

*Note:* 1. Pull-down is configurable and can be enabled in Deep Sx state; refer to DSX\_CFG register for more details.

## 22.4 I/O Signal Planes and States

Signal Name	Power Plane	During Reset <sup>18</sup>	Immediately after Reset <sup>18</sup>	S4/S5	Deep Sx
<b>ACPRESENT</b> <sup>6,10,15</sup>	DSW	Undriven /Driven Low <sup>4</sup>	Undriven	Undriven	Undriven/Internal Pull-down <sup>8</sup>
<b>BATLOW#</b>	DSW	Undriven	Undriven	Undriven	OFF
<b>CORE_VID0</b> <sup>11,17</sup>	Primary	Driven High	Driven High	Driven High	OFF
<b>CORE_VID1</b> <sup>11,17</sup>	Primary	Driven High	Driven High	Driven High	OFF
<b>PROC_C10_GATE#</b> <sup>1,17</sup>	Primary	Undriven <sup>19</sup>	Undriven <sup>19</sup>	Driven Low	OFF
<b>DRAM_RESET#</b> <sup>14</sup>	DSW	Undriven	Undriven	Undriven	Undriven
<b>DSW_PWROK</b>	RTC	Undriven	Undriven	Undriven	Undriven

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Signal Name	Power Plane	During Reset <sup>18</sup>	Immediately after Reset <sup>18</sup>	S4/S5	Deep Sx
<b>SPIVCCIOSEL</b>	DSW	Undriven	Undriven	Undriven	Undriven
<b>LAN_WAKE#</b> <sup>15</sup>	DSW	Undriven	Undriven	Undriven	Undriven/Internal Pull-down <sup>8</sup>
<b>LANPHYPC</b> <sup>10,16</sup>	DSW	Undriven	Undriven	Undriven <sub>7</sub>	Undriven <sub>7</sub>
<b>PCH_PWROK</b>	RTC	Undriven	Undriven	Undriven	Undriven
<b>PLTRST#</b> <sup>16</sup>	Primary	Driven Low	Driven High	Driven Low	OFF
<b>PWRBTN#</b> <sup>15</sup>	DSW	Internal Pull-up	Internal Pull-up	Internal Pull-up	Internal Pull-up
<b>RSMRST#</b>	RTC	Undriven	Undriven	Undriven	Undriven
<b>SLP_A#</b> <sup>6,16</sup>	DSW	Driven Low	Driven High	Driven High/ Driven Low <sup>12</sup>	Driven High/ Driven Low <sup>12</sup>
<b>SLP_LAN#</b> <sup>6,14</sup>	DSW	Driven Low	Driven Low	Driven High/ Driven Low <sup>7</sup>	Driven High/ Driven Low <sup>7</sup>
<b>SLP_S0#</b> <sup>1</sup>	Primary	Driven High	Driven High	Driven High	OFF
<b>SLP_S3#</b> <sup>6,16</sup>	DSW	Driven Low	Driven High	Driven Low	Driven Low
<b>SLP_S4#</b> <sup>6,16</sup>	DSW	Driven Low	Driven High	Driven Low	Driven Low <sup>9</sup>
<b>SLP_S5#</b> <sup>6,16</sup>	DSW	Driven Low	Driven High	Driven High/ Driven Low <sup>3</sup>	Driven High/ Driven Low <sup>9</sup>
<b>SLP_SUS#</b> <sup>6,14</sup>	DSW	Driven Low	Driven High	Driven High	Driven Low
<b>SLP_WLAN#</b> <sup>6,16</sup>	DSW	Driven Low	Driven Low	Driven High/ Driven Low <sup>7</sup>	Driven High/ Driven Low <sup>7</sup>
<b>SUSACK#</b> <sup>15</sup>	Primary	Internal Pull-up	Internal Pull-up	Internal Pull-up	OFF
<b>SUSCLK</b> <sup>10,16</sup>	DSW	Driven Low	Toggling	Toggling	Toggling <sup>10</sup>
<b>SUSWARN# / SUSPWRDNACK</b> <sup>10,16</sup>	Primary	Driven Low	Driven Low	Driven Low <sup>5</sup>	OFF
<b>SX_EXIT_HOLDOFF#</b> <sup>15</sup>	Primary	Undriven	Undriven	Undriven	OFF
<b>SYS_PWROK</b>	Primary	Undriven	Undriven	Undriven	OFF
<b>SYS_RESET#</b>	Primary	Undriven	Undriven	Undriven	OFF
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