Name	Type	Description
GPP_H18 / **PROC_C10_GATE#**	O	**External Power Gate**: Control for VCCIO, VCCSTG and VCCPLL_OC during C10. When asserted, VCCIO, VCCSTG and VCCPLL_OC can be 0 V, however the power good indicators for these rails must remain asserted. *Note:* An external pull-up resistor to the DRAM power plane is required.
DSW_PWROK	I	**DeepSx Well PWROK**: Power OK Indication for the VCCDSW_3p3 voltage rail. *Note:* This signal is in the RTC well. This signal cannot tie with RSMRST#.
GPD2 / **LAN_WAKE#**	I	**LAN WAKE**: An active low wake indicator from the Platform LAN Connect Device. *Note:* An external pull-up resistor is required.
GPD11 / **LANPHYPC**	O	**LAN PHY Power Control**: LANPHYPC is used to indicate that power needs to be restored to the Platform LAN Connect Device.
PCH_PWROK	I	**PCH Power OK**: When asserted, PCH_PWROK is an indication to the PCH that all of its core power rails have been stable. The platform may drive asynchronously. When PCH_PWROK is de-asserted, the PCH asserts PLTRST#. *Notes:* • PCH_PWROK must not glitch, even if RSMRST# is low • An external pull-down resistor is required.
GPP_B13 / **PLTRST#**	I	**Platform Reset**: The PCH asserts PLTRST# to reset devices on the platform. The PCH asserts PLTRST# low in Sx states and when a cold, warm, or global reset occurs. The PCH de-asserts PLTRST# upon exit from Sx states and the aforementioned resets. There is no guaranteed minimum assertion time for PLTRST#.
GPP_B11 / **PMCALERT#**	I/OD	**PMC Alert Pin**: Supports USB-C* PD controller architecture.
GPD3 / **PWRBTN#**	I	**Power Button**: The Power Button may cause an SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds (default; timing is configurable), this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S4 states. This signal has an internal Pull-up resistor and has an internal 16 ms de-bounce on the input. *Note:* Upon entry to S5 due to a power button override, if Deep Sx is enabled and conditions are met, the system will transition to Deep S5.
RSMRST#	I	**Primary Well Reset**: This signal is used for resetting the primary power plane logic. This signal must be asserted for at least 10 ms after the primary power wells are valid. When de-asserted, this signal is an indication that the primary power wells are stable. *Note:* An external pull down resistor is required
GPD6 **/ SLP_A#**	O	**SLP_A#**: Signal asserted when the Intel® CSME platform goes to M-Off or M3-PG. Depending on the platform, this pin may be used to control power to various devices that are part of the Intel® CSME sub-system in the platform. If you are not using SLP_A# for any functional purposes on your platform, or can tolerate lack of minimum assertion time, program the "SLP_A# minimum assertion width" value to the minimum. SLP_A# functionality can be utilized on the platform via either the physical pin or via the SLP_A# virtual wire over eSPI. *Note:* An external pull down resistor is required
SLP_LAN#	O	**LAN Sub-System Sleep Control**: When SLP_LAN# is de-asserted it indicates that the Platform LAN Connect Device must be powered. When SLP_LAN# is asserted, power can be shut off to the Platform LAN Connect Device. SLP_LAN# will always be de-asserted in S0 and anytime SLP_A# is de-asserted. *Note:* An external pull-down resistor is required.
GPD9 / **SLP_WLAN#**	O	**WLAN Sub-System Sleep Control**: When SLP_WLAN# is asserted, power can be shut off to the external wireless LAN device. SLP_WLAN# will always will be de-asserted in S0. If you are not using SLP_WLAN# for any functional purposes on your platform, or can tolerate lack of minimum assertion time, program the "SLP_A# minimum assertion width" value to the minimum.
GPP_B12 / **SLP_S0#**	O	**S0 Sleep Control**: When PCH is idle and processor is in C10 state, this pin will assert to indicate VR controller can go into a light load mode. This signal can also be connected to EC for other power management related optimizations.

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Name	Type	Description
		Note: An external pull-up resistor is required.
GPD4 / **SLP_S3#**	O	**S3 Sleep Control:**:SLP_S3# is for power plane control. This signal shuts off power to all non-critical systems when in the S4, or S5 state. *Note:* An external pull-down resistor is required.
GPD5 / **SLP_S4#**	O	**S4 Sleep Control**: SLP_S4# is for power plane control. This signal shuts power to all non-critical systems when in the S4 or S5 state. *Notes:* • This pin must be used to control the DRAM power in order to use the PCH DRAM power-cycling feature. • An external pull-down resistor is required.
GPD10 / **SLP_S5#**	O	**S5 Sleep Control**: SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 state. *Note:* An external pull-down resistor is required.
SLP_SUS#	O	**Deep Sx Indication**: When asserted (driven low), this signal indicates PCH is in Deep Sx state where internal primary power is shut off for enhanced power saving. When de-asserted (driven high), this signal indicates exit from Deep Sx state and primary power can be applied to PCH. For non- Deep Sx, this pin also needs to use to turn on VCCPRIM_1P8 VR. This pin cannot left unconnected. *Notes:* • This is in the DSW power well • An external pull-down resistor is required.
SPIVCCIOSEL	I	**SPI Operation Voltage Select** There is no internal pull-up or pull-down on the strap. An external resistor is required. 0 = SPI voltage is 3.3 V (4.7 kohm pull-down to GND), 1 = SPI voltage is 1.8V (4.7 kohm pull-up to VCCDSW_3p3).
GPP_A3 / ESPI_IO3 / **SUSACK#**	I	**SUSACK#**: If Deep Sx is supported, the EC/motherboard controlling logic must change SUSACK# to match SUSWARN# once the EC/motherboard controlling logic has completed the preparations discussed in the description for the SUSWARN# pin. *Note:* SUSACK# is only required to change in response to SUSWARN# if Deep Sx is supported by the platform.
GPD8 / **SUSCLK**	O	**Suspend Clock**: This clock is a digitally buffered version of the RTC clock.
GPP_A2 / ESPI_IO2 / **SUSWARN#** / SUSPWRDNACK	O	**SUSWARN#**: This pin asserts low when the PCH is planning to enter the Deep Sx power state and remove Primary power (using SLP_SUS#). The EC/motherboard controlling logic must observe edges on this pin, preparing for primary well power loss on a falling edge and preparing for Primary well related activity (host/Intel CSME wakes and runtime events) on a rising edge. SUSACK# must be driven to match SUSWARN# once the above preparation is complete. SUSACK# should be asserted within a minimal amount of time from SUSWARN# assertion as no wake events are supported if SUSWARN# is asserted but SUSACK# is not asserted. Platforms supporting Deep Sx, but not wishing to participate in the handshake during wake and Deep Sx entry may tie SUSACK# to SUSWARN#. This pin is multiplexed with SUSPWRDNACK since it is not needed in Deep Sx supported platforms.
GPP_A2 / ESPI_IO2 / SUSWARN# / **SUSPWRDNACK**	O	**SUSPWRDNACK**: Active high. Asserted by the PCH on behalf of the Intel CSME when it does not require the PCH Primary well to be powered. Platforms are not expected to use this signal when the PCH Deep Sx feature is used.
GPP_H3 / **SX_EXIT_HOLDOFF#**	I	**Sx Exit Holdoff Delay**: Delay exit from Sx state after SLP_A# is de-asserted. *Note:* When eSPI is enabled, SX_EXIT_HOLDOFF# functionality is not available, and assertion of the signal will not impact Sx exit flows.
SYS_PWROK	I	**System Power OK**: This generic power good input to the PCH is driven and utilized in a platform-specific manner. While PCH_PWROK always indicates that the core wells of the PCH are stable, SYS_PWROK is used to inform the PCH that power is stable to some other system component(s) and the system is ready to start the exit from reset. *Note:* An external pull-down resistor is required
SYS_RESET#	I	**System Reset**: This pin forces an internal reset after being de-bounced. *Note:* An external pull-up resistor is required.

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