

word f_pc = I
 M_icode == JXX && M_Cnd : M_valA ;
 W_icode == JRET : W_valM ;
 I: F_predPC ;
 J:
 word f_predPC = I
 f.icode in {IJXX, ICALL} : f_valC ;
 I: f_valP ;
 J:
 word f_start = I
 dmem_error: SADR ;
 !instr_valid: SINS ;
 f.icode == JHALT: SHLT ;
 I: SAOK ;
 J:

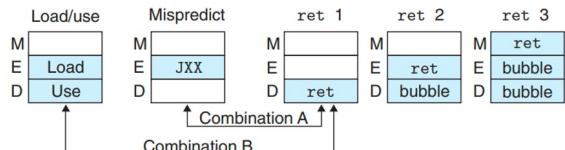
 word d_dstE = I
 D_icode in {IRMMOVW, IRMMOVW, IPOP} : D_valB ;
 D_icode in {ICALL, JRET, IPUSHQ, JPOPQ} : RRSP ;
 I: RNONE ;
 J:
 word d_valA = I
 D_icode in {ICALL, IJXX} : D_valP ;
 D_srcA == e_dstE : e_valE ;
 D_srcA == M_dstM : m_valM ;
 D_srcA == M_dstE : M_valE ;
 D_srcA == W_dstM : W_valM ;
 D_srcA == W_dstE : W_valE ;
 I: d_rvalA ;
 J:
 word d_valB = I
 d_srcB == e_dstE : e_valE ;
 d_srcB == M_dstM : m_valM ;
 d_srcB == M_dstE : M_valE ;
 d_srcB == W_dstM : W_valM ;
 d_srcB == W_dstE : W_valE ;
 I: d_rvalB ;
 J:
 word e_dstE = I
 E_icode == IRMMOVW && !E_Cnd : RNONE ;
 I: E_dstE ;
 J:

 bool F_stall =
 JRET in {D_icode, E_icode, M_icode} || ret
 (E_icode in {JMRMOVW, JPOPQ} &&
 E_dstM in {d_srcA, d_srcB}) ; load-use
 bool D_stall = E_icode in {JMRMOVW, JPOPQ} &&
 E_dstM in {d_srcA, d_srcB} ;
 bool D_bubble = (JRET in {D_icode, E_icode, M_icode}
 && !(E_icode in {JMRMOVW, JPOPQ}) &&
 wrong pred E_dstM in {d_srcA, d_srcB}) ||
 (E_icode == IJXX && !E_Cnd) ; not-use
 bool E_bubble = (E_icode in {JMRMOVW, JPOPQ} &&
 E_dstM in {d_srcA, d_srcB}) || ret
 wrong pred (E_icode == IJXX && E_Cnd)
 bool set_cc = M_stall == SAOK && W_stall == SAOK &&
 E_icode == IOPA ; exception not occurred
 word m_stat = I
 dmém_error: SADR ;
 I: M_stat ;
 J:
 word M_bubble = W_stall in {SADR, SINS, SHLT} || except.
 m_stat in {SADR, SINS, SHLT} ; occurred
 word W_stall = W_stall in {SADR, SINS, SHLT} ; occurred

也可以是normal，但是stall更好

		Pipeline register				
Condition		F	D	E	M	W
ret在Decode发现use指令在Decode时发现jXX在Execute时发现	Processing ret	stall	bubble	normal	normal	normal
	Load/use hazard	stall	stall	bubble	normal	normal
	Mispredicted branch	normal	bubble	bubble	normal	normal

也可以是stall



Pipeline register

Condition	F	D	E	M	W
Processing ret	stall	bubble	normal	normal	normal
Mispredicted branch	normal	bubble	bubble	normal	normal
Combination	stall	bubble	bubble	normal	normal
Condition	F	D	Pipeline register		
Processing ret	stall	bubble	normal	normal	normal
Load/use hazard	stall	stall	bubble	normal	normal
Combination	stall	bubble+stall	bubble	normal	normal
Desired	stall	stall	bubble	normal	normal