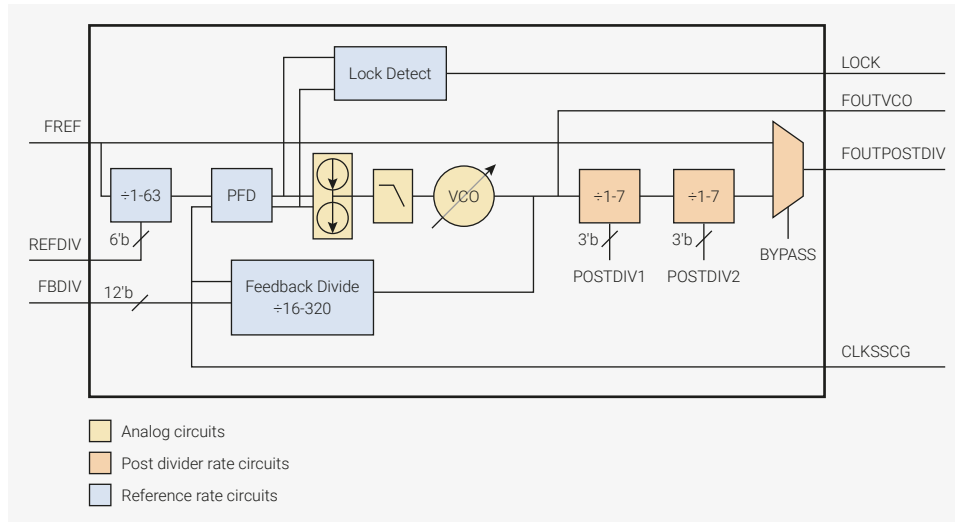


Figure 33. On both PLLs, the *FREF* (reference) input is connected to the crystal oscillator's XI input. The PLL contains a VCO, which is locked to a constant ratio of the reference clock via the feedback loop (phase-frequency detector and loop filter). This can synthesise very high frequencies, which may be divided down by the post-dividers.



2.17.2. Calculating PLL parameters

To configure the PLL, you must know the frequency of the reference clock, which on RP2040 is routed directly from the crystal oscillator. This will often be a 12 MHz crystal, for compatibility with RP2040's USB bootrom. The PLL's final output frequency *FOUTPOSTDIV* can then be calculated as $(FREF / REF DIV) * FBDIV / (POSTDIV1 * POSTDIV2)$. With a desired output frequency in mind, you must select PLL parameters according to the following constraints of the PLL design:

- Minimum reference frequency (*FREF* / *REF DIV*) is 5 MHz
- Oscillator frequency (*FOUTVCO*) must be in the range 400 MHz -> 1600 MHz
- Feedback divider (*FBDIV*) must be in the range 16 -> 320
- The post dividers *POSTDIV1* and *POSTDIV2* must be in the range 1 -> 7
- Maximum input frequency (*FREF* / *REF DIV*) is VCO frequency divided by 16, due to minimum feedback divisor

Additionally, the maximum frequencies of the chip's clock generators (attached to *FOUTPOSTDIV*) must be respected. For the system PLL this is 133 MHz, and for the USB PLL, 48 MHz.

NOTE

The crystal oscillator on RP2040 is designed for crystals between 5 and 15 MHz, so typically *REF DIV* should be 1. If the application circuit drives a faster reference directly into the XI input, and a low VCO frequency is desired, the reference divisor can be increased to keep the PLL input within a suitable range.

TIP

When two different values are required for *POSTDIV1* and *POSTDIV2*, it's preferable to assign the higher value to *POSTDIV1*, for lower power consumption.

In the RP2040 reference design, which attaches a 12 MHz crystal to the crystal oscillator, this implies that the minimum achievable and legal VCO frequency is $12 \text{ MHz} \times 34 = 408 \text{ MHz}$, and the maximum VCO is $12 \text{ MHz} \times 133 = 1596 \text{ MHz}$, so *FBDIV* must remain in the range 34 -> 133. For example, setting *FBDIV* to 100 would synthesise a 1200 MHz VCO frequency. A *POSTDIV1* value of 6 and a *POSTDIV2* value of 2 would divide this by 12 in total, producing a clean 100 MHz at the PLL's final output.