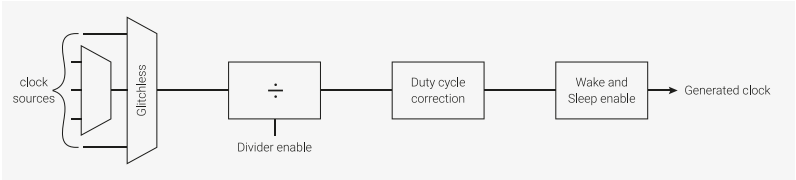
Figure 28. A generic clock generator



2.14.3.1. Multiplexers

The first multiplexer is referred to as the auxiliary mux and is a conventional design whose output will glitch when changing the select control. Clock glitches are to be avoided at all costs because they may corrupt the logic running on that clock. The clock generator output therefore cannot be used during such changes. If the clock generator has a glitchless mux, then that mux can be switched to an alternate source during the transition. If it does not have a glitchless mux then the divider must be disabled during the transition. The divider requires 2 cycles of the source clock to stop the output and 2 cycles of the new source to restart the output. The user must wait for the generator to stop before changing the auxiliary mux, therefore must be aware of the source clock frequency.

The second muliplexer switches glitchlessly, therefore the clock generator can continue running during changes of source clock. The glitchless mux is only implemented for always-on clocks. On RP2040 the always-on clocks are the reference clock (clk_ref) and the system clock (clk_sys). Such clocks must run continuously unless the chip is in DORMANT mode. The glitchless mux has a status output (SELECTED) which indicates which source is selected and can be read from software to confirm that a change of clock source has been completed.

The recommended control sequences are as follows.

To switch the glitchless mux:

- switch the glitchless mux to an alternate source
- poll the SELECTED register until the switch is completed

To switch the auxiliary mux when the generator has a glitchless mux:

- switch the glitchless mux to an alternate source
- poll the SELECTED register until the switch is completed
- change the auxiliary mux select control
- switch the glitchless mux back to the auxiliary mux output
- if required, poll the SELECTED register until the switch is completed

To switch the auxiliary mux when the generator does not have a glitchless mux:

- disable the clock divider
- wait for the generated clock to stop (2 cycles of the clock source)
- change the auxiliary mux select control
- enable the clock divider
- if required, wait for the clock generator to restart (2 cycles of the clock source)

2.14.3.2. Divider

A fully featured divider divides by 1 or a fractional number in the range 2.0 to 2^24-0.01. Fractional division is achieved by toggling between 2 integer divisors therefore it yields a jittery clock which may not be suitable for some applications. For example, when dividing by 2.4 the divider will divide by 2 for 3 cycles and by 3 for 2 cycles. For divisors with large integer components the jitter will be much smaller and less critical.