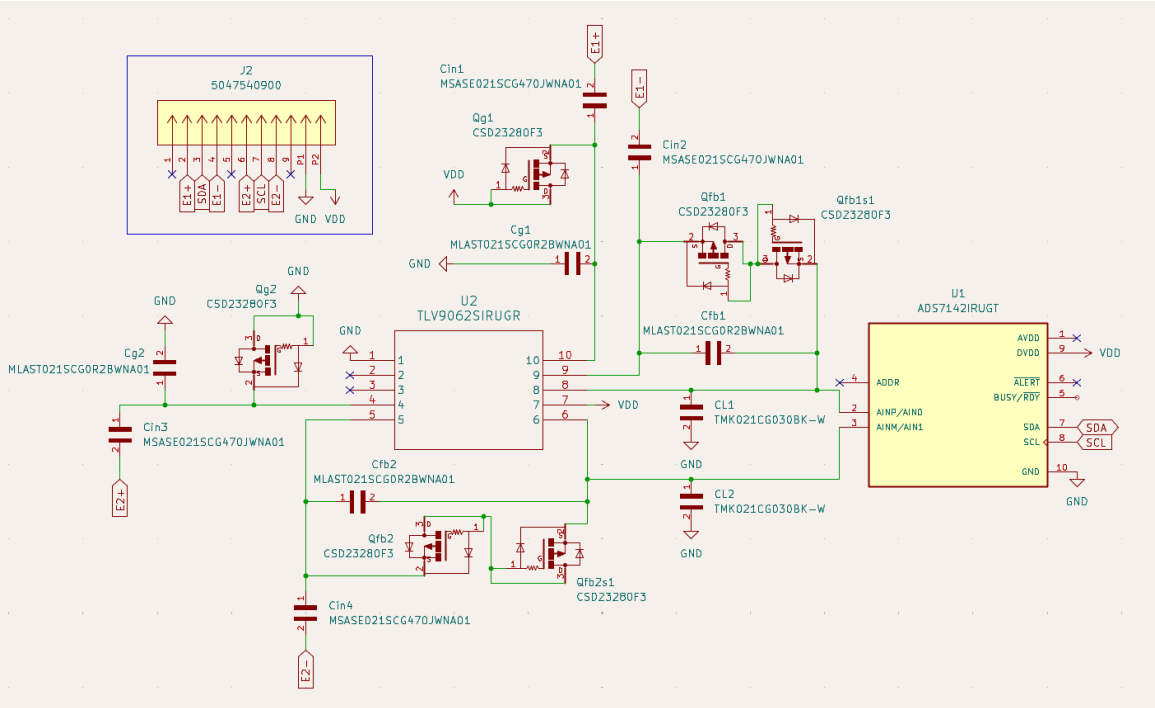
A Dual-Channel ADC Module Design for Neural Recording

1. Circuit Design:



In response to this challenge's design specifications — namely, the acquisition of ~20 µV extracellular action potentials across 100 channels, within a stringent power budget (<10 mW) and extremely compact module dimensions (<3 mm × 3 mm × 2 mm) — careful consideration was required in selecting the amplifier front-end topology. The amplifier needed to provide approximately 60 dB of gain, high input impedance suitable for a ~200 kΩ probe, low noise, and precise bandpass filtering to isolate the ~10 kHz neural signal bandwidth.

Extracellular neural recordings are particularly sensitive to environmental noise due to the extremely small signal amplitudes involved. Moreover, because the electrodes are placed in the extracellular fluid and not inside the neuron, there is no true, low-impedance "reference ground" available in the tissue. Therefore, this design makes use of a differential amplifier configuration with a single-ended op amp, effectively rejecting common-mode noise shared between the two input probes.

Initially, a closed-loop operational amplifier design was pursued, following conventional practices for high-fidelity low-noise amplification of neural signals. Closed-loop topologies offer well-defined and stable gain settings, superior linearity, and excellent suppression of external disturbances, which seemed highly desirable given the low signal amplitudes inherent in extracellular neural recording. However, during design development, substantial practical challenges emerged. Achieving a suitable low-frequency cutoff near 1 Hz to block electrode offset voltages, while simultaneously maintaining a large closed-loop gain, imposed a severe tradeoff between the coupling capacitor size (Cin) and the feedback impedance. Larger Cin values would relax feedback resistor requirements, but would simultaneously lower the input impedance, increase parasitic loading, and occupy prohibitive board area — a critical constraint in a 3×3 mm² footprint. Conversely, maintaining high input impedance with modest capacitor sizes would necessitate feedback resistances in the tens to hundreds of megaohms, introducing excessive thermal noise, leakage currents, and instability concerns.

Recognizing these constraints, and informed by modern advances in neural amplifier architectures - particularly the work done by Chaturvedi & Amrutur (2011) "An Area-Efficient Noise-Adaptive Neural Amplifier in 130 nm CMOS Technology" - the design pivoted toward an open-loop architecture using a standard operational amplifier (op-amp) in a single-ended, high-impedance, AC-coupled configuration. The open-loop architecture fundamentally relaxes the tradeoff between coupling capacitor size and low-frequency cutoff by providing an overall higher gain. This simultaneously maximizes ADC dynamic range utilization while minimizing component area and static power consumption — key advantages for high-channel-count implants. Furthermore, Chaturvedi & Amrutur make use of a "pseudoresistor" - a transistor device operating in deep subthreshold, at which point the drain-source resistance becomes extremely large. Properly biased, the pseudoresistor can achieve effective resistance values exceeding 10^9 Ω (gigaohms) and even into the teraohm range, allowing preservative low-frequency cutoffs <1 Hz. Together, the input capacitor and pseudoresistor creates a high-pass RC pole that effectively blocks low-frequency noise and electrode offsets without requiring large capacitors or bulky feedback resistors.

However, during detailed simulation, the open-loop configuration revealed stability challenges at high gain settings. Without a stabilizing feedback network, small mismatches and input disturbances caused output saturation and oscillations, particularly given the high open-loop gain of the amplifier and the absence of dominant-pole compensation in the standalone op-amp design. While theoretical stabilization strategies exist (e.g., downstream low-pass filtering or local feedback compensation), implementing these within the strict size and power constraints was not practical in this prototype. As a result, the final design reverted to a closed-loop configuration, but retained the use of pseudoresistor feedback to achieve extremely high effective resistance and maintain a low-frequency cutoff near 1 Hz without requiring large discrete resistors. The closed-loop amplifier thus combines the advantages of well-controlled gain and enhanced stability, while preserving the area-saving and low-noise benefits of pseudoresistor-based AC coupling. LTSpice simulations verified that the closed-loop architecture with deep-subthreshold PMOS pseudoresistors achieves ~54 dB of gain, appropriate bandwidth (1.7Hz–9.9kHz), high input impedance (>1GΩ), and power consumption compatible with the challenge's specifications. Note the pseudoresistors were modeled as 1 TΩ resistors, achievable based on the work by Sharma & Goyal in "Implementation of Tunable and Non-Tunable Pseudo- Resistors using 0.18µm Technology".

Overall, while open-loop architectures remain highly attractive for future designs with more advanced stabilization or downstream signal conditioning, the final implementation of a closed-loop, AC-coupled amplifier with pseudoresistor feedback represents the best practical solution for satisfying the system's strict space, power, stability, and performance requirements.

1.1. System Overview:

The architecture includes AC coupling at the input, a feedback network to define gain and bandwidth precisely, and a carefully selected low-noise operational amplifier (TLV9062) operating from a 1.8 V single supply. The input stage utilizes 47 pF ceramic capacitors (0201 package) for high-pass filtering, together with pseudoresistor elements implemented using ultra-low leakage PMOS devices. A 3 pF capacitor (0201), together with the system's equivalent output resistance, provide low-pass functionality. Overall, the system forms a second-order bandpass filter, shaping the overall response to cover the 1 Hz to ~10 kHz frequency range critical for extracellular spike acquisition.

The design was tailored to match the input range and resolution of the selected ADS7142 ADC, with an amplifier gain of approximately 54dB based on LTSpice simulations with pseudoresistors modelled as 1TΩ resistances. This scaling ensures that typical neural spike amplitudes (~20 µV) are mapped into ~10 mV swings at the ADC input, yielding sufficient resolution (~23 LSBs per spike, given the 12-bit ADC has a resolution of 0.44mV/LSB). The ADC's 70 kSps sampling rate per channel provides oversampling relative to the 10 kHz bandwidth, enabling accurate spike waveform reconstruction.

All passive components were selected to balance size, thermal stability, and electrical performance within the tight physical constraints, and a 2-layer PCB stackup was planned to enable integration of signal and ground planes within the 2 mm maximum height.

1.2. Design Specs:

Input Signal	The module shall accept voltage inputs coming from extracellular neuronal signals, with amplitude ~20μV and bandwidth ~10kHz.
Number of Input Channels	The prototype shall support 2 input channels using 2 single-channel or 1 dual-channel placeholder COTS amplifier(s). The final design shall support 100 input channels.
Power Dissipation	The board shall dissipate less than 10 mW of power (for 100 channels, ideally). <200μW for 2 channels, <100μW/channel ideal.
Board Size	The board volume shall be less than 3mm x 3mm x 2mm.
Probe Impedance	Signals shall be measured with a probe impedance of approximately 200kΩ.
Thermal Constraints	The implant must limit the surface heat flux to <40 mW/cm² and temperature rise to <2°C above normal body temperature to avoid adverse tissue responses, particularly in sensitive brain tissue (Thermal Considerations for the Design of an Implanted Cortical Brain–Machine Interface (BMI) - Indwelling Neural Implants - NCBI Bookshelf).
Signal to Noise Ratio	The signal to noise ratio shall be > 5 (doi.org/10.3389/fnins.2017.00665).

2. System Components:

See accompanying Excel table for power, board area, and cost tallies.

2.1. Op Amp:

Part Spec	Impacted Requirement	Relationship to Design Parameter	Design Requirement
Quiescent Current (I_Q)	Power	Assuming a 1.8V power supply, the power consumed by each amplifier channel will be: $P_A = I_Q V_{DD} = 1.8\, I_Q$ However, the design problem assumes this power will be reduced by 90% from the actual power of the amplifier part selected. $P_A = 0.1 \cdot 1.8 \cdot I_Q$ $P_A = 0.18\, I_Q$	$P_{total} < 10mW$ The board will have 100 amplifiers (or 50 dual-channel ICs). Therefore, if there were no other components on the board: $P_A < 0.1mW$ $I_Q < 0.555mA$ Allowing for margin from other power dissipation: $I_Q < 0.3mA\ or\ 300\mu A$
Bandwidth (BW)	Signal Accuracy	As per the design prompt, neural signals have 10kHz bandwidth. Thus, the amplifier	For proper margin: $GBW > 100kHz$

	(Frequency response)	BW must be significantly greater than this to prevent distortion and phase lag.	
Input Impedance (Zin)	Signal Integrity (Input loading)	Zin will form a voltage divider with the 200kΩ probe, controlling the "amount" of voltage signal that gets amplified.	The input impedance should be at least 100x the probe resistance, for ~99% retention: $Zin \geq 2M\Omega$
Open-Loop Gain	Precision (ADC Input Range)	Neural signals (~20μV) must be amplified to mV range for digitization by 10-12 bit ADC.	Within reason: $A > 500 \; or \sim 27dB$ Closed-loop gain will be less.
Common Mode Rejection Ratio	Signal Integrity (Noise)	A high CMRR is needed to reject environmental noise common to both amplifier inputs.	Within reason: $CMRR > 70dB$
Package	Board space	Part takes up critical board area.	The amplifying IC shall be a dual channel, single-ended op amp to optimize space. Therefore, only one IC will be needed for both channels. The smallest package size shall be selected.

Part Option	Notes
TLV9062S Dual, 5.5-V, 10-Mhz CMOS operational amplifier	- **Ideal (smallest possible) size** 1mm x 1mm (DSBGA package) - Low broadband noise - Sufficient open-loop gain of >100dB - Sufficient unity-gain bandwidth of 10MHz (specifically 15848) - CMRR of ~50-100dB (within reasonable range) - **Quiescent current is too high (534μA)** - Lowest supported supply voltage is 1.8V. - Typical input resistance of 10^{13} Ω which is very high. - Input capacitance is 4 pF. In series with the probe impedance ~200 kΩ, this creates a low-pass filter with cutoff 1/2πRC ~ 200kHz. Since the neural signal bandwidth is only up to ~10kHz, the cutoff is sufficiently high. - Cost is $0.83 per unit
TLV8542	- Ideal size 1.5mm x 1.5mm (X2QFN package) - Nanopower quiescent current (500nA per channel) - Unity gain bandwidth of 8 kHz is far too low :(
TLV9102	- Available in SOIC, SOT-23, TSSOP, VSSOP, which are all too large

After evaluation of several amplifier options, the TLV9062 operational amplifier was selected. The TLV9062 offers a combination of high open-loop gain, low input noise, excellent input impedance, and small package size, all of which align with the design constraints for power, area, and neural spike fidelity.

Based on the datasheet, the TLV9062 provides an open-loop gain of approximately 104 dB (corresponding to ~15,848 V/V), ensuring sufficient linearity and amplification capability for the very low-amplitude extracellular neural signals (~20 μV). The device exhibits extremely low input bias currents (~0.5 pA), corresponding to an input resistance in the teraohm range, thereby minimizing signal loading effects even when interfacing with 200 kΩ probe

impedances. Input-referred voltage noise is approximately 10 nV/√Hz at 10 kHz, which supports a high signal-to-noise ratio (SNR) after amplification.

$$Pdiss \simeq I_{Quiescent} \cdot V_{supply}$$

While the TLV9062's quiescent current of approximately 538 µA per channel is slightly higher than ideal for the cumulative implant power budget, the device family offers integrated low-power standby functionality. The TLV906xS variants include a shutdown mode that reduces the amplifier's current consumption to less than 1 µA per channel when not active. In the final system design, this shutdown feature can be leveraged to dynamically manage power depending on recording needs, such as disabling idle channels or implementing duty cycling strategies during non-critical periods. This would ensure that the overall module remains within the strict <10 mW power envelope even as channel count scales.

2.2. Capacitors:

Name	Value	Part selection	Specs & Considerations
C_L	3pF	TMK021CG030BK-W	- Cost $0.45 per unit - Smallest 0201 casing (~0.25mm x 0.125mm) - Great tolerance of 0.1pF - Rated voltage of 25V leaves plenty of headroom for system VDD of 1.8V - ESR between 0-100Ω in frequency band of interest: this will compound with op amp's (small) finite output resistance to form an RC pole. However, the corner frequency for the parasitic RC circuit would be *huge* and therefore not degrade circuit behaviour. Assuming an ESR of 100Ω and op amp output of 50Ω, the RC constant would be 450ps, for a corner frequency of ~350MHz (*huge*). - Excellent insulation resistance >10^{10}Ω to prevent leakage currents
2 x C_f	0.1pF	D10NA0R1A5PX	- Unfortunately, not available in 0201. Second smallest possible casing (0.25mm x 0.25mm) - Reasonable tolerance margin of 0.05pF - Rated voltage of 50V is absolutely no concern - Cost per unit is $4.6995 (on the expensive side, but worth it for this piece) - Good insulation resistance >10^6Ω to prevent leakage currents - Reasonable dissipation factor (0.15%) helps meet power management requirement - estimated ESR is DF/2πfc which is approximately 100Ω at 10kHz frequency - Stable temperature coefficient - Medical grade
2 x C_{in}	47pF	MSASE021SCG470JWNA01	- Cost $0.104 per unit (minimum 50,000 order at a time) - Smallest 0201 casing (~0.25mm x 0.125mm) - 5% tolerance reasonable - Rated voltage of 16V leaves plenty of headroom for system VDD of 1.8V - Extremely low temperature drift & excellent frequency stability - Low DF (0.001), high Q factor (since Q=1/DF, Q>1000 at 1MHz) decreases energy loss across signal bandwidth - Estimated ESR is DF/2πfc which is approximately 338Ω at

			10kHz frequency - Again, good insulation resistance >$10^{10}\Omega$ - General-purpose high reliability (industry standard)

2.3. Pseudoresistor:

The pseudoresistor is used in the op amp feedback path to achieve extremely high resistance values to enable AC coupling at low frequencies without impractically large input capacitors, or other area/noise penalties associated with large discrete resistors. In this design, the pseudoresistor will be implemented using a PMOS device operating in the subthreshold region, achieved by tying the gate to the drain, with the bulk tied (intrinsically) to source. In this mode of operation, the gate-source voltage is below the threshold voltage, and a very small drain current flows exponentially with applied voltage. As described by Sharma & Gupta (2016), the drain current of a P-MOSFET in subthreshold is approximately:

$$I_{SD} \simeq I_{D0}\, e^{(VBG-VTH)/nU_T}(e^{-VBS/U_T} - e^{-VBD/U_T})$$

The incremental resistance r_{inc} then governs the small-signal behavior and is given by:

$$r_{inc} = \frac{\partial VDS}{\partial I_D}$$

The CSD23280F3 P-Channel MOSFET was selected for subthreshold pseudo-resistor implementation due to its ultra-compact PicoStar™ package (0.7mm × 0.6mm), low threshold voltage (–0.65V typical), and low leakage characteristics (50nA max at Vgs = 0V, Vds = –9.6V). The low threshold voltage is especially critical in this application, as it enables subthreshold conduction even when the gate and source are nearly equal, allowing the device to operate reliably in the weak inversion region without requiring additional gate biasing. This simplifies the design and helps ensure consistent pseudo-resistor behavior across channels. The component is also cost-effective, priced at approximately $0.035 per unit in 3000-piece quantities, supporting scalability toward a 100-channel architecture.

Spec	Target	Justification
Drain source current (I_{DS})	pA range 1nA maximum for ~1G resistance	To create large effective resistance
Package Size	Very small	To reduce parasitic capacitance and optimize board space
W/L	Minimum possible	Smaller W/L increases R_{DS} and reduces parasitics
Gate leakage current (I_{GS})	≤ 1 pA	To avoid signal injection through the gate during coupling
Number of channels	Dual or quadruple	To save board space, since we need four pseudo resistors total (two per signal channel)

Power Calculations:

To estimate the effective subthreshold current under application conditions, the datasheet leakage current at Vgs = 0V was scaled linearly according to the operating drain-source voltage.

- For the feedback resistor - given the amplifier's simulated midband gain (~450×) and a typical neural input spike of 20μV, the resulting output swing (~9-10mV) defines the effective Vds. Scaling accordingly, the drain current is estimated at ~47pA, yielding an effective pseudo-resistance of approximately 192MΩ.
- For the equivalent (impedance-matching) pseudo-resistor on the non-inverting, the voltage across it would be that of the neural signal, which is approximately 20μV. The corresponding drain current is proportionally reduced to ~104fA. This current yields an effective pseudo-resistance of approximately 192GΩ, calculated by $R_{pseudo} \cong V_{DS} / I_{DS}$ where V_{DS} is the applied differential signal voltage.

Because the pseudo resistor operates in subthreshold and the biasing is for a very low current, the power consumption is also extremely small.

$$P(fb) = I_{DS} \cdot V_{DS} = 9mV \cdot 46.9 \cdot 10^{-12}A = 422\,fW$$

$$P(+) = I_{DS} \cdot V_{DS} = 20 \cdot 10^{-6}V \cdot 104 \cdot 10^{-15}A = 2.08\,aW$$

2.4. ADC:

Based on the selected amplifier type, the ADC must accept single ended inputs. Since there are two channels in this prototype, it will be a dual-channel input ADC. In the final design, the number of channels is expanded to 100, and as such, an analog multiplexer could be used such that 50 amplifiers can share one half of the ADC channels and the other 50 can share the other half.

Part Spec	Impacted Requirement	Relationship to Design Parameter	Design Requirement
Quiescent Current (I_Q)	Power	ADC idle power adds to total system power.	Keep I_Q as low as possible.
Resolution (bits)	Precision	ADC must have sufficient resolution to faithfully digitize amplified neural signals (20μV spikes amplified to ~1mV–100mV based on the selected amplifier topology).	For a mV signal range, the ADC should have a maximum LSB of ~1mV according to this formula: $LSB = VREF/2^n$ where VREF is the full scale voltage and n is the number of bits.
Sampling rate	Signal Integrity	Neural signals have bandwidth up to 10kHz. To properly capture spike shape in the time domain, sampling must be ≥7× the maximum frequency content of 10kHz.	Sampling rate > 70kSps per channel
Package	Board space	Part takes up critical board area.	The ADC shall be dual channel, such that only one IC will be needed for both channels. The smallest package size shall be selected.

Selection: **ADS7142** Nanopower, Dual-Channel, Programmable Sensor Monitor

- Power consumption is extremely low (analog: ~265 μA at 140kSps; can be much lower at slower rates).

- Sampling rate is up to 140kSps (manual mode), which meets 100kSps threshold for signal integrity in time domain.
- In this IC analog supply input is used as the reference (full-scale) voltage for analog-to-digital conversion.
- The supply voltage 1.65-3.6V is compatible with the 1.8V system.
- I2C interface for simple wiring and easy to hook up to MCU.
- The unit cost is $1.19 USD for tape & reel.
- The size is ideal, having an X2QFN package of 1.5mm x 2mm.

The ADS7142 12-bit ADC was selected to digitize the amplified extracellular neural signals in this design. Its input range, spanning 0V to VDD, aligns with the amplifier's output configuration, with VDD set to 1.8V. The amplifier output is centered around a stable voltage (VDD = 1.8V) using pseudoresistor biasing, ensuring that the output swing remains within the ADC's operating range (non-negative).

With a 1.8V full-scale range, the ADS7142 provides an LSB size of approximately 0.44 mV. Following amplification with a gain of approximately 54dB, typical extracellular neural spikes with amplitudes in the 20μV range produce output signals ~10mV. This corresponds to approximately 23 LSBs per spike, which is sufficient to resolve individual spikes, preserve basic waveform structure, and enable reliable spike detection and basic sorting in post-processing. The ADC's sampling rate further supports signal fidelity. In dual-channel mode, the ADS7142 samples each channel at up to 70kSps, which comfortably satisfies the Nyquist criterion for neural signals with maximum bandwidth around 10kHz. Given typical extracellular spike durations of approximately 1 ms, the sampling rate provides roughly 70 samples per spike, allowing for high-fidelity temporal representation of the signal features.

2.5. Connector:

An FPC-to-board connector was selected for the neural signal acquisition module to achieve maximum miniaturization, low mass, and reliable high-density interconnects, making it ideal for compact biomedical systems. FPC connectors allow flexible, thin cabling between the module and external circuits, minimizing mechanical strain and preserving a small module footprint. The Hirose BK13C06-6DP/2-0.35V connector specifically was chosen due to its low-power operating conditions, and extremely compact size—2.35 mm in length, 1.6 mm in width, and 0.475 mm in stacking height—meeting the module's strict 3 mm × 3 mm × 2 mm space constraint.

The connector features 6 signal contacts and 2 power contacts. In this design, 2 signal contacts are used to route the I²C lines (SCL and SDA) for the ADC output to interface with an offboard MCU. I^2C lines operate at low voltages (typically less than 3.3V), and modest speeds (~100kHz to 400kHz standard mode), which are supported by this connector's electrical specifications. The pull-up resistors necessary to hold the I^2C lines high will need to be implemented on the MCU, or elsewhere on the connecting bus. The remaining 4 signal contacts will be used to route the extracellular neural probe signals directly. Each probe carries a a small analog extracellular voltage, ~20μV for this application, well-suited for this low-power connector. Finally, the 2 dedicated power contacts provide reliable GND and VDD supply connections. With a rated voltage of 50 V DC, 0.3 A per signal contact, and 5 A per power contact, the connector offers ample electrical margin for the module's low-voltage, low-current operation.

Power Calculation:

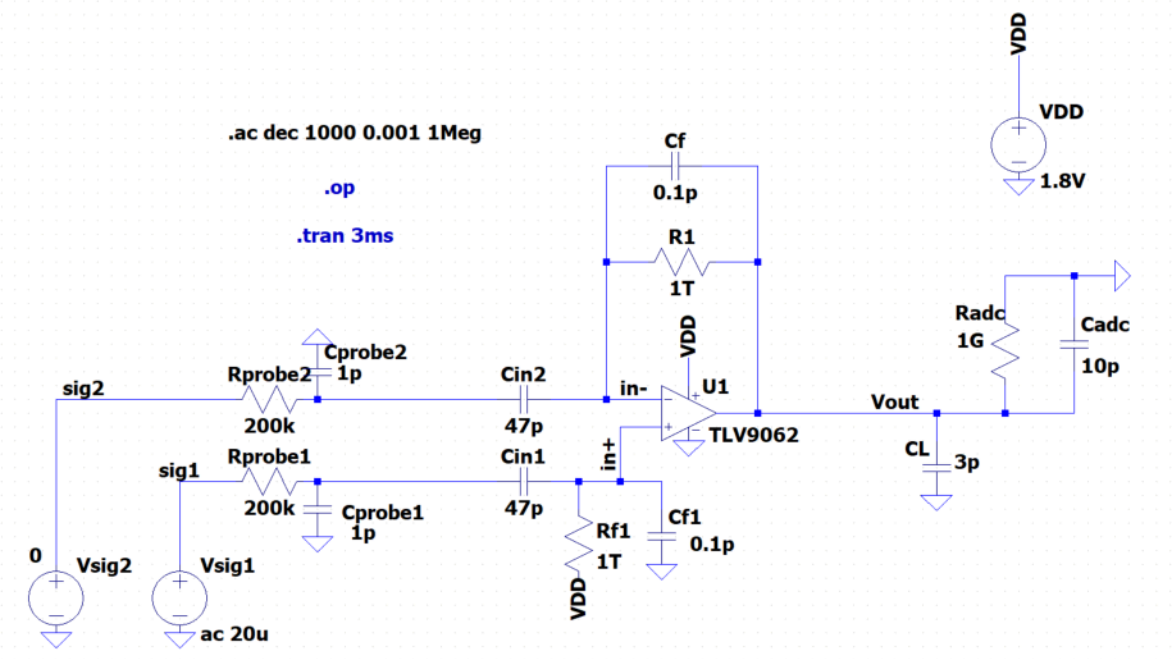
With a 1.8V supply and assuming the maximum module power constraint of 10mW is met, the total supply current is approximately 5.56mA (P/V). Based on the connector's typical power contact resistance of 30mΩ, the estimated I^2R conduction losses across both power contacts can be estimated at 1.86μW. Signal contact losses would be negligible due to the extremely low current draw of the analog inputs and I^2C communication lines.

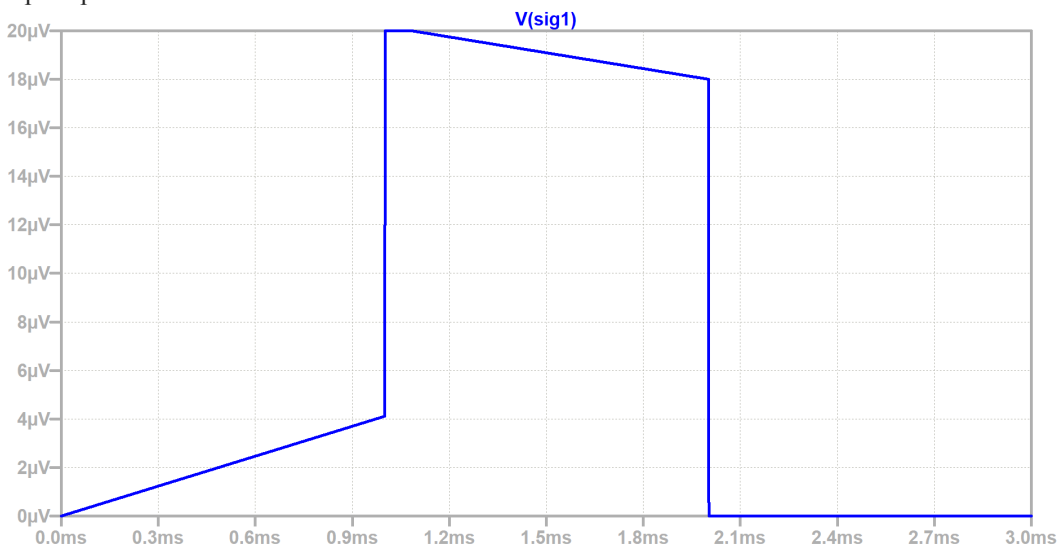
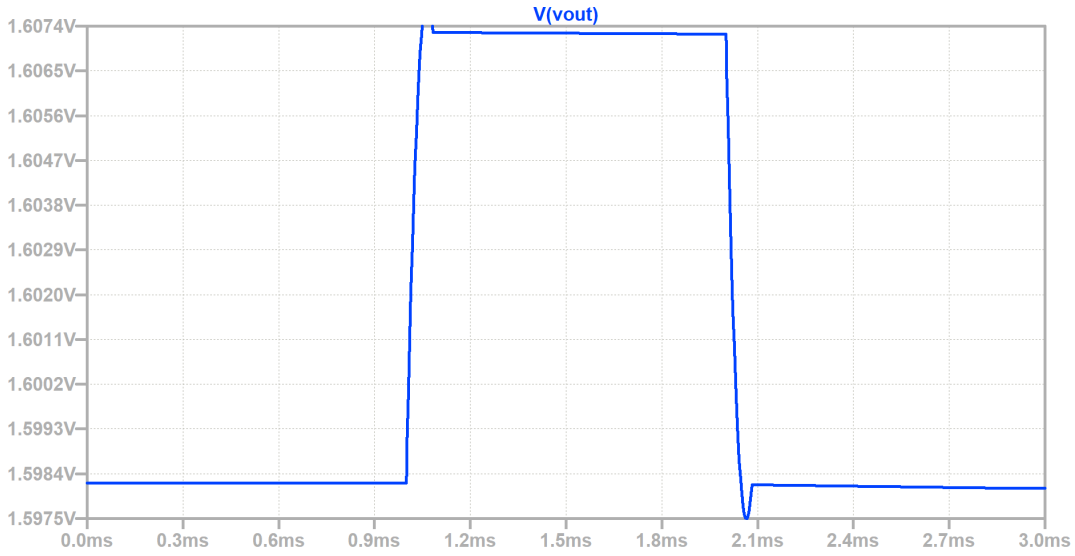
3. Circuit Simulations in LTSpice:

3.1. Equivalent Circuit Model:

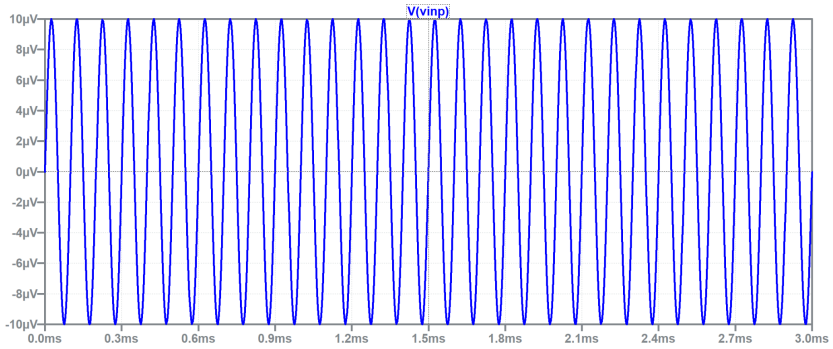
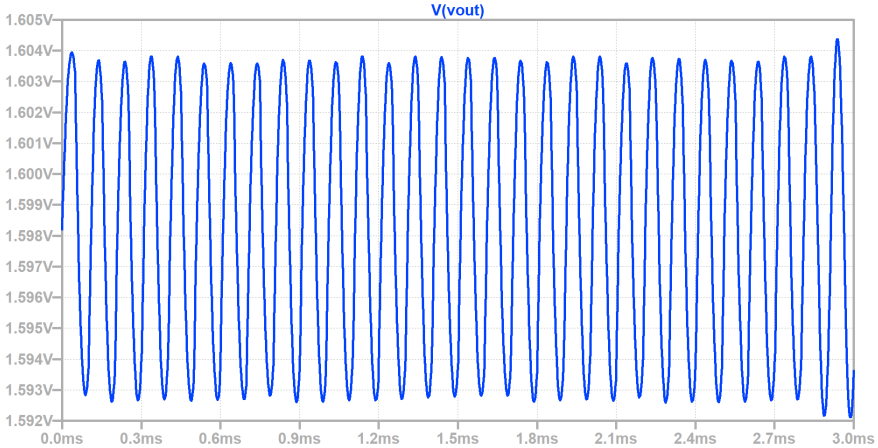
The ADS7142 input was first modeled as a 1 GΩ resistor in parallel with a 10pF capacitance based on datasheet specifications, ensuring minimal loading impact on the amplifier output stage. The pseudo resistors were modelled by their approximate equivalent resistance of a tera-ohm, achievable based on the work by Sharma & Goyal in "Implementation of Tunable and Non-Tunable Pseudo- Resistors using 0.18µm Technology".

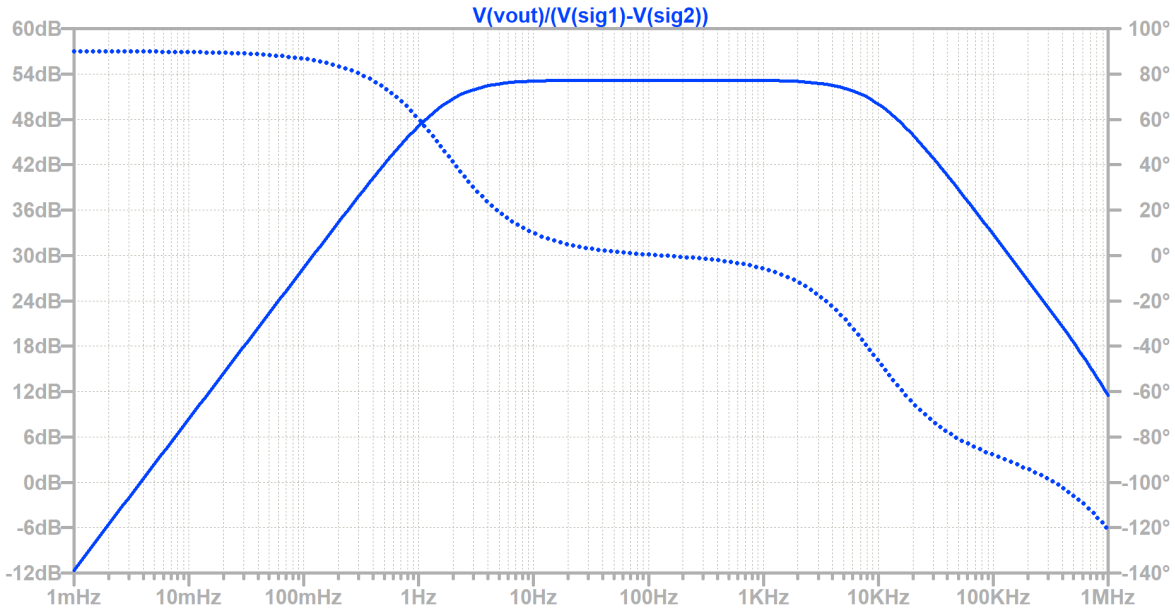
To model the extracellular neural probe in simulation, an equivalent circuit was created consisting of a 200kΩ series resistance and a 1pF shunt capacitance. The resistance represents the probe and tissue interface impedance, as specified in the design problem description. The capacitance models the parasitic effects of the electrode surface area and cabling. This equivalent circuit ensures that the analog front-end response is tested under realistic input loading and high-frequency behavior.

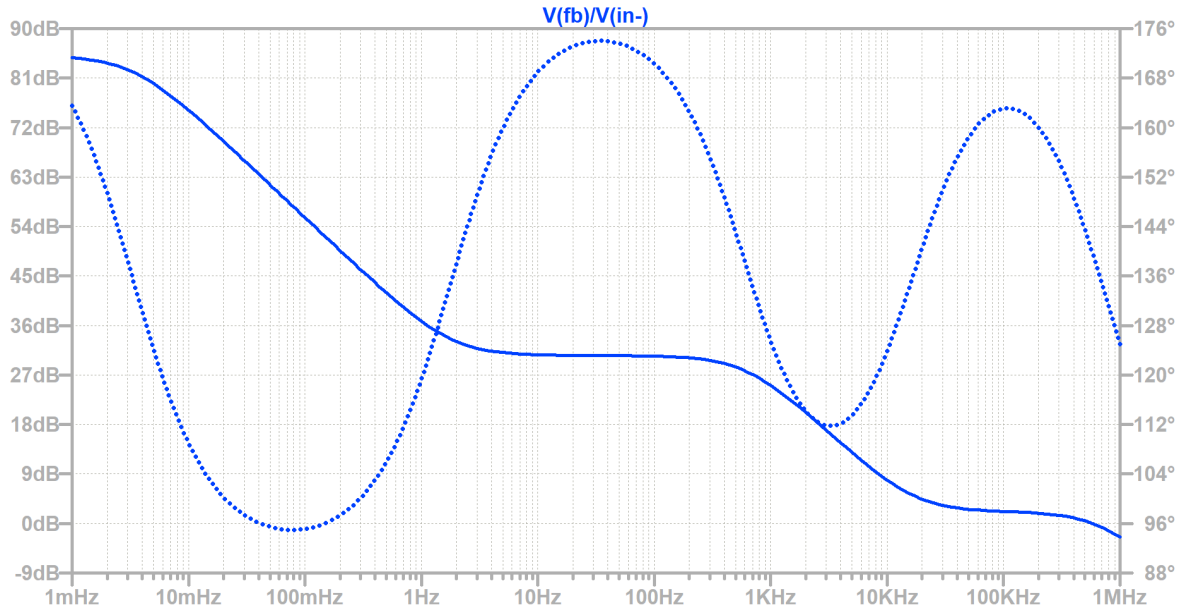


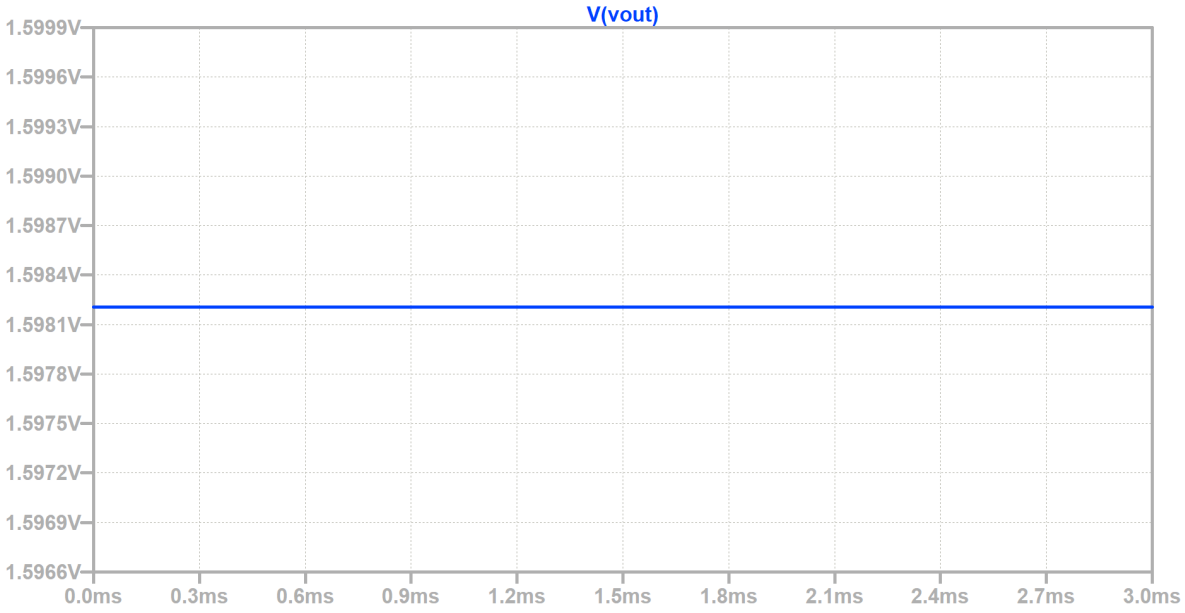
Spike Response	
Test Setup	Inject ~1ms 20µV spike into Vin+ and ground Vin-, then run transient analysis Input: PULSE(0 20u 1m 1u 1u 1m 10m)
Expectation	Output shows a large amplified spike at the right time
Simulation	Input Spike:  Output: Amplitude of ~10mV <u>Logic Levels:</u> • Von (signal) = ~1.6074 V • Center (reference, or “no signal”) voltage = ~1.5982 V 
Additional test: Setting V- to 0.9V and adding the same DC offset to V2 in addition to the 20µV pulse shows the common-mode DC signal is effectively removed.	
Conclusion(s)	• The output shows **clear amplification by the midband gain of ~500 or ~54dB (~20 µV input to ~10mV output), correct timing**, and stable, appropriately level-shifted baseline without drift (when

	pseudoresistor is connected to VDD), indicating the amplifier is working as intended. ● The input pulse generated by the SPICE PULSE source exhibits slight rounding at the rising edge and minor droop during the pulse high state. This behavior arises from the combined effects of source resistance (200kΩ), probe capacitance (1pF), and finite rise/fall times defined in the simulation. These effects are acceptable for the application because extracellular neural spikes are not perfect square waves, and the slight non-idealities occur at frequencies well within the amplifier's intended bandwidth (~10kHz). The observed input behavior remains representative of realistic biological signals and does not impact the system's ability to correctly amplify and sample neural activity. ● The observed overshoot at the rising and falling edges of the output pulse is due to underdamped transient behavior resulting from the interaction between the amplifier output impedance, the equivalent ADC load resistance, and the load capacitance (3pF + 10pF). Sharp input transitions (high dv/dt) excite high-frequency modes, producing small overshoot peaks that are typical in capacitive-loaded amplifier stages. This behavior is acceptable for this application because the overshoot magnitude remains very small relative to the neural signal amplitude (~20μV spikes) and settles quickly (within microseconds), well before the next significant neural event. The amplifier remains within its linear region, and the overshoot does not cause distortion, clipping, or long-term ringing that would corrupt the sampled data. Therefore, the transient peaks do not significantly impact signal fidelity for the intended neural signal bandwidth (~10kHz).

Differential Signal	
Test Setup	Inject sine waves of different frequencies between 0-10kHz into both Vin+ and Vin− (differential mode), of magnitude ~10µV for 20µV differential signal, and run transient analysis • Also add DC offsets to ensure they are killed effectively. • Try grounding one terminal and injecting a 20µV signal into the other to ensure they are both functional, and that no unexpected signal inversions occur (e.g., if negative terminal contains a signal).
Expectation	Check Output = amplified differential signal, and that gain (~1500 from pulse simulation above) doesn't roll off within desired 10kHz bandwidth • DC offsets should not impact output.
Transient Analysis (Sample)	<u>Input Signals</u>: (single sample case shown here) • Oppositely phased sine waves with amplitudes of 10µV for 20µV differential • Frequency of 10kHz (upper limit, worst case) • DC offset of 0V  <u>Output</u>: • New amplitude of ~10mV (agrees with midband gain of ~54dB) • Appropriately level shifted to center voltage of ~1.5982V (acceptable for ADC range) • Timing is correct (extremely slight delay/distortion, reasonable for neural application that mainly involves discrete "all-or-nothing" spike signalling) 
Additional Note(s)	The center (reference, or "no signal") voltage remains to be about 1.5982 V across different input frequencies. Gain & DC offset begin to vary *slightly* based on frequency of input signal at edges of passband (where midband gain starts to drop off, e.g. in the example shown above for a 10kHz signal). These extreme cases would need to be accounted for / mitigated in the final design solution for high precision quantization, potentially using a PGA or VGA before the ADC or implementing digital compensation logic.

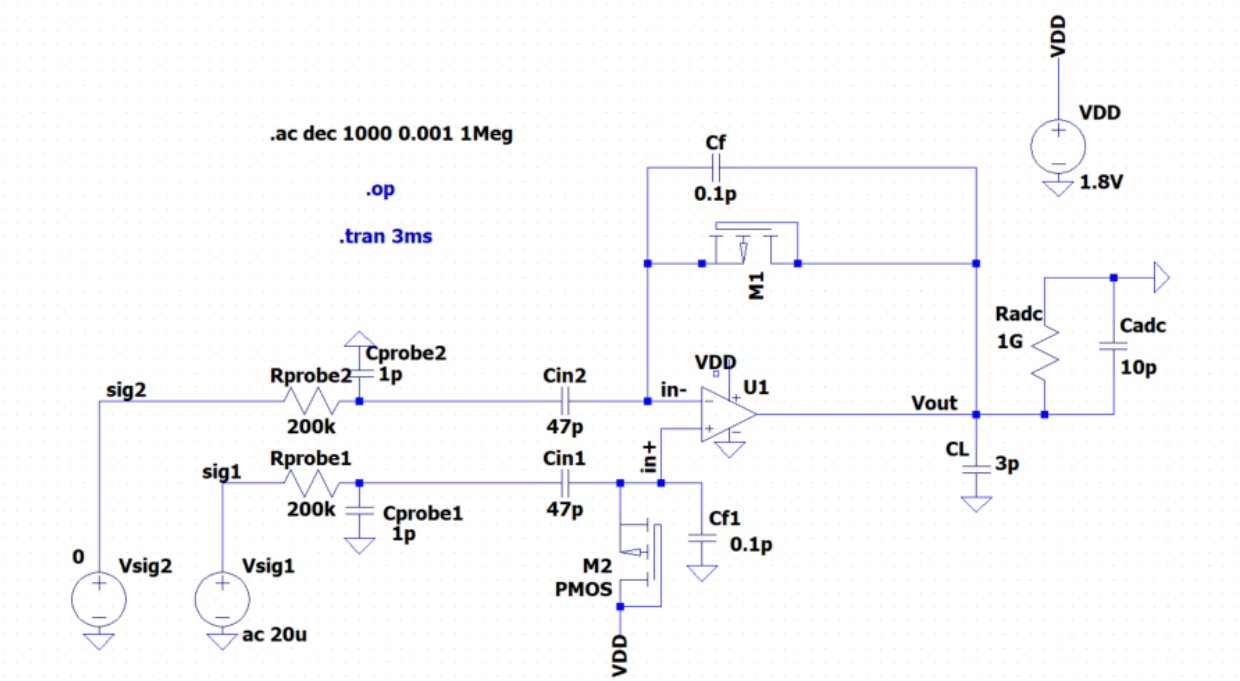
Frequency Response - Closed-Loop System	
Test Setup	Inject AC signals into both Vin+ and Vin− (differential mode), of magnitude ~20µV, and AC sweep from 1mHz to 1MHz ● Signals: ac 20u
Expectation	Check system Bode plot shows correct bandpass behavior (fL and fH) V(vout)/(V(sig1)-V(sig2))
Frequency Response (Bode Plot of System)	
Conclusion(s)	Optimized trade-off between gain to satisfy ADC requirements for signal recovery, and 10kHz bandwidth. Using some .meas directives, we can get exact midband gain, as well as simulated upper and lower 3dB frequencies using cursors: ● **Midband gain = ~53.5 dB** ● **fL = ~1.7Hz** ● **fH = ~9.9kHz** ● BW ~10kHz met within reasonable precision for this application System is closed loop stable (no 0dB/180 crossover in this Bode plot)

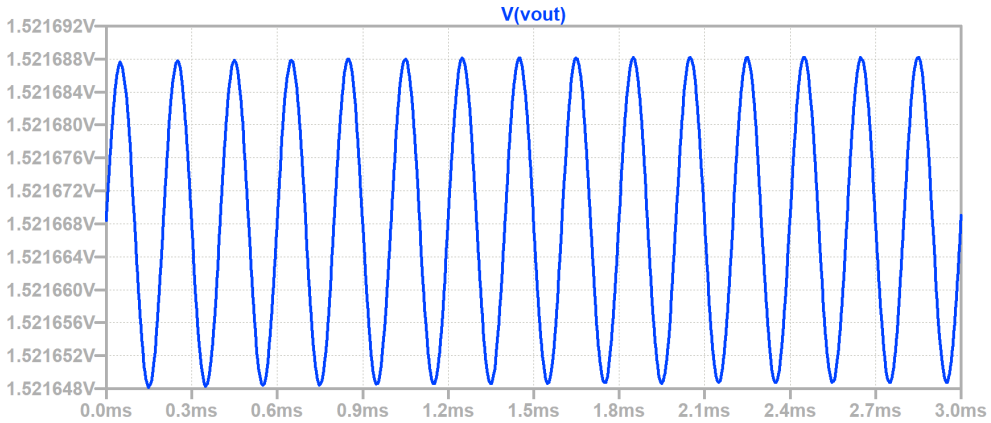
Frequency Response (Stability Analysis) - Open-Loop System	
Test Setup	- Use the standard loop-breaking technique - Break the feedback loop at the amplifier's inverting input node - Add a small-signal AC source (Vartificial) between input node and feedback node - Measure the open loop gain V(fb)/V(in-) across wide frequency range with AC sweep
Expectation	- Check that phase shift remains well above -180 degrees at the unity gain (0dB) frequency, providing a comfortable phase margin - Check that no excessive peaking occurs near the crossover point (excessive underdamped behaviour)
Open-Loop Bode Plot	
Conclusion(s)	Stability Analysis: By the Barkhausen criteria, **this system is stable**, because the loop gain never reaches the critical (-1) point, at which the phase is -180 degrees, and the gain is unity. In fact, the phase remains well above -180 degrees throughout this range of frequencies. ● *Phase Margin*: The unity gain crossover occurs at a frequency of ~575kHz, at which point the phase is ~140 degrees, providing a considerable phase margin of 320 degrees. ● *Phase Response*: The slight undulations observed in the open-loop phase plot are likely caused by the interaction of multiple poles and zeros within the system. Capacitive elements in the input network, feedback path, and load create different low-pass and high-pass effects that introduce phase shifts at different frequencies. As the frequency sweeps across these effects, the phase alternately decreases and recovers, resulting in the observed "bumps" in the phase curve. This behavior is expected in systems with multiple interacting frequency-dependent elements and does not indicate instability.

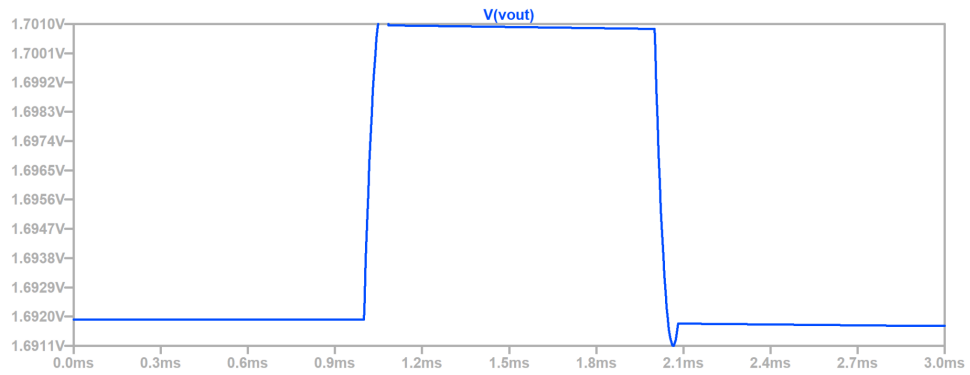
Common Mode Rejection	
Test Setup	Inject identical AC signals into both terminals (pulses and sine waves)
Expectation	Output should be flat line, level shifted to appropriate “0” reference, which is ~1.5982 V
Transient Analysis	Output observed for 10kHz signal: 
Conclusion(s)	Common mode signals (noise) are successfully rejected with the appropriate level shift of 1.5982V.

3.2. Circuit Model with PMOS as pseudoresistor:

In the two-channel prototype amplifier, non-tunable pseudo-resistors are used, implemented using PMOS devices with bulk tied to source (pre-wired in transistor part), and gate tied to drain. This topology is well known to yield large resistance values with minimal area and power consumption but introduces strong nonlinearity and variability with voltage. As described by Sharma & Gupta (2016), non-tunable pseudo-resistors exhibit highly nonlinear resistance-voltage behavior, with resistance decreasing substantially as the drain-source voltage increases. Additionally, at higher frequencies such as 10 kHz, the MOS transistor’s parasitic gate and junction capacitances can begin to dominate the impedance, effectively reducing the feedback impedance and causing gain rolloff. This behavior was observed in LTSpice simulations: while square pulse inputs (low-frequency dominant) exhibited an almost full amplifier gain of approximately 46dB, sinusoidal inputs at 10 kHz were amplified by a mere factor of 2, indicating significant bandwidth limitation imposed by the pseudo-resistor and associated parasitics. A future improvement (re: adding another pseudo-resistor in series to stabilize resistance) is presented next.

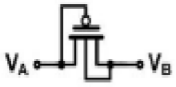


Test	Outcome
10kHz (high frequency) input	• Signal is not amplified to the desired amount due to pseudo resistance rolloff at upper end of passband. • New amplitude of ~0.04mV, much lower than anticipated ~10mV (corresponds to a tiny gain of 2!) • Measuring V/I across pseudoresistor suggests it's acting as 430MΩ resistance (0.43GΩ) at this high frequency, which is orders of magnitude below desired 1TΩ • The gain is less than expected as a result of poor pseudoresistance due to rolloff at higher frequencies 
Square pulse (low frequency) input	• Signal is amplified by about 10x, which is more than we had at high frequency, but not as much as was seen when the pseudo resistor was modelled as 1TΩ, indicating it is standalone insufficient.

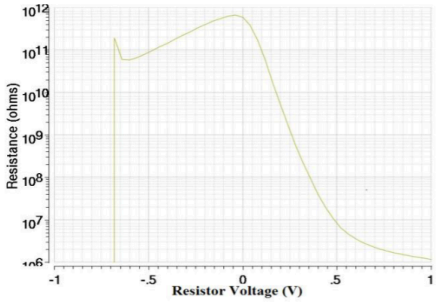


***3.3. Pseudoresistor Improvement*:**

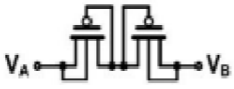
The current implementation must be revisited to increase the pseudoresistance to ~1TΩ, ensuring the RC constant remains consistently high enough to provide a low cutoff frequency, while preserving gain. The current implementation provides insufficient gain, and uses one PMOS with its gate tied to its drain, as shown here:



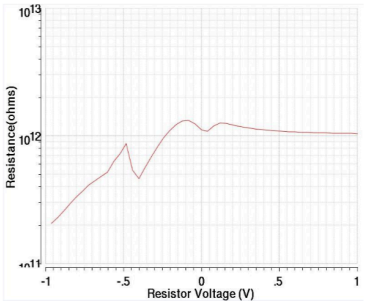
Work published by Sharma & Gupta has reviewed the operation of various FET-based pseudo resistors and simulated their equivalent resistance across a range of drain to source voltages. They found that a single PMOS achieves *just below* 1 TΩ of resistance at a peak V_{DS} of ~0V, afterward rolling off.



This poses a problem in the current design. Should V_{DS} vary slightly, the stable resistance around which the data acquisition system is built would decrease, losing important low-frequency information, and providing an unreliable gain at these frequencies. Therefore, the final, scaled design would further add another PMOS in series with the current one, with their gates tied together, as follows:

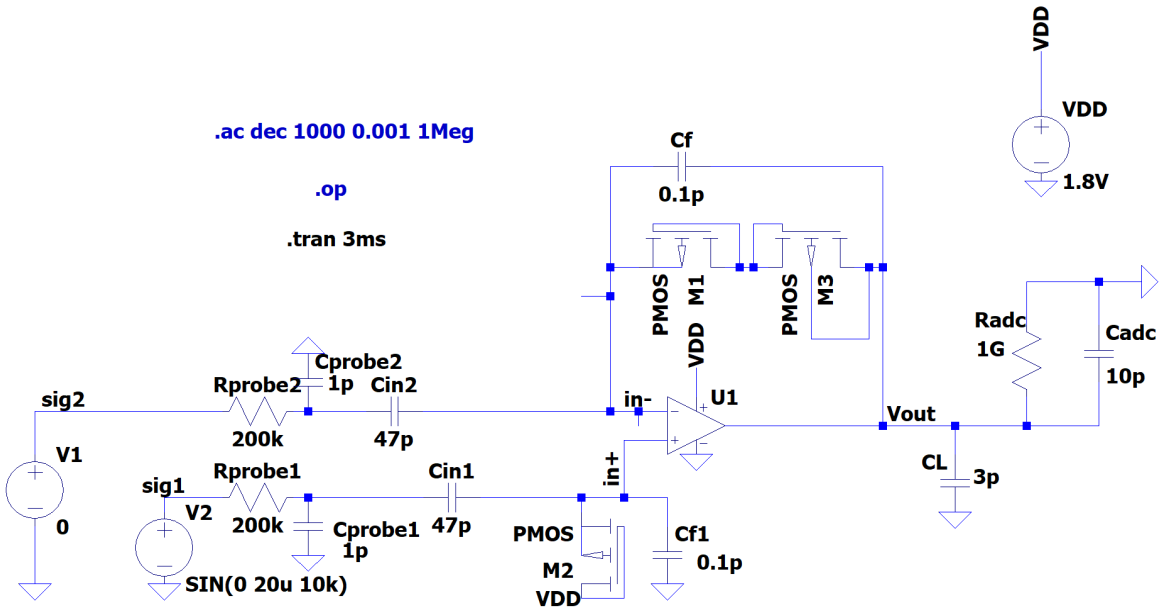


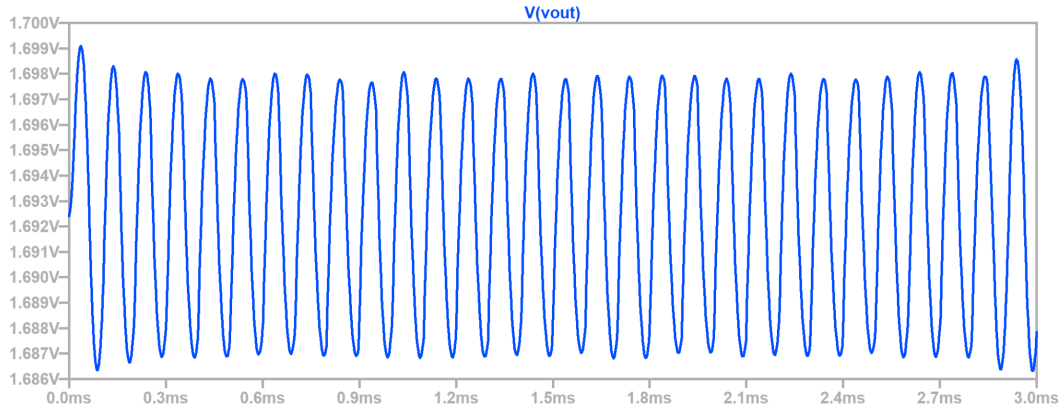
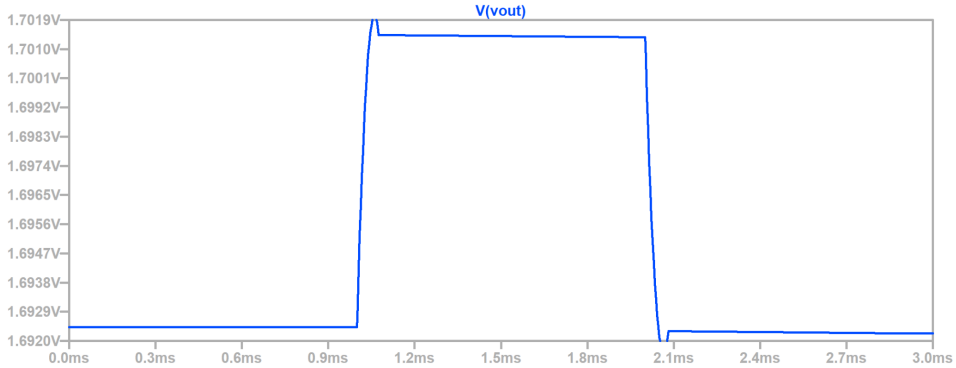
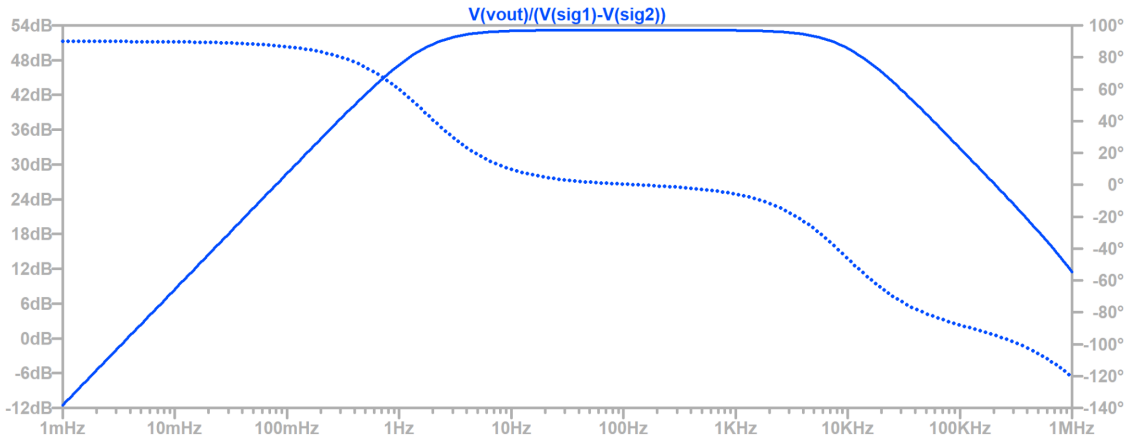
According to Sharma & Gupta, this topology provides a much more reliable 1 TΩ resistance across a wider range of V_{DS} values.



The functionality of this final circuit was verified in LTSpice for the frequency band of interest.

3.4. Circuit Model with 2 PMOS (gates connected) as pseudoresistor:



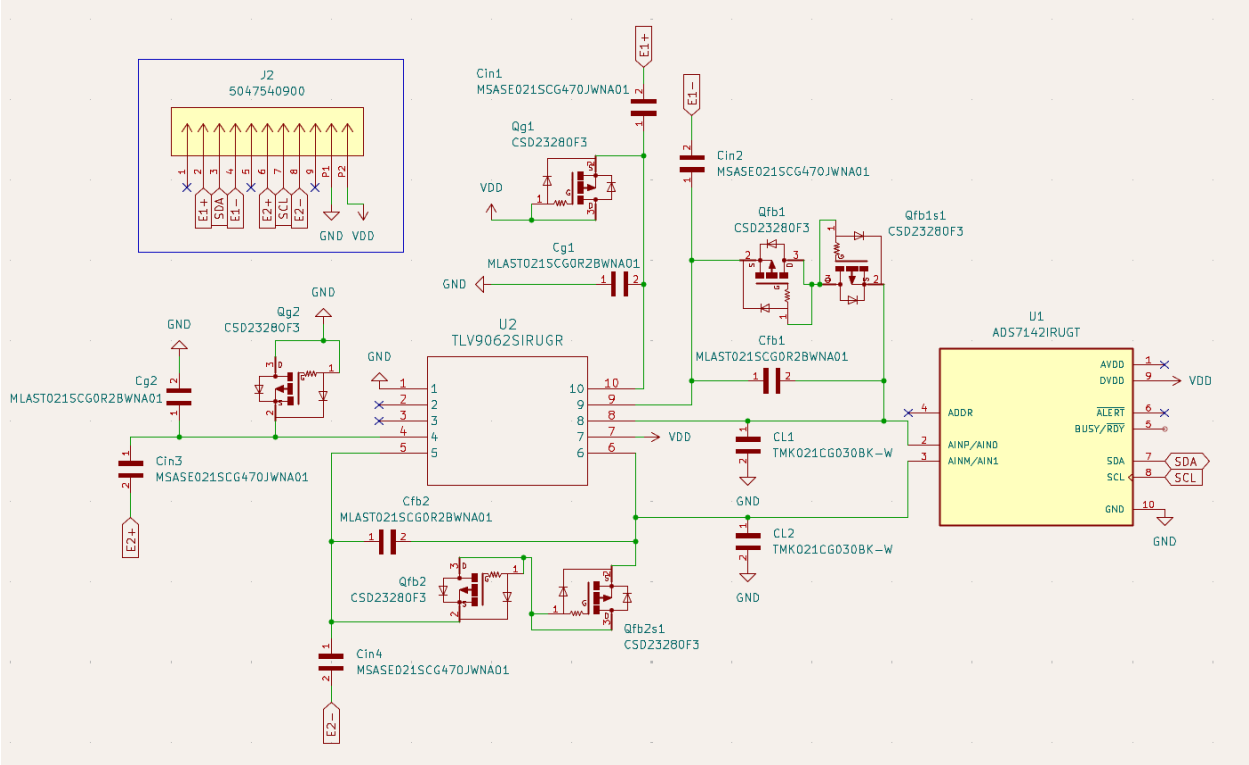
Test	Outcome
10kHz (high frequency) input	• New amplitude of ~10mV (agrees with midband gain of ~54dB) • Appropriately level shifted to center voltage of ~1.5982V (acceptable for ADC range) 
Square pulse (low frequency) input	 • The output shows clear amplification by the midband gain of ~500 or ~54dB (~20 µV input size to ~10mV output), correct timing, and stable, appropriately level-shifted baseline without drift (when pseudoresistor is connected to VDD), indicating the amplifier is working as intended.
Frequency response	 • As expected, the midband gain is approximately 54 dB, and the bandwidth is about 1.7Hz-9.9kHz.
Not shown here, because document is getting very long, but stability analyses also passed for this circuit, agreeing with the initial circuit that modelled the PMOS as ~1TΩ resistor.	

4. Schematic & Preliminary PCB Design in KiCad:

This preliminary board uses interim parts that are larger than the ones truly selected, breaking the 3mm x 3mm area constraint. However, based on the calculations provided in the Excel sheet, and the plan for a dual-sided PCB, the selected parts will be able to meet the constraint. For the final design, custom-made symbols and footprints can easily be made for all the missing parts using KiCad's symbol and footprint editors.

There exists no current symbol, footprint or 2D models for the non-standard 0.25mm x 0.25mm D10NA0R1A5PX casing. Therefore, in the current layout, a capacitor closest in value to the D10NA0R1A5PX 0.1pF was used for C_f (and its matched counterpart at non-inverting terminal). The interim part (Taiyo Yuden MLAST021SCG0R2BWNA01, 0201 case size) would be replaced with D10NA0R1A5PX in the real design for optimal tuning and performance. Otherwise, this slight change in capacitance would lower the high-pass corner frequency of the amplifier stage, leading to marginally greater attenuation of low-frequency components.

Similarly, there was no available footprint or 2D model for the connector choice (BK13C06-6DP/2-0.35V). Therefore, a similarly sized connector (5047540900) of the same pitch was used to simulate it. This connector has 9 positions rather than 6, and is slightly bigger, but was edited to more closely match the BK13C06-6DP 2.35mm x 1.6mm. The current prototype further uses the X2QFN package for the op amp, which is bigger, because the ECAD model is not available for the smaller DSBGA. However, the final design will take advantage of the ideal 1mm x 1mm part.



4.1. PCB layout plan:

A 2-layer PCB was selected for the neural signal acquisition module to meet stringent size, cost, and complexity constraints, while still maintaining sufficient signal integrity for low-frequency analog and digital signals. Although the module operates at relatively low bandwidths (~10kHz neural signals and low-speed I²C

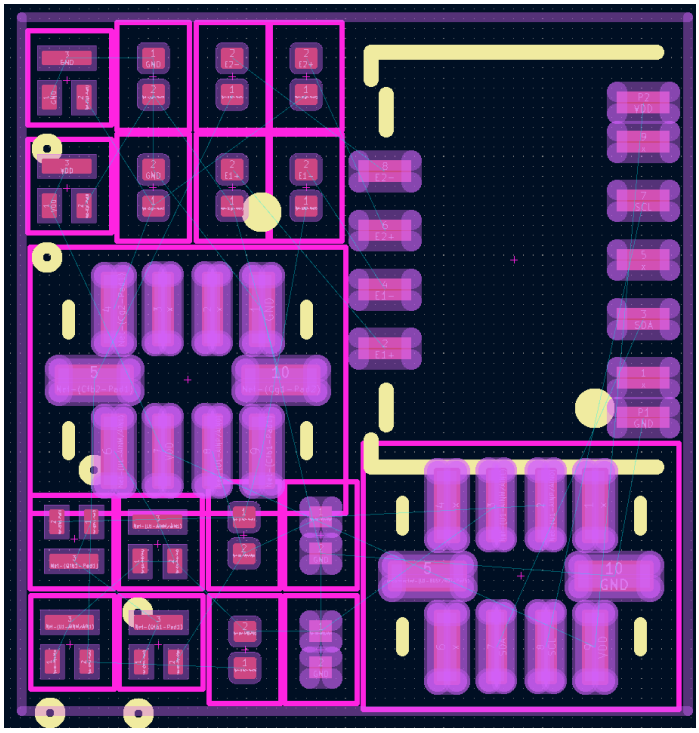
communication), proper grounding remains essential to suppress noise, minimize EMI susceptibility, and maintain clean analog performance. Based on best practices outlined in PCB design guidelines, the bottom layer of the PCB will be primarily used as a continuous ground plane, providing a low-inductance return path and reducing loop areas for both analog and digital signals. Ground connections will be made by placing short vias directly from signal traces and component grounds to the bottom ground plane wherever possible, ensuring minimal impedance and reducing noise coupling.

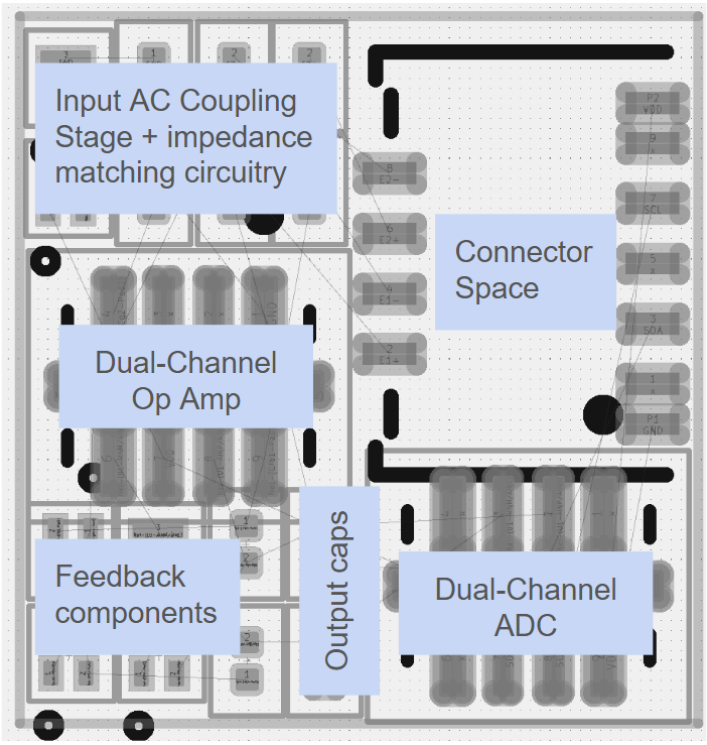
L1 (Top)	**Critical analog path: Connector Input, AC coupling & Amplification** - Highest priority parts here (op amp and Cin are essential) - Via must be placed close to op amp output pad - Minimize feedback loop area (inductance), critical for stability	- Connector (neural inputs, I^2C, power) - Op amp (U2) - Input coupling capacitors (Cin1-Cin4) - Pseudoresistor PMOS FETs (Qfb) - Feedback capacitors (Cfb) - Direct traces toward bottom - Ideally impedance balancing network (Qg, Cg) will also fit on the top, near non-inverting op amp input
L1 (Bottom)	**Auxiliary capacitors & ADC routing (slower signals)** - "Less critical" signal path (post-amp passive elements) - Ideally minimize signal path from op amp output to ADC input with vias close to pads	- CL to ground (decoupling) - ADC chip (U1) - I^2C routing - Impedance balancing network *if it does not fit on top layer*
Ground (Copper Pour)	**Bottom of board acts as a continuous ground plane under critical analog sections** - Stitching vias shall be placed near every critical node (op amp inputs, outputs, Cin grounds) - Minimize return path impedance for analog signals	- Continuous ground pour

4.2. Current (Sped-Run) Implementation:

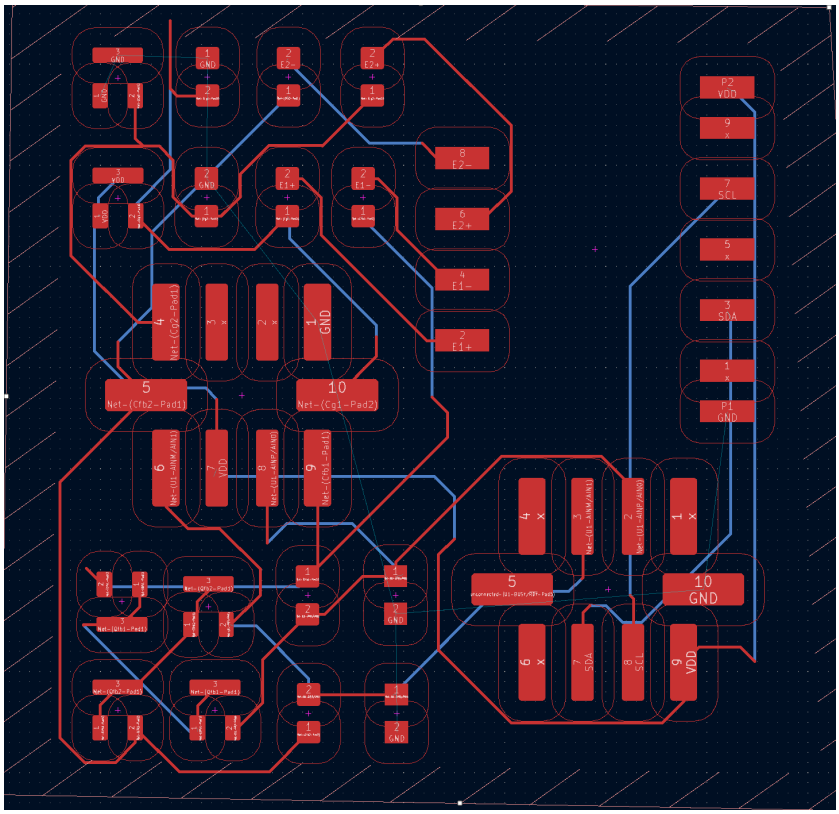
The current PCB layout serves primarily as a rough demonstration of component placement and signal flow, rather than a finalized compact implementation. For example, in this preliminary design, the ADC (U1) overlaps significantly with the connector (J2), under the knowledge that the actual chosen connector is much shorter in physical length than the interim one used here. Similarly, part of the feedback network components purposefully overlap with the amplifier IC, since the truly selected part is much smaller than the interim used here. Nonetheless, in designing this preliminary prototype layout, several important practices were applied to establish a strong foundation. Input capacitors (Cin1–Cin4) were placed close to the incoming probe signals and amplifier inputs to ensure proper AC coupling and minimal parasitic pickup. Feedback loops, including pseudoresistor FETs and feedback capacitors, were placed near their corresponding amplifier nodes to minimize loop areas. The ADC was placed near the connector and to the side, such that digital control signals may be routed along the periphery of the board. This serves to isolate them from sensitive analog sections, reducing potential cross-coupling and noise injection. Load capacitors were positioned near the amplifier outputs to maintain output stability. In the final design plan, the ADC chip and accompanying output passives will be placed on the bottom of the main layer.

Detailed component area calculations, summarized in the accompanying Excel sheet, show that the cumulative footprint of all active and passive components totals approximately 10.72 mm^2. This analysis confirms that achieving a final board size of 3 mm × 3 mm (9 mm^2) is feasible, particularly with the use of a dual-sided PCB.




Input AC Coupling Stage + impedance matching circuitry
Connector Space
Dual-Channel Op Amp
Output caps
Feedback components
Dual-Channel ADC

Preliminary Wiring: (All grounds connected through top/bottom copper pour)



5. Design Scalability & Future Improvements:

The use of flexible, thin PCB materials and modular stacking strategies could allow this design to scale to 100 channels without requiring major system-level redesign.

5.1. Analog Signals:

Based on the project's prompt, when scaling to 100 channels, the two discrete amplifiers used in this prototype would be replaced by a custom 100-channel IC. In this hypothetical final version, each amplifier's power consumption is reduced by 90%, yielding a total amplifier power of approximately 9.61 mW across 100 channels (see Excel sheet). Including the ADC and connector contributions, the final total board power is estimated at 10.23 mW, slightly exceeding the 10 mW design target specified in the project prompt. However, this overhead will be effectively mitigated by leveraging the integrated low-power shutdown mode available in the TLV9062 operational amplifier used in the design. The TLV9062 features an enable pin (EN) that allows each amplifier channel to enter a standby mode, reducing its typical supply current to less than 1 µA per channel when not actively sampling. In the final system implementation, the enable pins of the amplifiers will be controlled by a digital logic line or microcontroller that synchronizes with the ADC sampling schedule, ensuring that the amplifiers are placed into shutdown during periods when signal acquisition is not occurring. By activating the amplifiers only briefly before each sampling window and disabling them immediately afterward, the average power consumption can be reduced well below the continuous 10 mW constraint while preserving signal integrity, especially noting that the op amps constitute the main source of power dissipation on the board.

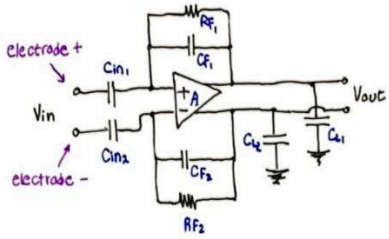
***5.2. Digital Signals*:**

To extend the architecture to support many more channels, additional multiplexing will be incorporated to efficiently select between amplifier outputs before digitization. A time-division multiplexing (TDM) or parallel-bus multiplexer strategy would allow multiple analog outputs to share a single ADC input or a few ADCs. The acquisition module would be controlled by a low-power microcontroller or FPGA capable of I^2C communication, fast clocking and basic data handling. A cortex-M0+/M4 MCU or small FPGA would be suitable, balancing power budget and performance. The current I^2C setup may be extended to SPI for higher speeds and enhanced waveform recovery of fast transients. This would require an additional two wires, minimum, meaning the current 8-pin connector would need to be swapped for one that offers at least 10-pins.

6. Appendices

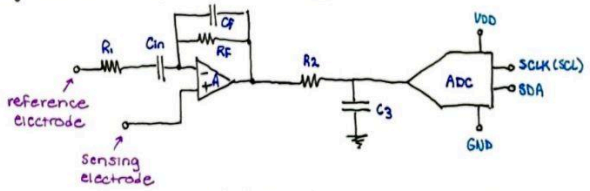
6.1. Preliminary Designs:

① Fully differential amp. (+ bandpass filter): Industry standard for neural recording.



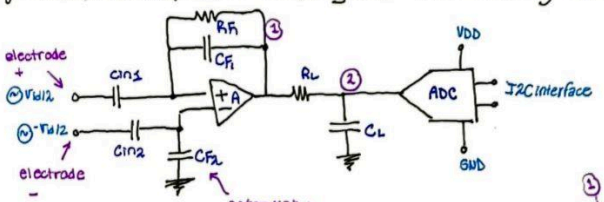
- A is typically a transconductance, low noise, high/moderate gain amp.
- R_{F1}, R_{F2} often replaced w/ pseudoresistors (FET) for >10GΩ resistance when signal freq. of interest is low (to decrease high pass cutoff from feedback circuit)

② Single Ended diff. amp. w/ AC coupling & 2nd order Filtering action (V1)



* Works under the assumption that sensing electrode input path is clean (i.e. that there is a reliable tissue GND) which is not the case for extracellular neural recording, which uses electrode-pairs necessarily for a truly differential input (noise-cancelling).

③ Single Ended. diff. amp. w/ AC Coupling & 2nd order Filtering (V2)



potentially add R_{F2} in parallel (check matching in sim.)

① ② : where RC low pass action introduces pole.

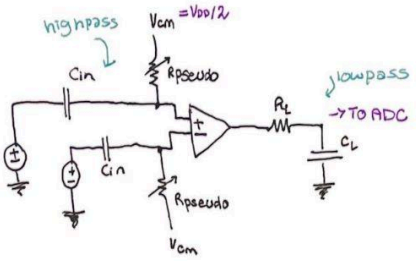
① high ②

R_{F1} ⇒ potentially FET based pseudoresistor (based on f_{c1} requirement)

correctons

- X feedback on ⊖ terminal for non-inverting config.
- X R_{F2} added in parallel for impedance matching
- X R_{in1} required on ⊖ terminal to keep high input impedance & set gain. ? R_{F1} may be sufficient.
- ? consider removing R_L to save space (close anti-aliasing filter → we'd only have high pass action → risk issues from high freq. spikes into ADC) ↳ C_L alone would shunt AC noise but could lead to reflections/ringing/underdamped behaviour...
- X (probably...) might need to add DC biasing resistors in series w/ input caps. since op. amps. bias currents need a DC path...
- ? 1st thing to sacrifice for board space since currents are tiny...

6.2. (Not Pursued) Open Loop Topology



open loop configuration? would allow us to ↓Cin for same gain... even ↑gain to better use ADC Vfullscale

$I_{out} = G_m(V_+ - V_-)$ A_V: open loop gain

$V_{out} = A_V(V_p - V_n)$

highpass, lowpass

$$H(s) = \left(\frac{sR_{pseudo}C_{in}}{1+sR_{pseudo}C_{in}}\right) \cdot A_V \cdot \frac{1}{R_LC_Ls+1}$$

call R_{pseudo} R_p for simplicity

$$H(s) = \frac{A_V R_{pseudo} C_{in}\, s}{s^2 + \frac{R_LC_L + R_pC_{in}}{R_LC_LR_pC_{in}}s + \frac{1}{R_LC_LR_pC_{in}}}$$

$$= \frac{A_VR_pC_{in}R_LC_LR_pC_{in}}{R_LC_L+R_pC_{in}} \cdot \frac{\left(\frac{R_LC_L+R_pC_{in}}{R_LC_LR_pC_{in}}\right)s}{\text{denom.}}$$

→ with this topology, Cin is in num. twice & A_V is added too meaning ↓ Cin for same gain

→ Based on these formulas (from a lil Python script 😊) can achieve: Gain of 1592

$C_{in} = 10\mu F$, $R_L = 10K\Omega$, $C_L = 1.59nF$ with $R_{pseudo} = 1G\Omega$ (achievable), $A_V = 10^4$

or $C_{in} = 1\mu F$, $A_V = 10^5$

(...& other variations)

with TLV9062 op amp:

$A_V = 15848$, $C_{in} = 3\mu F$, $R_L = 10K\Omega$, $C_L = 1.59nF$ *need gain ≈ 750, $R_{pseudo} = 1G\Omega$

$A_V = 15848$, $C_{in} = 0.1\mu F$ ↙ max in 0201 case

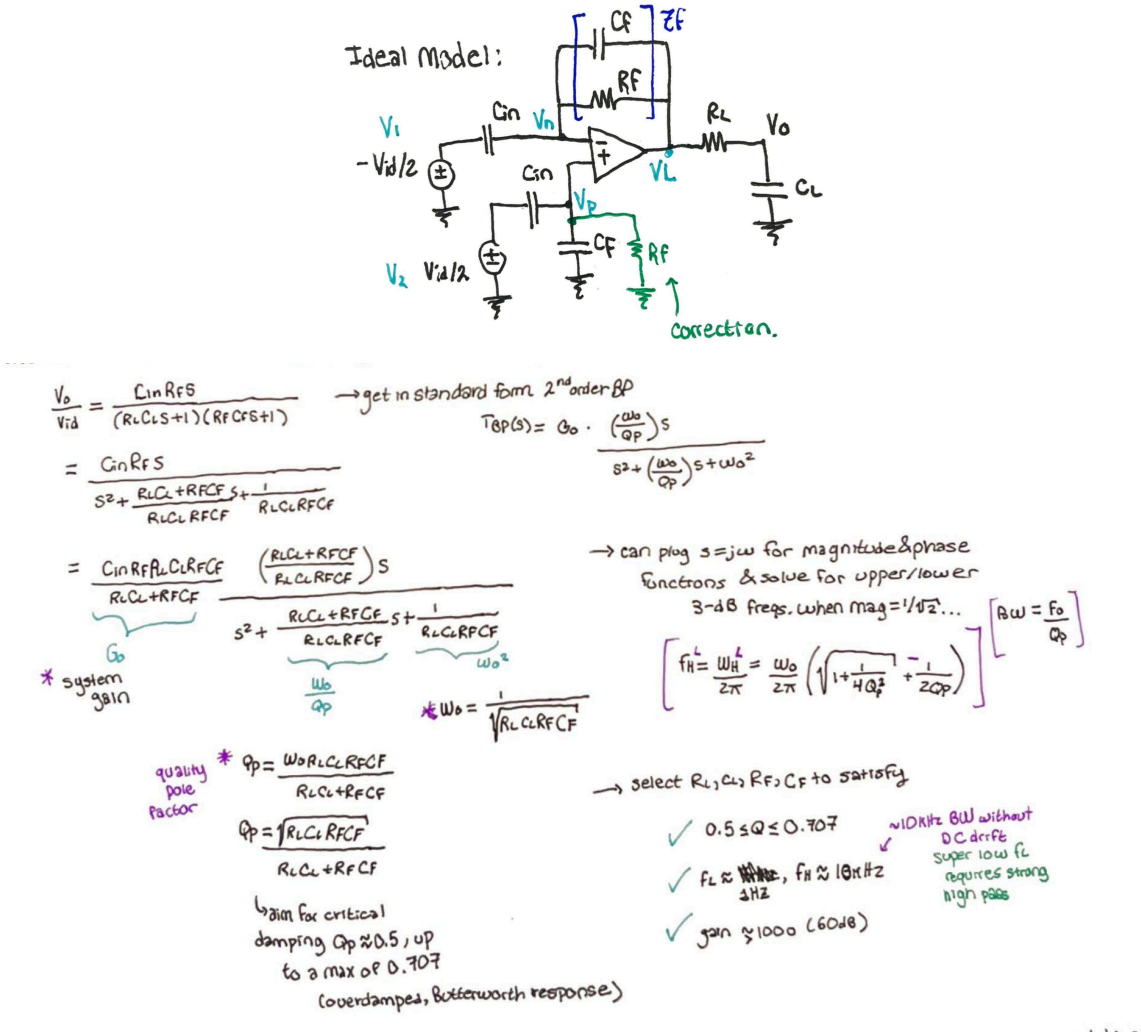
$R_{pseudo} = 50G\Omega$ (min.) for gain ≈ 1000 ← could be a bit less & it's okay (conservative gain of 750)

$C_L = 4700pF$, $R_L = 3.3K\Omega$, 4 off 2 rad from 3.3877K ideal

$C_L = 1nF$, $R_L = 16K\Omega$, 4 off 2 rad from 15.923K

$f_H \approx 10.3KHz$ which gives wriggle room. ← nevermind ±5% tol on 3.3K & too much... get 1%!

6.3. Transfer Function of selected closed-loop topology:

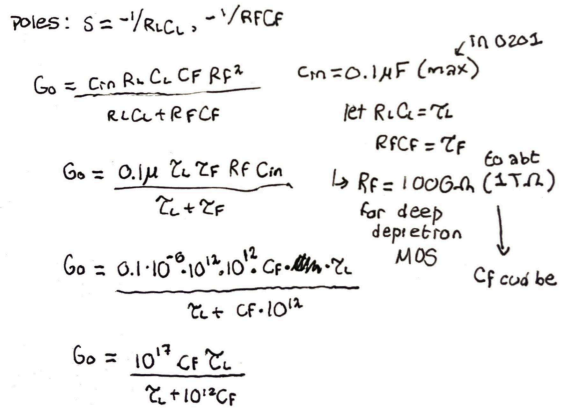


Therefore, the transfer function of the ideal selected system is that of a standard 2nd order bandpass filter:

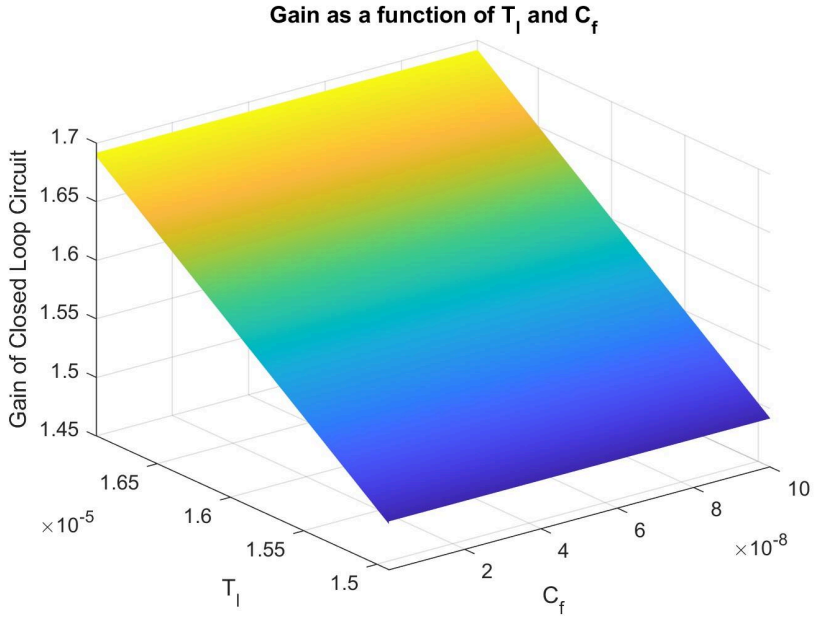
6.4. Tuning component values for selection:

A Matlab script was written to optimize the amplifier's gain based on the maximum possible Cin value (available in an 0201 casing), and the approximate pseudo-resistance that can be offered by a FET operating in the subthreshold region. The optimal values of C_L and C_F could thus be selected to strike a balance between maintaining high gain and ensuring the bandwidth rests near 10kHz.

Based on the transfer function:



Surface plots were generated to better visualize how altering each tuning parameter impacts the overall gain, Go.



6.5. Literature Review Log:

Article Source	Key Points	Design Takeaways
Miscellaneous notes	• A differential OTA-based amplifier architecture is typically selected for neural recording modules to achieve low-noise amplification of extracellular microvolt signals while maintaining low power consumption. • A multi-stage amplifier architecture is often used to achieve the high overall gain (~60–80 dB) necessary for extracellular neural signal amplification while preserving stability. The multi-stage approach also reduces the need for impractically large passive components, enables improved low-frequency noise performance, and offers flexibility for filtering and anti-aliasing prior to digitization.	

	• Many applications use time-division multiplexing (TDM) to share ADCs across multiple channels to save power and pins. Probably too complex for now, but if expanding to many channels, should consider sharing ADC.	

https://kth.diva-portal.org/smash/get/diva2:1304287/FULLTEXT01.pdf Circuit Design Techniques for Implantable Closed-Loop Neural Interfaces	• Neural signals are small (microvolt range)
	• Electrode interfaces cause:
	  ○ Large DC offsets (hundreds of mV)
	  ○ High impedance
	• Must reject large DC offsets while keeping small AC neural signals
	• Need high input impedance to avoid loading electrodes
	• Need high CMRR (common-mode rejection) to reject noise
	• Amplifier must have ultra-low noise (ideally below 5μV RMS)
	• Amplifiers must use AC coupling at the input (with a 1-10 Hz cutoff) to block DC.
	• Power consumption must be micro-watts per channel.
		• Use **AC-coupled differential amplifiers** (achieve high CMRR while amplifying tiny signals).
		• Add high pass filters between electrode and amplifier input.
		• Use chopper stabilization if even lower noise is needed (but more complex).
		• Use bypass capacitors to stabilize supply rails.
		• Insert simple RC low-pass filters between amplifier and ADC to prevent aliasing, at a cutoff frequency slightly above maximum signal of interest.

https://synthneuro.org/wp-content/uploads/2021/08/16-08-scholvin.pdf Heterogeneous Neural Amplifier Integration for Scalable Extracellular Microelectrodes	• Ground planes are critical for signal isolation and low noise in PCB design. • Analog signals and digital signals (outputs like SPI lines) should be routed far apart to avoid crosstalk. • Power rail decoupling with bypass capacitors is important.	• Include a solid ground plane under the whole PCB. • Keep SPI lines away from neural input traces. • Place bypass capacitors near power pins.
https://sghoreish.github.io/BioCAS_Dorian.pdf Design Considerations for Ground Referencing in Multi-Module Neural Implants	• Solid ground planes and good layout make a massive difference to noise performance. • AC signals must be centered about the system's ground (AC coupling). • If AC ground referencing is bad, effective CMRR will suffer, and noise will dominate the signal. • 3 grounding schemes: passive, drive and sense.	• Use a solid ground plane (so that all circuits “see” the same GND). • Ground plane should be low impedance (copper pour). • Connect the cable ground pin (from outside) directly to the board ground. • Keep analog ground clean by avoiding noisy digital signals near amplifier inputs → use capacitor & bias resistor to achieve AC GND. ○ Bias resistor pulls DC level to 0V by being connected to GND.
https://ietresearch.onlinelibrary.wiley.com/doi/epdf/10.1049/ell2.12765 An expandable 36-channel neural recording ASIC with	• Confirms that low input-referred noise (target: few μVrms) is a top priority in the amplifier selection. They achieved ~5.9 μVrms. • They use a selectable 0.3-300 Hz	

modular digital pixel design technique	highpass - confirms 1Hz AC-coupling cutoff is in range. ● They sample at 31.25 kSps with a 12-bit SAR ADC. ● Their 36 channels use a time-multiplexed digital bus after ADCs. ● Simple ground tied to skull during *in vivo* test.	
https://www.researchgate.net/publication/349912652_A_253_NEF_8-bit_10_kSs_05_mm_CMOS_Neural_Recording_Read-Out_Circuit_with_High_Linearity_for_Neuromodulation_Implants A 2.53 NEF 8-bit 10 kS/s 0.5 µm CMOS Neural Recording Read-Out Circuit with High Linearity for Neuromodulation Implants	● They describe a two-stage fully differential OTA (transconductance) amplifier with resistive-capacitive feedback. Optimized for low noise and low power. ● OTA has feedback Rf and Cf to set gain and low corner frequency. ● Use of AC coupling caps (large values like 1nF) at input to eliminate large electrode DC offset without saturating amplifier. ● They used an 8-bit SAR ADC with ~10kSps sampling, matching low-frequency neural signals. ● Manual layout of capacitors using common centroid placement to minimize mismatch and parasitics. ● Full system draws about 26µW total. ● Achieved low noise input of ~3 µVrms. ● The amplifier gain is around 60dB (1000x).	● Consider differential OTA + RC feedback rather than voltage differential amplifier. *Common centroid method:* 1. use identical unit capacitors (or resistors). Ex: all 1pF or all 1kΩ. 2. interleave and mirror them so that any error affects both sides equally and cancels out.
https://www.researchgate.net/publication/339120753_Multi-Channel_Neural_Recording_Implants_A_Review Multi-Channel Neural Recording Implants: A Review	● Amplifier topologies: AC-coupled amplifiers (like the capacitive feedback network) are preferred for multi-channel, low-noise designs. ● Noise reduction with chopper stabilization (CHS): Flicker noise dominates at low frequencies. CHS can massively reduce it, but greatly complicates the design (e.g., needs careful chopping & ripple cancellation). ● Low-power OTA design: Prioritize low flicker noise, high gm, and operate in subthreshold. ● Multi-stage amplification: Use two or three stages instead of one in order to avoid huge input caps; total gain should be distributed across stages. ● Capacitor matching (common centroid): Use common centroid layout technique to minimize errors due to manufacturing variation. ● ADC choice: For low-bandwidth neural signals, SAR ADCs are low-power and fit the application. 8-10 bit resolution is typical. ● Area constraints: Large input caps and resistors eat up chip area. Multistage amps help mitigate this.	
http://journal.auric.kr/AURIC_OPEN_temp/RDOC/ieie02/ieiejsts_202210_009.pdf A low-power neural signal	● Two stage amplification: They use a folded cascode OTA with moderate gain (~20 dB) followed by a programmable gain amplifier (PGA) for flexible, tunable gain. ○ Moderate initial stage gain prevents saturation during artifacts.	

acquisition analog front-end IC for closed-loop neural interfaces	○ This circuit could handle up to 280 mVpp common-mode artifacts without distortion. ● AC coupling with capacitive feedback: simple way to eliminate DC offsets without complex chopper circuits (Cin and Cf) ● OTA uses common-mode feedback. ● They use a pseudo-resistor (MOSFET) across Cf to enable ultra-low highpass cutoff in small chip areas. ● They use large W/L input devices at OTA for low noise.They use 300/1 µm PMOS and 200/2.5 µm NMOS. ● They have programmable bandwidth control with a second stage amplifier (PGA), but this feature is out of scope for my project.
https://www.researchgate.net/publication/235217911_A_low-noise_low-power_front-end_amplifier_for_neural-recording_applications A low-noise, low-power front-end amplifier for neural recording applications	● Single stage folded-cascode OTA used for low noise, wide input range, and high open-loop gain (~60-70 dB).... Custom-fabricated; unlikely to be available from COTS OTA. ● AC coupling with programmable capacitive feedback around OTA to remove DC offset ● MOS pseudo resistors are used in parallel with the feedback capacitor. They act as ultra-high resistance (~GΩ) to allow very low high pass cutoffs (~10mHz to Hz range) ● Biasing stability circuit to bias OTA independent of supply variation (wide-swing constant gm biasing) ● Power budget of 10µW
https://eprints.soton.ac.uk/451603/1/TCASI_ACCEPTED.pdf A Compact, Low-Power Analog Front-End with Event-Driven Input Biasing for High-Density Neural Recording in 22-nm FDSOI	● Instead of fighting electrode DC offsets with huge resistors or complex feedback, they reset the input node to bias voltage when needed (too complex for my purposes). ● They use an incremental 11-bit ADC with oversampling. ● Folded-cascode Gm-C OTA with common mode feedback at output used again for the first stage: low noise, high input impedance. ● They chose an input cap of 2.5pF for AC coupling specifically to have a small area and high input impedance. ● Ground shielding under input capacitors

CMFB Method	Components Needed	Pros	Cons
Resistive Divider CMFB	- Two large resistors (~100kΩ) from OUT+ and OUT- to common-mode reference (say, 1.65V)	Very simple	May slightly load the outputs if resistor values are too small
OTA Internal Tail Biasing	- Bias the differential pair's tail current to fix common-mode naturally	Cleaner outputs	Needs good OTA part selection

Common Topologies:

Option	Advantages	Disadvantages
Single-Stage (Single-Ended Output Op Amp)	- Fewer components - Simpler PCB layout - Easier to fit in 3×3mm constraint	- Potentially lower total gain - Lower gain means the amplified neural signal (~mV range) could use only ~10–20% of ADC

	- Lower total power - Very fast design and build - Mature, robust, stable - Easier to AC couple inputs since there's only one "active" input per channel (plus the reference), so there's no need to worry about matching - No need for common-mode feedback (CMFB) network	full-scale input range - Single-ended output more susceptible to noise pickup compared to differential - Can't easily cancel out common-mode disturbances (like 60Hz mains noise) - Not industry standard. Typically, differential signals should employ differential amplification & differential ADC.
Single-Stage (Fully differential OTA)	- Fewer components than two stage - Differential signal better for noise immunity (environmental EMI, crosstalk) - Direct match to fully differential ADCs - Some integrated OTAs are already optimized for biomedical signals (low noise floors)	- ADC input might get slightly low signal (~mV range) - Needs careful OTA selection to make sure noise and gain are good enough - More complex & more components than single-ended - Feedback and CMFB circuits add complexity
Pseudo differential amplifier	- Simplified circuitry: PDA circuits are often simpler to implement than true differential amplifiers, as they only require one input signal and a ground reference. - Reduced common-mode noise: By referencing the signal to ground, PDAs can help to reduce common-mode noise, which is noise that is present on both input signals.	- Reduced dynamic common-mode rejection: While PDAs are good at rejecting DC common-mode signals, their ability to reject dynamic (changing) common-mode noise is less than that of true differential amplifiers. - Not ideal for all applications: PDAs are best suited for applications where the signal is relatively clean and the common-mode noise is primarily DC in nature.
Two-Stage (OTA + PGA)	- Higher total gain (~60–80dB) - Easier to fully saturate ADC input range - More flexible for future tuning (gain stages, bandwidth, etc)	- Many more components (another amp stage) - Harder PCB routing - Bigger size might violate 3x3mm - More complex biasing and power management - More noise and instability risk