**<<< Atmega328p/Harvard Architecture >>>**

**IS32, Computer Organization and Architecture**

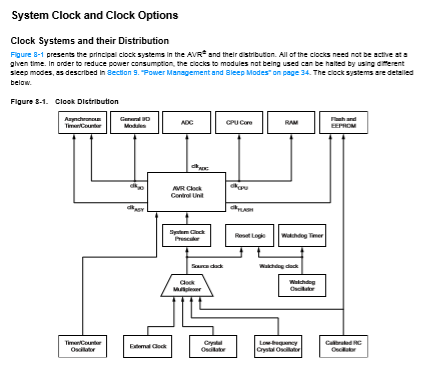
**Report**

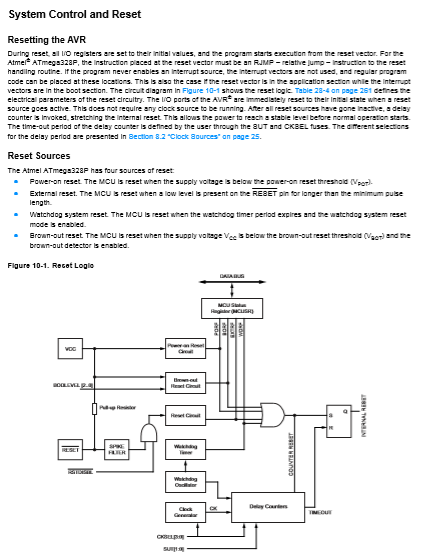
**on**

**Processor Architecture**

**Name: Nimish Nikhil Bongale**

**USN: 1MS17IS077**

1. Combinational circuits  
   **System clock**   
   

**System Control**

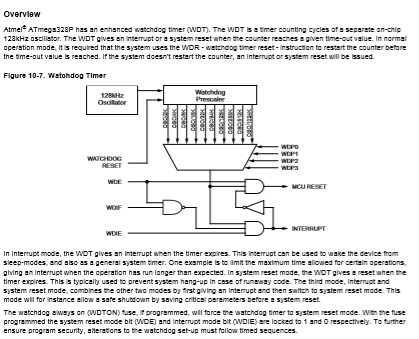
*AND gate*

*OR gate*

*Pull up Resistor*

*(flip flop part of external circuit)*

**Watchdog Timer**

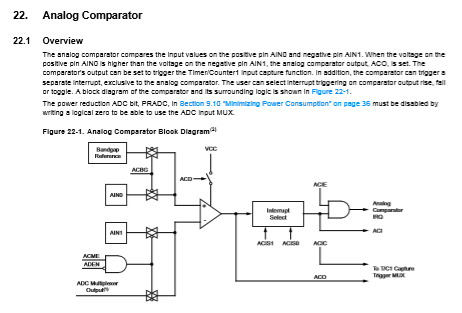


*AND gate*

*NOT gate*

*NAND gate*

**Analog Comparator**

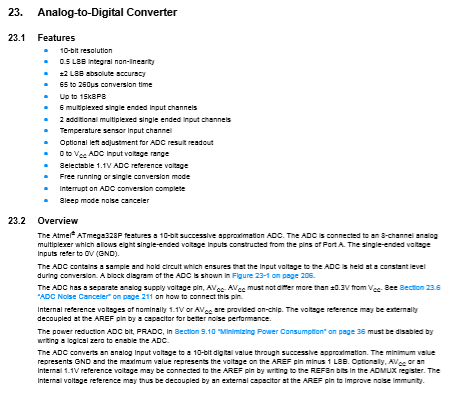
****

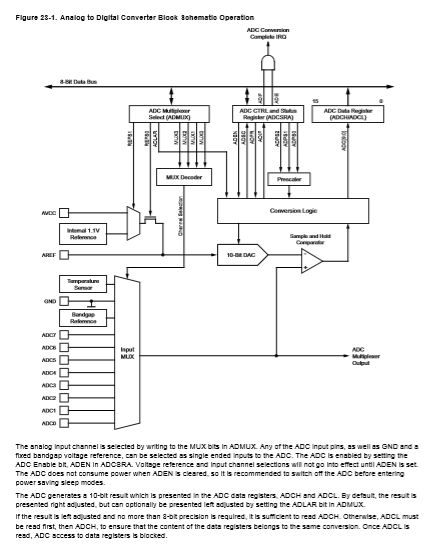
*Op-Amp*

*AND gate*

*Interrupt Selector (some type of multiplexer)*

**Analog to Digital Convertor**

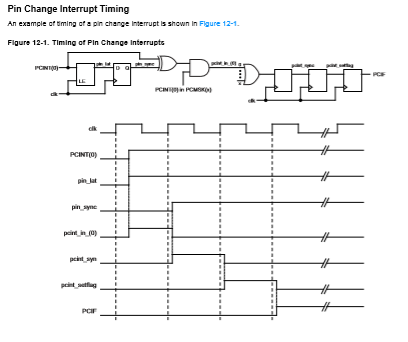




*Input MUX(to select between ports for activation) AND gate*

*Comparator Conversion Logic*

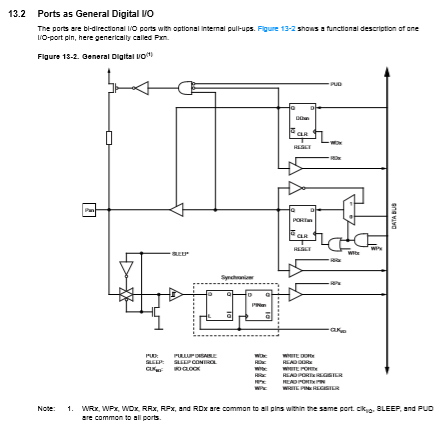
2. Sequential Circuits

**Pin Change interrupt**   


*XOR gate AND gate*

*D flip flop(multiple) OR gate*

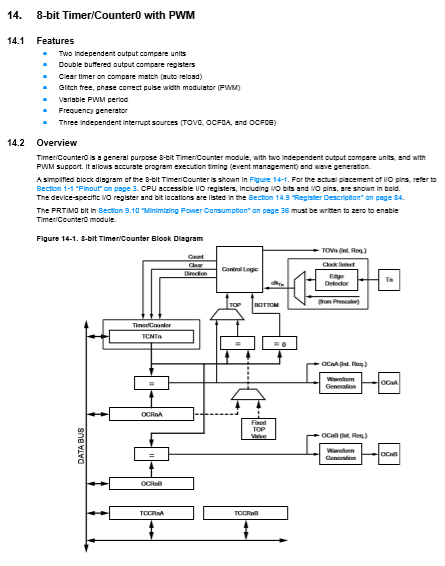
**Ports as Digital I/O**

****

*NOT gate AND gate D flip flop Synchronizer unit*

*OR gate*

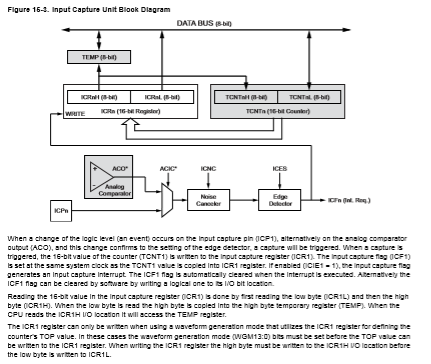
**8 bit counter**

****

*Edge Detector (capacitor, resistors) Control logic(as discussed earlier)*

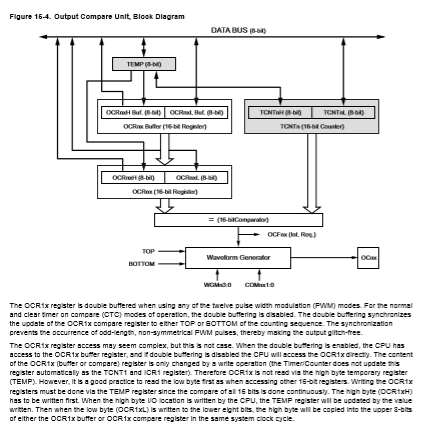
*Waveform Generator Timer/Counters*

**Input Capture Unit**

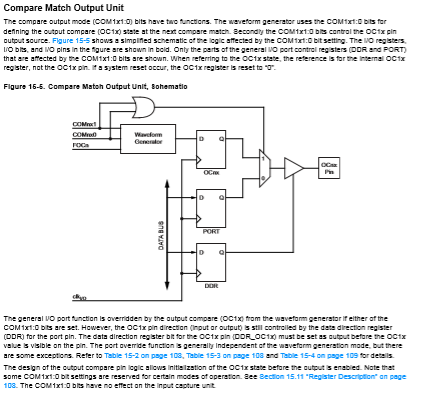
****

*Registers Edge Detectors Comparators*

**Output Capture Unit**

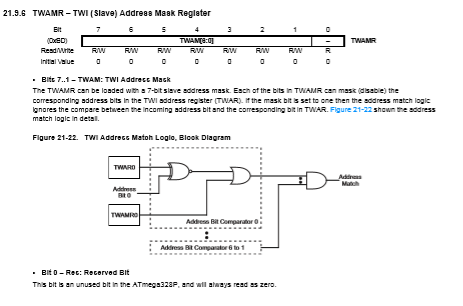


*Waveform Generator OCR1x Register (Flip Flops)*

**Compare Match Output Unit** 

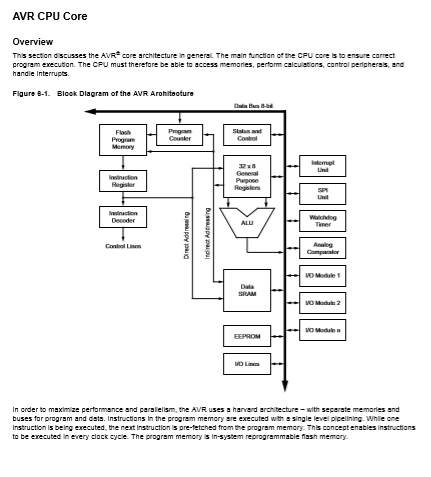
*AND gate D flip flop Waveform generator*

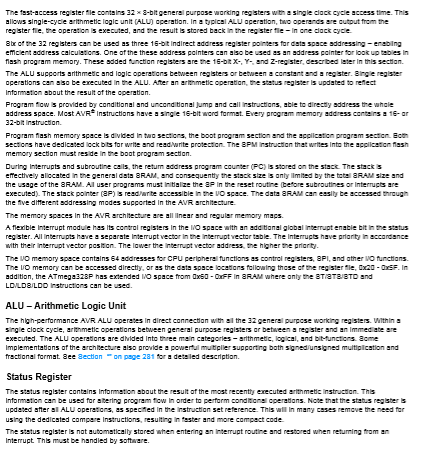
**Address Mask Register**

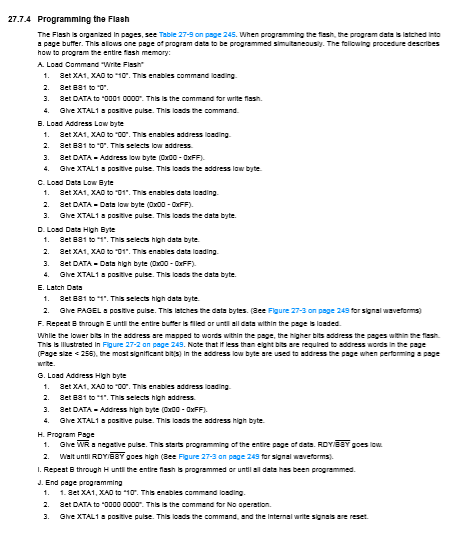
****

*X-NOR gate OR gate AND gate*

3.CPU and Memory Features

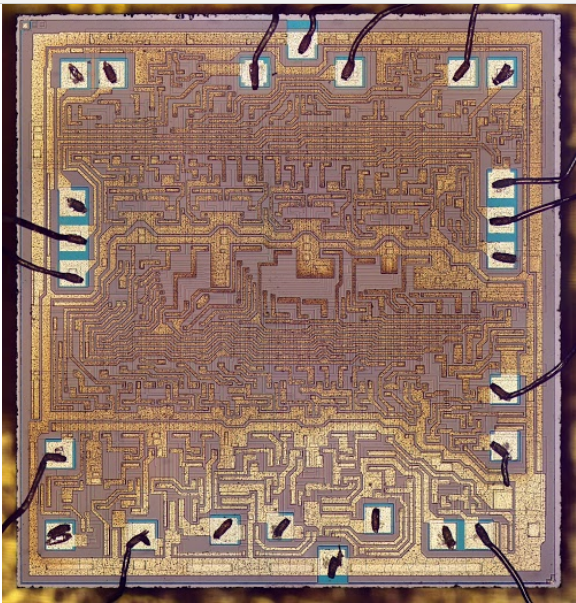






4. ALU logic, Addressing modules, Instruction set features and CPU organisation

It provides 8-bit arithmetic and logic functions, and could be combined to handle larger words, making it a key part  
of many CPUs. But if you look at the chip more closely, there are a few mysteries. It implements addition,   
subtraction, and the Boolean functions you’d expect, but why does it provide several bizarre functions such as   
“A plus(A and not B)”? And if you look at the circuit diagram (below), It looks like a random pile of gates rather   
than being built from standard full adder circuits.

****

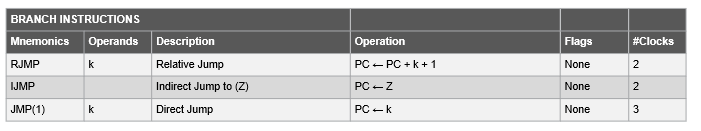
Some of the different registers (with flags and their associated usage commands) are covered here:-



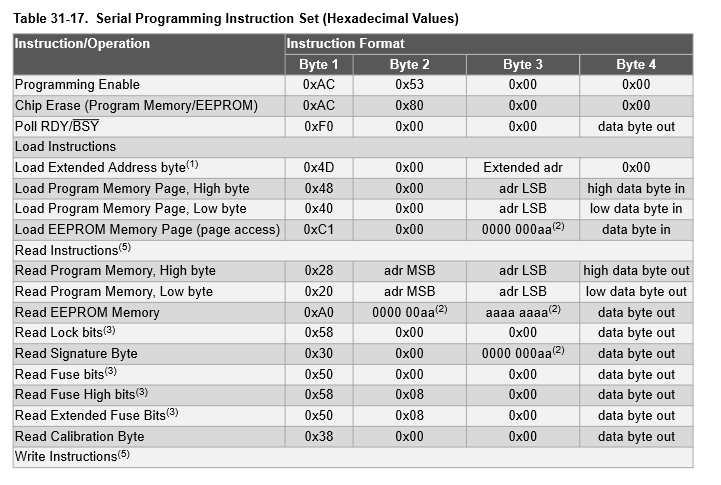
Being a microprocessor based on the RISC (Reduced instruction set) architecture, all the commands are simple,

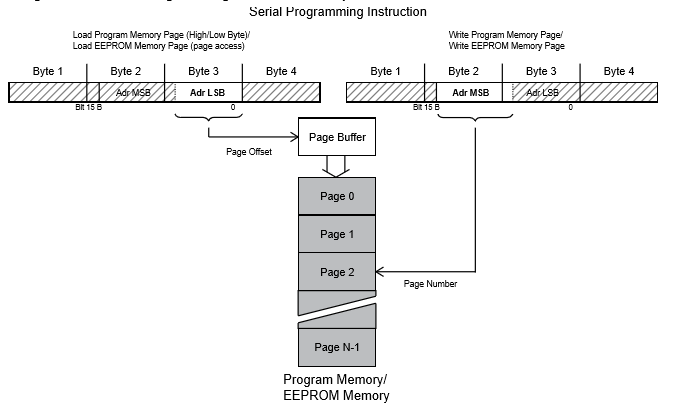
yet effective.

Some branch instructions:-

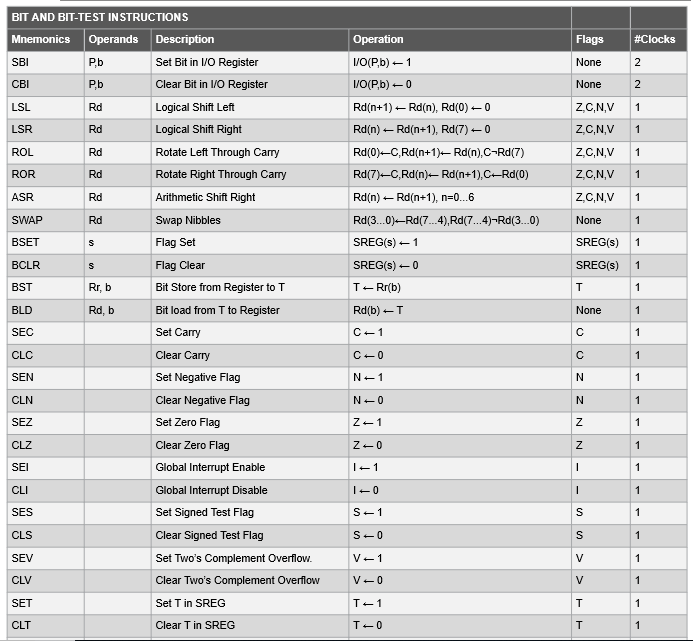


The Serial programming instruction set:-

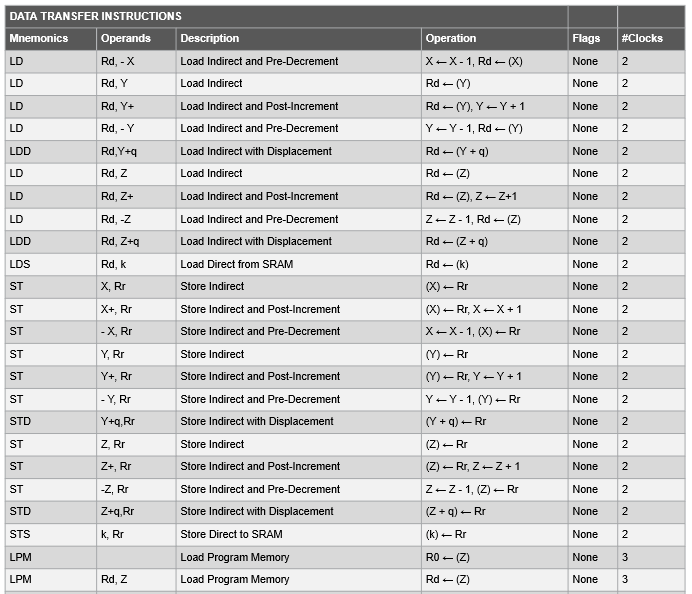




The Bit and Bit test instructions:-

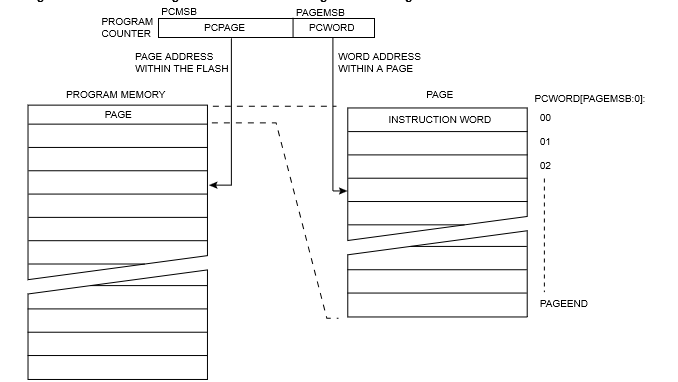


Some data transfer instructions:-

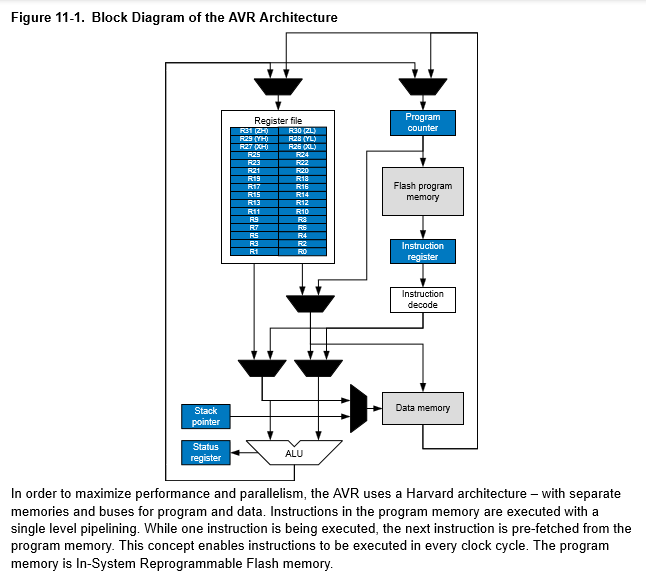


As seen from the data transfer instructions, Atmega328p supports Immediate, Direct Addressing, Relative   
(with pre and post increment), and Displacement and Indirect forms of Addressing modes.

**Instruction processing:-**



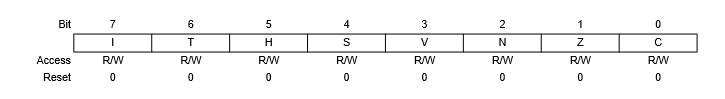
**CPU Organisation**



There exists single level pipelining (as mentioned), with instruction pre-fetch to solve the problem of pipeline hazards.

As we can see, there are a lot of registers. Here we touch upon the main ones:-

1. Status register

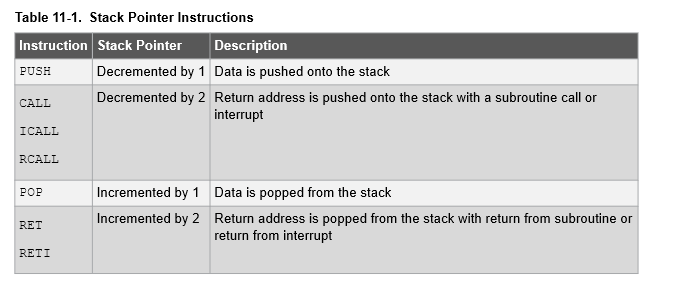


Bit 7 – I Global Interrupt Enable  
Bit 6 – T Copy Storage  
Bit 5 – H Half Carry Flag  
Bit 4 – S Sign Flag, S = N ㊉ V  
Bit 3 – V Two’s Complement Overflow Flag

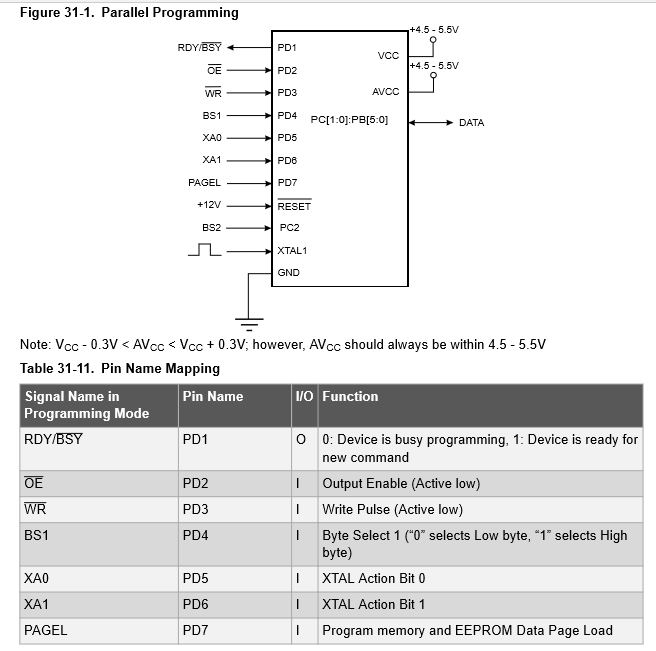
Bit 2 – N Negative Flag

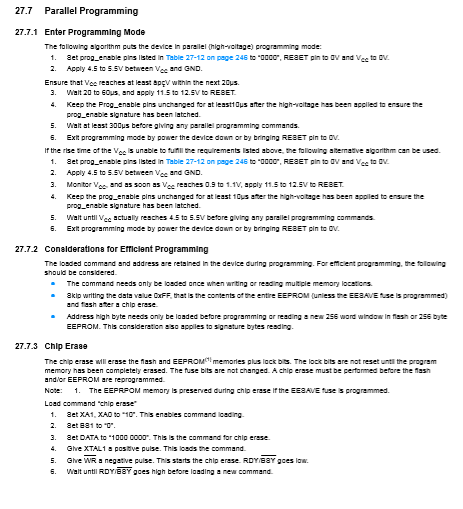
Bit 1 – Z Zero Flag

Bit 0 – C Carry Flag

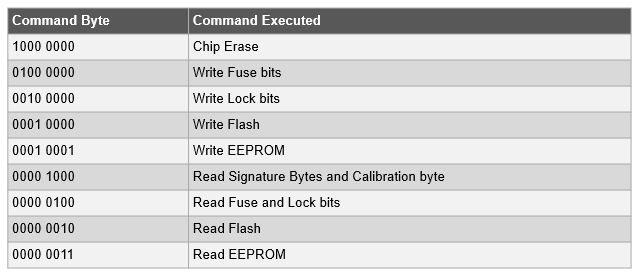
1. General purpose register file
2. X,Y,Z registers
3. Stack Pointer   
   

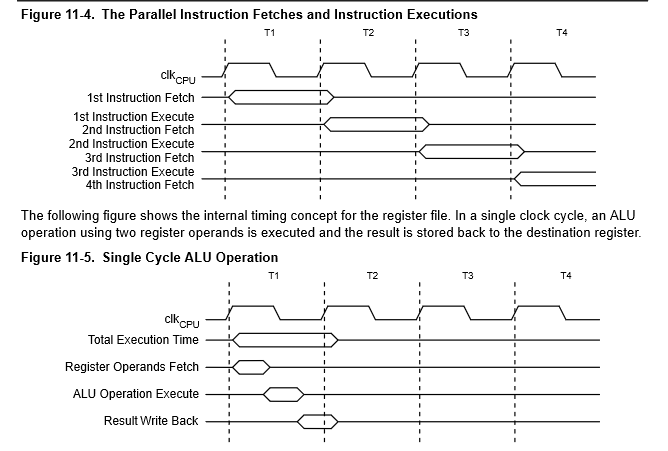
5. Parallel Programing and Parallel Processing features, with advanced architecture





Command byte bit coding:-



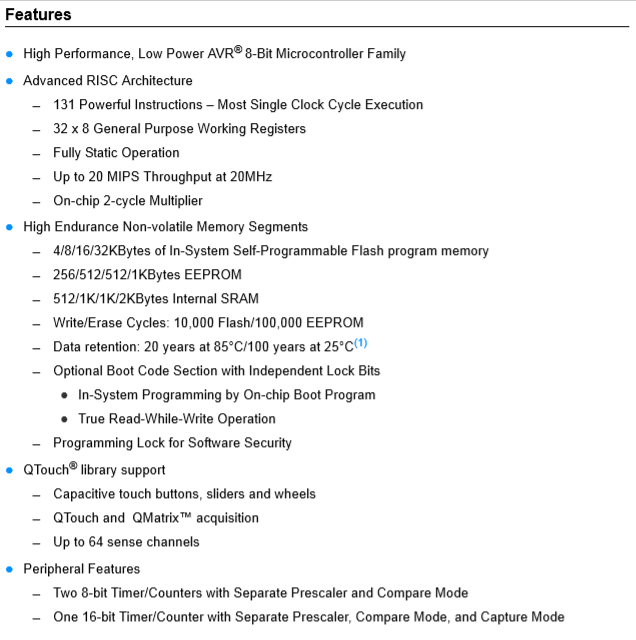


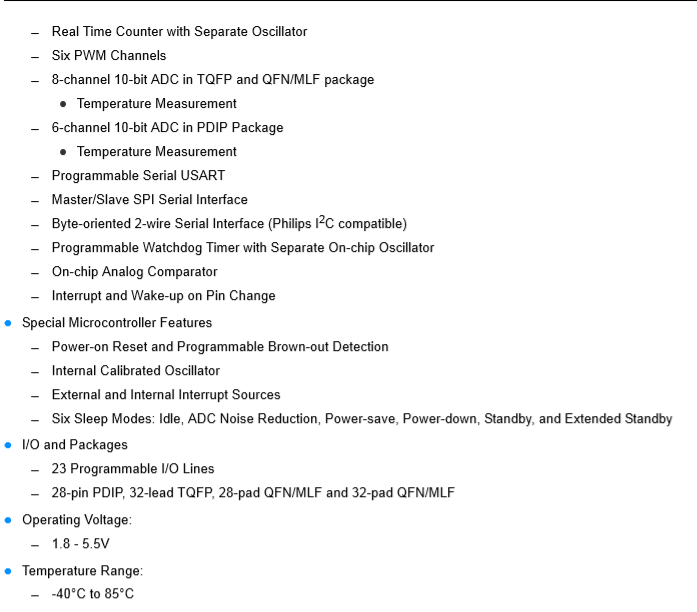
Parallel Processing features:-

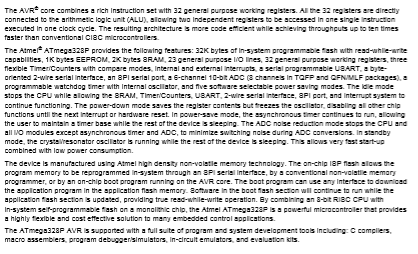
1. Supports processing instruction level parallelism as well as memory access parallelism.
2. Multiple data accesses in a single instruction (SIMD)
3. Extensive research is still ongoing wrt this architecture, and information about detailed parallel processing features   
   is currently unavailable for public viewing.

Memory Addressing features:-

1. SHARC 32-bit address space for accesses
2. Accesses 16 GB or 20 GB or 24 GB as per the word size ( 32-bit, 40-bit or 48 bit) configured in the memory for each address.
3. When word size = 32-bit then external memory configuration addressable space is 16 GB(232 ×4) bytes

****

****



References:-  
 1. <http://ww1.microchip.com/downloads/en/DeviceDoc/Atmel-7810-Automotive-Microcontrollers-ATmega328P_Datasheet.pdf>