

# RTL design of 32-bit Arithmetic Logic unit

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## Abstract

This paper presents the design of a 32bit ALU(Arithmetic logic unit) which can perform the various Arithmetic operations like Adder,Subtractor,Multiplier Divider and logical operations like all logic gates implementation This design also contains error check tests like Addition overflow condition and division divide by zero condition .It consists of an Accumulator register which stores the current system value and a D flipflop which contains an Error value in it.

OP-CODE TABLE			
0000: no-operation	0110: AND	1101: SHL-logic	<b>Error Check:</b> • Divide-by-Zero (ACC/Input) 32-bit Input == Low RED if(Input) == Low • Overflow 32-bit Adder Overflow RED if(ACC+Input) == Overflow
0001: ADD	0111: OR	1110: SHR-logic	
0010: SUB	1000: XOR	1111: RESET	
0011: MUL	1001: NOT		
0100: DIV	1010: NAND		
0101: MOD	1011: NOR		
	1100: XNOR		

Fig. 2.Opcodes for the ALU

## I. DESCRIPTION

An arithmetic unit, or ALU, enables computers to perform mathematical operations on binary numbers. They can be found at the heart of every digital computer and are one of the most important parts of a CPU which is called as Central Processing Unit).This design follows a OP-Code table which consists of 16 commands including arithmetic and logical operations which deals with 32-bit numbers.The present values and the next values are stored in two different registers and checks for the errors conditions and stored in another register meant for storing the error values.

## III. WAVEFORM

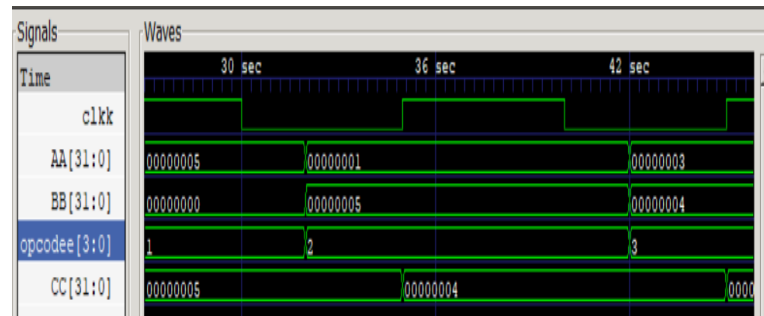


Fig. 3. ALU operations in wave form

## II. MODULE

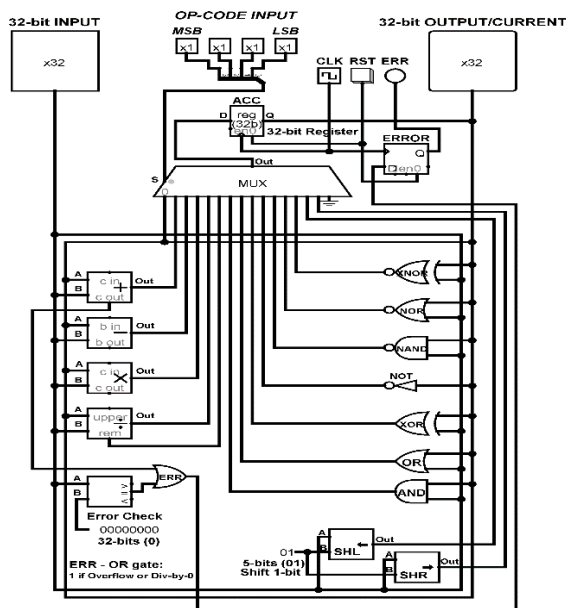


Fig. 1. Block diagram for 32-bit ALU

## REFERENCES

- [1] <https://github.com/armixz/32bit-ALU/blob/main/LICENSE>