Input Capture Module for Embedded Systems

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***Abstract*—This paper presents the design of an input capture module used in embedded systems to deal with input signals.The input capture module timestamps every rising edge in the input signal to timestamps in memory of the embedded system.This rising edge also triggers an interrupt to set a flag indicating that an input has been received. This enables us to trigger events on the exact time when an external signal is received, which can be of great help in highly real time applications.**

***Index Terms*—input capture, embedded system, interrupt, trigger**

I. Introduction

The timer capture module performs an important task of capturing the current value of a timer counter to timestamp an input event triggered by a rising edge of an external signal. On capturing the input signal, this module also sets an interrupt flag indicating the a signal has been captured [1]. This interrupt flag can then be used by the embedded system to perform various task which demands accurate timing, such as time period measurements and pulse measurements.

II. Design Description

The input capture module consists of an 8-bit timer counter which counts from 0 to 255, on each rising edge of the clock pulse to the clock input pin of the module. When an external signal is input to the signal input pin of the module the current timer counter value is transferred to a register and the signal input interrupt flag is set. The timer counter is independent of the input signal and is only dependent on the input clock [2].

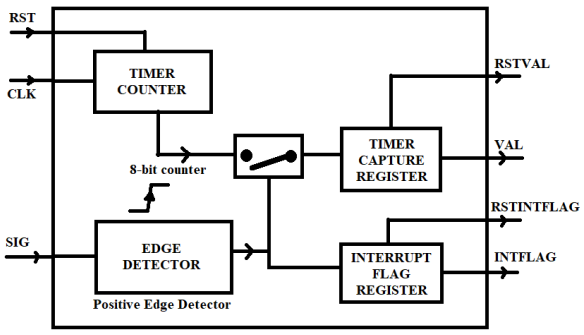

Fig. 1. Block Diagram of the Input Capture Module

Fig:1 shows the block diagram of the input capture module with its input and output pins.

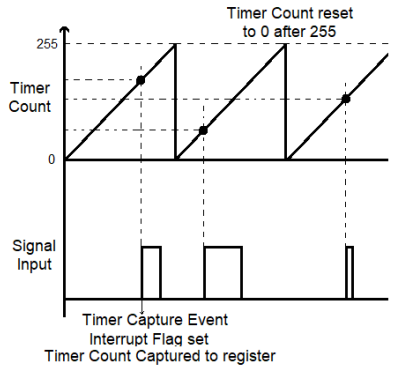

Fig. 2. Timer value capture on external signal input event

Fig:2 shows the timer value captured when rising edge of an external signal is detected on the signal input pin.

III. Waveform

The waveform of the Input capture module designed in verilog hardware description language is obtained by using opensource Icarus Iverilog tool.

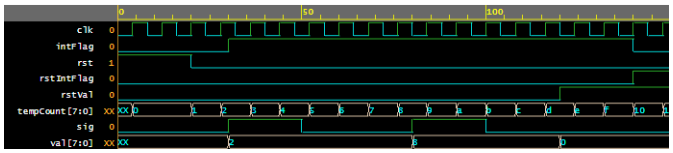

Fig. 3. Input capture module waveform with external signal input and clock

Fig:3 shows the input capture module in action with input external input signal and clock input.

The clock input, the external signal is fed to the input ports clk and sig respectively. The captured timer value is output from the 8 bit val register. The $intFlag$ port gives the interrupt flag from the module when rising edge of an external signal is detected.

References

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[2] J. Ding and Q. Shen, "Research and Application of Capture Module Based on C8051F020," 2010 International Conference on Measuring Technology and Mechatronics Automation, 2010, pp. 1024-1026, doi: 10.1109/ICMTMA.2010.201.
[3] https://github.com/pramitpal/InputCaptureModule