4-bit Adder using half adder and full adder modules using Verilog HDL

Toushik Santra
Kolkata, West Bengal, India
toushiksantra@gmail.com

Abstract—In this paper, a 4 bit adder is implemented in verilog using structural modeling with half adder and full adder modules. The input is given in the form of two 4-bit numbers and an initial carry. The output is produced in the form of a 4-bit sum and a carry bit.

Keywords—Half Adder, Full Adder.

I. Introduction

An adder circuit is used to add two or numbers. half adder adds two 1-bit numbers and gives the output as a combination of a sum bit and a carry bit. This circuit falls short when there is some inital third bit that needs to be considered in the adder circuit. This problem is solved by a full adder where a third bit can be given as input. Structurally, a full adder can be represented by combining two half adders which can simplify the design complexity by considering a half adder as a block or module with 2 input ports and 2 output ports. In this paper, I have represented a 4-bit adder circuit using the aforementioned method of using half adder module to design a full adder and using full adder module to design a 4-bit adder circuit.

II. Modules and Design Flow

A. Half Adder

A half adder gate diagram is simulated using a "XOR" gate, to calculate the sum of the two 1-bit inputs (here, 'a' and 'b'), and an "AND" gate, to calculate the carry bit that is generated during the addition of 'a' and 'b'.

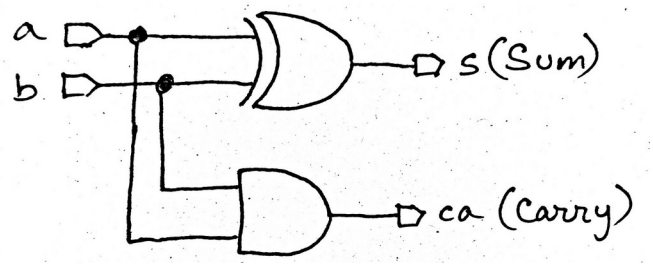

Figure. 2(a): Half Adder module

Figure 2(a) represents the schematic structure of a half adder circuit module composed of logic gates logic gates.

B. Full Adder

The aforementioned half adder circuit is considered as a block with 2 input ports and 2 output ports. First, 2 input bits 'a1' and 'b1' is given as input to 1 half adder. The sum of this half adder is given as input to the second half adder along with the third bit (Cin) becoming the second input. The sum obtained from the second half adder gives the final sum and the 2 carry bit output is fed to an "OR" gate to give the final carry bit as the output.

Figure 2(b) represents the schematic structure of a full adder module that is composed of 2 individual half adder modules and a "OR" gate to compute the final carry output.

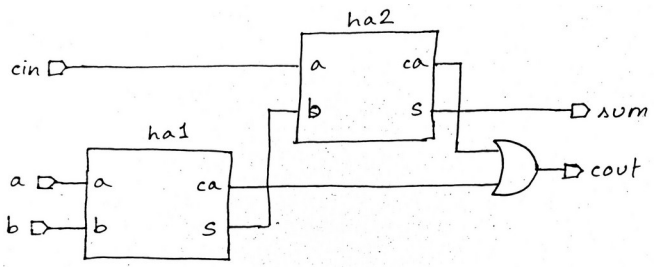

Figure 2(b): Full Adder module composed of 2 half adder modules

C. 4-bit Adder

The aforementioned full adder circuit is considered as a block with 3 input ports and 2 output ports. In the case of 4-bit adder, the input is given as 2 arrays of 4-bit each and a carry input for the third bit of the full adder. Each bit of the input arrays are fed as input for a single full adder block. The sum of this full adder block gives the output of that particular input bit position of the input array. The carry output bit is fed as carry input to the next full adder block.

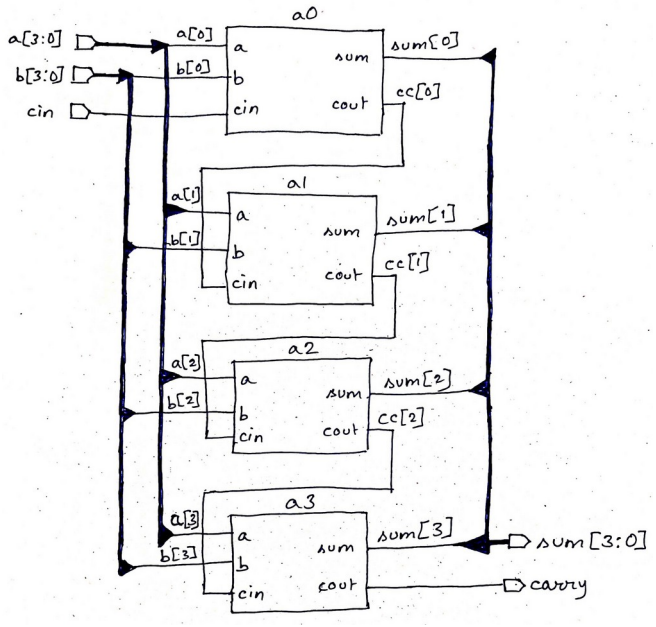

Figure 2(c): 4-bit adder module composed of full adder module

Figure 2(c) represents a 4-bit Adder where addition every bit combination of the array is computed using aforementioned full adder module.

References

[1] T. R. Padmanabhan, B. Bala Tripura Sundari, "Design Through Verilog HDL", A John Wiley and Sons, INC. publication (IEEE Press).